IWR1843 Single-Chip 76- to 81-GHz FMCW mmWave Sensor

1 Device Overview

1.1 Features

- FMCW transceiver
  - Integrated PLL, transmitter, receiver, Baseband, and A2D
  - 76- to 81-GHz coverage with 4 GHz available bandwidth
  - Four receive channels
  - Three transmit channels
  - Ultra-accurate chirp engine based on fractional-N PLL
  - TX power: 12 dBm
- Built-in calibration and self-test (monitoring)
  - ARM® Cortex®-R4F-based radio control system
  - Built-in firmware (ROM)
  - Self-calibrating system across frequency and temperature
- C674x DSP for FMCW signal processing
- On-chip Memory: 2MB
- Cortex-R4F microcontroller for object tracking and classification, and interface control
  - Supports autonomous mode (loading user application from QSPI flash memory)
- Integrated peripherals
  - Internal memories With ECC
- Host interface
  - CAN and CAN-FD
- Other interfaces available to user application
  - Up to 6 ADC channels
  - Up to 2 SPI channels
  - Up to 2 UARTs
  - I^2C
  - GPIOs
  - 2-lane LVDS interface for raw ADC data and debug instrumentation
- IWR1843 advanced features
  - Embedded self-monitoring with no host processor involvement
  - Complex baseband architecture
  - Embedded interference detection capability
  - Programmable phase rotators in transmit path to enable beam forming
- Power management
  - Built-in LDO network for enhanced PSRR
  - I/Os support dual voltage 3.3 V/1.8 V
- Clock source
  - Supports external oscillator at 40 MHz
  - Supports externally driven clock (square/sine) at 40 MHz
  - Supports 40 MHz crystal connection with load capacitors
- Easy hardware design
  - 0.65-mm pitch, 161-pin 10.4 mm × 10.4 mm flip chip BGA package for easy assembly and low-cost PCB design
  - Small solution size

1.2 Applications

- Smart/Automatic door openers Industrial sensor for measuring range, velocity, and angle
- Tank level probing radar
- Displacement sensing
- Field transmitters
- Traffic monitoring
- Proximity sensing
- Security and surveillance
- Factory automation safety guards
- People counting
- Motion detection

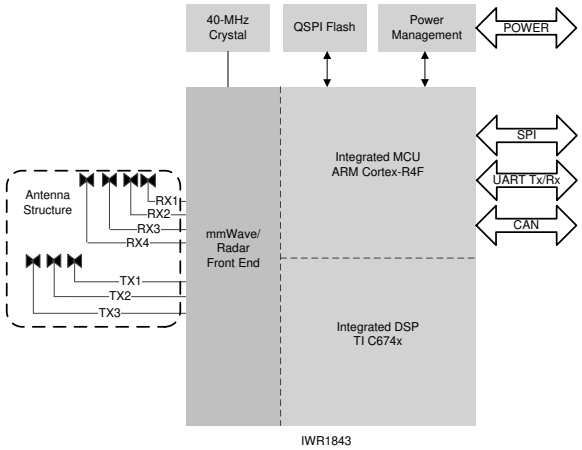


Figure 1-1. Autonomous Sensor For Industrial Applications

1.3 Description

The IWR1843 device is an integrated single-chip mmWave sensor based on FMCW radar technology capable of operating in the 76- to 81-GHz band with up to 4-GHz continuous chirp. The device is built with the low-power 45-nm RFCMOS process from Texas Instruments. This solution enables unprecedented levels of integration in an extremely small form factor. The IWR1843 is an ideal solution for low-power, self-monitored, ultra-accurate radar systems in industrial applications, such as, building automation, factory automation, drones, material handling, traffic monitoring, and surveillance.

The IWR1843 device is a self-contained, single-chip solution that simplifies the implementation of mmWave sensors in the band of 76 to 81 GHz. The IWR1843 includes a monolithic implementation of a 3TX, 4RX system with built-in PLL, and A2D converters. The IWR1843 also integrates a DSP subsystem, which contains a TI high-performance C674x DSP for the radar signal processing. The device includes an ARM R4F-based processor subsystem, which is responsible for front-end configuration, control, and calibration. Simple programming model changes can enable a wide variety of sensor implementation with the possibility of dynamic reconfiguration for implementing a multimode sensor. The Hardware Accelerator block (HWA) can perform radar processing and can help save MIPS on the DSP for higher-level algorithms. Additionally, the device is provided as a complete platform solution including TI reference designs, software drivers, sample configurations, API guides, training, and user documentation.

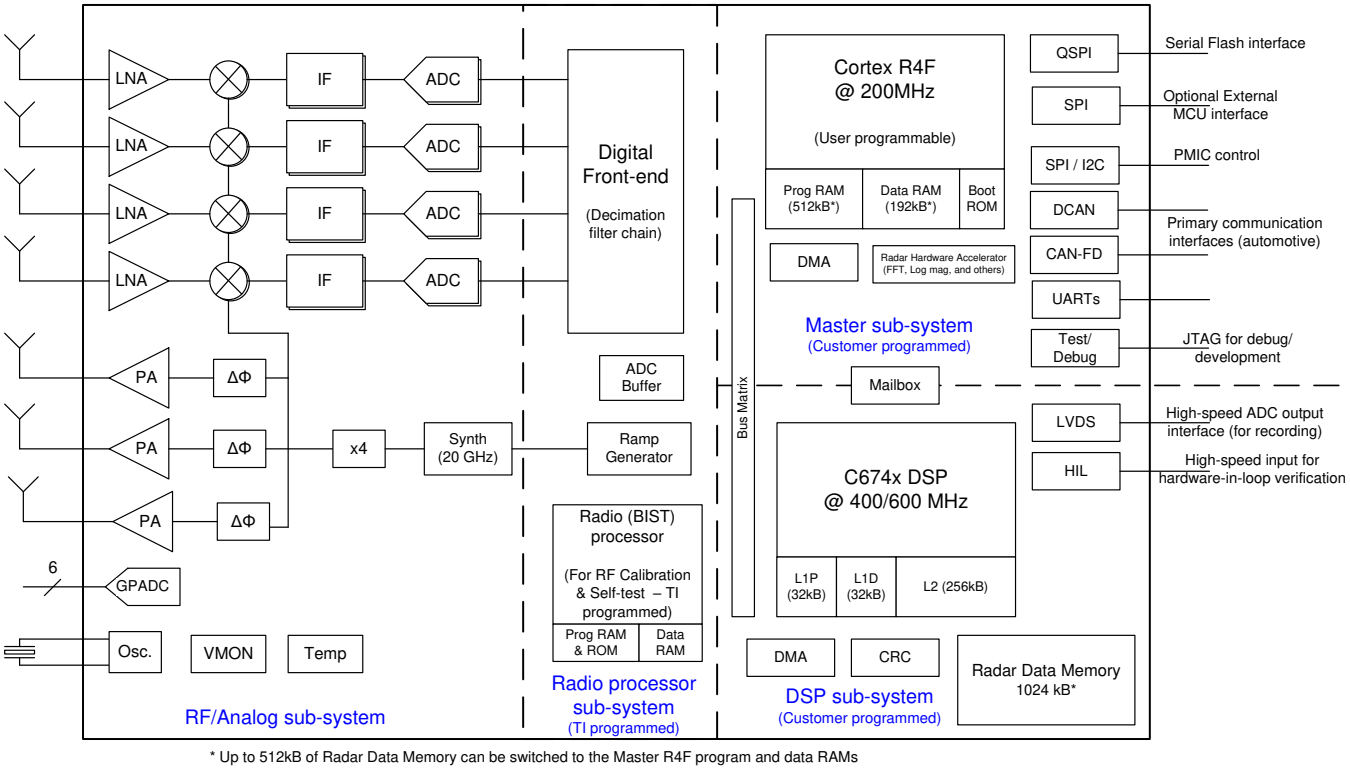
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
IWR1843AQGABL (Tray)	FCBGA (161)	10.4 mm × 10.4 mm
IWR1843AQGABLR (Reel)	FCBGA (161)	10.4 mm × 10.4 mm

(1) For more information, see Section 10, *Mechanical, Packaging, and Orderable Information*.

1.4 Functional Block Diagram

Figure 1-2 shows the functional block diagram of the device.



* Up to 512kB of Radar Data Memory can be switched to the Master R4F program and data RAMs

Figure 1-2. Functional Block Diagram

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2 Revision History

DATE	REVISION	NOTES
September 2019	*	Initial Release

3 Device Comparison

Table 3-1. Device Features Comparison

FUNCTION		IWR6843AOP	IWR6843	IWR1843	IWR1642	IWR1443
Antenna on Package (AOP)		Yes	—	—	—	—
Number of receivers		4	4	4	4	4
Number of transmitters		3	3	3(1)	2	3
RF frequency range		60 to 64 GHz	60 to 64 GHz	76 to 81 GHz	76 to 81 GHz	76 to 81 GHz
On-chip memory		1.75MB	1.75MB	2MB	1.5MB	576KB
Max I/F (Intermediate Frequency) (MHz)		10	10	10	5	15
Max real sampling rate (Msps)		25	25	25	12.5	37.5
Max complex sampling rate (Msps)		12.5	12.5	12.5	6.25	18.75
Processors						
MCU (R4F)		Yes	Yes	Yes	Yes	Yes
DSP (C674x)		Yes	Yes	Yes	Yes	—
Peripherals						
Serial Peripheral Interface (SPI) ports		2	2	2	2	1
Quad Serial Peripheral Interface (QSPI)		Yes	Yes	Yes	Yes	Yes
Inter-Integrated Circuit (I^2C) interface		1	1	1	1	1
Controller Area Network (DCAN) interface		—	—	Yes	Yes	Yes
Controller Area Network (CAN-FD) interface		Yes	Yes	Yes	—	—
Trace		Yes	Yes	Yes	Yes	—
PWM		Yes	Yes	Yes	Yes	—
Hardware In Loop (HIL/DMM)		Yes	Yes	Yes	Yes	—
GPADC		Yes	Yes	Yes	Yes	Yes
LVDS/Debug		Yes	Yes	Yes	Yes	Yes
CSI2		—	—	—	—	Yes
Hardware accelerator		Yes	Yes	Yes	—	Yes
1-V bypass mode		Yes	Yes	Yes	Yes	Yes
JTAG		Yes	Yes	Yes	Yes	Yes
Product status	Product Preview (PP), Advance Information (AI), or Production Data (PD)	AI(2)	AI(2)	PD(3)	PD(3)	PD(3)

(1) 3 Tx Simultaneous operation is supported only with 1-V LDO bypass and PA LDO disable mode. In this mode, the 1-V supply needs to be fed on the VOUT PA pin.
(2) ADVANCE INFORMATION for pre-production products; subject to change without notice.
(3) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty.

3.1 Related Products

For information about other devices in this family of products or related products see the links that follow.

mmWave sensors TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for industrial applications.

mmWave IWR sensors The Texas Instruments IWR1xxx family of mmWave Sensors are highly integrated and built on RFCMOS technology operating in 76- to 81-GHz frequency band. The devices have a closed-loop PLL for precise and linear chirp synthesis, includes a built-in radio processor (BIST) for RF calibration and safety monitoring. The devices have a very small-form factor, low power consumption, and are highly accurate. Industrial applications from long range to ultra short range can be realized using these devices.

Companion products for IWR1843 Review products that are frequently purchased or used in conjunction with this product.

Reference designs for IWR1843 TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the pin locations for the 161-pin FCBGA package. Figure 4-2, Figure 4-3, Figure 4-4, and Figure 4-5 show the same pins, but split into four quadrants.

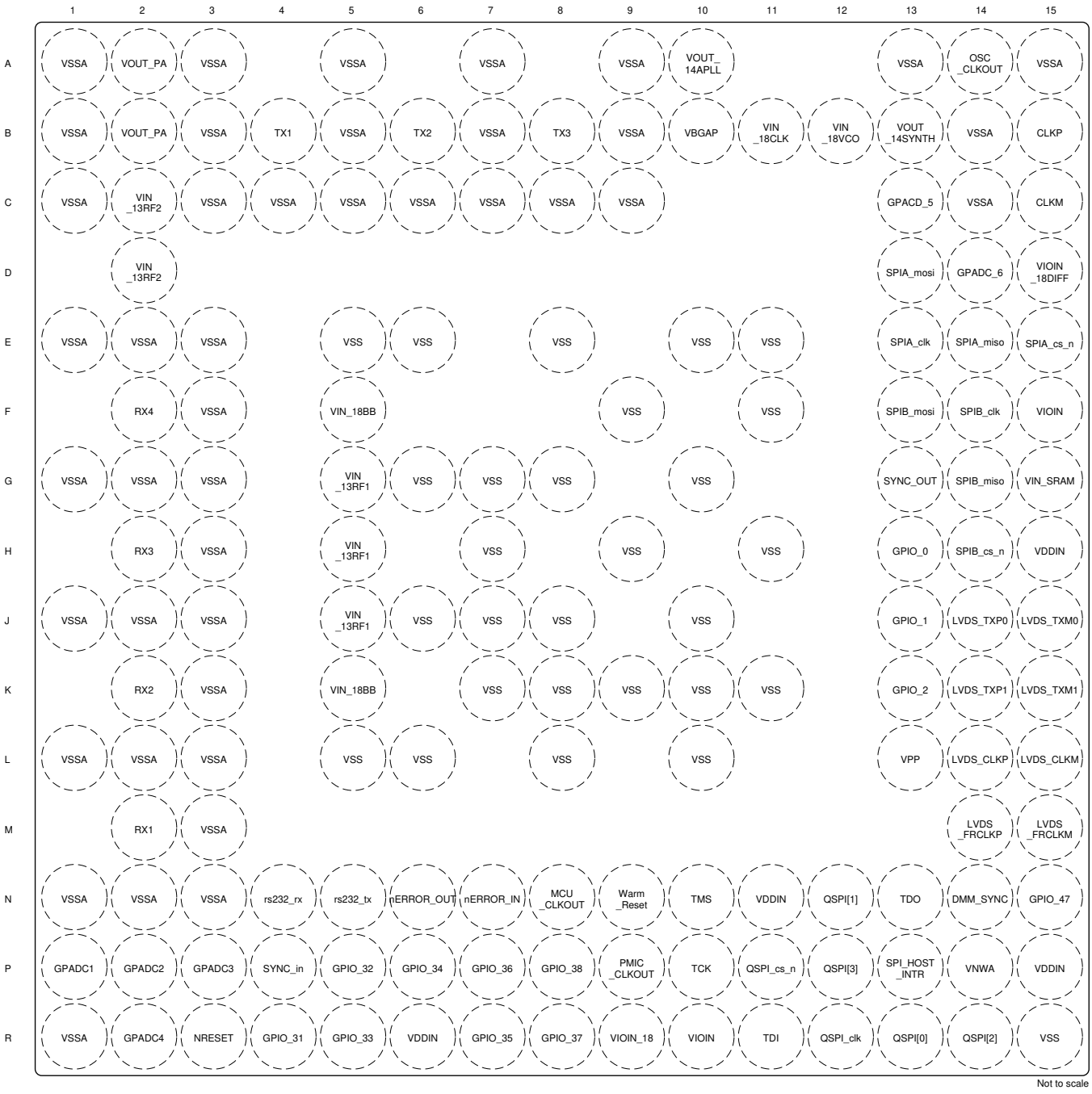


Figure 4-1. Pin Diagram

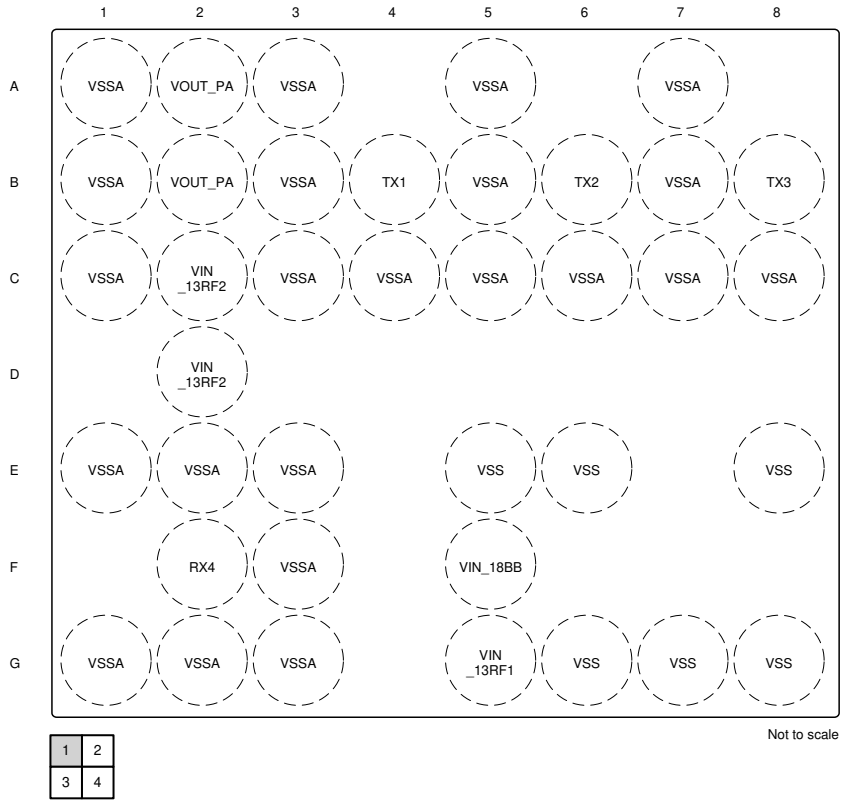


Figure 4-2. Top Left Quadrant

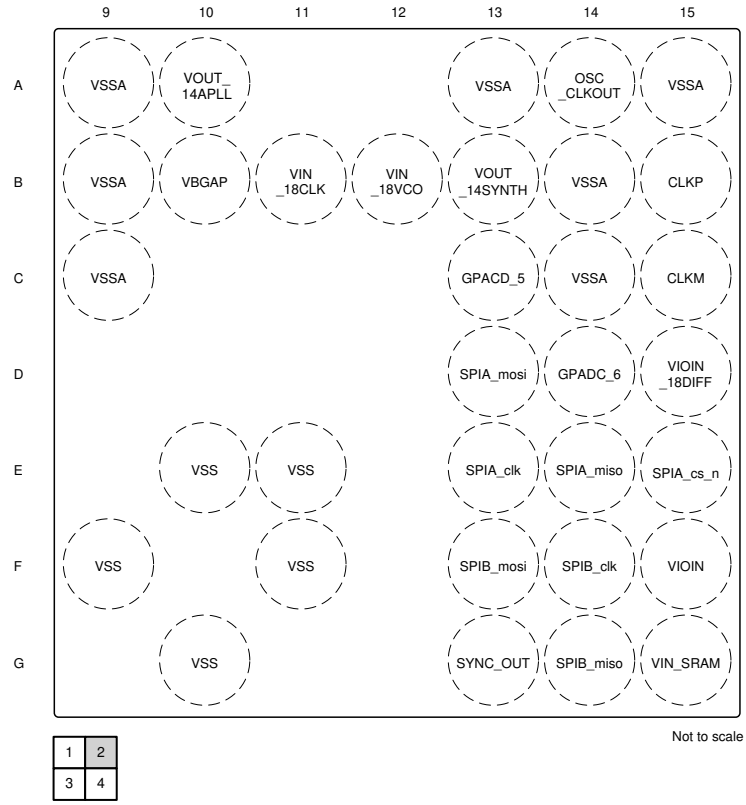


Figure 4-3. Top Right Quadrant

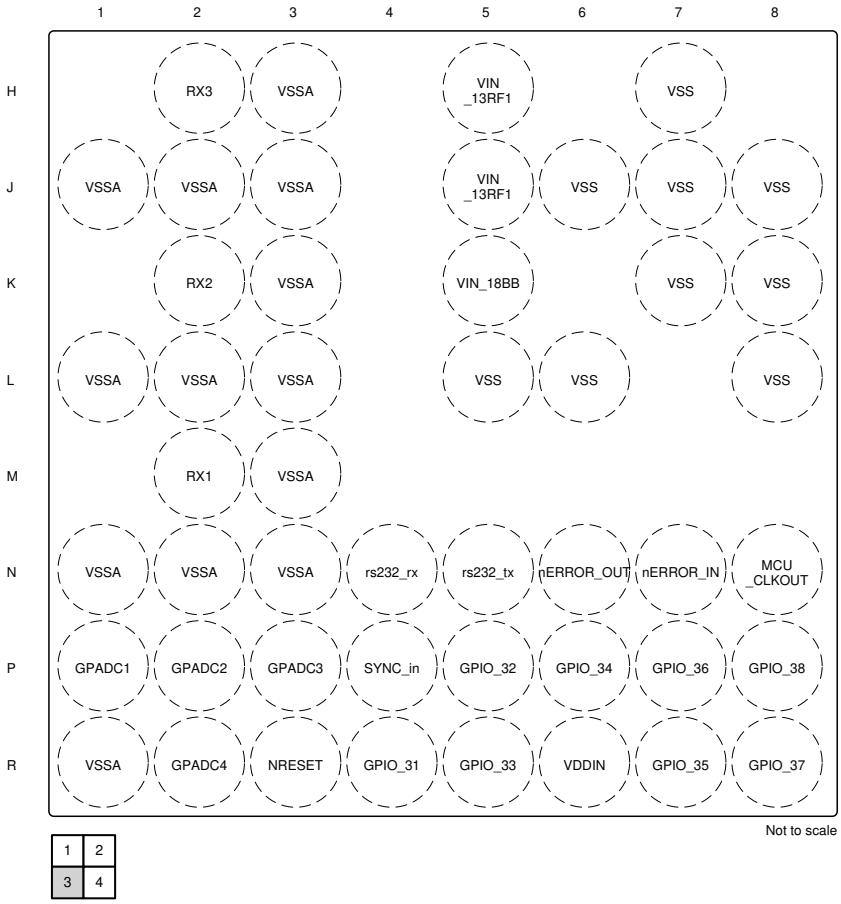


Figure 4-4. Bottom Left Quadrant

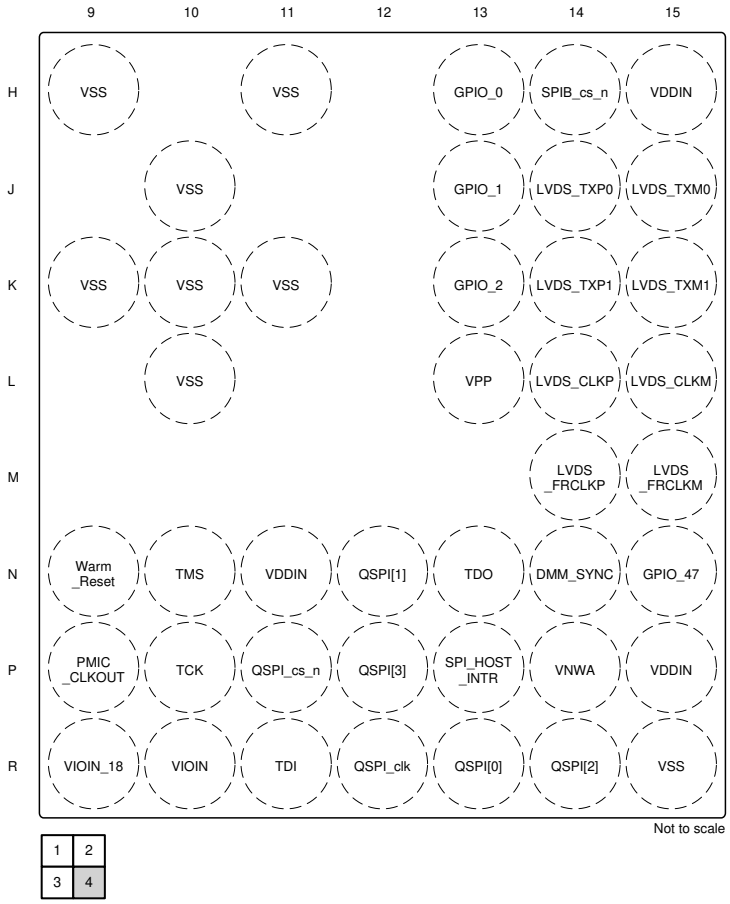


Figure 4-5. Bottom Right Quadrant

4.2 Pin Attributes

Table 4-1. Pin Attributes (ABL0161 Package)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
H13	GPIO_0	GPIO_13	0xFFFFEA04	0	IO	Output Disabled	Pull Down
		GPIO_0		1	IO		
		PMIC_CLKOUT		2	O		
		ePWM1b		10	O		
		ePWM2a		11	O		
J13	GPIO_1	GPIO_16	0xFFFFEA08	0	IO	Output Disabled	Pull Down
		GPIO_1		1	IO		
		SYNC_OUT		2	O		
		DMM_MUX_IN		12	I		
		SPIB_cs_n_1		13	IO		
		SPIB_cs_n_2		14	IO		
		ePWM1SYNCI		15	I		
K13	GPIO_2	GPIO_26	0xFFFFEA64	0	IO	Output Disabled	Pull Down
		GPIO_2		1	IO		
		OSC_CLKOUT		2	O		
		MSS_uartb_tx		7	O		
		BSS_uart_tx		8	O		
		SYNC_OUT		9	O		
		PMIC_CLKOUT		10	O		
R4	GPIO_31	TRACE_DATA_0	0xFFFFEA7C	0	O	Output Disabled	Pull Down
		GPIO_31		1	IO		
		DMM0		2	I		
		MSS_uarta_tx		4	IO		
P5	GPIO_32	TRACE_DATA_1	0xFFFFEA80	0	O	Output Disabled	Pull Down
		GPIO_32		1	IO		
		DMM1		2	I		
R5	GPIO_33	TRACE_DATA_2	0xFFFFEA84	0	O	Output Disabled	Pull Down
		GPIO_33		1	IO		
		DMM2		2	I		
P6	GPIO_34	TRACE_DATA_3	0xFFFFEA88	0	O	Output Disabled	Pull Down
		GPIO_34		1	IO		
		DMM3		2	I		
		ePWM3SYNCO		4	O		

Table 4-1. Pin Attributes (ABL0161 Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
R7	GPIO_35	TRACE_DATA_4	0xFFFFEA8C	0	O	Output Disabled	Pull Down
		GPIO_35		1	IO		
		DMM4		2	I		
		ePWM2SYNCO		4	O		
P7	GPIO_36	TRACE_DATA_5	0xFFFFEA90	0	O	Output Disabled	Pull Down
		GPIO_36		1	IO		
		DMM5		2	I		
		MSS_uartb_tx		5	O		
R8	GPIO_37	TRACE_DATA_6	0xFFFFEA94	0	O	Output Disabled	Pull Down
		GPIO_37		1	IO		
		DMM6		2	I		
		BSS_uart_tx		5	O		
P8	GPIO_38	TRACE_DATA_7	0xFFFFEA98	0	O	Output Disabled	Pull Down
		GPIO_38		1	IO		
		DMM7		2	I		
		DSS_uart_tx		5	O		
D14	GPIO_39	TRACE_DATA_8	0xFFFFEA9C	0	O	Output Disabled	Pull Down
		GPIO_39		1	IO		
		DMM8		2	I		
		CAN_FD_tx		4	IO		
		ePWM1SYNCI		5	I		
B14	GPIO_40	TRACE_DATA_9	0xFFFFEAA0	0	O	Output Disabled	Pull Down
		GPIO_40		1	IO		
		DMM9		2	I		
		CAN_FD_rx		4	IO		
		ePWM1SYNCO		5	O		
B15	GPIO_41	TRACE_DATA_10	0xFFFFEAA4	0	O	Output Disabled	Pull Down
		GPIO_41		1	IO		
		DMM10		2	I		
		ePWM3a		4	O		
C9	GPIO_42	TRACE_DATA_11	0xFFFFEAA8	0	O	Output Disabled	Pull Down
		GPIO_42		1	IO		
		DMM11		2	I		
		ePWM3b		4	O		
C8	GPIO_43	TRACE_DATA_12	0xFFFFEAAC	0	O	Output Disabled	Pull Down
		GPIO_43		1	IO		
		DMM12		2	I		
		ePWM1a		4	O		
		CAN_tx		5	IO		

Table 4-1. Pin Attributes (ABL0161 Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
B9	GPIO_44	TRACE_DATA_13	0xFFFFEAB0	0	O	Output Disabled	Pull Down
		GPIO_44		1	IO		
		DMM13		2	I		
		ePWM1b		4	O		
		CAN_rx		5	I		
B8	GPIO_45	TRACE_DATA_14	0xFFFFEAB4	0	O	Output Disabled	Pull Down
		GPIO_45		1	IO		
		DMM14		2	I		
		ePWM2a		4	O		
A9	GPIO_46	TRACE_DATA_15	0xFFFFEAB8	0	O	Output Disabled	Pull Down
		GPIO_46		1	IO		
		DMM15		2	I		
		ePWM2b		4	O		
N15	GPIO_47	TRACE_CLK	0xFFFFEABC	0	O	Output Disabled	Pull Down
		GPIO_47		1	IO		
		DMM_CLK		2	I		
N14	DMM_SYNC	TRACE_CTL	0xFFFFEAC0	0	O	Output Disabled	Pull Down
		RESERVED		1	IO		
		DMM_SYNC		2	I		
N8	MCU_CLKOUT	GPIO_25	0xFFFFEA60	0	IO	Output Disabled	Pull Down
		MCU_CLKOUT		1	O		
		ePWM1a		12	O		
N7	nERROR_IN	nERROR_IN	0xFFFFEA44	0	I	Input	
N6	nERROR_OUT	nERROR_OUT	0xFFFFEA4C	0	O	Hi-Z (Open Drain)	
P9	PMIC_CLKOUT	SOP[2]	0xFFFFEA68	During Power Up	I	Output Disabled	Pull Down
		GPIO_27		0	IO		
		PMIC_CLKOUT		1	O		
		ePWM1b		11	O		
		ePWM2a		12	O		
R13	QSPI[0]	GPIO_8	0xFFFFEA2C	0	IO	Output Disabled	Pull Down
		QSPI[0]		1	IO		
		SPIB_miso		2	IO		
N12	QSPI[1]	GPIO_9	0xFFFFEA30	0	IO	Output Disabled	Pull Down
		QSPI[1]		1	IO		
		SPIB_mosi		2	IO		
		SPIB_cs_n_2		8	IO		
R14	QSPI[2]	GPIO_10	0xFFFFEA34	0	IO	Output Disabled	Pull Down
		QSPI[2]		1	I		
		CAN_FD_tx		8	O		

Table 4-1. Pin Attributes (ABL0161 Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
P12	QSPI[3]	GPIO_11	0xFFFFEA38	0	IO	Output Disabled	Pull Down
		QSPI[3]		1	IO		
		CAN_FD_rx		8	I		
R12	QSPI_clk	GPIO_7	0xFFFFEA3C	0	IO	Output Disabled	Pull Down
		QSPI_clk		1	IO		
		SPIB_clk		2	O		
		DSS_uart_tx		6	O		
P11	QSPI_cs_n	GPIO_6	0xFFFFEA40	0	IO	Output Disabled	Pull Up
		QSPI_cs_n		1	IO		
		SPIB_cs_n		2	IO		
N4	rs232_rx	GPIO_15	0xFFFFEA74	0	IO	Input Enabled	Pull Up
		rs232_rx		1	I		
		MSS_uarta_rx		2	I		
		BSS_uart_tx		6	IO		
		MSS_uartb_rx		7	IO		
		CAN_FD_rx		8	I		
		I2C_scl		9	IO		
		ePWM2a		10	O		
		ePWM2b		11	O		
		ePWM3a		12	O		
N5	rs232_tx	GPIO_14	0xFFFFEA78	0	IO	Output Enabled	
		rs232_tx		1	O		
		MSS_uarta_tx		5	IO		
		MSS_uartb_tx		6	IO		
		BSS_uart_tx		7	IO		
		CAN_FD_tx		10	O		
		I2C_sda		11	IO		
		ePWM1a		12	O		
		ePWM1b		13	O		
		NDMM_EN		14	I		
		ePWM2a		15	O		
E13	SPIA_clk	GPIO_3	0xFFFFEA14	0	IO	Output Disabled	Pull Up
		SPIA_clk		1	IO		
		CAN_rx		6	I		
		DSS_uart_tx		7	O		
C13	SPIA_cs_n	SPIA_cs_n	0xFFFFEA18	0	IO	Output Disabled	Pull Up
		SPIA_cs_n		1	IO		
		CAN_tx		6	O		

Table 4-1. Pin Attributes (ABL0161 Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
E14	SPIA_miso	GPIO_20	0xFFFFEA10	0	IO	Output Disabled	Pull Up
		SPIA_miso		1	IO		
		CAN_FD_tx		2	O		
D13	SPIA_mosi	GPIO_19	0xFFFFEA0C	0	IO	Output Disabled	Pull Up
		SPIA_mosi		1	IO		
		CAN_FD_rx		2	I		
		DSS_uart_tx		8	O		
F14	SPIB_clk	GPIO_5	0xFFFFEA24	0	IO	Output Disabled	Pull Up
		SPIB_clk1		1	IO		
		MSS_uarta_rx		2	I		
		MSS_uartb_tx		6	O		
		BSS_uart_tx		7	O		
		CAN_FD_rx		8	I		
H14	SPIB_cs_n	GPIO_4	0xFFFFEA28	0	IO	Output Disabled	Pull Up
		SPIB_cs_n		1	IO		
		MSS_uarta_tx		2	O		
		MSS_uartb_tx		6	O		
		BSS_uart_tx		7	IO		
		QSPI_clk_ext		8	I		
		CAN_FD_tx		9	O		
G14	SPIB_miso	GPIO_22	0xFFFFEA20	0	IO	Output Disabled	Pull Up
		SPIB_miso		1	IO		
		I2C_scl		2	IO		
		DSS_uart_tx		6	O		
F13	SPIB_mosi	GPIO_21	0xFFFFEA1C	0	IO	Output Disabled	Pull Up
		SPIB_mosi		1	IO		
		I2C_sda		2	IO		
P13	SPI_HOST_INTR	GPIO_12	0xFFFFEA00	0	IO	Output Disabled	Pull Down
		SPI_HOST_INTR		1	O		
		SPIB_cs_n_1		6	IO		
P4	SYNC_in	GPIO_28	0xFFFFEA6C	0	IO	Output Disabled	Pull Down
		SYNC_IN		1	I		
		MSS_uartb_rx		6	IO		
		DMM_MUX_IN		7	I		
		SYNC_OUT		9	O		

Table 4-1. Pin Attributes (ABL0161 Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL ADDRESS [4]	MODE [5]	TYPE [6]	BALL RESET STATE [7]	PULL UP/DOWN TYPE [8]
G13	SYNC_OUT	SOP[1]	0xFFFFEA70	During Power Up	I	Output Disabled	Pull Down
		GPIO_29		0	IO		
		SYNC_OUT		1	O		
		DMM_MUX_IN		9	I		
		SPIB_cs_n_1		10	IO		
		SPIB_cs_n_2		11	IO		
P10	TCK	GPIO_17	0xFFFFEA50	0	IO	Input Enabled	Pull Down
		TCK		1	I		
		MSS_uartb_tx		2	O		
		CAN_FD_tx		8	O		
R11	TDI	GPIO_23	0xFFFFEA58	0	IO	Input Enabled	Pull Up
		TDI		1	I		
		MSS_uarta_rx		2	I		
N13	TDO	SOP[0]	0xFFFFEA5C	During Power Up	I	Output Enabled	
		GPIO_24		0	IO		
		TDO		1	O		
		MSS_uarta_tx		2	O		
		MSS_uartb_tx		6	O		
		BSS_uart_tx		7	O		
		NDMM_EN		9	I		
N10	TMS	GPIO_18	0xFFFFEA54	0	IO	Input Enabled	Pull Down
		TMS		1	I		
		BSS_uart_tx		2	O		
		CAN_FD_rx		6	I		
N9	Warm_Reset	Warm_Reset	0xFFFFEA48	0	IO	Hi-Z Input (Open Drain)	

The following list describes the table column headers:

1. **BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.
2. **BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
3. **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).
4. **PINCNTL ADDRESS:** MSS Address for PinMux Control
5. **MODE:** Multiplexing mode number: value written to PinMux Cntl register to select specific Signal name for this Ball number. Mode column has bit range value.
6. **TYPE:** Signal type and direction:
   - I = Input
   - O = Output
   - IO = Input or Output
7. **BALL RESET STATE:** The state of the terminal at power-on reset
8. **PULL UP/DOWN TYPE:** indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
   - Pull Up: Internal pullup
   - Pull Down: Internal pulldown
   - An empty box means No pull.
9. Pin Mux Control Value maps to lower 4 bits of register.

IO MUX registers are available in the MSS memory map and the respective mapping to device pins is as follows:

Table 4-2. PAD IO Control Registers

Default Pin/Ball Name	Package Ball /Pin (Address)	Pin Mux Config Register
SPI_HOST_INTR	P13	0xFFFFEA00
GPIO_0	H13	0xFFFFEA04
GPIO_1	J13	0xFFFFEA08
SPIA_MOSI	D13	0xFFFFEA0C
SPIA_MISO	E14	0xFFFFEA10
SPIA_CLK	E13	0xFFFFEA14
SPIA_CN_EN	E15	0xFFFFEA18
SPIB_MOSI	F13	0xFFFFEA1C
SPIB_MISO	G14	0xFFFFEA20
SPIB_CLK	F14	0xFFFFEA24
SPIB_CS_N	H14	0xFFFFEA28
QSPI[0]	R13	0xFFFFEA2C
QSPI[1]	N12	0xFFFFEA30
QSPI[2]	R14	0xFFFFEA34
QSPI[3]	P12	0xFFFFEA38
QSPI_CLK	R12	0xFFFFEA3C
QSPI_CS_N	P11	0xFFFFEA40
NERROR_IN	N7	0xFFFFEA44
WARM_RESET	N9	0xFFFFEA48
NERROR_OUT	N6	0xFFFFEA4C
TCK	P10	0xFFFFEA50
TMS	N10	0xFFFFEA54
TDI	R11	0xFFFFEA58
TDO	N13	0xFFFFEA5C
MCU_CLKOUT	N8	0xFFFFEA60
GPIO_2	K13	0xFFFFEA64
PMIC_CLKOUT	P9	0xFFFFEA68
SYNC_IN	P4	0xFFFFEA6C
SYNC_OUT	G13	0xFFFFEA70
RS232_RX	N4	0xFFFFEA74
RS232_TX	N5	0xFFFFEA78
GPIO_31	R4	0xFFFFEA7C
GPIO_32	P5	0xFFFFEA80
GPIO_33	R5	0xFFFFEA84
GPIO_34	P6	0xFFFFEA88
GPIO_35	R7	0xFFFFEA8C
GPIO_36	P7	0xFFFFEA90
GPIO_37	R8	0xFFFFEA94
GPIO_38	P8	0xFFFFEA98
GPIO_47	N15	0xFFFFEABC
DMM_SYNC	N14	0xFFFFEAC0

The register layout is as follows:

Table 4-3. PAD IO Register Bit Descriptions

BIT	FIELD	TYPE	RESET (POWER ON DEFAULT)	DESCRIPTION
31-11	NU	RW	0	Reserved
10	SC	RW	0	IO slew rate control: 0 = Higher slew rate 1 = Lower slew rate
9	PUPDSEL	RW	0	Pullup/PullDown Selection 0 = Pull Down 1 = Pull Up (This field is valid only if Pull Inhibit is set as '0')
8	PI	RW	0	Pull Inhibit/Pull Disable 0 = Enable 1 = Disable
7	OE_OVERRIDE	RW	1	Output Override
6	OE_OVERRIDE_CTRL	RW	1	Output Override Control: (A '1' here overrides any o/p manipulation of this IO by any of the peripheral block hardware it is associated with for example a SPI Chip select)
5	IE_OVERRIDE	RW	0	Input Override
4	IE_OVERRIDE_CTRL	RW	0	Input Override Control: (A '1' here overrides any i/p value on this IO with a desired value)
3-0	FUNC_SEL	RW	1	Function select for Pin Multiplexing (Refer to the Pin Mux Sheet)

4.3 Signal Descriptions

NOTE

All digital IO pins of the device (except NERROR IN, NERROR_OUT, and WARM_RESET) are non-failsafe; hence, care needs to be taken that they are not driven externally without the VIO supply being present to the device.

Table 4-4. Signal Descriptions - Digital

SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NO.
BSS_UART_TX	O	Debug UART Transmit [Radar Block]	F14, H14, K13, N10, N13, N4, N5, R8
CAN_FD_RX	I	CAN FD (MCAN) Receive Signal	D13, F14, N10, N4, P12
CAN_FD_TX	O	CAN FD (MCAN) Transmit Signal	E14, H14, N5, P10, R14
CAN_RX	I	CAN (DCAN) Receive Signal	E13
CAN_TX	IO	CAN (DCAN) Transmit Signal	E15
DMM0	I	Debug Interface (Hardware In Loop) - Data Line	R4
DMM1	I	Debug Interface (Hardware In Loop) - Data Line	P5
DMM2	I	Debug Interface (Hardware In Loop) - Data Line	R5
DMM3	I	Debug Interface (Hardware In Loop) - Data Line	P6
DMM4	I	Debug Interface (Hardware In Loop) - Data Line	R7
DMM5	I	Debug Interface (Hardware In Loop) - Data Line	P7
DMM6	I	Debug Interface (Hardware In Loop) - Data Line	R8
DMM7	I	Debug Interface (Hardware In Loop) - Data Line	P8
DMM_CLK	I	Debug Interface (Hardware In Loop) - Clock	N15
DMM_MUX_IN	I	Debug Interface (Hardware In Loop) Mux Select between DMM1 and DMM2 (Two Instances)	G13, J13, P4
DMM_SYNC	I	Debug Interface (Hardware In Loop) - Sync	N14
DSS_UART_TX	O	Debug UART Transmit [DSP]	D13, E13, G14, P8, R12
EPWM1A	O	PWM Module 1 - Output A	N5, N8
EPWM1B	O	PWM Module 1 - Output B	H13, N5, P9
EPWM1SYNCI	I		D14, J13
EPWM2A	O	PWM Module 2- Output A	H13, N4, N5, P9
EPWM2B	O	PWM Module 2 - Output B	N4
EPWM2SYNCO	O		R7
EPWM3A	O	PWM Module 3 - Output A	N4
EPWM3SYNCO	O		P6
GPIO_0	IO	General-purpose I/O	H13
GPIO_1	IO	General-purpose I/O	J13
GPIO_2	IO	General-purpose I/O	K13
GPIO_3	IO	General-purpose I/O	E13
GPIO_4	IO	General-purpose I/O	H14
GPIO_5	IO	General-purpose I/O	F14
GPIO_6	IO	General-purpose I/O	P11
GPIO_7	IO	General-purpose I/O	R12
GPIO_8	IO	General-purpose I/O	R13
GPIO_9	IO	General-purpose I/O	N12
GPIO_10	IO	General-purpose I/O	R14
GPIO_11	IO	General-purpose I/O	P12
GPIO_12	IO	General-purpose I/O	P13
GPIO_13	IO	General-purpose I/O	H13

Table 4-4. Signal Descriptions - Digital (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NO.
GPIO_14	IO	General-purpose I/O	N5
GPIO_15	IO	General-purpose I/O	N4
GPIO_16	IO	General-purpose I/O	J13
GPIO_17	IO	General-purpose I/O	P10
GPIO_18	IO	General-purpose I/O	N10
GPIO_19	IO	General-purpose I/O	D13
GPIO_20	IO	General-purpose I/O	E14
GPIO_21	IO	General-purpose I/O	F13
GPIO_22	IO	General-purpose I/O	G14
GPIO_23	IO	General-purpose I/O	R11
GPIO_24	IO	General-purpose I/O	N13
GPIO_25	IO	General-purpose I/O	N8
GPIO_26	IO	General-purpose I/O	K13
GPIO_27	IO	General-purpose I/O	P9
GPIO_28	IO	General-purpose I/O	P4
GPIO_29	IO	General-purpose I/O	G13
GPIO_30	IO	General-purpose I/O	E15
GPIO_31	IO	General-purpose I/O	R4
GPIO_32	IO	General-purpose I/O	P5
GPIO_33	IO	General-purpose I/O	R5
GPIO_34	IO	General-purpose I/O	P6
GPIO_35	IO	General-purpose I/O	R7
GPIO_36	IO	General-purpose I/O	P7
GPIO_37	IO	General-purpose I/O	R8
GPIO_38	IO	General-purpose I/O	P8
GPIO_47	IO	General-purpose I/O	N15
I2C_SCL	IO	I2C Clock	G14, N4
I2C_SDA	IO	I2C Data	F13, N5
LVDS_TXP[0]	O	Differential data Out – Lane 0	J14
LVDS_TXM[0]	O		J15
LVDS_TXP[1]	O	Differential data Out – Lane 1	K14
LVDS_TXM[1]	O		K15
LVDS_CLKP	O	Differential clock Out	L14
LVDS_CLKM	O		L15
LVDS_FRCLKP	O	Differential Frame Clock	M14
LVDS_FRCLKM	O		M15
MCU_CLKOUT	O	Programmable clock given out to external MCU or the processor	N8
MSS_UARTA_RX	I	Master Subsystem - UART A Receive	F14, N4, R11
MSS_UARTA_TX	O	Master Subsystem - UART A Transmit	H14, N13, N5, R4
MSS_UARTB_RX	IO	Master Subsystem - UART B Receive	N4, P4
MSS_UARTB_TX	O	Master Subsystem - UART B Transmit	F14, H14, K13, N13, N5, P10, P7
NDMM_EN	I	Debug Interface (Hardware In Loop) Enable - Active Low Signal	N13, N5
NERROR_IN	I	Failsafe input to the device. Nerror output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by Firmware	N7
NERROR_OUT	O	Open drain fail safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.	N6

Table 4-4. Signal Descriptions - Digital (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NO.
PMIC_CLKOUT	O	Output Clock from IWR1843 device for PMIC	H13, K13, P9
QSPI[0]	IO	QSPI Data Line #0 (Used with Serial Data Flash)	R13
QSPI[1]	IO	QSPI Data Line #1 (Used with Serial Data Flash)	N12
QSPI[2]	I	QSPI Data Line #2 (Used with Serial Data Flash)	R14
QSPI[3]	IO	QSPI Data Line #3 (Used with Serial Data Flash)	P12
QSPI_CLK	IO	QSPI Clock (Used with Serial Data Flash)	R12
QSPI_CLK_EXT	I	QSPI Clock (Used with Serial Data Flash)	H14
QSPI_CS_N	IO	QSPI Chip Select (Used with Serial Data Flash)	P11
RS232_RX	I	Debug UART (Operates as Bus Master) - Receive Signal	N4
RS232_TX	O	Debug UART (Operates as Bus Master) - Transmit Signal	N5
SOP[0]	I	Sense On Power - Line#0	N13
SOP[1]	I	Sense On Power - Line#1	G13
SOP[2]	I	Sense On Power - Line#2	P9
SPIA_CLK	IO	SPI Channel A - Clock	E13
SPIA_CS_N	IO	SPI Channel A - Chip Select	E15
SPIA_MISO	IO	SPI Channel A - Master In Slave Out	E14
SPIA_MOSI	IO	SPI Channel A - Master Out Slave In	D13
SPIB_CLK	IO	SPI Channel B - Clock	F14, R12
SPIB_CS_N	IO	SPI Channel B Chip Select (Instance ID 0)	H14, P11
SPIB_CS_N_1	IO	SPI Channel B Chip Select (Instance ID 1)	G13, J13, P13
SPIB_CS_N_2	IO	SPI Channel B Chip Select (Instance ID 2)	G13, J13, N12
SPIB_MISO	IO	SPI Channel B - Master In Slave Out	G14, R13
SPIB_MOSI	IO	SPI Channel B - Master Out Slave In	F13, N12
SPI_HOST_INTR	O	Out of Band Interrupt to an external host communicating over SPI	P13
SYNC_IN	I	Low frequency Synchronization signal input	P4
SYNC_OUT	O	Low Frequency Synchronization Signal output	G13, J13, K13, P4
TCK	I	JTAG Test Clock	P10
TDI	I	JTAG Test Data Input	R11
TDO	O	JTAG Test Data Output	N13
TMS	I	JTAG Test Mode Signal	N10
TRACE_CLK	O	Debug Trace Output - Clock	N15
TRACE_CTL	O	Debug Trace Output - Control	N14
TRACE_DATA_0	O	Debug Trace Output - Data Line	R4
TRACE_DATA_1	O	Debug Trace Output - Data Line	P5
TRACE_DATA_2	O	Debug Trace Output - Data Line	R5
TRACE_DATA_3	O	Debug Trace Output - Data Line	P6
TRACE_DATA_4	O	Debug Trace Output - Data Line	R7
TRACE_DATA_5	O	Debug Trace Output - Data Line	P7
TRACE_DATA_6	O	Debug Trace Output - Data Line	R8
TRACE_DATA_7	O	Debug Trace Output - Data Line	P8
WARM_RESET	IO	Open drain fail safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset.	N9

Table 4-5. Signal Descriptions - Analog

INTERFACE	SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NO.
Transmitters	TX1	O	Single ended transmitter1 o/p	B4
	TX2	O	Single ended transmitter2 o/p	B6
	TX3	O	Single ended transmitter3 o/p	B8
Receivers	RX1	I	Single ended receiver1 i/p	M2
	RX2	I	Single ended receiver2 i/p	K2
	RX3	I	Single ended receiver3 i/p	H2
	RX4	I	Single ended receiver4 i/p	F2
Reset	NRESET	I	Power on reset for chip. Active low	R3
Reference Oscillator	CLKP	I	In XTAL mode: Differential port for reference crystal In External clock mode: Single ended input reference clock port	B15
	CLKM	I	In XTAL mode: Differential port for reference crystal In External clock mode: Connect this port to ground	C15
Reference clock	OSC_CLKOUT	O	Reference clock output from clocking subsystem after cleanup PLL (1.4V output voltage swing).	A14
Bandgap voltage	VBGAP	O	Device's Band Gap Reference Output	B10
Power supply	VDDIN	Power	1.2V digital power supply	H15, N11, P15, R6
	VIN_SRAM	Power	1.2V power rail for internal SRAM	G15
	VNWA	Power	1.2V power rail for SRAM array back bias	P14
	VIOIN	Power	I/O Supply (3.3V or 1.8V): All CMOS I/Os would operate on this supply	R10, F15
	VIOIN_18	Power	1.8V supply for CMOS IO	R9
	VIN_18CLK	Power	1.8V supply for clock module	B11
	VIOIN_18DIFF	Power	1.8V supply for LVDS port	D15
	VPP	Power	Voltage supply for fuse chain	L13
Power supply	VIN_13RF1	Power	1.3V Analog and RF supply,VIN_13RF1 and VIN_13RF2 could be shorted on the board	G5, H5, J5
	VIN_13RF2	Power	1.3V Analog and RF supply	C2,D2
	VIN_18BB	Power	1.8V Analog base band power supply	K5, F5
	VIN_18VCO	Power	1.8V RF VCO supply	B12
	VSS	Ground	Digital ground	L5, L6, L8, L10, K7, K8, K9, K10, K11, J6, J7, J8, J10, H7, H9, H11, G6, G7, G8, G10, F9, F11, E5, E6, E8, E10, E11, R15
	VSSA	Ground	Analog ground	A1, A3, A5, A7, A15, B1, B3, B5, B7, C1, C3, C4, C5, C6, C7, E1, E2, E3, F3, G1, G2, G3, H3, J1, J2, J3, K3, L1, L2, L3, M3, N1, N2, N3, R1, A13, C8,A9, B9, C9, B14, C14
Internal LDO output/inputs	VOUT_14APLL	O	Internal LDO output	A10
	VOUT_14SYNTH	O	Internal LDO output	B13
	VOUT_PA	IO	When internal PA LDO is used this pin provides the output voltage of the LDO. When the internal PA LDO is bypassed and disabled 1V supply should be fed on this pin. This is mandatory in 3TX simultaneous use case.	A2, B2

Table 4-5. Signal Descriptions - Analog (continued)

INTERFACE	SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NO.
Test and Debug output for pre-production phase. Can be pinned out on production hardware for field debug	Analog Test1 / ADC1	IO	ADC Channel 1 (1)	P1
	Analog Test2 / ADC2	IO	ADC Channel 2 (1)	P2
	Analog Test3 / ADC3	IO	ADC Channel 3 (1)	P3
	Analog Test4 / ADC4	IO	ADC Channel 4 (1)	R2
	ANAMUX / ADC5	IO	ADC Channel 5 (1)	C13
	VSENSE / ADC6	IO	ADC Channel 6 (1)	D14

(1) For details, see Section 6.4.1.

5 Specifications

5.1 Absolute Maximum Ratings (1) (2)

PARAMETERS		MIN	MAX	UNIT
VDDIN	1.2 V digital power supply	–0.5	1.4	V
VIN_SRAM	1.2 V power rail for internal SRAM	–0.5	1.4	V
VNWA	1.2 V power rail for SRAM array back bias	–0.5	1.4	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	–0.5	3.8	V
VIOIN_18	1.8 V supply for CMOS IO	–0.5	2	V
VIN_18CLK	1.8 V supply for clock module	–0.5	2	V
VIOIN_18DIFF	1.8 V supply for LVDS port	–0.5	2	V
VIN_13RF1	1.3 V Analog and RF supply, VIN_13RF1 and VIN_13RF2 could be shorted on the board.	–0.5	1.45	V
VIN_13RF2				
VIN_13RF1	1-V Internal LDO bypass mode. Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	–0.5	1.4	V
VIN_13RF2				
VIN_18BB	1.8-V Analog baseband power supply	–0.5	2	V
VIN_18VCO supply	1.8-V RF VCO supply	–0.5	2	V
Input and output voltage range	Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State)	–0.3V	VIOIN + 0.3	V
	Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input		VIOIN + 20% up to 20% of signal period	
CLKP, CLKM	Input ports for reference crystal	–0.5	2	V
Clamp current	Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	–20	20	mA
T_J	Operating junction temperature range	–40	105	ºC
T_{STG}	Storage temperature range after soldered onto PC board	–55	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) (1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002	±250	

(1) ANSI/ESDA/JEDEC JS0991 specification.

5.3 Power-On Hours (POH)(1)

JUNCTION TEMPERATURE (T_j)	OPERATING CONDITION	NOMINAL CVDD VOLTAGE (V)	POWER-ON HOURS [POH] (HOURS)
90% at 85ºC T_j 10% at 105ºC T_j	50% duty cycle	1.2	80,000
100% at 85ºC T_j			100,000

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VDDIN	1.2 V digital power supply	1.14	1.2	1.32	V
VIN_SRAM	1.2 V power rail for internal SRAM	1.14	1.2	1.32	V
VNWA	1.2 V power rail for SRAM array back bias	1.14	1.2	1.32	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	3.135	3.3	3.465	V
		1.71	1.8	1.89	
VIOIN_18	1.8 V supply for CMOS IO	1.71	1.8	1.9	V
VIN_18CLK	1.8 V supply for clock module	1.71	1.8	1.9	V
VIOIN_18DIFF	1.8 V supply for LVDS port	1.71	1.8	1.9	V
VIN_13RF1	1.3 V Analog and RF supply. VIN_13RF1 and VIN_13RF2 could be shorted on the board	1.23	1.3	1.36	V
VIN_13RF2					
VIN_13RF1 (1-V Internal LDO bypass mode)		0.95	1	1.05	V
VIN_13RF2 (1-V Internal LDO bypass mode)					
VIN18BB	1.8-V Analog baseband power supply	1.71	1.8	1.9	V
VIN_18VCO	1.8V RF VCO supply	1.71	1.8	1.9	V
V_{IH}	Voltage Input High (1.8 V mode)	1.17			V
	Voltage Input High (3.3 V mode)	2.25			
V_{IL}	Voltage Input Low (1.8 V mode)			0.3*VIOIN	V
	Voltage Input Low (3.3 V mode)			0.62	
V_{OH}	High-level output threshold (I_{OH} = 6 mA)	VIOIN – 450			mV
V_{OL}	Low-level output threshold (I_{OL} = 6 mA)			450	mV
NRESET SOP[2:0]	V_{IL} (1.8V Mode)			0.2	V
	V_{IH} (1.8V Mode)	0.96			
	V_{IL} (3.3V Mode)			0.3	
	V_{IH} (3.3V Mode)	1.57			

5.5 Power Supply Specifications

Table 5-1 describes the four rails from an external power supply block of the IWR1843 device.

Table 5-1. Power Supply Rails Characteristics

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOS IN THE DEVICE
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, LVDS	Input: VIN_18VCO, VIN18CLK, VIN_18BB, VIOIN_18DIFF, VIOIN_18IO LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.3 V (or 1 V in internal LDO bypass mode)	Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution	Input: VIN_13RF2, VIN_13RF1 LDO Output: VOUT_PA
3.3 V (or 1.8 V for 1.8 V I/O mode)	Digital I/Os	Input VIOIN
1.2 V	Core Digital and SRAMs	Input: VDDIN, VIN_SRAM

The 1.3-V (1.0 V) and 1.8-V power supply ripple specifications mentioned in are defined to meet a target spur level of –105 dBc (RF Pin = –15 dBm) at the RX. The spur and ripple levels have a dB-to-dB relationship, for example, a 1-dB increase in supply ripple leads to a ~1 dB increase in spur level. Values quoted are rms levels for a sinusoidal input applied at the specified frequency.

Table 5-2. Ripple Specifications

FREQUENCY (kHz)	RF RAIL		VCO/IF RAIL
	1.0 V (INTERNAL LDO BYPASS) (μV_{RMS})	1.3 V (μV_{RMS})	1.8 V (μV_{RMS})
137.5	7	648	83
275	5	76	21
550	3	22	11
1100	2	4	6
2200	11	82	13
4400	13	93	19
6600	22	117	29

5.6 Power Consumption Summary

Table 5-3 and summarize the power consumption at the power terminals.

Table 5-3. Maximum Current Ratings at Power Terminals

PARAMETER	SUPPLY NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
Current consumption	VDDIN, VIN_SRAM, VNWA	Total current drawn by all nodes driven by 1.2V rail			1000	mA
	VIN_13RF1, VIN_13RF2	Total current drawn by all nodes driven by 1.3V or 1.0V rail (2TX, 4 RX simultaneously) (1)			2000	
	VIOIN_18, VIN_18CLK, VIOIN_18DIFF, VIN_18BB, VIN_18VCO	Total current drawn by all nodes driven by 1.8V rail			850	
	VIOIN	Total current drawn by all nodes driven by 3.3V rail (2)		50		

(1) 3 Transmitters can simultaneously be deployed only in devices with 1V / LDO bypass and PA LDO disable mode. In this mode 1-V supply needs to be fed on the VOUT PA pin. In this case the peak 1-V supply current goes up to 2500 mA.
(2) The exact VIOIN current depends on the peripherals used and their frequency of operation.

Table 5-4. Average Power Consumption at Power Terminals

PARAMETER	CONDITION			DESCRIPTION	MIN	TYP	MAX	UNIT
Average power consumption	1.0-V internal LDO bypass mode	25% Duty Cycle	1TX, 4RX	Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 128 chirps, 128 samples/chirp, 8-µs interchirp time (25% duty cycle), DSP active		1.3		W
			2TX, 4RX			1.38		
		50% Duty Cycle	1TX, 4RX	Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 256 chirps, 128 samples/chirp, 8-µs interchirp time (50% duty cycle), DSP active		1.77		
			2TX, 4RX			1.92		
	1.3-V internal LDO enabled mode	25% Duty Cycle	1TX, 4RX	Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 128 chirps, 128 samples/chirp, 8-µs interchirp time (25% duty cycle), DSP active		1.4		
			2TX, 4RX			1.48		
		50% Duty Cycle	1TX, 4RX	Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 256 chirps, 128 samples/chirp, 8-µs interchirp time (50% duty cycle), DSP active		1.94		
			2TX, 4RX			2.14		

5.7 RF Specification

over recommended operating conditions and with run time calibrations enabled (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Receiver	Noise figure[1]	76 to 77 GHz		14		dB
		77 to 81 GHz		15		
	1-dB compression point (Out Of Band / Specified at 10 kHz)[2]			–8		dBm
	Maximum gain			48		dB
	Gain range			24		dB
	Gain step size			2		dB
	Image Rejection Ratio (IMRR)			30		dB
	IF bandwidth[3]				10	MHz
	A2D sampling rate (real)				25	Msps
	A2D sampling rate (complex 1x)				12.5	Msps
	A2D resolution			12		Bits
	Return loss (S11)			<–10		dB
	Gain mismatch variation (over temperature)			±0.5		dB
	Phase mismatch variation (over temperature)			±3		°
	In-band IIP2	RX gain = 30dB IF = 1.5, 2 MHz at –12 dBFS		16		dBm
	Out-of-band IIP2	RX gain = 24dB IF = 10 kHz at -10dBm, 1.9 MHz at -30 dBm		24		dBm
	Idle Channel Spurs			–90		dBFS
Transmitter	Output power			12		dBm
	Amplitude noise			–145		dBc/Hz
Clock subsystem	Frequency range		76		81	GHz
	Ramp rate				100	MHz/µs
	Phase noise at 1-MHz offset	76 to 77 GHz		–95		dBc/Hz
		77 to 81 GHz		–93		

(1) Specification is quoted for complex 1x mode.
(2) 1-dB Compression Point (Out Of Band) is measured by feed a Continuous wave Tone below the lowest HPF cut-off frequency (50 kHz).
(3) The analog IF stages include high-pass filtering, with two independently configurable first-order high-pass corner frequencies. The set of available HPF corners is summarized as follows:

Available HPF Corner Frequencies (kHz)

HPF1	HPF2
175, 235, 350, 700	350, 700, 1400, 2800

The filtering performed by the digital baseband chain is targeted to provide:
- Less than ±0.5 dB pass-band ripple/droop, and
- Better than 60 dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

5.8 CPU Specifications

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
DSP Subsystem (C674 Family)	Clock Speed		600		MHz
	L1 Code Memory		32		KB
	L1 Data Memory		32		KB
	L2 Memory		256		KB
Master Controller Subsystem (R4F Family)	Clock Speed		200		MHz
	Tightly Coupled Memory - A (Program)		512		KB
	Tightly Coupled Memory - B (Data)		192		KB

CPU Specifications *(continued)*

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Shared Memory	Shared L3 Memory		1024		KB

5.9 Thermal Resistance Characteristics for FCBGA Package [ABL0161]

THERMAL METRICS(1)		°C/W(2) (3)
$R\Theta_{JC}$	Junction-to-case	4.2
$R\Theta_{JB}$	Junction-to-board	5.7
$R\Theta_{JA}$	Junction-to-free air	20.9
$R\Theta_{JMA}$	Junction-to-moving air	14.5(4)
Psi_{JT}	Junction-to-package top	0.38
Psi_{JB}	Junction-to-board	5.6

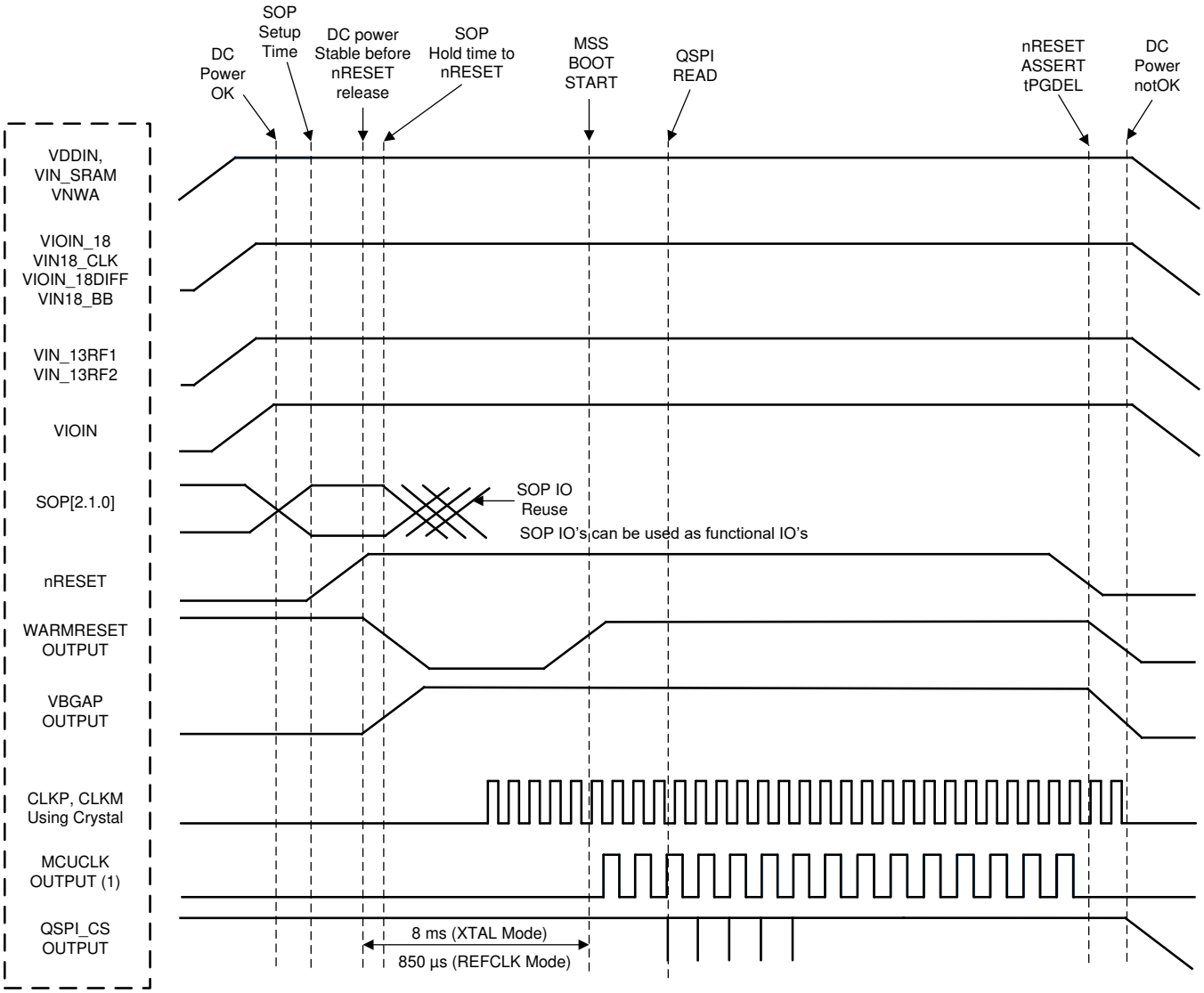
(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

A junction temperature of 105ºC is assumed.
(4)

5.10 Timing and Switching Characteristics

5.10.1 Power Supply Sequencing and Reset Timing

The IWR1843 device expects all external voltage rails and SOP lines to be stable before reset is deasserted. describes the device wake-up sequence.



(1) MCU_CLK_OUT in autonomous mode, where IWR1843 application is booted from the serial flash, MCU_CLK_OUT is not enabled by default by the device bootloader.

Figure 5-1. Device Wake-up Sequence

5.10.2 Input Clocks and Oscillators

5.10.2.1 Clock Specifications

The IWR1843 requires external clock source (that is, a 40-MHz crystal) for initial boot and as a reference for an internal APLL hosted in the device. An external crystal is connected to the device pins. Figure 5-2 shows the crystal implementation.

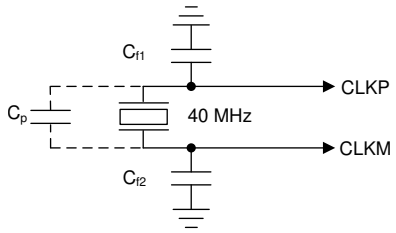


Figure 5-2. Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 5-2, should be chosen such that Equation 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

Table 5-5 lists the electrical characteristics of the clock crystal.

Table 5-5. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_P	Parallel resonance crystal frequency		40		MHz
C_L	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	–40		105	ºC
Frequency tolerance	Crystal frequency tolerance(1)(2)	–200		200	ppm
Drive level			50	200	µW

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.

Table 5-6. External Clock Mode Specifications

PARAMETER		SPECIFICATION			UNIT
		MIN	TYP	MAX	
Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referred to 40 MHz	Frequency		40		MHz
	AC-Amplitude	700		1200	mV (pp)
	Phase Noise at 1 kHz			–132	dBc/Hz
	Phase Noise at 10 kHz			–143	dBc/Hz
	Phase Noise at 100 kHz			–152	dBc/Hz
	Phase Noise at 1 MHz			–153	dBc/Hz
	Duty Cycle	35		65	%
	Freq Tolerance	–50		50	ppm

5.10.3 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

5.10.3.1 Peripheral Description

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The MibSPI/SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit baud clock generator
- SPICLK can be internally-generated (master mode) or received from an external clock source (slave mode)
- Each word transferred can have a unique format.
- SPI I/Os not used in the communication can be used as digital input/output signals

5.10.3.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 256 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

Table 5-8 and Table 5-9 assume the operating conditions stated in Table 5-7.

Table 5-7. SPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

Table 5-8. SPI Master Mode Switching Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)

NO.	PARAMETER			MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)		25		$256t_{c(VCLK)}$	ns
2(4)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
3(4)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
4(4)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 3$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 3$			
5(4)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 10.5$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 10.5$			
6(5)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$(C2TDELAY+2)*t_{c(VCLK)} - 7.5$		$(C2TDELAY+2) * t_{c(VCLK)} + 7$	ns
			CSHOLD = 1	$(C2TDELAY+3) * t_{c(VCLK)} - 7.5$		$(C2TDELAY+3) * t_{c(VCLK)} + 7$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$(C2TDELAY+2)*t_{c(VCLK)} - 7.5$		$(C2TDELAY+2) * t_{c(VCLK)} + 7$	
			CSHOLD = 1	$(C2TDELAY+3) * t_{c(VCLK)} - 7.5$		$(C2TDELAY+3) * t_{c(VCLK)} + 7$	
7(5)	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)		$0.5*t_{c(SPC)M} + (T2CDELAY + 1) *t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (T2CDELAY + 1) * t_{c(VCLK)} + 7.5$	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)		$0.5*t_{c(SPC)M} + (T2CDELAY + 1) *t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (T2CDELAY + 1) * t_{c(VCLK)} + 7.5$	
8(4)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		5			
9(4)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		3			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		3			

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared (where x= 0 or 1).
(2) $t_{c(MSS\_VCLK)}$ = master subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS+1)t_{c(MSS\_VCLK)} \geq 25ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS\_VCLK)} \geq 25ns$.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

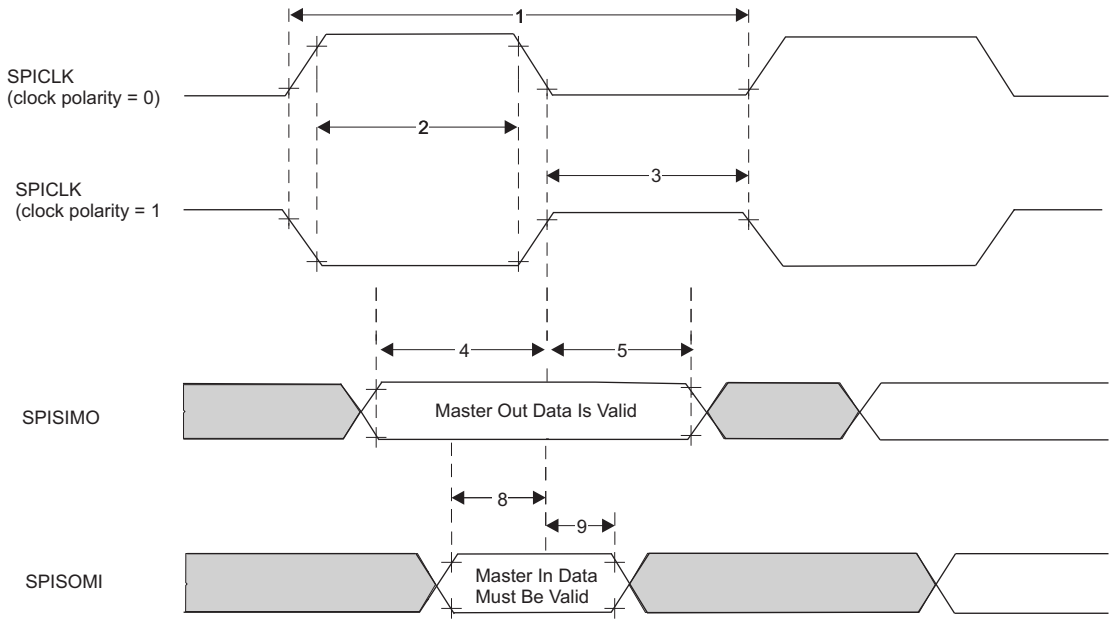


Figure 5-3. SPI Master Mode External Timing (CLOCK PHASE = 0)

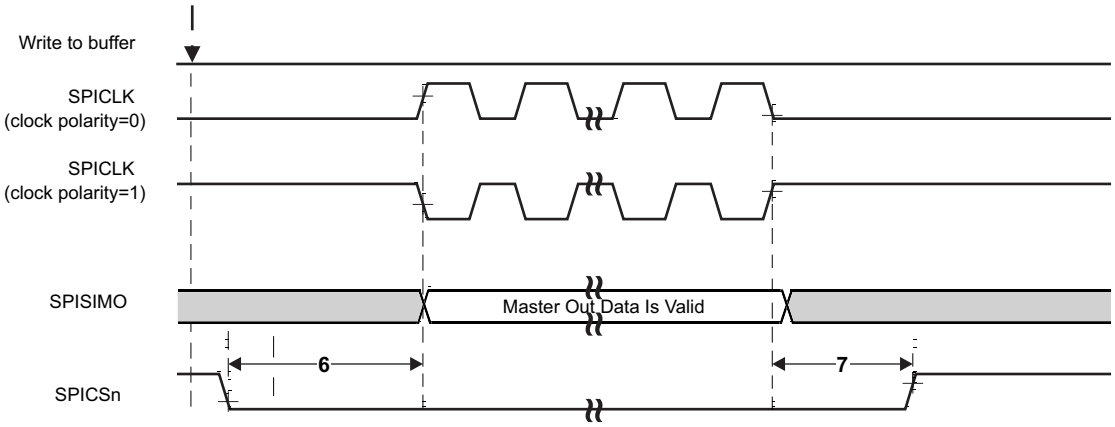


Figure 5-4. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)

Table 5-9. SPI Master Mode Switching Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)

NO.	PARAMETER			MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)		25		$256t_{c(VCLK)}$	ns
2(4)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
3(4)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
4(4)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 3$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 3$			
5(4)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 10.5$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 10.5$			
6(5)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} + 7.5$	
7(5)	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)		$(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)		$(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	
8(4)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		5			
9(4)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		3			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		3			

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set (where x = 0 or 1).
(2) $t_{c(MSS\_VCLK)}$ = master subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS +1)t_{c(MSS\_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS\_VCLK)} \geq 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

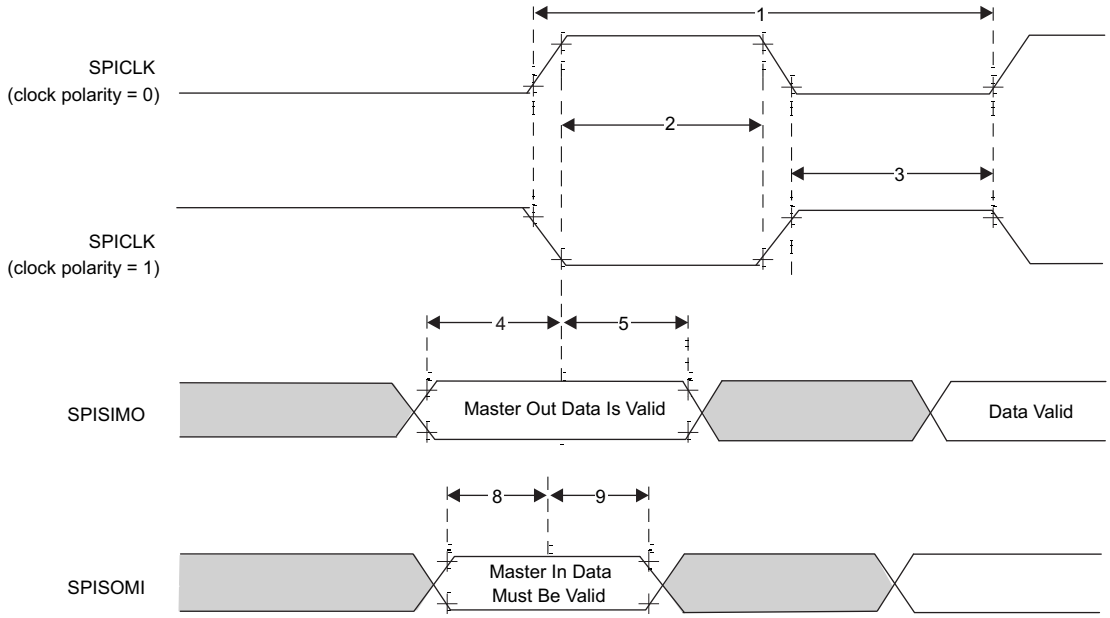


Figure 5-5. SPI Master Mode External Timing (CLOCK PHASE = 1)

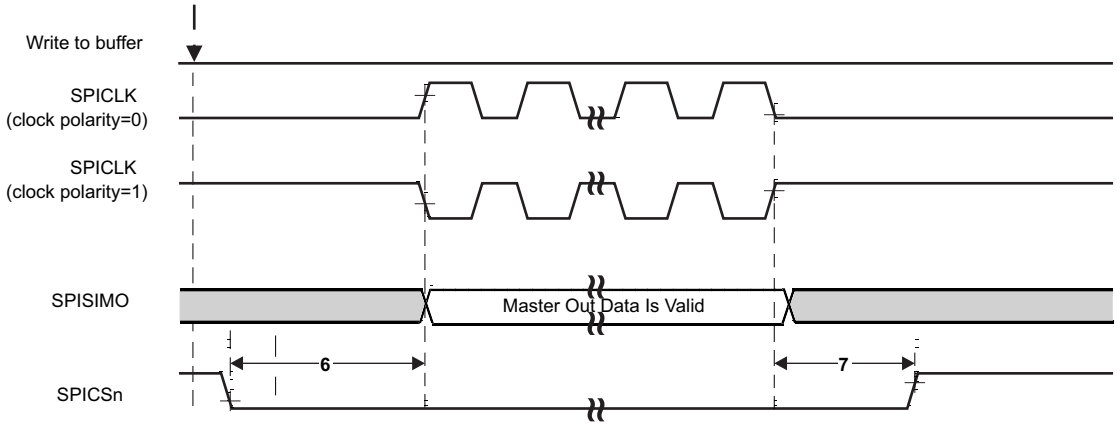


Figure 5-6. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)

5.10.3.3 SPI Slave Mode I/O Timings

Table 5-10. SPI Slave Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK(4)	25			ns
2(5)	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	10			ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	10			
3(5)	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	10			ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	10			
4(5)	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)			10	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1)			10	
5(5)	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	2			ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	2			
4(5)	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)			10	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)			10	
5(5)	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	2			ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	2			
6(5)	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	3			ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	3			
7(5)	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	1			ns
	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	1			

(1) The MASTER bit (SPIGCRx.0) is cleared (where x = 0 or 1).
(2) The CLOCK PHASE bit (SPIFMTx.16) is either cleared or set for CLOCK PHASE = 0 or CLOCK PHASE = 1 respectively.
(3) $t_{c(MSS\_VCLK)}$ = master subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(4) When the SPI is in Slave mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS+1)t_{c(MSS\_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.For PS values of 0: $t_{c(SPC)S} = 2t_{c(MSS\_VCLK)} \geq 25$ ns.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

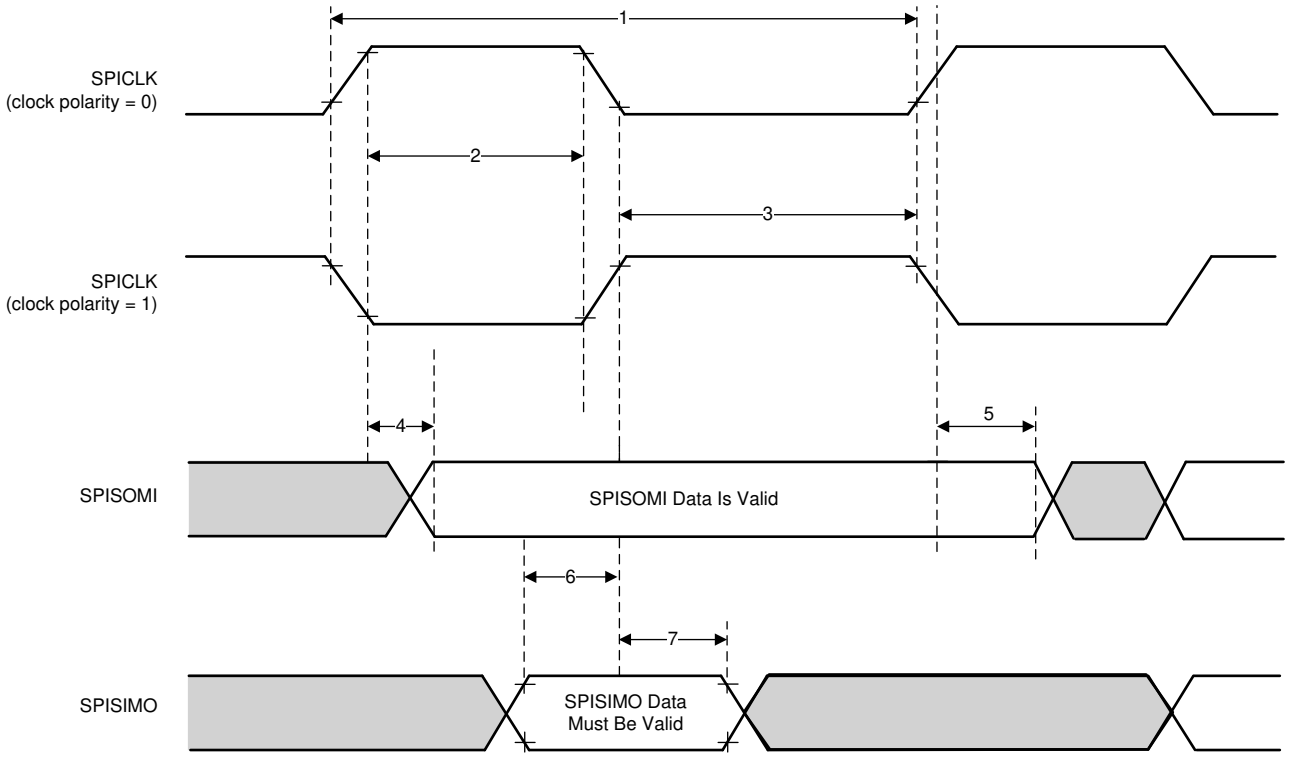


Figure 5-7. SPI Slave Mode External Timing (CLOCK PHASE = 0)

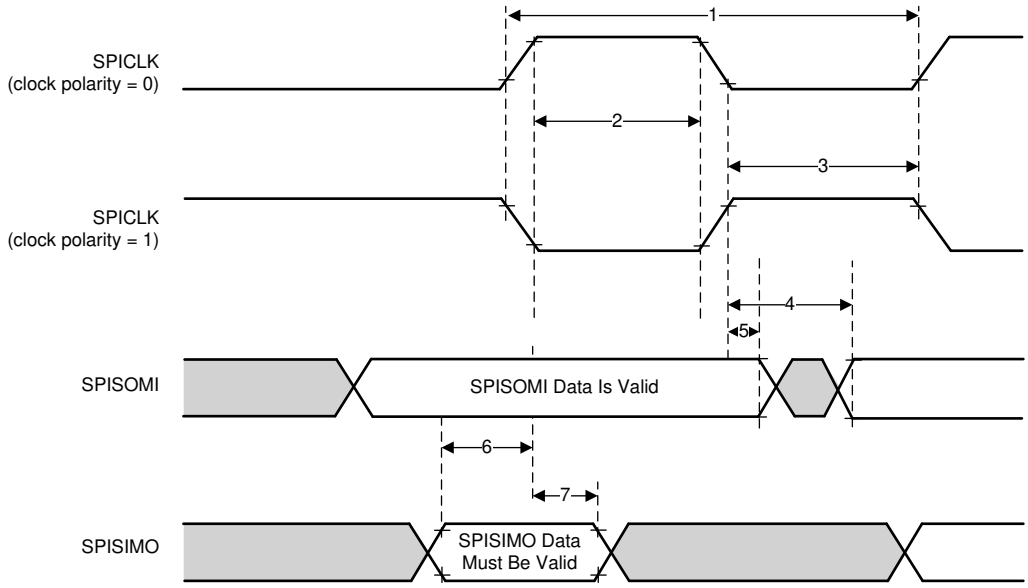


Figure 5-8. SPI Slave Mode External Timing (CLOCK PHASE = 1)

5.10.3.4 Typical Interface Protocol Diagram (Slave Mode)

1. Host should ensure that there is a delay of two SPI clocks between CS going low and start of SPI clock.
2. Host should ensure that CS is toggled for every 16 bits of transfer through SPI.

Figure 5-9 shows the SPI communication timing of the typical interface protocol.

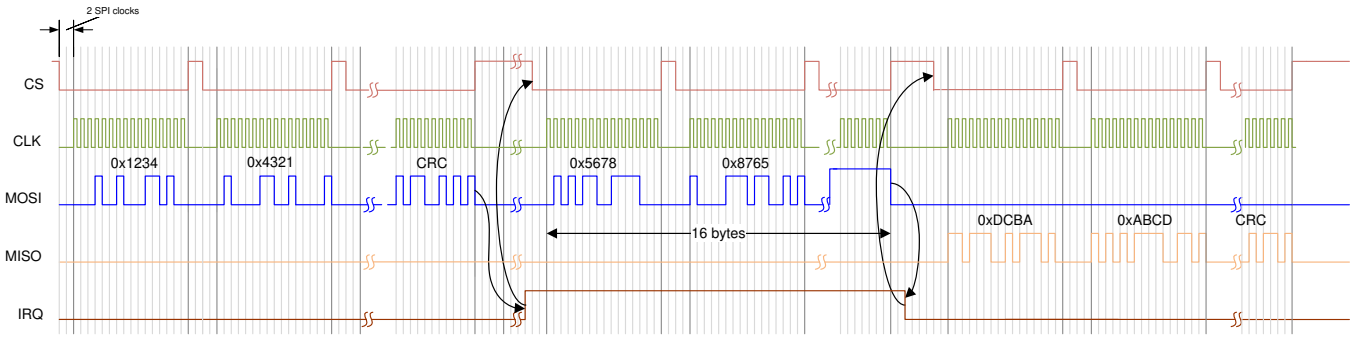


Figure 5-9. SPI Communication

5.10.4 LVDS Interface Configuration

The supported IWR1843 LVDS lane configuration is two Data lanes (LVDS_TXP/M), one Bit Clock lane (LVDS_CLKP/M) and one Frame clock lane (LVDS_FRCLKP/M). The LVDS interface is used for debugging. The LVDS interface supports the following data rates:

- 900 Mbps (450 MHz DDR Clock)
- 600 Mbps (300 MHz DDR Clock)
- 450 Mbps (225 MHz DDR Clock)
- 400 Mbps (200 MHz DDR Clock)
- 300 Mbps (150 MHz DDR Clock)
- 225 Mbps (112.5 MHz DDR Clock)
- 150 Mbps (75 MHz DDR Clock)

Note that the bit clock is in DDR format and hence the numbers of toggles in the clock is equivalent to data.

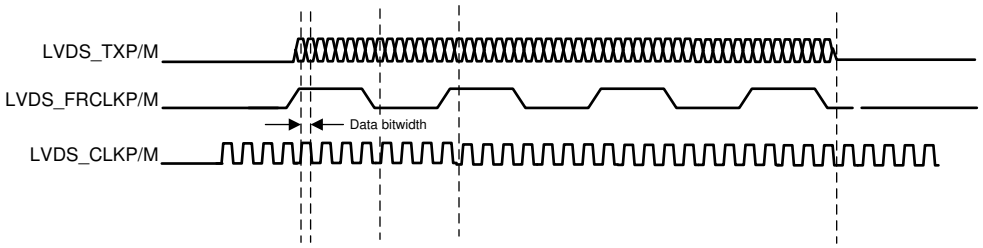


Figure 5-10. LVDS Interface Lane Configuration And Relative Timings

5.10.4.1 LVDS Interface Timings

Table 5-11. LVDS Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty Cycle Requirements	max 1 pF lumped capacitive load on LVDS lanes	48%		52%	
Output Differential Voltage	peak-to-peak single-ended with 100 Ω resistive load between differential pairs	250		450	mV
Output Offset Voltage		1125		1275	mV
Trise and Tfall	20%-80%, 900 Mbps				ps
Jitter (pk-pk)	900 Mbps		80		ps

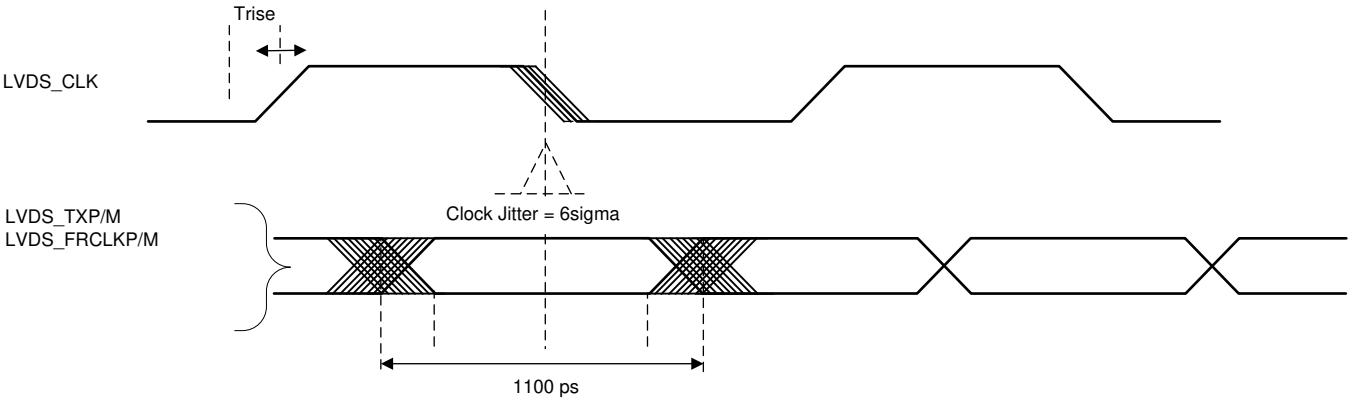


Figure 5-11. Timing Parameters

5.10.5 General-Purpose Input/Output

Table 5-12 lists the switching characteristics of output timing relative to load capacitance.

Table 5-12. Switching Characteristics for Output Timing versus Load Capacitance (C_L)(1)(2)

PARAMETER		TEST CONDITIONS		VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t_r	Max rise time	Slew control = 0	C_L = 20 pF	2.8	3.0	ns
			C_L = 50 pF	6.4	6.9	
			C_L = 75 pF	9.4	10.2	
t_f	Max fall time		C_L = 20 pF	2.8	2.8	ns
			C_L = 50 pF	6.4	6.6	
			C_L = 75 pF	9.4	9.8	
t_r	Max rise time	Slew control = 1	C_L = 20 pF	3.3	3.3	ns
			C_L = 50 pF	6.7	7.2	
			C_L = 75 pF	9.6	10.5	
t_f	Max fall time		C_L = 20 pF	3.1	3.1	ns
			C_L = 50 pF	6.6	6.6	
			C_L = 75 pF	9.6	9.6	

(1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

5.10.6 Controller Area Network Interface (DCAN)

The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 Mbps. The DCAN is ideal for applications operating in noisy and harsh environments that require reliable serial communication or multiplexed wiring.

The DCAN has the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 Mbps
- Configurable Message objects
- Individual identifier masks for each message object
- Programmable FIFO mode for message objects
- Suspend mode for debug support
- Programmable loop-back modes for self-test operation
- Direct access to Message RAM in test mode
- Supports two interrupt lines - Level 0 and Level 1
- Automatic Message RAM initialization

Table 5-13. Dynamic Characteristics for the DCANx TX and RX Pins

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CAN\_tx)}$	Delay time, transmit shift register to CAN_tx pin(1)			15	ns
$t_{d(CAN\_rx)}$	Delay time, CAN_rx pin to receive shift register(1)			10	ns

(1) These values do not include rise/fall times of the output buffer.

5.10.7 Controller Area Network - Flexible Data-rate (CAN-FD)

The CAN-FD module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The CAN-FD has the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1
- Full CAN FD support (up to 64 data bytes per frame)
- AUTOSAR and SAE J1939 support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 11-bit filter elements
- Internal Loopback mode for self-test
- Mask-able interrupts, two interrupt lines
- Two clock domains (CAN clock / Host clock)
- Parity / ECC support - Message RAM single error correction and double error detection (SECDED) mechanism
- Full Message Memory capacity (4352 words).

Table 5-14. Dynamic Characteristics for the CANx TX and RX Pins

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CAN\_FD\_tx)}$	Delay time, transmit shift register to CAN_FD_tx pin(1)			15	ns
$t_{d(CAN\_FD\_rx)}$	Delay time, CAN_FD_rx pin to receive shift register(1)			10	ns

(1) These values do not include rise/fall times of the output buffer.

5.10.8 Serial Communication Interface (SCI)

The SCI has the following features:

- Standard universal asynchronous receiver-transmitter (UART) communication
- Standard non-return to zero (NRZ) format
- Double-buffered receive and transmit functions
- Asynchronous or iso-synchronous communication modes with no CLK pin
- Capability to use Direct Memory Access (DMA) for transmit and receive data
- Two external pins: RS232_RX and RS232_TX

Table 5-15. SCI Timing Requirements

		MIN	TYP	MAX	UNIT
f(baud)	Supported baud rate at 20 pF		921.6		kHz

5.10.9 Inter-Integrated Circuit Interface (I2C)

The inter-integrated circuit (I2C) module is a multimaster communication module providing an interface between devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I^2C-bus™. This module will support any slave or master I2C compatible device.

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - General call
  - START byte
  - Multi-master transmitter/ slave receiver mode
  - Multi-master receiver/ slave transmitter mode
  - Combined master transmit/receive and receive/transmit mode
  - Transfer rates of 100 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

NOTE

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the slave address second byte every time it sends the slave address first byte)

Table 5-16. I2C Timing Requirements(1)

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high	250		100		µs
$t_{h(SCLL-SDA)}$	Hold time, SDA valid after SCL low	0	3.45(1)	0	0.9	µs
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
C_b(2)(3)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum th(SDA-SCLL) for I2C bus devices has only to be met if the device does not stretch the low period (tw(SCLL)) of the SCL signal.
(3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

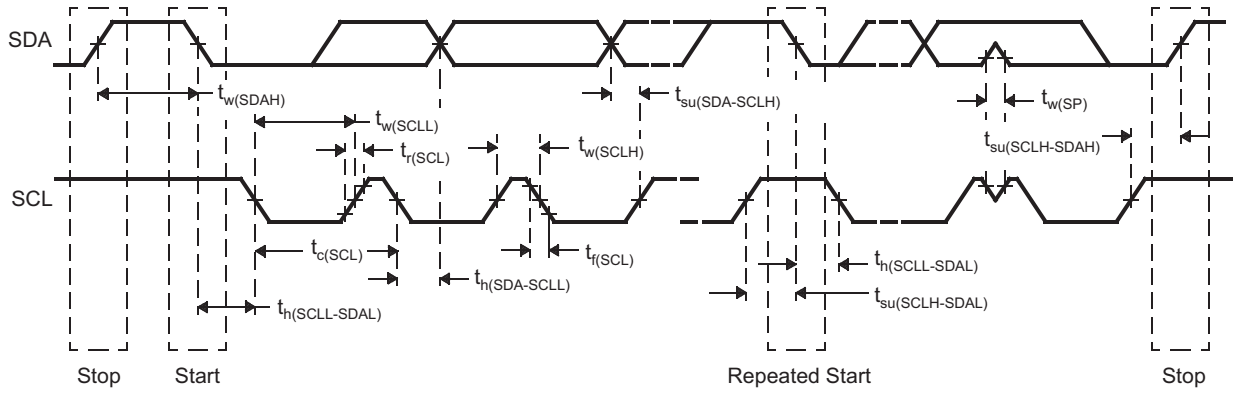


Figure 5-12. I2C Timing Diagram

NOTE

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum th(SDA-SCLL) has only to be met if the device does not stretch the LOW period (tw(SCLL)) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.

5.10.10 Quad Serial Peripheral Interface (QSPI)

The quad serial peripheral interface (QSPI) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a master only. The QSPI in the device is primarily intended for fast booting from quad-SPI flash memories.

The QSPI supports the following features:

- Programmable clock divider
- Six-pin interface
- Programmable length (from 1 to 128 bits) of the words transferred
- Programmable number (from 1 to 4096) of the words transferred
- Support for 3-, 4-, or 6-pin SPI interface
- Optional interrupt generation on word or frame (number of words) completion
- Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles

Table 5-18 and Table 5-19 assume the operating conditions stated in Table 5-17.

Table 5-17. QSPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

Table 5-18. Timing Requirements for QSPI Input (Read) Timings(1)(2)

		MIN	TYP	MAX	UNIT
$t_{su(D-SCLK)}$	Setup time, d[3:0] valid before falling sclk edge (Q12)	7.3			ns
$t_{h(SCLK-D)}$	Hold time, d[3:0] valid after falling sclk edge (Q13)	1.5			ns
$t_{su(D-SCLK)}$	Setup time, final d[3:0] bit valid before final falling sclk edge	7.3 – P(3)			ns
$t_{h(SCLK-D)}$	Hold time, final d[3:0] bit valid after final falling sclk edge	1.5 + P(3)			ns

(1) Clock Mode 0 (clk polarity = 0 ; clk phase = 0) is the mode of operation.
(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.
(3) P = SCLK period in ns.

Table 5-19. QSPI Switching Characteristics

NO.	PARAMETER		MIN	TYP	MAX	UNIT
Q1	$t_{c(SCLK)}$	Cycle time, sclk	25			ns
Q2	$t_{w(SCLKL)}$	Pulse duration, sclk low	0.5*P – 3 (1)			ns
Q3	$t_{w(SCLKH)}$	Pulse duration, sclk high	0.5*P – 3			ns
Q4	$t_{d(CS-SCLK)}$	Delay time, sclk falling edge to cs active edge	–M*P – 1 (2)		–M*P + 2.5 (2)	ns
Q5	$t_{d(SCLK-CS)}$	Delay time, sclk falling edge to cs inactive edge	N*P – 1 (2)		N*P + 2.5 (2)	ns
Q6	$t_{d(SCLK-D1)}$	Delay time, sclk falling edge to d[0] transition	–3.5		7	ns
Q7	$t_{ena(CS-D1LZ)}$	Enable time, cs active edge to d[0] driven (lo-z)	–P – 4 (2)		–P +1 (2)	ns
Q8	$t_{dis(CS-D1Z)}$	Disable time, cs active edge to d[0] tri-stated (hi-z)	–P – 4 (2)		–P +1 (2)	ns
Q9	$t_{d(SCLK-D1)}$	Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only)	–3.5 – P (2)		7 – P (2)	ns

(1) P = SCLK period in ns.
(2) M = QSPI_SPI_DC_REG.DDx + 1, N = 2

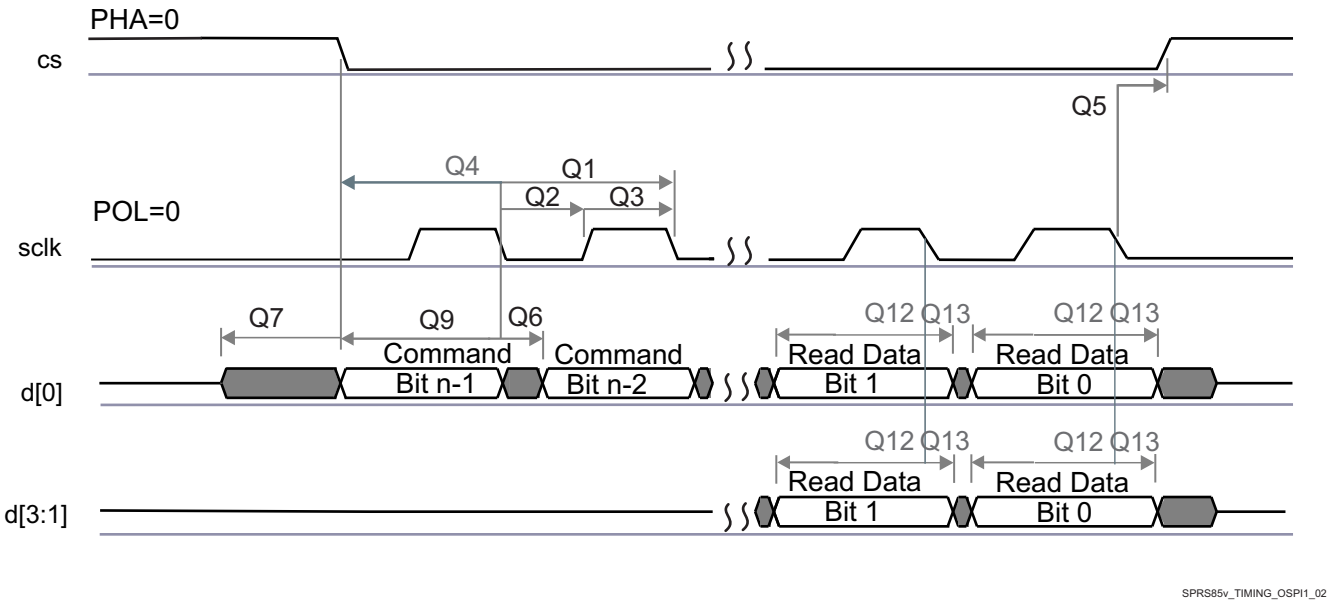


Figure 5-13. QSPI Read (Clock Mode 0)

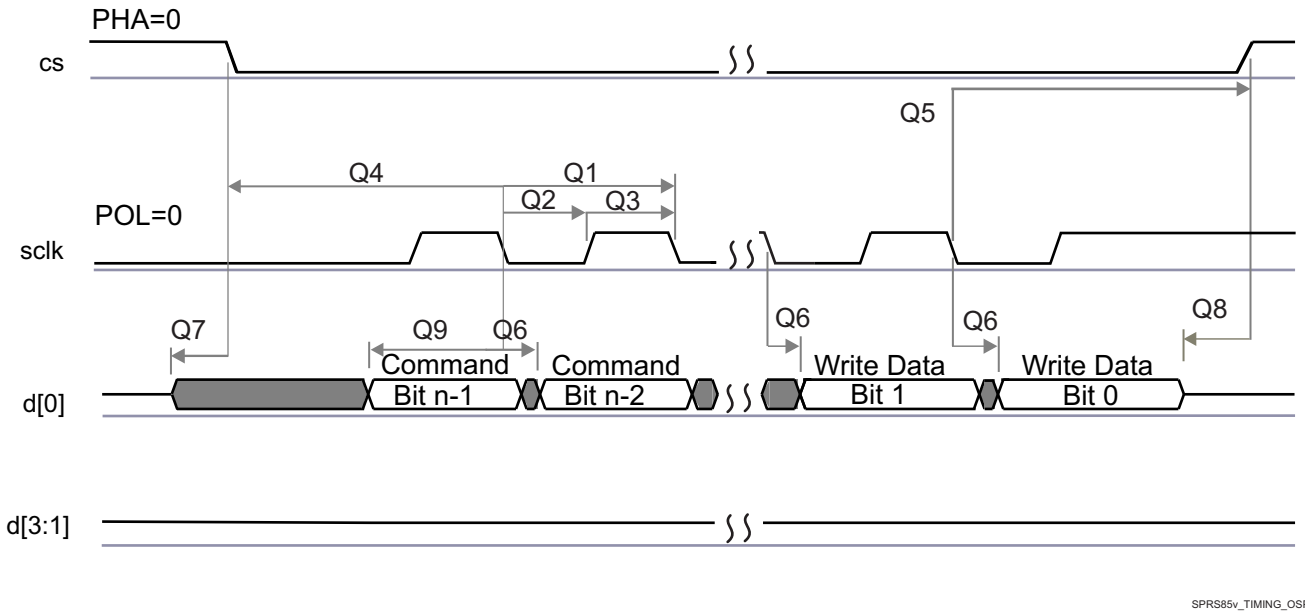


Figure 5-14. QSPI Write (Clock Mode 0)

5.10.11 ETM Trace Interface

Table 5-21 and assume the recommended operating conditions stated in Table 5-20.

Table 5-20. ETMTRACE Timing Conditions

		MIN	TYP	MAX	UNIT
Output Conditions					
C_{LOAD}	Output load capacitance	2		20	pF

Table 5-21. ETM TRACE Switching Characteristics

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{cyc(ETM)}$	Cycle time, TRACECLK period	20			ns
2	$t_{h(ETM)}$	Pulse Duration, TRACECLK High	9			ns
3	$t_{l(ETM)}$	Pulse Duration, TRACECLK Low	9			ns
4	$t_{r(ETM)}$	Clock and data rise time			3.3	ns
5	$t_{f(ETM)}$	Clock and data fall time			3.3	ns
6	$t_{d(ETMTRACECLKH-ETMDATAV)}$	Delay time, ETM trace clock high to ETM data valid	1		7	ns
7	$t_{d(ETMTRACECLKl-ETMDATAV)}$	Delay time, ETM trace clock low to ETM data valid	1		7	ns

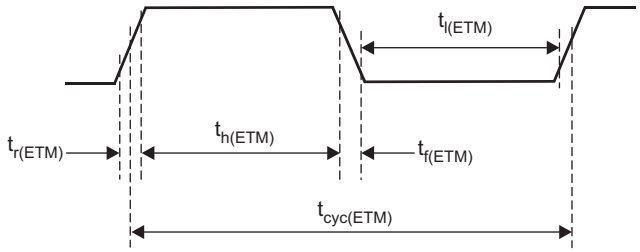


Figure 5-15. ETMTRACECLKOUT Timing

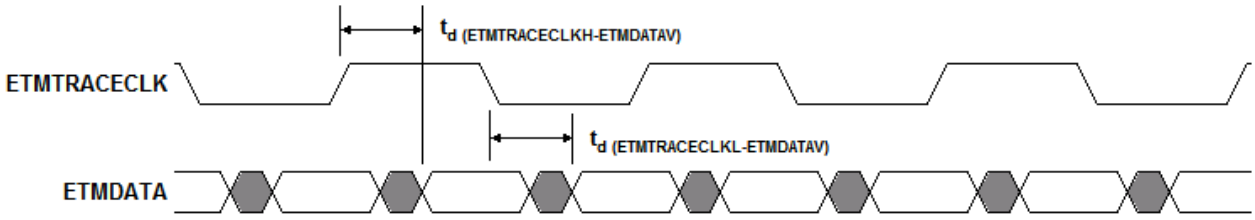


Figure 5-16. ETMDATA Timing

5.10.12 Data Modification Module (DMM)

A Data Modification Module (DMM) gives the ability to write external data into the device memory.

The DMM has the following features:

- Acts as a bus master, thus enabling direct writes to the 4GB address space without CPU intervention
- Writes to memory locations specified in the received packet (leverages packets defined by trace mode of the RAM trace port [RTP] module)
- Writes received data to consecutive addresses, which are specified by the DMM (leverages packets defined by direct data mode of RTP module)
- Configurable port width (1, 2, 4, 8, 16 pins)
- Up to 65 Mbit/s pin data rate

Table 5-22. DMM Timing Requirements

		MIN	TYP	MAX	UNIT
$t_{cyc(DMM)}$	Clock period	15.4			ns
t_R	Clock rise time	1		3	ns
t_F	Clock fall time	1		3	ns
$t_{h(DMM)}$	High pulse width	6			ns
$t_{l(DMM)}$	Low pulse width	6			ns
$t_{ssu(DMM)}$	SYNC active to clk falling edge setup time	2			ns
$t_{sh(DMM)}$	DMM clk falling edge to SYNC deactive hold time	3			ns
$t_{dsu(DMM)}$	DATA to DMM clk falling edge setup time	2			ns
$t_{dh(DMM)}$	DMM clk falling edge to DATA hold time	3			ns

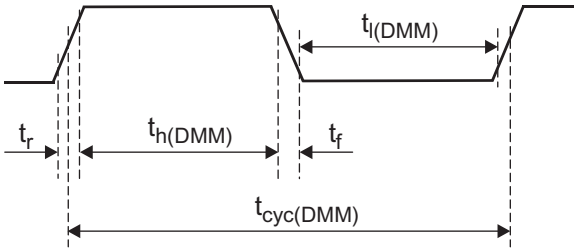


Figure 5-17. DMMCLK Timing

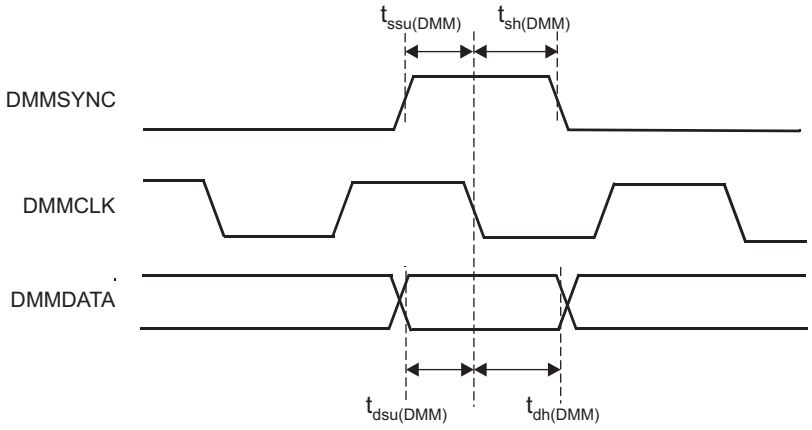


Figure 5-18. DMMDATA Timing

5.10.13 JTAG Interface

Table 5-24 and Table 5-25 assume the operating conditions stated in Table 5-23.

Table 5-23. JTAG Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

Table 5-24. Timing Requirements for IEEE 1149.1 JTAG

NO.			MIN	TYP	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time TCK	66.66			ns
1a	$t_{w(TCKH)}$	Pulse duration TCK high (40% of tc)	26.67			ns
1b	$t_{w(TCKL)}$	Pulse duration TCK low(40% of tc)	26.67			ns
3	$t_{su(TDI-TCK)}$	Input setup time TDI valid to TCK high	2.5			ns
	$t_{su(TMS-TCK)}$	Input setup time TMS valid to TCK high	2.5			ns
4	$t_{h(TCK-TDI)}$	Input hold time TDI valid from TCK high	18			ns
	$t_{h(TCK-TMS)}$	Input hold time TMS valid from TCK high	18			ns

Table 5-25. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

NO.	PARAMETER		MIN	TYP	MAX	UNIT
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0		25	ns

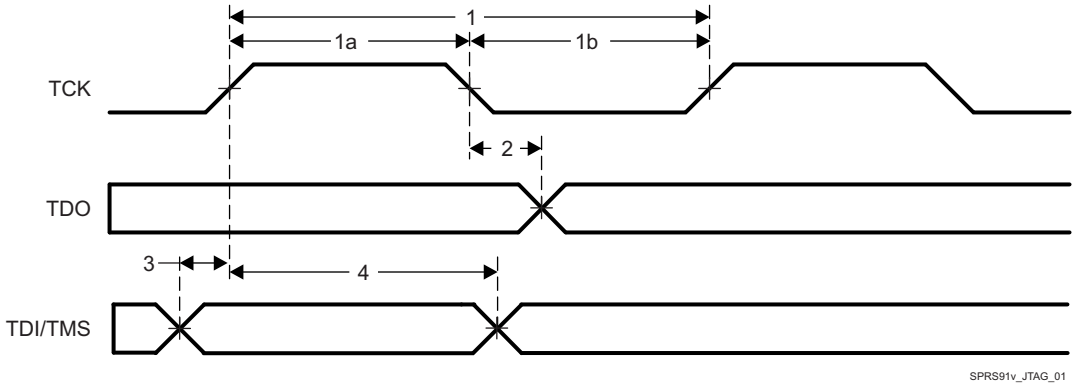


Figure 5-19. JTAG Timing

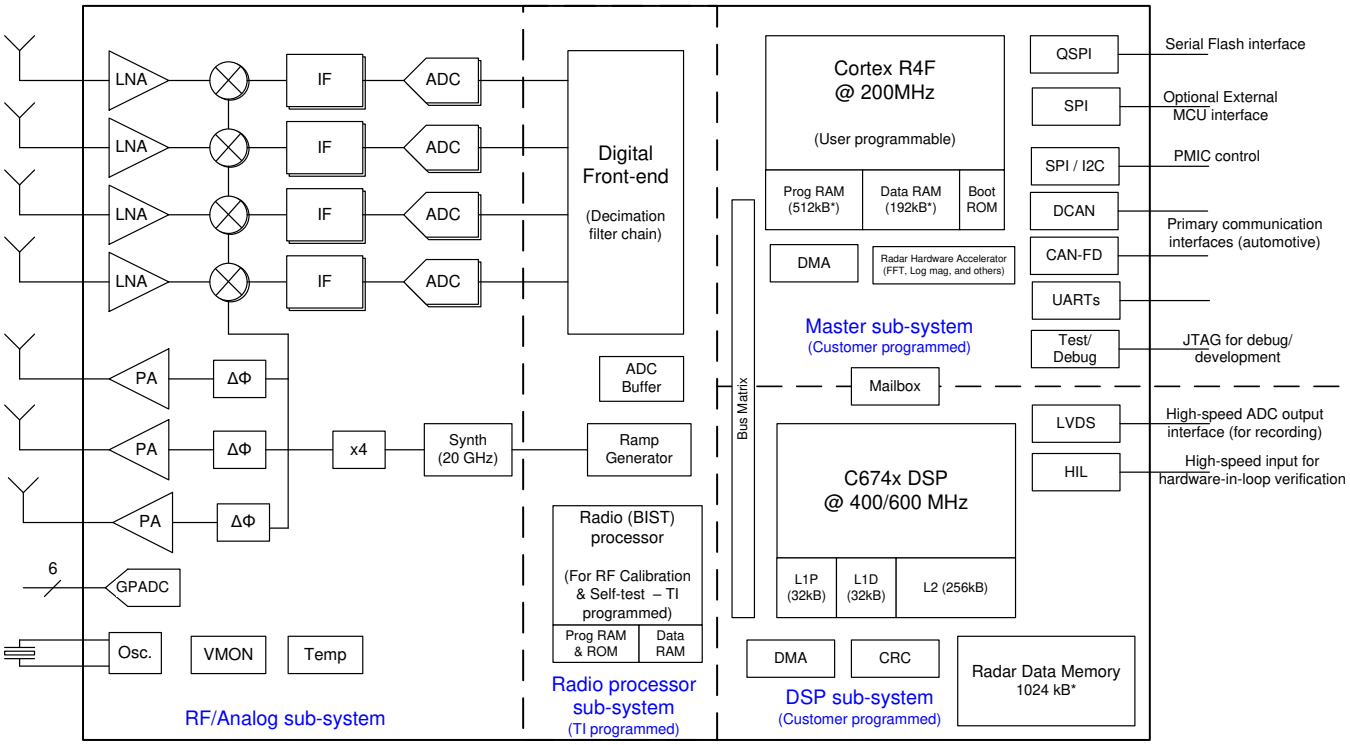
6 Detailed Description

6.1 Overview

The IWR1843 device includes the entire Millimeter Wave blocks and analog baseband signal chain for three transmitters and four receivers, as well as a customer-programmable MCU, Radar Hardware accelerator, and a DSP. This device is applicable as a radar-on-a-chip in use-cases with modest requirements for memory, processing capacity, and application code size. These could be cost-sensitive industrial radar-sensing applications. Examples are:

- Industrial-level sensing
- Industrial automation sensor fusion with radar
- Traffic intersection monitoring with radar
- Industrial radar-proximity monitoring
- People counting
- Gesturing

6.2 Functional Block Diagram



* Up to 512kB of Radar Data Memory can be switched to the Master R4F program and data RAMs

Figure 6-1. Functional Block Diagram

6.3 Subsystems

6.3.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The three transmit channels can be operated up to a maximum of two at a time (simultaneously) for transmit beamforming purpose as required; whereas the four receive channels can all be operated simultaneously.

6.3.1.1 Clock Subsystem

The IWR1843 clock subsystem generates 76 to 81 GHz from an input reference of 40-MHz crystal. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X4 multiplier to create the required frequency in the 76 to 81 GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

Figure 6-2 describes the clock subsystem.

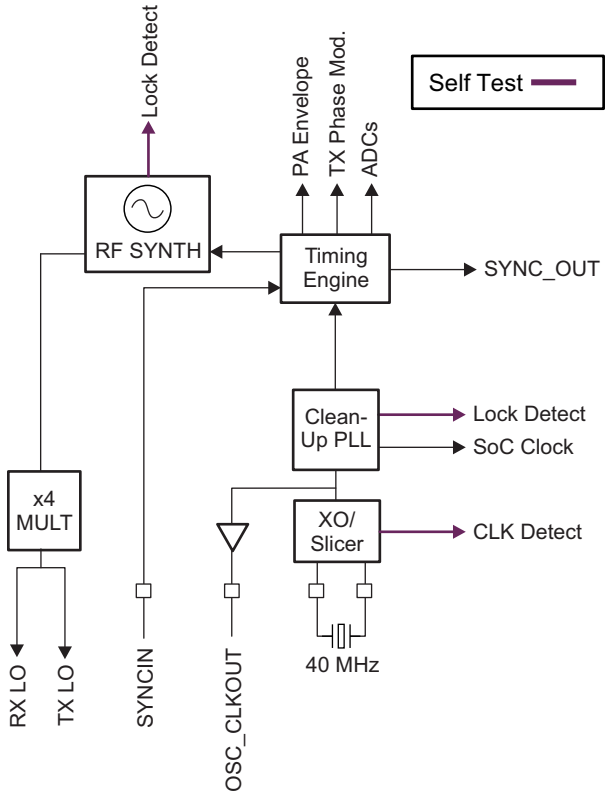


Figure 6-2. Clock Subsystem

6.3.1.2 Transmit Subsystem

The IWR1843 transmit subsystem consists of three parallel transmit chains, each with independent phase and amplitude control. All three transmitters can be used simultaneously. For IWR1843, additional phase shifters are associated with Tx channels, and these can programmed on a per chirp basis.

Each transmit chain can deliver a maximum of 12 dBm at the antenna port on the PCB. The transmit chains also support programmable backoff for system optimization.

Figure 6-3 describes the transmit subsystem.

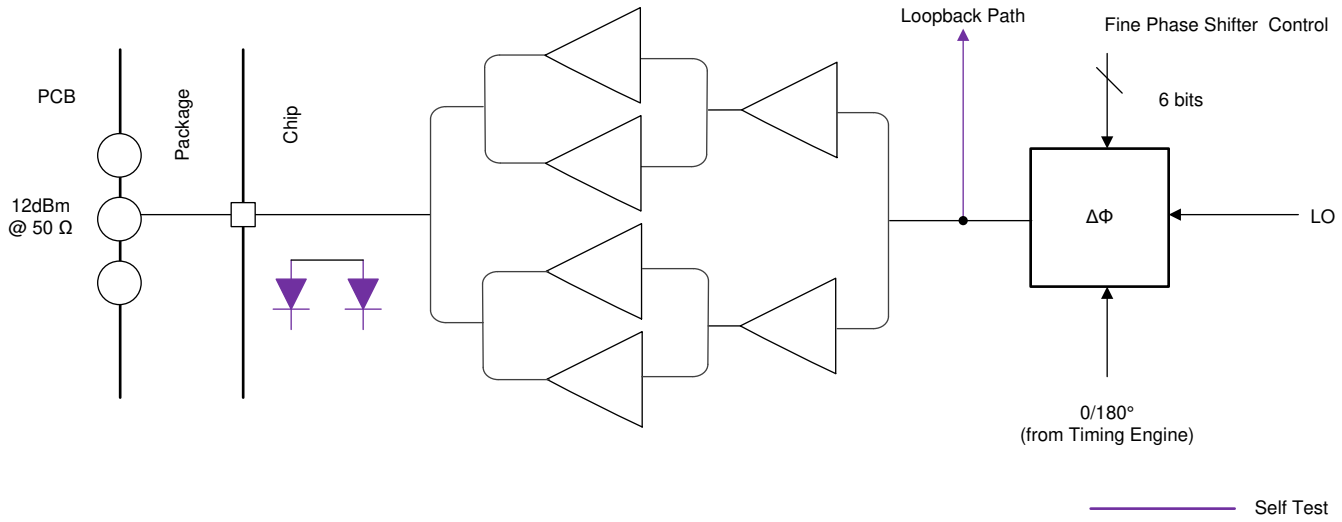


Figure 6-3. Transmit Subsystem (Per Channel)

6.3.1.3 Receive Subsystem

The IWR1843 receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, A2D conversion, and decimation. All four receive channels can be operational at the same time an individual power-down option is also available for system optimization.

Unlike conventional real-only receivers, the IWR1843 device supports a complex baseband architecture, which uses quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs for each receiver channel. The IWR1843 is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175 kHz and can support bandwidths up to 10 MHz.

Figure 6-4 describes the receive subsystem.

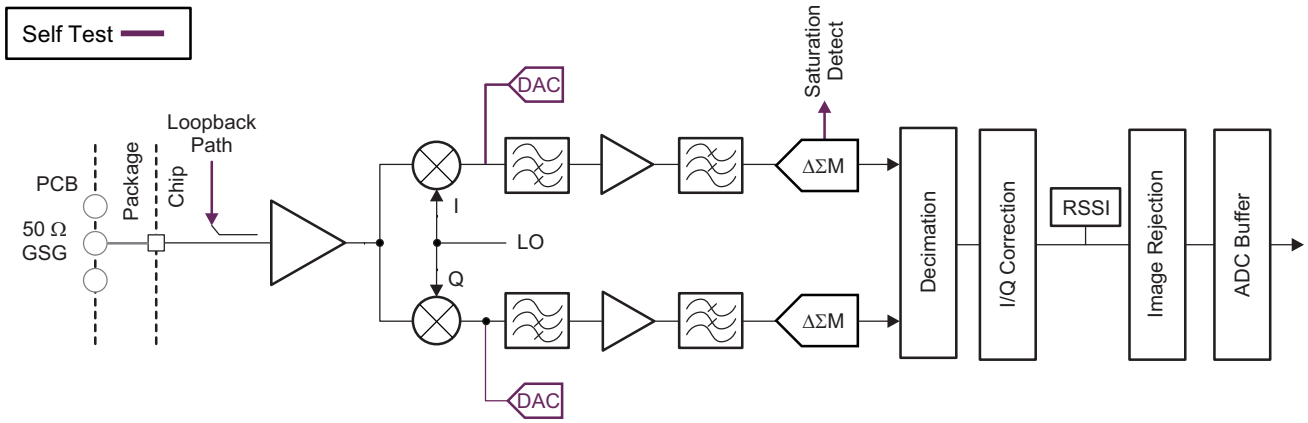


Figure 6-4. Receive Subsystem (Per Channel)

6.3.2 Processor Subsystem

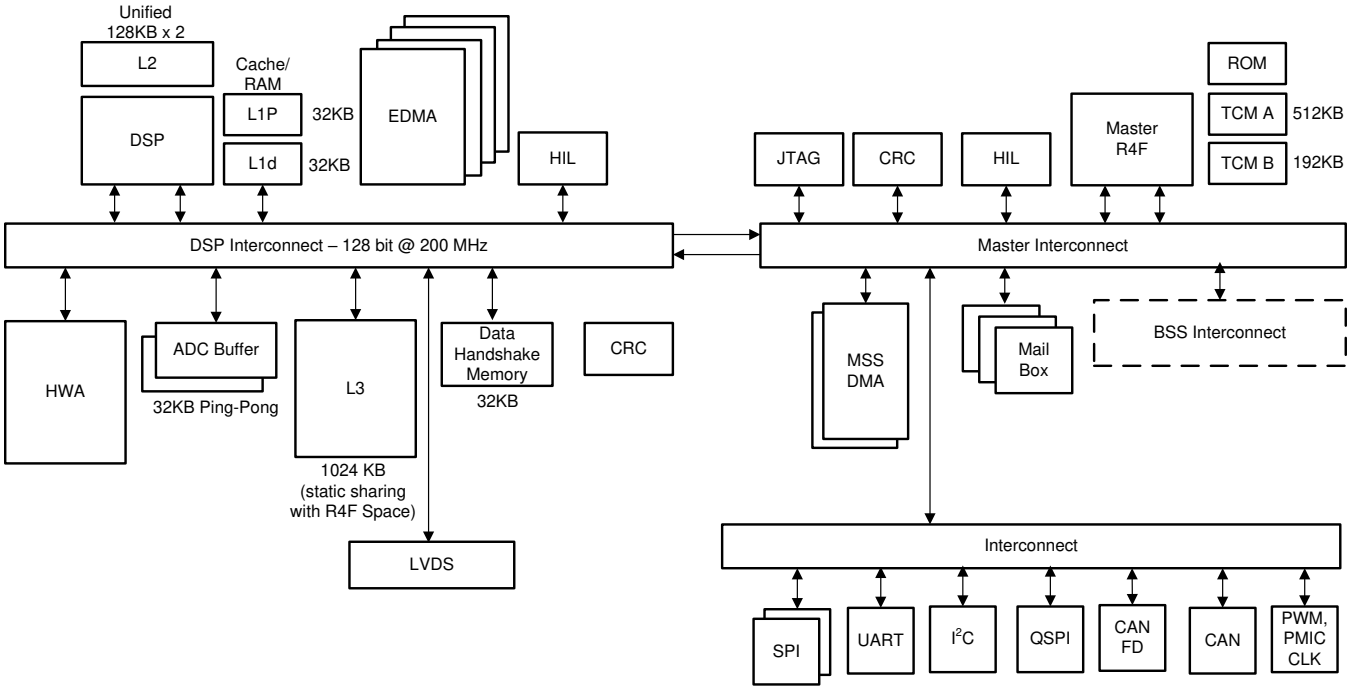


Figure 6-5. Processor Subsystem

Figure 6-5 shows the block diagram for customer programmable processor subsystems in the IWR1843 device. At a high level there are two customer programmable subsystems, as shown separated by a dotted line in the diagram. Left hand side shows the DSP Subsystem which contains TI's high-performance C674x DSP, a hardware accelerator, a high-bandwidth interconnect for high performance (128-bit, 200MHz), and associated peripherals – four DMAs for data transfer,

LVDS interface for Measurement data output, L3 Radar data cube memory, ADC buffers, CRC engine, and data handshake memory (additional memory provided on interconnect).

The right side of the diagram shows the Master subsystem. Master subsystem as name suggests is the master of the device and controls all the device peripherals and house-keeping activities of the device. Master subsystem contains Cortex-R4F (Master R4F) processor and associated peripherals and house-keeping components such as DMAs, CRC and Peripherals (I^2C, UART, SPIs, CAN, PMIC clocking module, PWM, and others) connected to Master Interconnect through Peripheral Central Resource (PCR interconnect).

Details of the DSP CPU core can be found at http://www.ti.com/product/TMS320C6748.

HIL module is shown in both the subsystems and can be used to perform the radar operations feeding the captured data from outside into the device without involving the RF subsystem. HIL on master SS is for controlling the configuration and HIL on DSPSS for high speed ADC data input to the device. Both HIL modules uses the same IOs on the device, one additional IO (DMM_MUX_IN) allows selecting either of the two.

6.3.3 Host Interface

The host interface can be provided through a SPI, UART, or CAN-FD interface. In some cases the serial interface for industrial applications is transcoded to a different serial standard.

The IWR1843 device communicates with the host radar processor over the following main interfaces:

- Reference Clock – Reference clock available for host processor after device wakeup
- Control – 4-port standard SPI (slave) for host control. All radio control commands (and response) flow through this interface.
- Reset – Active-low reset for device wakeup from host
- Host Interrupt - an indication that the mmwave sensor needs host interface
- Error – Used for notifying the host in case the radio controller detects a fault

6.3.4 Master Subsystem Cortex-R4F Memory Map

Table 6-1 shows the master subsystem, Cortex-R4F memory map.

NOTE

There are separate Cortex-R4F addresses and DMA MSS addresses for the master subsystem. See the Technical Reference Manual for a complete list.

Table 6-1. Master Subsystem, Cortex-R4F Memory Map

NAME	FRAME ADDRESS (HEX)		SIZE	DESCRIPTION
	START	END		
CPU Tightly-Coupled Memories				
TCMA ROM	0x0000_0000	0x0001_FFFF	128 KiB	Program ROM
TCM RAM-A	0x0020_0000	0x0023_FFFF (or 0x0027_FFFF)	512 KiB	
TCM RAM-B	0x0800_0000	0x0802_FFFF	192 KB	Data RAM
S/W Scratch Pad Memory				
SW_ Buffer	0x0C20_0000	0x0C20_1FFF	8 KB	S/W Scratchpad memory
System Peripherals				
Mail Box MSS<->RADARSS	0xF060_1000	0xF060_17FF	2 KB	RADARSS to MSS mailbox memory space
	0xF060_2000	0xF060_27FF		MSS to RADARSS mailbox memory space
	0xF060_8000	0xF060_80FF	188 B	MSS to RADARSS mailbox Configuration registers
	0xF060_8060	0xF060_86FF		RADARSS to MSS mailbox Configuration registers
Mail Box MSS<->DSPSS	0xF060_4000	0xF060_47FF	2 KB	DSPSS to MSS mailbox memory space
	0xF060_5000	0xF060_57FF		MSS to DSPSS mailbox memory space
	0xF060_8400	0xF060_84FF	188 B	MSS to DSPSS mailbox Configuration registers
	0xF060_8300	0xF060_83FF		DSPSS to MSS mailbox Configuration registers
Mail Box RADARSS<->DSPSS	0xF060_6000	0xF060_67FF	2 KB	RADARSS to DSPSS mailbox memory space
	0xF060_7000	0xF060_7FFF		DSPSS to RADARSS mailbox memory space
	0xF060_8200	0xF060_82FF	188 B	RADARSS to DSPSS mailbox Configuration registers
	0xF060_8100	0xF060_81FF		DSPSS to RADARSS mailbox Configuration registers
PRCM and Control Module	0xFFFF_E100	0xFFFF_E2FF	756 B	TOP Level Reset, Clock management registers
	0xFFFF_FF00	0xFFFF_FFFF	256 B	MSS Reset, Clock management registers
	0xFFFF_EA00	0xFFFF_EBFF	512 KB	IO Mux module registers
	0xFFFF_F800	0xFFFF_FBFF	352 B	General-purpose control registers

Table 6-1. Master Subsystem, Cortex-R4F Memory Map (continued)

NAME	FRAME ADDRESS (HEX)		SIZE	DESCRIPTION
	START	END		
GIO	0xFFF7_BC00	0xFFF7_BDFF	180 B	GIO module configuration registers
DMA-1	0xFFFF_F000	0xFFFF_F3FF	1 KB	DMA-1 module configuration registers
DMA-2	0xFCFF_F800	0xFCFF_FBFF	1 KB	DMA-2 module configuration registers
DMM-1	0xFCFF_F700	0xFCFF_F7FF	472 B	DMM-1 module configuration registers
DMM-2	0xFCFF_F600	0xFCFF_F6FF	472 B	DMM-2 module configuration registers
VIM	0xFFFF_FD00	0xFFFF_FEFF	512 B	VIM module configuration registers
RTI-A/WD	0xFFFF_FC00	0xFFFF_FCFF	192 B	RTI-A module configuration registers
RTI-B	0xFFFF_EE00	0xFFFF_EEFF	192 B	RTI-B module configuration registers
Serial Interfaces and Connectivity				
QSPI	0xC000_0000	0xC07F_FFFF	8 MB	QSPI –flash memory space
	0xC080_0000	0xC0FF_FFFF	116 B	QSPI module configuration registers
MIBSPI-A	0xFFF7_F400	0xFFF7_F5FF	512 B	MIBSPI-A module configuration registers
MIBSPI-B	0xFFF7_F600	0xFFF7_F7FF	512 B	MIBSPI-B module configuration registers
SCI-A	0xFFF7_E500	0xFFF7_E5FF	148 B	SCI-A module configuration registers
SCI-B	0xFFF7_E700	0xFFF7_E7FF	148 B	SCI-B module configuration registers
CAN	0xFFF7_DC00	0xFFF7_DDFF	512 B	CAN module configuration registers
CAN_FD(MCAN)	0xFFF7_C800	0xFFF7_CFFF	768 B	CAN-FD module configuration registers
	0xFFF7_A000	0xFFF7_A1FF	452 B	MCAN ECC module registers
I2C	0xFFF7_D400	0xFFF7_D4FF	112 B	I2C module configuration registers
Interconnects				
PCR-1	0xFFF7_8000	0xFFF7_87FF	1 KiB	PCR-1 interconnect configuration port
PCR-2	0xFCFF_1000	0xFCFF_17FF	1 KiB	PCR-2 interconnect configuration port
Safety Modules				
CRC	0xFE00_0000	0xFEFF_FFFF	16 KiB	CRC module configuration registers
PBIST	0xFFFF_E400	0xFFFF_E5FF	464 B	PBIST module configuration registers
STC	0xFFFF_E600	0xFFFF_E7FF	284 B	STC module configuration registers
DCC-A	0xFFFF_EC00	0xFFFF_ECFF	44 B	DCC-A module configuration registers
DCC-B	0xFFFF_F400	0xFFFF_F4FF	44 B	DCC-B module configuration registers
ESM	0xFFFF_F500	0xFFFF_F5FF	156 B	ESM module configuration registers
CCMR4	0xFFFF_F600	0xFFFF_F6FF	136 B	CCMR4 module configuration registers
Security Modules				
Crypto	0xFD00_0000	0XFDFF_FFFF	3 KiB	Crypto module configuration registers
Other Subsystems				
DSS_TPTC0	0x5000 0000	0x5000 0317	792 B	TPTC0 module configuration space
DSS_REG	0x5000 0400	0x5000 075F	864 B	DSPSS control module registers
DSS_TPTC1	0x5000 0800	0x5000 0B17	792 B	TPTC1 module configuration space
DSS_REG2	0x5000 0C00	0x5000 0EA3	676 B	DSPSS control module registers
DSS_TPCC0	0x5001 0000	0x5001 3FFF	16 KB	TPCC0 module configuration space
DSS_RTIA/WDT	0x5002 0000	0x5002 00BF	192 B	DSS_RTIA/WDT configuration space
DSS_SCI	0x5003 0000	0x5003 0093	148 B	SCI memory space
DSS_STC	0x5004 0000	0x5004 011B	284 B	STC module configuration space
DSS_CBUFF	0x5007 0000	0x5007 0233	564 B	Common Buffer module configuration registers
DSS_TPTC2	0x5009 0000	0x5009 0317	792 B	TPTC2 module configuration space
DSS_TPTC3	0x5009 0400	0x5009 0717	792 B	TPTC3 module configuration space
DSS_TPCC1	0x500A 0000	0x500A 3FFF	16 KB	TPCC1 module configuration space
DSS_ESM	0x500D 0000	0x500D 005B	92 B	ESM module configuration registers

Table 6-1. Master Subsystem, Cortex-R4F Memory Map (continued)

NAME	FRAME ADDRESS (HEX)		SIZE	DESCRIPTION
	START	END		
DSS_RTIB	0x500F 0000	0x500F 00BF	192 B	RTI-B module configuration registers
DSS_L3RAM Shared memory	0x5100 0000	0x511F FFFF	2 MB (1)	L3 shared memory space
DSS_ADCBUF Buffer	0x5200 0000	0x5200 7FFF	32 KB	ADC buffer memory space
DSS_CBUFF_FIFO	0x5202 0000	0x5202 3FFF	16 KB	Common buffer FIFO space
DSS_HSRAM1	0x5208 0000	0x5208 7FFF	32 KB	Handshake memory space
DSS_DSP_L2_UMAP1	0x577E 0000	0x577F FFFF	128 KB	L2 RAM space
DSS_DSP_L2_UMAP0	0x5780 0000	0x5781 FFFF	128 KB	L2 RAM space
DSS_DSP_L1P	0x57E0 0000	0x57E0 7FFF	32 KB	L1 program memory space
DSS_DSP_L1D	0x57F0 0000	0x57F0 7FFF	32 KB	L1 data memory space
Peripheral Memories (System and Nonsystem)				
CAN RAM	0xFF1E_0000	0xFF1F_FFFF	128 KB	CAN RAM memory space
CAN-FD RAM	0xFF50_0000	0xFF51_FFFF	68 KB	CAN-FD RAM memory space
DMA1 RAM	0xFFF8_0000	0xFFF8_0FFF	4 KB	DMA1 RAM memory space
DMA2 RAM	0xFCF8 1000	0xFCF8_0FFF	4 KB	DMA2 RAM memory space
VIM RAM	0xFFF8_2000	0xFFF8_2FFF	2 KB	VIM RAM memory space
MIBSPIB-TX RAM	0xFF0C_0000	0xFF0C_01FF	0.5 KB	MIBSPIB-TX RAM memory space
MIBSPIB-RX RAM	0xFF0C_0200	0xFF0C_03FF	0.5 KB	MIBSPIB-RX RAM memory space
MIBSPIA-TX RAM	0xFF0E_0000	0xFF0E_01FF	0.5 KB	MIBSPIA-TX RAM memory space
MIBSPIA- RX RAM	0xFF0E_0200	0xFF0E_03FF	0.5 KB	MIBSPIA- RX RAM memory space
Debug Modules				
Debug subsystem	0xFFA0_0000	0xFFAF_FFFF	244 KB	Debug subsystem memory space and registers

(1) 768 KB memory within 2 MB memory space

6.3.5 DSP Subsystem Memory Map

Table 6-2 shows the DSP C674x memory map.

Table 6-2. DSP C674x Memory Map

Name	Frame Address (Hex)		Size	Description
	Start	End		
DSP Memories				
DSP_L1D	0x00F0_0000	0x00F0_7FFF	32 KiB	L1 data memory space
DSP_L1P	0x00E0_0000	0x00E0_7FFF	32 KiB	L1 program memory space
DSP_L2_UMAP0	0x0080_0000	0x0081_FFFF	128 KiB	L2 RAM space
DSP_L2_UMAP1	0x007E_0000	0x007F_FFFF	128 KiB	L2 RAM space
EDMA				
TPCC0	0x0201_0000	0x0201_3FFF	16 KiB	TPCC0 module configuration space
TPCC1	0x020A_0000	0x020A_3FFF	16 KiB	TPCC1 module configuration space
TPTC0	0x0200 0000	0x0200 03FF	1 KiB	TPTC0 module configuration space
TPTC1	0x0200 0800	0x0200 0BFF	1 KiB	TPTC1 module configuration space

Table 6-2. DSP C674x Memory Map (continued)

Name	Frame Address (Hex)		Size	Description
	Start	End		
TPTC2	0x0209_0000	0x0209_03FF	1 KiB	TPTC2 module configuration space
TPTC3	0x0209_0400	0x0209_07FF	1 KiB	TPTC3 module configuration space
Control Registers				
DSS_REG	0x0200_0400	0x0200_07FF	864 B	DSPSS control module registers
DSS_REG2	0x0200_0C00	0x0200_0FFF	624 B	DSPSS control module registers
System Memories				
ADC Buffer	0x2100_0000	0x2100_7FFC	32 KiB	ADC buffer memory space
CBUFF-FIFO	0x2102_0000	0x2102_3FFC	16 KiB	Common buffer FIFO space
L3-Shared memory	0x2000_0000	0x201F_FFFF	2 MB	L3 shared memory space
HS-RAM	0x2108_0000	0x2108_7FFC	32 KiB	Handshake memory space
System Peripherals				
RTI-A/WD	0x0202_0000	0x0202_00FF	192 B	RTI-A module configuration registers
RTI-B	0x020F_0000	0x020F_00FF	192 B	RTI-B module configuration registers
CBUFF	0x0207_0000	0x0207_03FF	564 B	Common Buffer module Configuration registers
Mail Box MSS<->RADARSS	0x5060_1000	0x5060_17FF	2 KiB	RADARSS to MSS mailbox memory space
	0x5060_2000	0x5060_27FF		MSS to RADARSS mailbox memory space
	0x0460_8000	0x0460_80FF	188 B	MSS to RADARSS mailbox Configuration registers
	0x0460_8060	0x0460_86FF		RADARSS to MSS mailbox Configuration registers
Mail Box MSS<->DSPSS	0x5060_4000	0x5060_47FF	2 KiB	DSPSS to MSS mailbox memory space
	0x5060_5000	0x5060_57FF		MSS to DSPSS mailbox memory space
	0x0460_8400	0x0460_84FF	188 B	MSS to DSPSS mailbox Configuration registers
	0x0460_8300	0x0460_83FF		DSPSS to MSS mailbox Configuration registers
Mail Box RADARSS<->DSPSS	0x5060_6000	0x5060_67FF	2 KiB	RADARSS to DSPSS mailbox memory space
	0x5060_7000	0x5060_7FFF		DSPSS to RADARSS mailbox memory space
	0x0460_8200	0x0460_82FF	188 B	RADARSS to DSPSS mailbox Configuration registers
	0x0460_8100	0x0460_81FF		DSPSS to RADARSS mailbox Configuration registers
Safety Modules				
ESM	0x020D_0000		92 B	ESM module Configuration registers

Table 6-2. DSP C674x Memory Map (continued)

Name	Frame Address (Hex)		Size	Description
	Start	End		
CRC	0x2200_0000	0x2200_03FF	1 KiB	CRC module Configuration registers
STC	0x0204_0000	0x0204_01FF	284 B	STC module Configuration registers
Nonsystem Peripherals				
SCI	0x0203_0000	0x0203_00FF	148 B	SCI module Configuration registers

6.3.6 Hardware Accelerator

The Radar Hardware Accelerator (HWA) is an IP that enables off-loading the burden of certain frequently used computations in FMCW radar signal processing from the main processor. FMCW radar signal processing involves the use of FFT and Log-Magnitude computations to obtain a radar image across the range, velocity, and angle dimensions. Some of the frequently used functions in FMCW radar signal processing can be done within the radar hardware accelerator, while still retaining the flexibility of implementing other proprietary algorithms in the main processor. See the Radar Hardware Accelerator User's Guide for a functional description and features of this module and see the Technical Reference Manual for a complete list of register and memory map.

6.4 Other Subsystems

6.4.1 ADC Channels (Service) for User Application

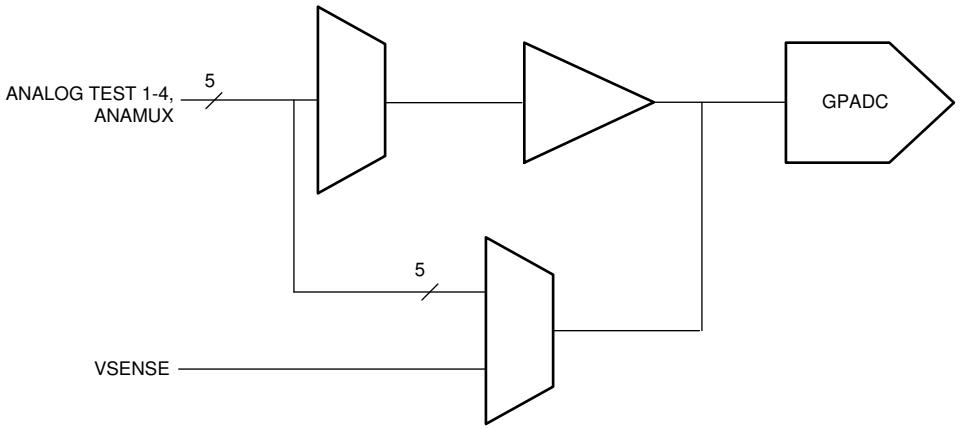
The IWR1843 device includes provision for an ADC service for user application, where the

GPADC engine present inside the device can be used to measure up to six external voltages. The ADC1, ADC2, ADC3, ADC4, ADC5, and ADC6 pins are used for this purpose.

- ADC itself is controlled by TI firmware running inside the BIST subsystem and access to it for customer's external voltage monitoring purpose is via 'monitoring API' calls routed to the BIST subsystem. This API could be linked with the user application running on the Master R4.
- BIST subsystem firmware will internally schedule these measurements along with other RF and Analog monitoring operations. The API allows configuring the settling time (number of ADC samples to skip) and number of consecutive samples to take. At the end of a frame, the minimum, maximum and average of the readings will be reported for each of the monitored voltages.

GPADC Specifications:

- 625 Ksps SAR ADC
- 0 to 1.8V input range
- 10-bit resolution
- For 5 out of the 6 inputs, an optional internal buffer is available. Without the buffer, the ADC has a switched capacitor input load modeled with 5pF of sampling capacitance and 12pF parasitic capacitance (GPADC channel 6, the internal buffer is not available).



A. GPADC structures are used for measuring the output of internal temperature sensors. The accuracy of these measurements is ±7ºC.

Figure 6-6. ADC Path

Table 6-3. GP-ADC Parameter

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TYP	UNIT
ADC supply	1.8	V
ADC unbuffered input voltage range	0 – 1.8	V
ADC buffered input voltage range (1)	0.4 – 1.3	V
ADC resolution	10	bits
ADC offset error	±5	LSB
ADC gain error	±5	LSB
ADC DNL	–1/+2.5	LSB
ADC INL	±2.5	LSB
ADC sample rate (2)	625	Ksps
ADC sampling time (2)	400	ns
ADC internal cap	10	pF
ADC buffer input capacitance	2	pF
ADC input leakage current	3	uA

(1) Outside of given range, the buffer output will become nonlinear.
(2) ADC itself is controlled by TI firmware running inside the BIST subsystem. For more details please refer to the API calls.

7 Monitoring and Diagnostics

7.1 Monitoring and Diagnostic Mechanisms

Table 7-1 is a list of the main monitoring and diagnostic mechanisms available in the IWR1843.

Table 7-1. Monitoring and Diagnostic Mechanisms for IWR1843

NO	FEATURE	DESCRIPTION
1	Temperature Sensors	IWR1843 architecture supports various temperature sensors all across the device (next to power hungry modules such as PAs, DSP, etc.) which is monitored during the inter-frame period.(1)
2	RX saturation detect	Provision to detect ADC saturation du;e to excessive incoming signal level and/or interference.

(1) Monitoring is done by the TI's code running on BIST R4F. There are two modes in which it could be configured to report the temperature sensed via API by customer application.
- Report the temperature sensed after every N frames
- Report the condition once the temperature crosses programmed threshold.

It is completely up to customer SW to decide on the appropriate action based on the message from BIST R4Fvia Mailbox.

7.1.1 Error Signaling Module

When a diagnostic detects a fault, the error must be indicated. IWR1843 architecture provides aggregation of fault indication from internal diagnostic mechanisms using a peripheral logic known as the error signaling module (ESM). The ESM provides mechanisms to classify faults by severity and allows programmable error response. Below is the high level block diagram for ESM module.

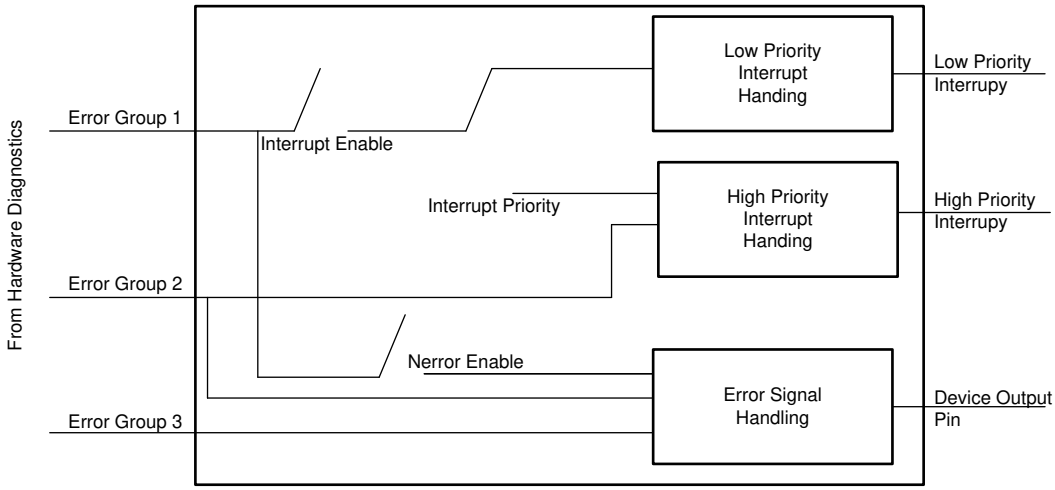


Figure 7-1. ESM Module Diagram

8 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The IWR1843 can be a radar sensor, or can be combined with an MSP432, or for LVDS processing with a LVDS to DSP subsystem for more advanced applications. Some applications are:

- Liquid and solid level sensing for process sensors or industrial automation
- Industrial proximity sensing, non-contact sensing for security, traffic monitoring, and industrial transportation
- Sensor fusion of camera and radar instruments for security, factory automation, robotics
- Sensor fusion with multiple camera and radar instruments for object identification, manipulation, and flight avoidance for security, robotics, material handling, or drone devices
- People counting
- Gesturing
- Motion detection

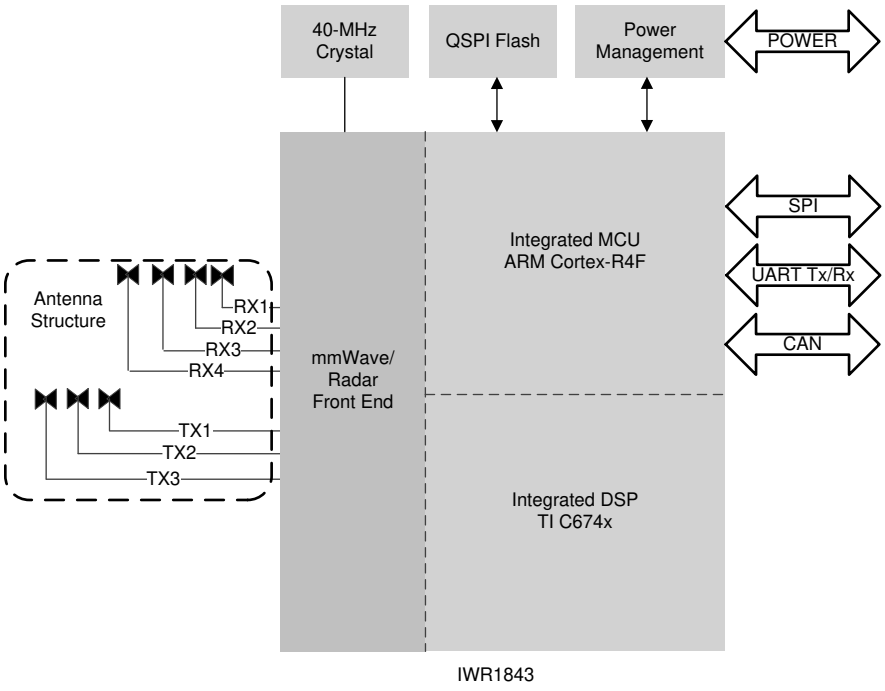


Figure 8-1. Autonomous Sensor For Industrial Applications

8.2 Reference Schematic

Figure 8-2 shows the reference schematic for the IWR1843 device.

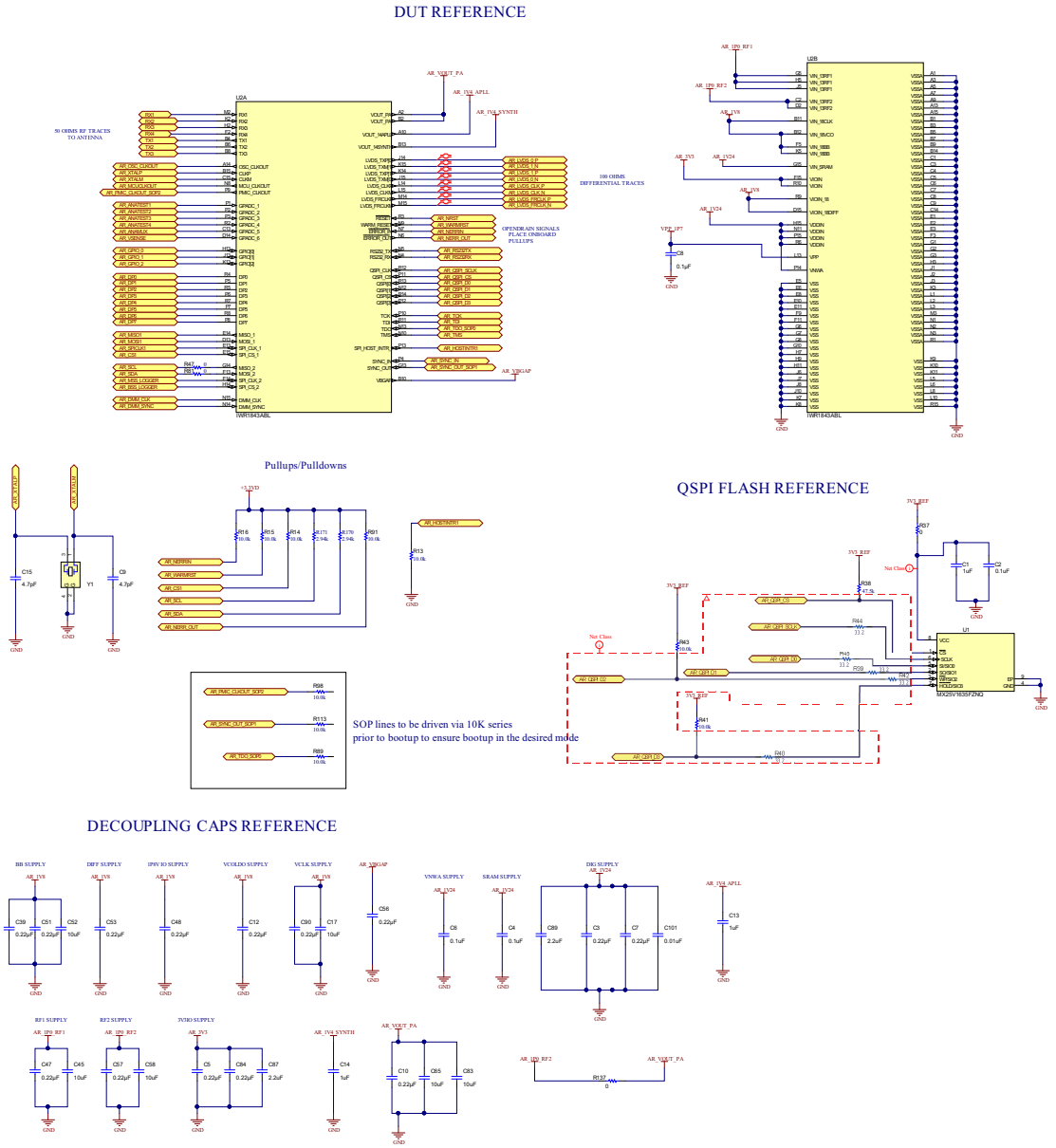


Figure 8-2. IWR1843 Reference Schematic

8.3 Layout

The top layer routing, top layer closeup, and bottom layer routing are shown in Figure 8-3, Figure 8-4, and Figure 8-5, respectively.

8.3.1 Layout Guidelines

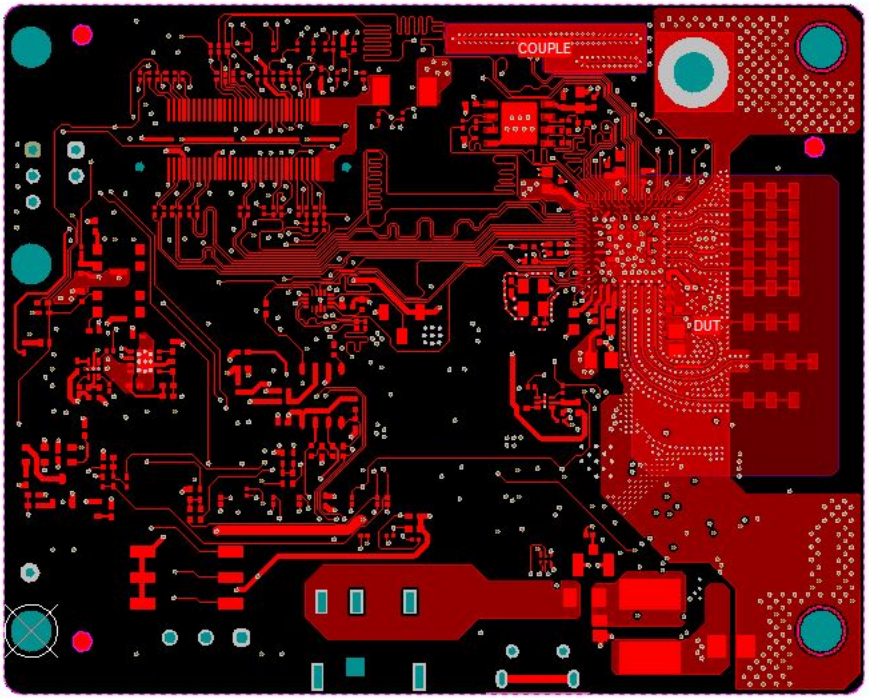


Figure 8-3. Top Layer Routing

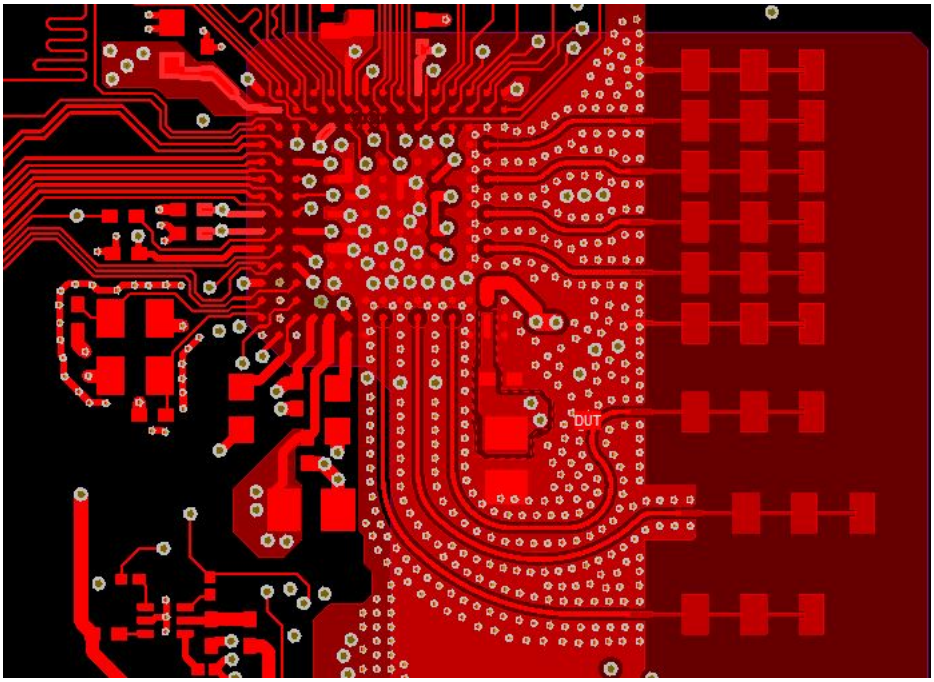


Figure 8-4. Top Layer Routing Closeup

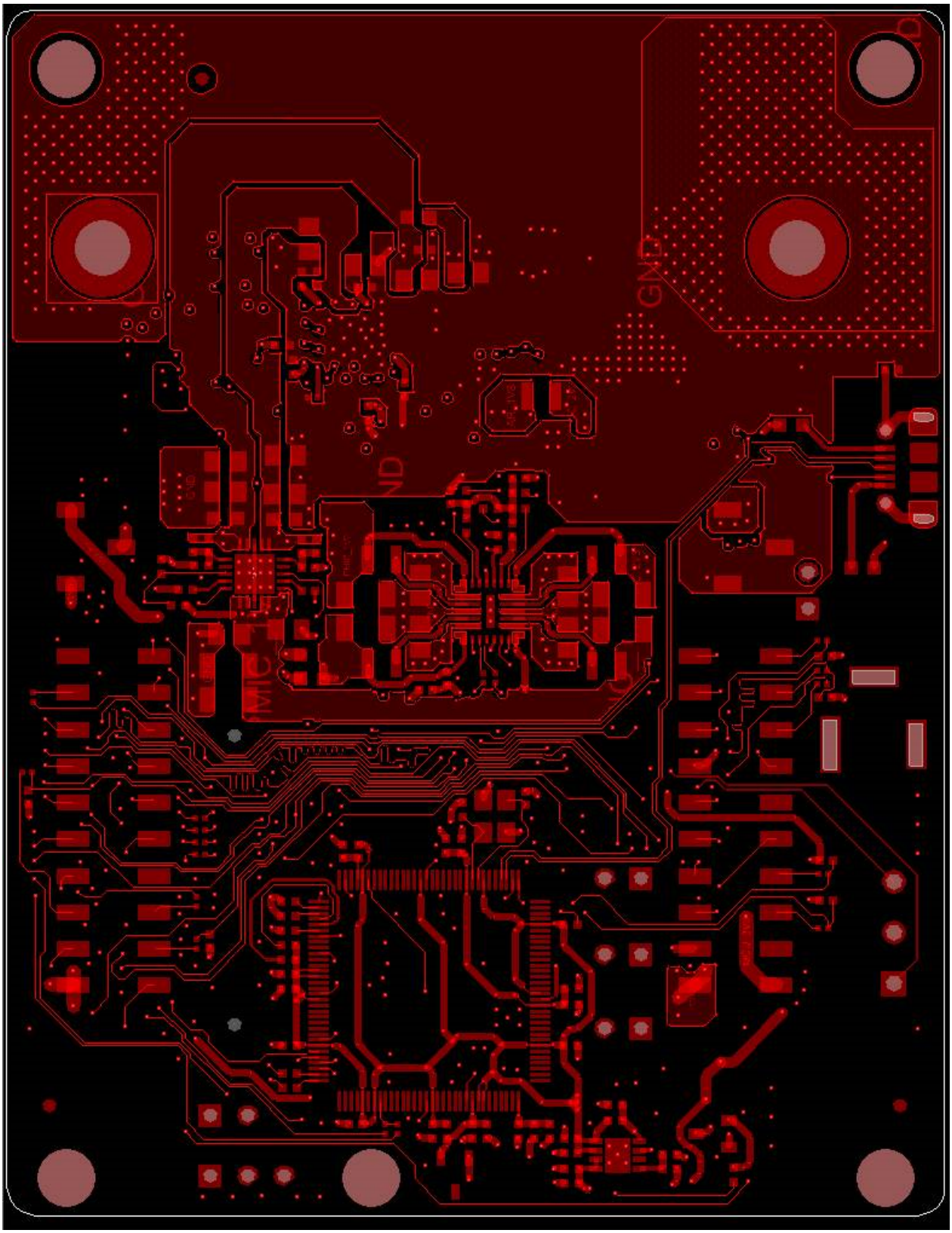
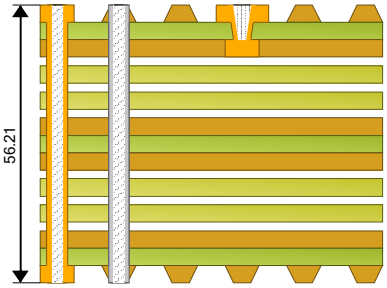


Figure 8-5. Bottom Layer Routing

8.3.2 Stackup Details



Layer	Stack up	Description	Type	Base Thickness	Processed Thickness	εr	Copper Coverage
1				0.689	2.067		100.000
		Rogers 4835 4mil coreH/1 Low Pro	Rogers 4835	4.000	4.000	3.480	
2				1.260	1.260		73.000
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.830	3.700	
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.830	3.700	
3				1.260	1.260		69.000
		Iteq IT180A 28 mil core 1/1	FR4	28.000	28.000	4.280	
4				1.260	1.260		48.000
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.691	3.700	
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.691	3.700	
5				1.260	1.260		72.000
		Iteq IT180A 4 mil core 1/H	FR4	4.000	4.000	3.790	
6				0.689	2.067		100.000

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *IWR1843*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example,), the temperature range (for example, blank is the default commercial temperature range). Figure 9-1 provides a legend for reading the complete device name for any *IWR1843* device.

For orderable part numbers of *IWR1843* devices in the ABL0161 package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *IWR1843 Device Errata*.

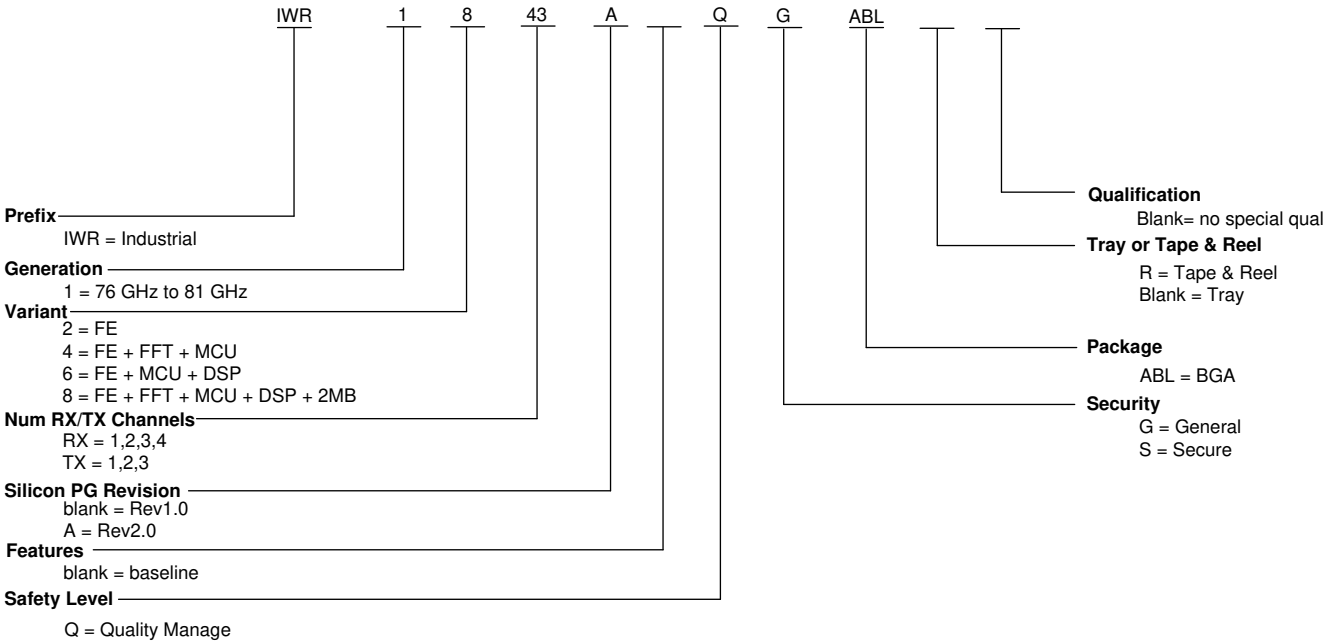


Figure 9-1. Device Nomenclature

9.2 Tools and Software

Models

IWR1843 BSDL model Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.

IWR1843 IBIS model IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.

Software Tools

Code Composer Studio™ (CCS) Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking the user through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

UniFlash Standalone Flash Tool

UniFlash is a standalone tool used to program on-chip flash memory through a GUI, command line, or scripting interface.

9.3 Documentation Support

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (IWR1843). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral follows.

Errata

IWR1843 device errata Describes known advisories, limitations, and cautions on silicon and provides workarounds.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help—straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

E2E is a trademark of Texas Instruments.
ARM, Cortex are registered trademarks of ARM Limited.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

10.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

CAUTION

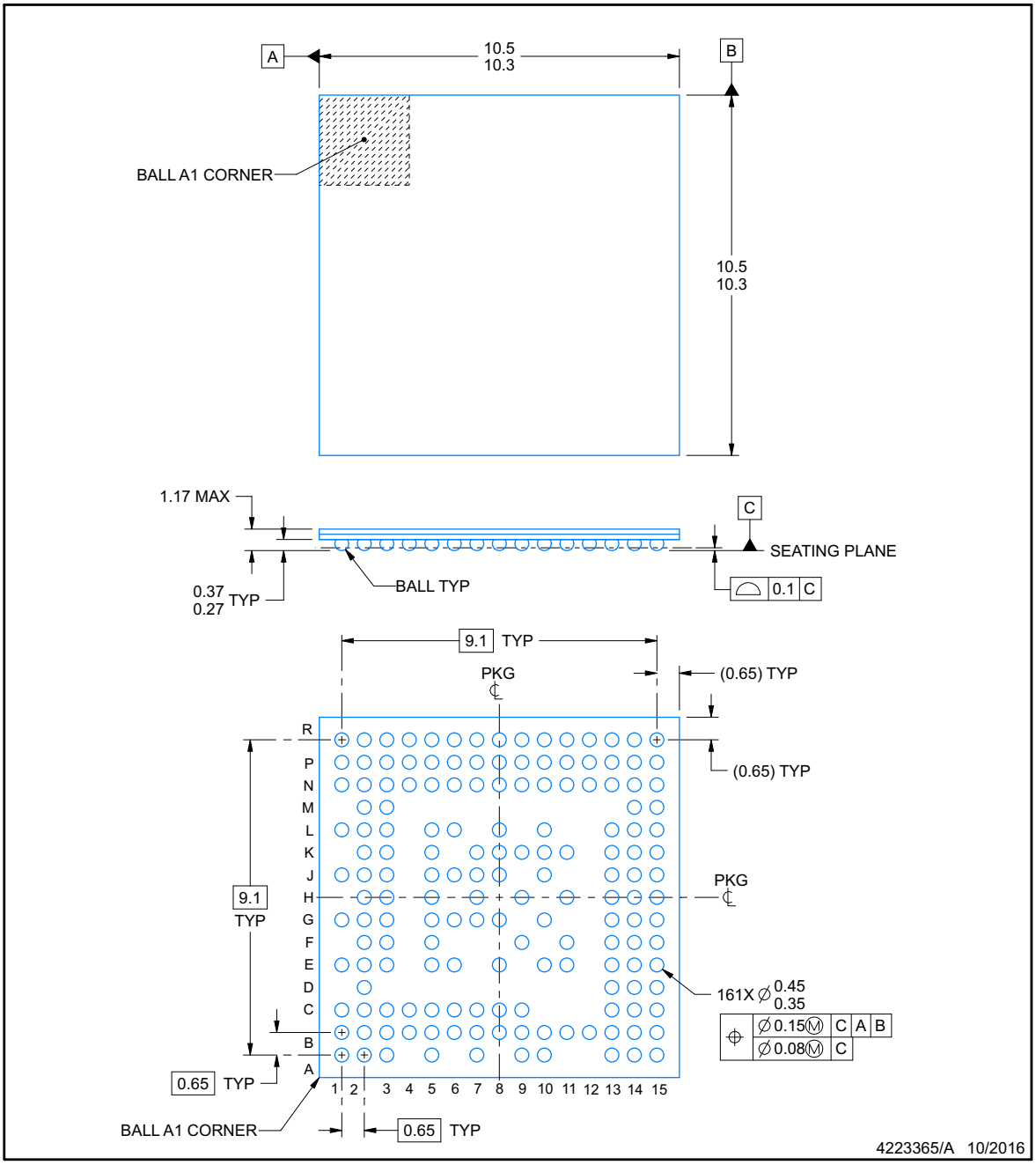
The following package information is subject to change without notice.

PACKAGE OUTLINE

ABL0161B

FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

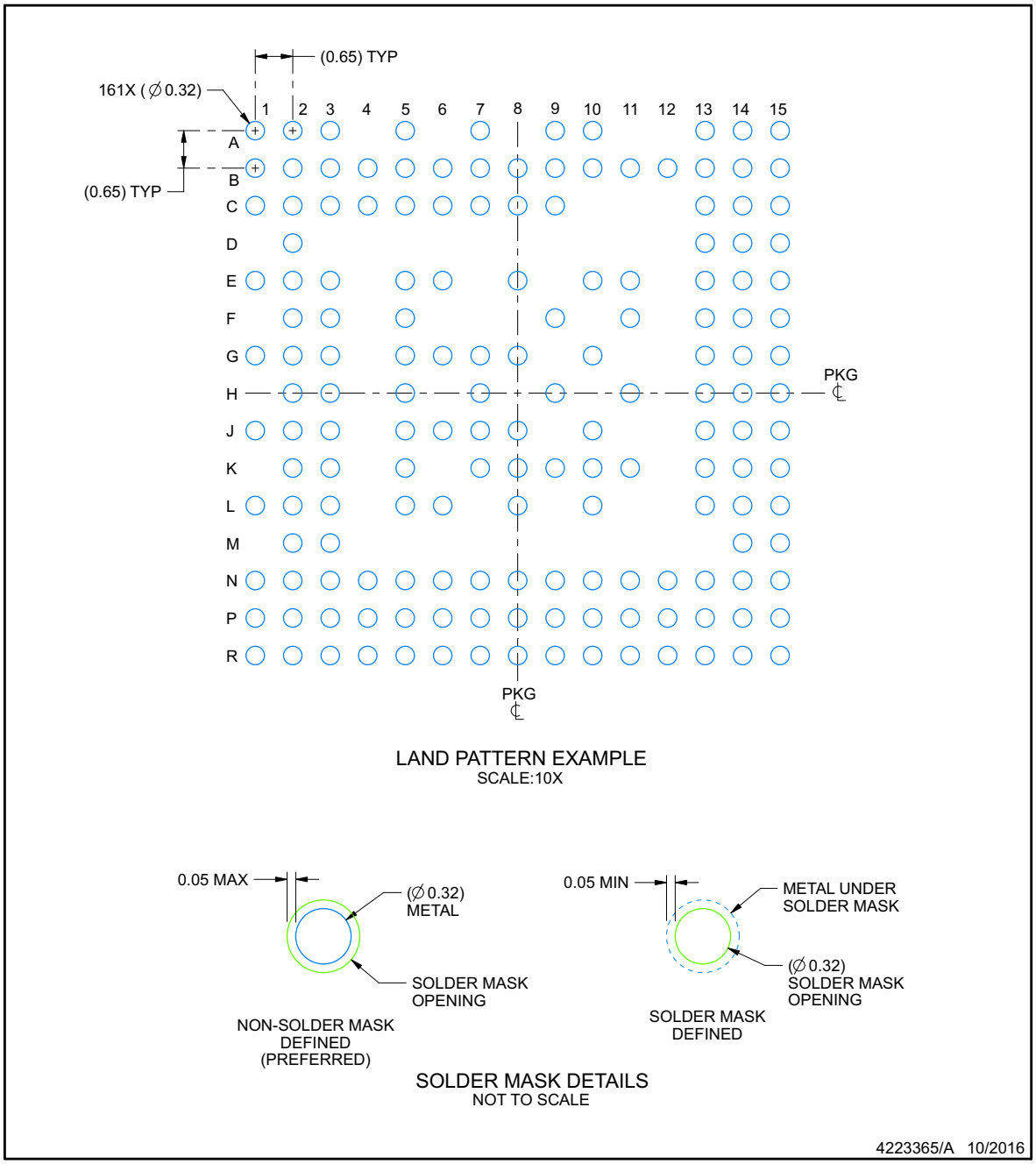
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

ABL0161B

FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY



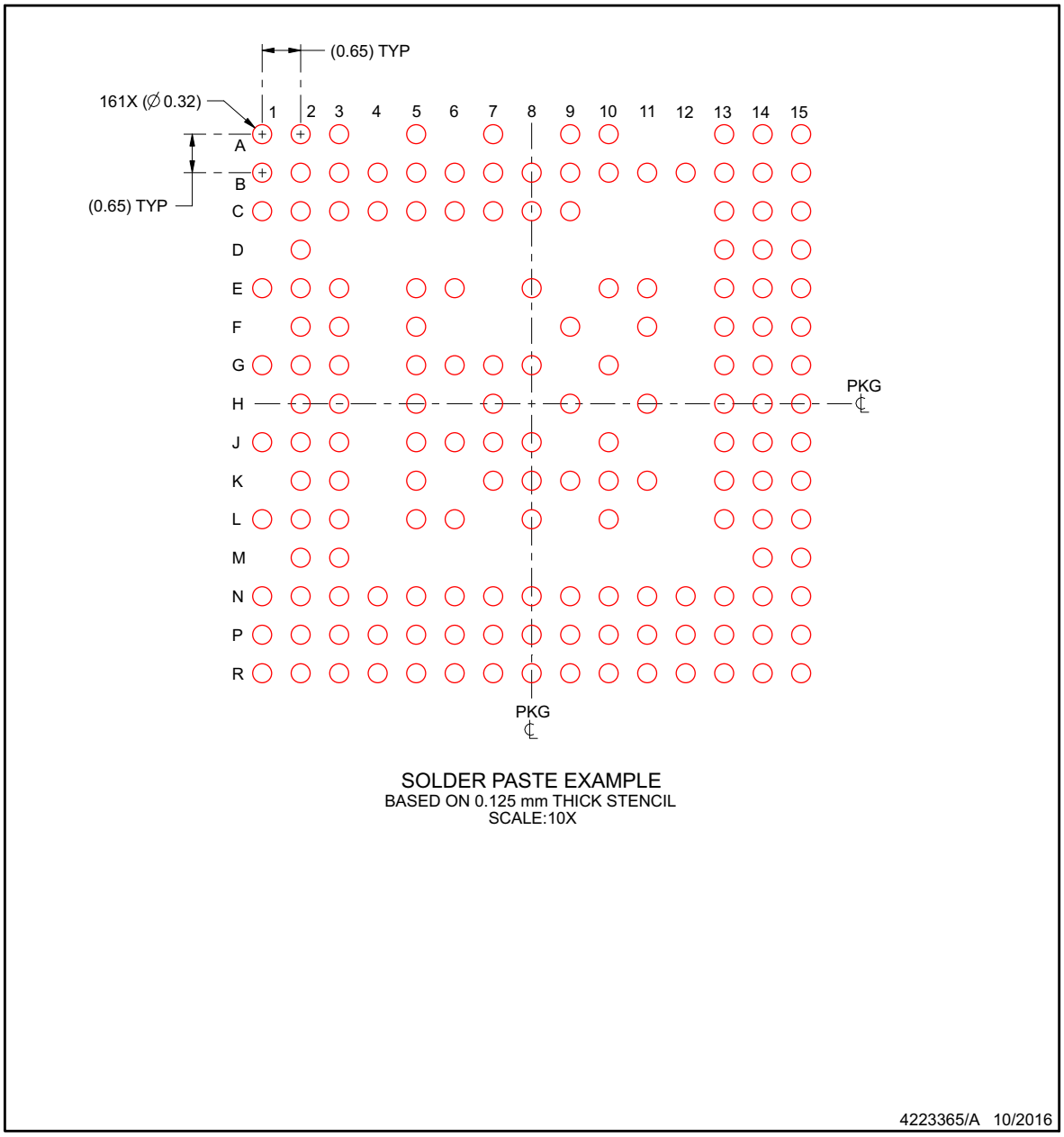
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ABL0161B — **FCBGA - 1.17 mm max height**

PLASTIC BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
IWR1843AQGABL	ACTIVE	FC/CSP	ABL	161	176	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	IWR1843 QG (502A, 502AD) D (502AD ABL, 502A D ABL)	Samples
IWR1843AQGABLR	ACTIVE	FC/CSP	ABL	161	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	IWR1843 QG (502A, 502AD) D (502AD ABL, 502A D ABL)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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