DESIGNING TOMORROW

Sitara™
AMIC110
SoCs

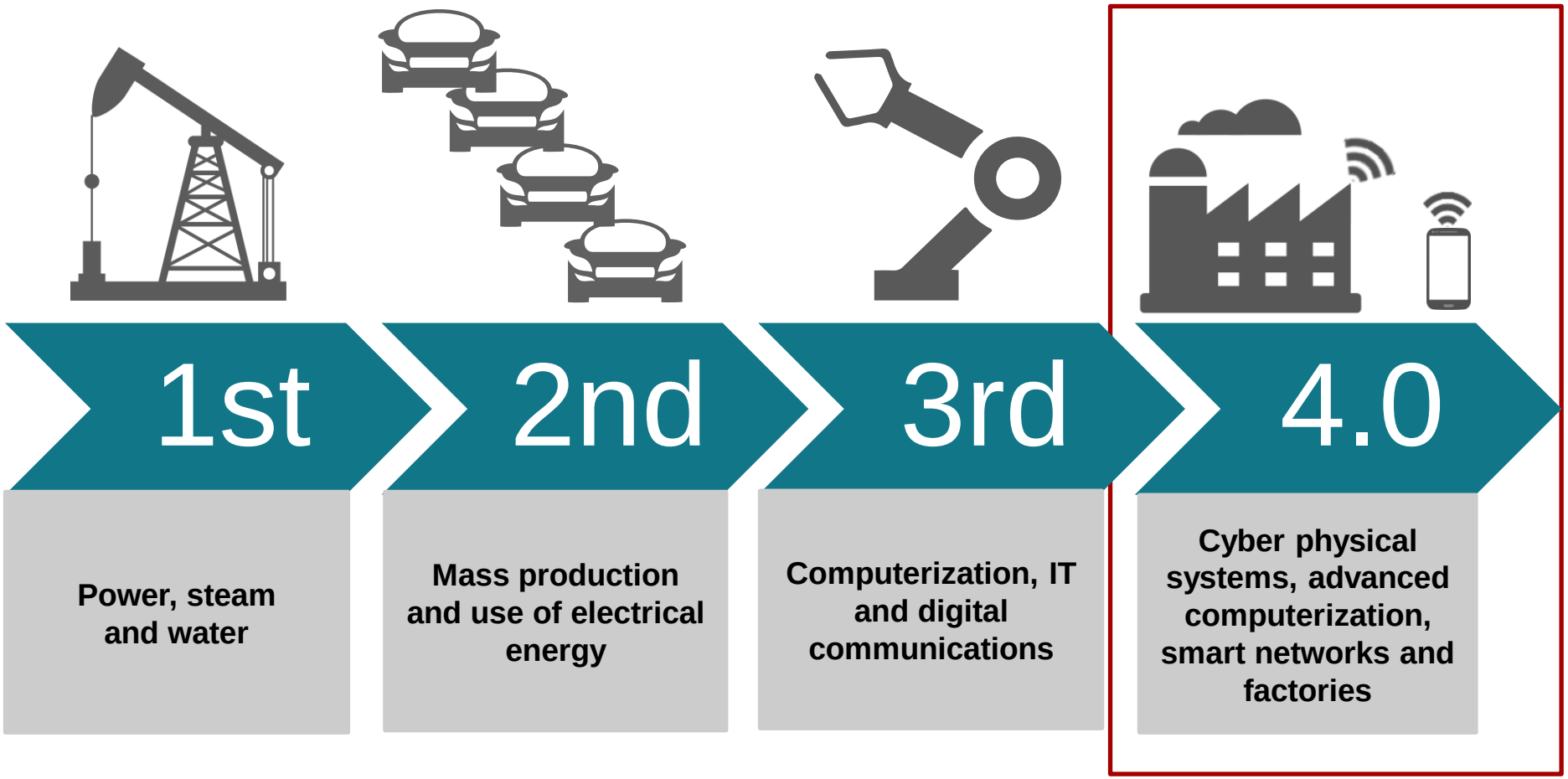
Texas Instruments

Drive down cost of multi-protocol Industrial Ethernet communication

Agenda

- AMIC110 features and benefits
- Supported protocols roadmap (including Mechatrolink, EtherCAT, etc)
- DDR-less operation
- 3P stack working model
- Q&A

Industry 4.0 and China 2025



AMIC1x SoC for Industry 4.0

Multiple protocols

Communicate with more than 10 protocols without redesigning your product and provide more solutions to your factory automation applications

Build on your foundation

Extend your existing solution by adding AMIC110 SoC for industrial Ethernet while reusing your hardware and software platform

Versatility

Easy migration from existing EtherCAT® ASICs to achieve more performance, scalability and software compatibility

Cost optimized

Supports low-cost system implementation and re-use of existing platforms, while allowing support for additional protocols

The right SoC for your industrial automation application

Connected drives

Allows legacy drives to connect to industrial Ethernet by supporting protocols such as EtherCAT, Profinet…

Factory automation

Extends industrial Ethernet across the factory floor from PLCs, CNCs, motor drives, sensors and other IO devices

Grid infrastructure

Supports Ethernet redundancy protocols such as HSR and PRP which are commonly used in protection relays and grid automation

Programmable solution allows re-use across multiple applications using Processor SDK software

HIGH RELIABILITY

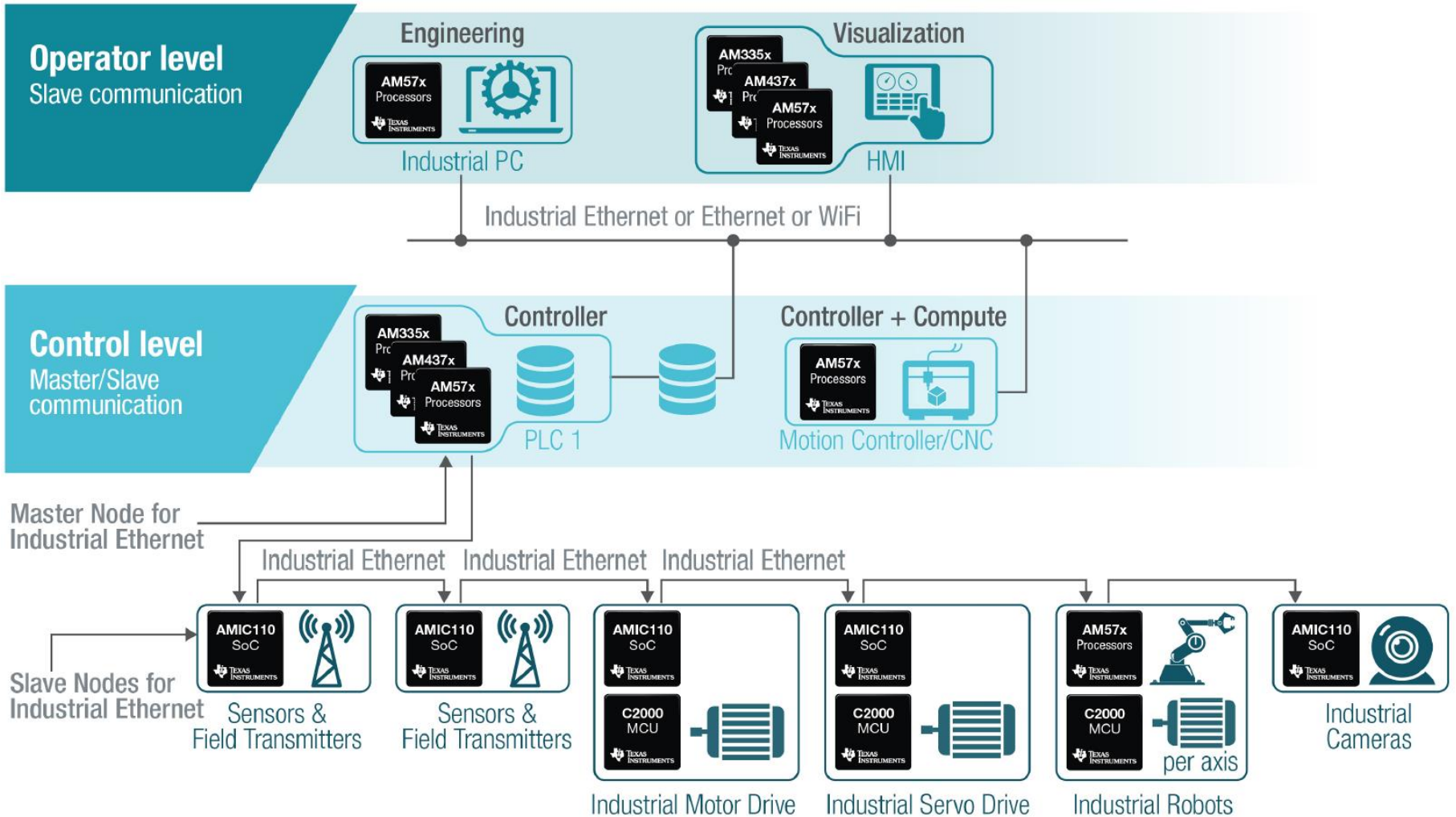
CONNECTIVITY

INTELLIGENT

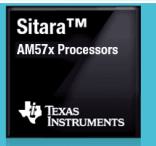
LOW POWER

SENSING

Factory automation systems with AMIC110 SoCs



Sitara™ servo drive solutions

Servo drive solutions from TI						
Safety	Integrated functional safety features					✔
Industry 4.0 services	Time-Sensitive Networking (TSN)					✔
	Integrated security features		✔	✔	✔	✔
	Predictive maintenance		✔	✔	✔	✔
Control	High speed PCIe interface				✔	✔
	Integrated motor control			✔		✔
Communications	Multi-protocol industrial Ethernet	✔	✔	✔	✔	✔

Implementing Industrial Communications is a complex problem

- **Key requirements:**
- Real-time, low-latency and reliability
- Several standards are developed to meet these requirements
  - +120 Serial based standards.
  - +25 Ethernet based standards.
- Enhanced MAC (medium-access layer) functionality for different standards requiring **specialized hardware**

Serial-based popular standards

CAN
- CAN-Open
- DeviceNet

Modbus
Profibus
CC-Link

✓ **Implementation of several of these protocols TODAY require ASICs or FPGAs**

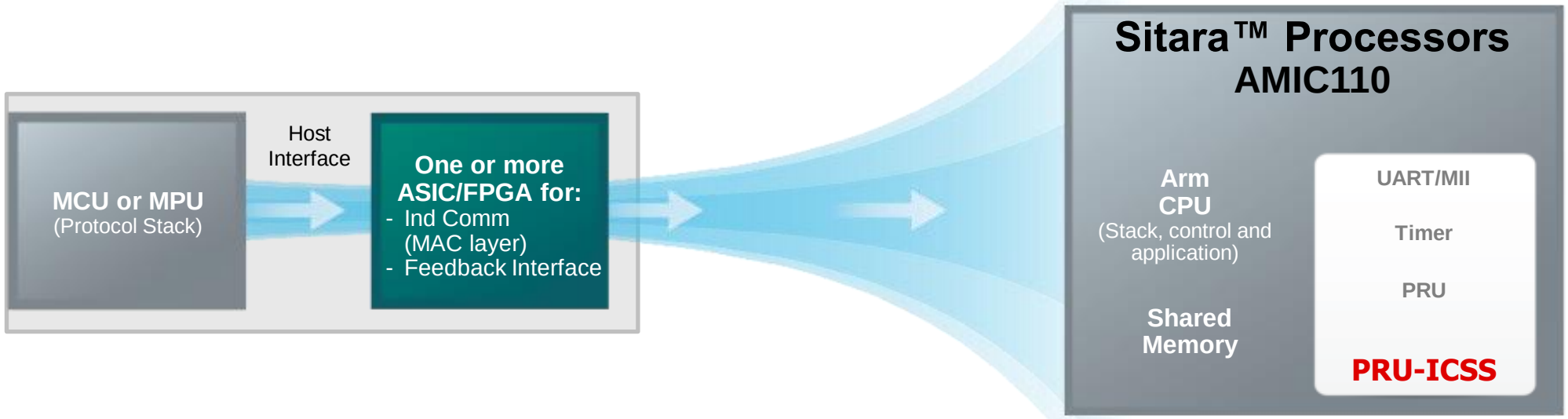
✓ **TI's Arm processors have a flexible, cost-efficient solution that eliminates this need**

Ethernet-based popular standards

EtherCAT
Ethernet/IP
Profinet
Powerlink
Sercos III
CC-Link IE
Mechatrolink
Modbus TCP

Similar requirements for Smart Grid Infrastructure
- Substation Monitoring – protocols such as IEC61850 and DNP3
- Solar Inverters – Ethernet based Industrial communications

Solving complex industrial communications



TI's Arm® + PRU solution

✓PRU-ICSS (PRU based Industrial Communications Subsystem)

- For low-end Sensors and IO devices, AMIC110 can be used standalone
- Supports **multiple protocols** using the same hardware
- Easily adapt to changing standards
- Scalable solution for HMI, PLC and I/O devices

AMIC110

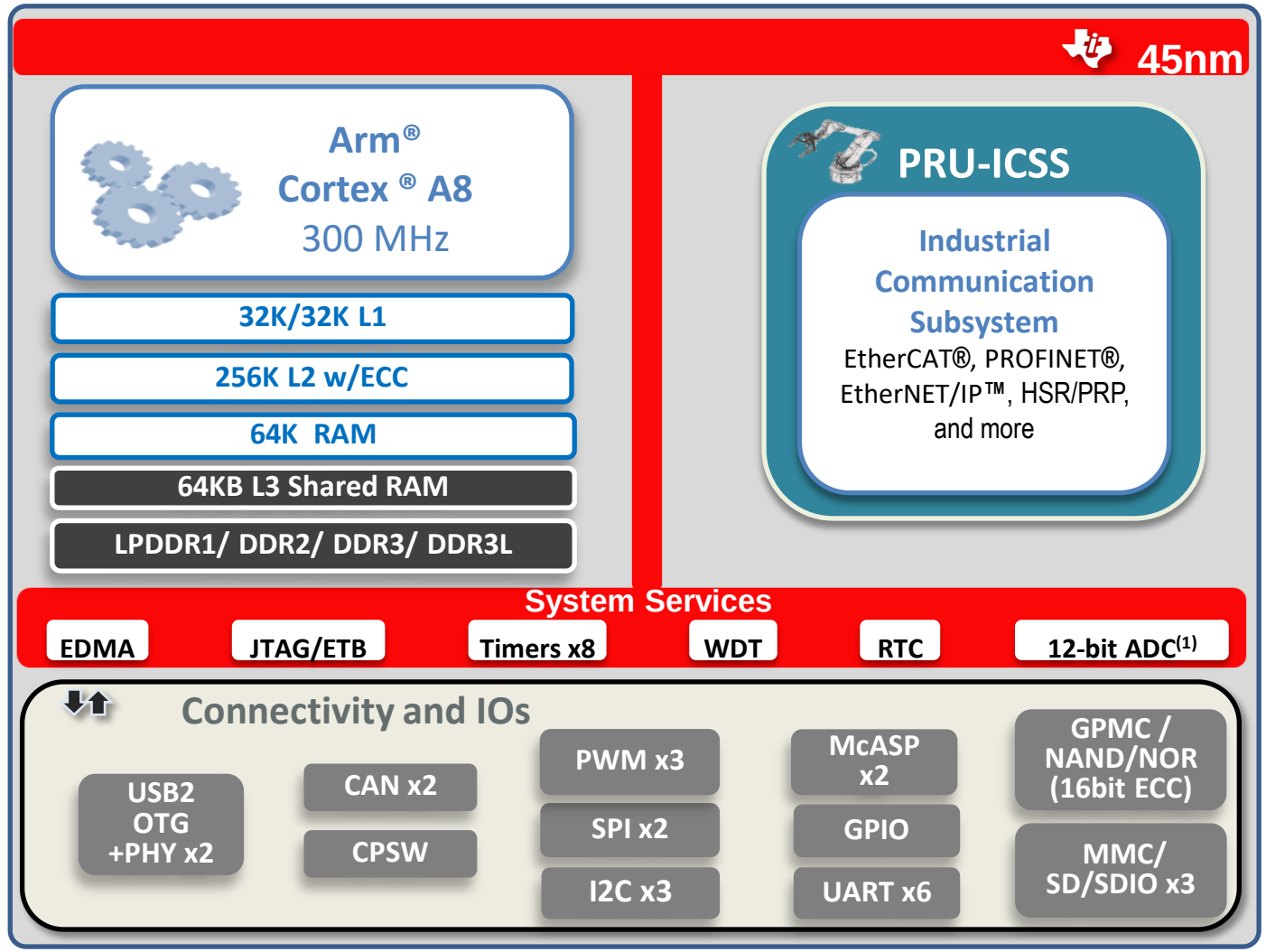
Benefits
- PRU-ICSS provides a programmable solution to multiprotocol fieldbus support
- Protocols supported include: EtherCAT, PROFINET, EtherNET/IP, MECHATROLINK III, HSR, PRP, and more

Industrial Ethernet & Fieldbus Comms for:
- Factory Automation & Controls
- Motor Drives
- Grid Infrastructure

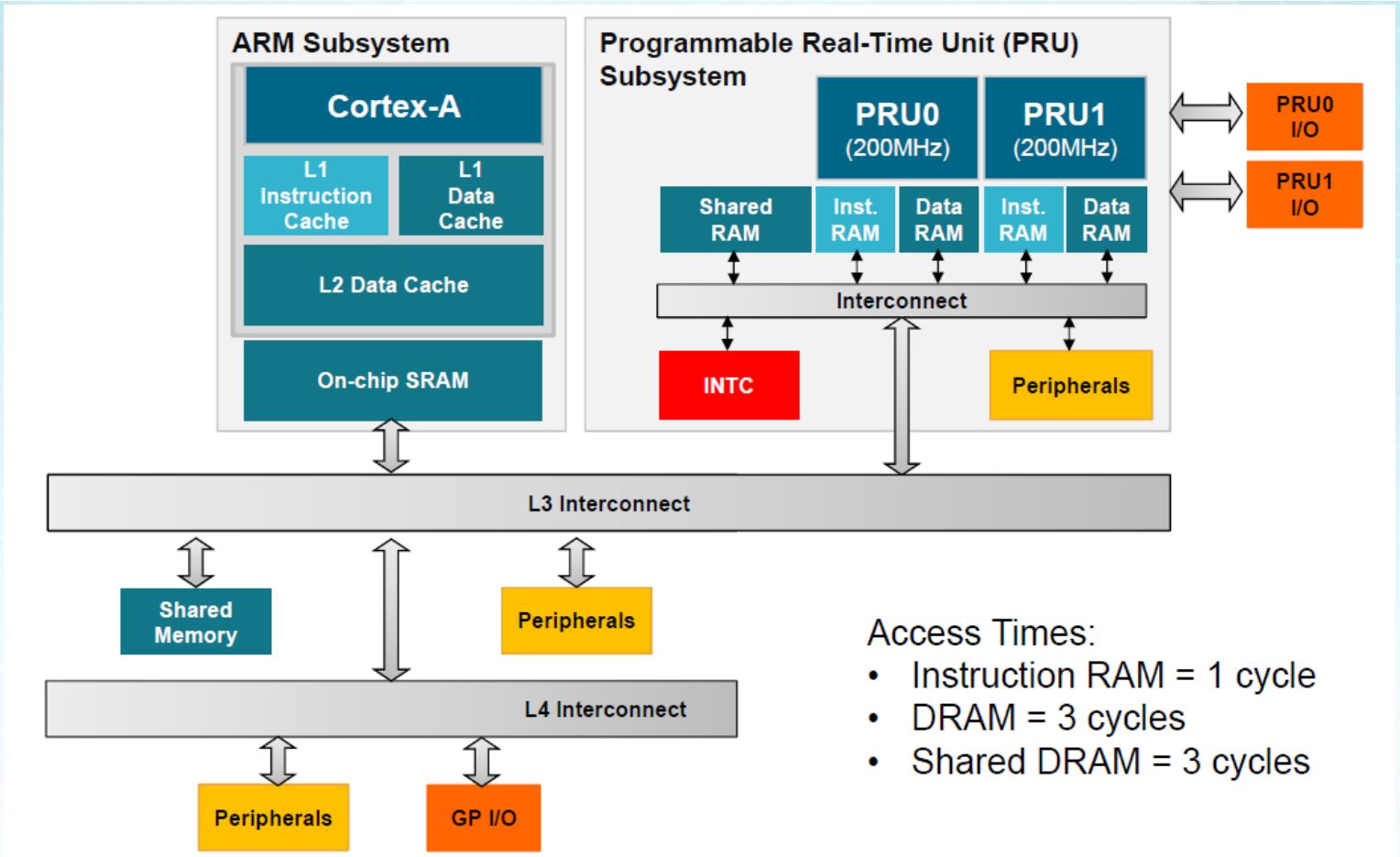
Software and development tools
- Free TI-RTOS directly from TI
- Other RTOS from partners

Power Estimates
- Total Power: <500mW

Schedule and packaging
- Status: In Production, Docs: Now
- AMIC110 ICE Board: Now
- EtherCAT slave TI Design: Now
- Packaging: 15x15, 0.8mm
- Extended Temp only (-40C to 105C junction)

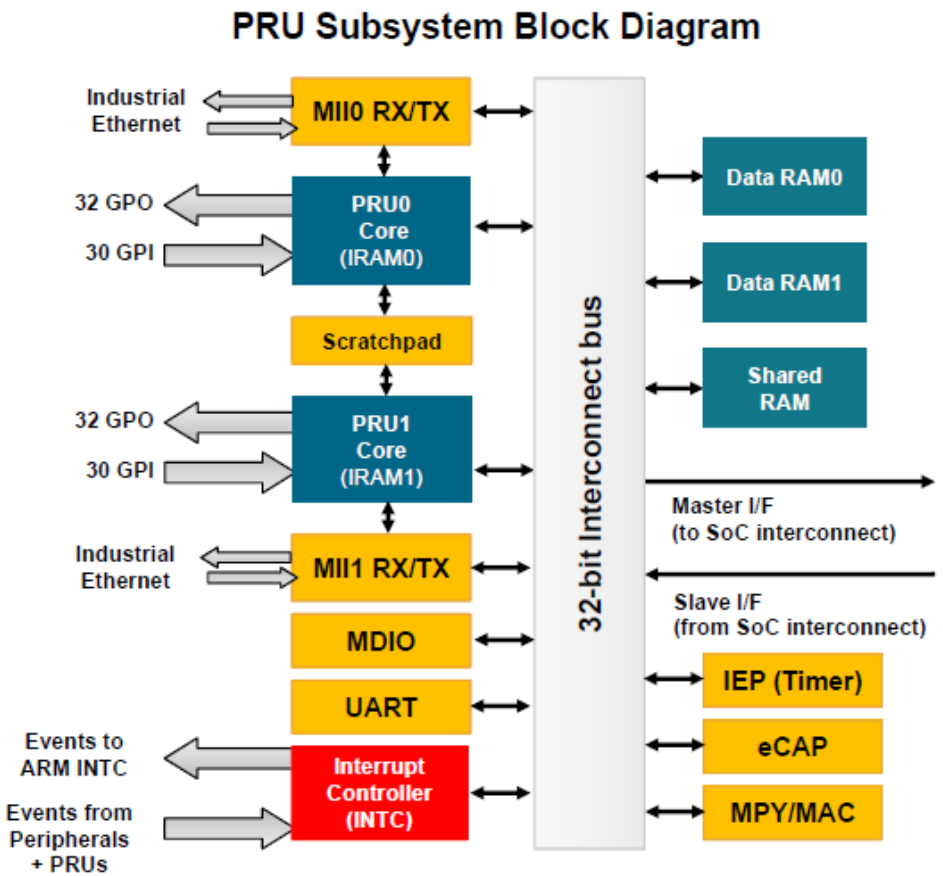


Arm + PRU SoC Architecture



Programmable Real-Time Unit (PRU) Subsystem

- Programmable Real-Time Unit (PRU) is a low-latency microcontroller subsystem
- Two independent PRU execution units
  - 32-Bit RISC architecture
  - 200MHz – 5ns per instruction
  - Single cycle execution - No pipeline
  - Dedicated instruction and data RAM per core
  - Shared RAM
- Includes Interrupt Controller for system event handling
- Fast I/O interface
  - Up to 30 inputs and 32 outputs on external pins per PRU unit



PRU Features & Benefits

Feature	Benefit
Each PRU has dedicated instruction and data memory and can operate independently or in coordination with the ARM or the other PRU core	Use each PRU for a different task; use PRUs in tandem for more advanced tasks
Access all SoC resources (peripherals, memory, etc.)	Direct access to buffer data; leverage system peripherals for various implementations
Interrupt controller for monitoring and generating system events	Communication with higher level software running on ARM; detection of peripheral events
Dedicated, fast input and output pins	Input/output interface implementation; detect and react to I/O event within two PRU cycles
Small, deterministic instruction set with multiple bit-manipulation instructions	Easy to use; fast learning curve

Certified Industrial Communication Protocols

Faster time to market

TI offers firmware to enable multiple industrial protocols on the PRU-ICSS in Sitara processors free of charge

App note pictured on the right for specific protocols supported

ABSTRACT

This document shows the industrial communication protocols supported by each of the devices in the Sitara™ Arm® Cortex®-A processor portfolio, as well as where and how to get these protocols.

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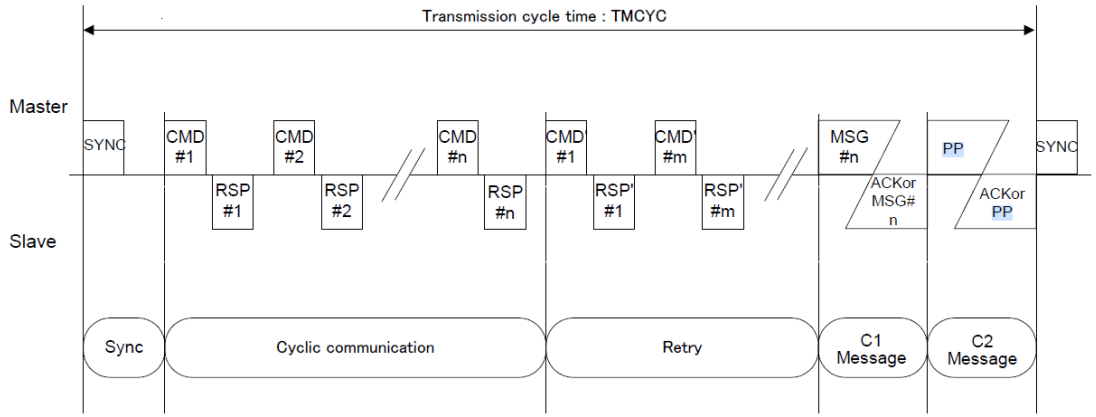
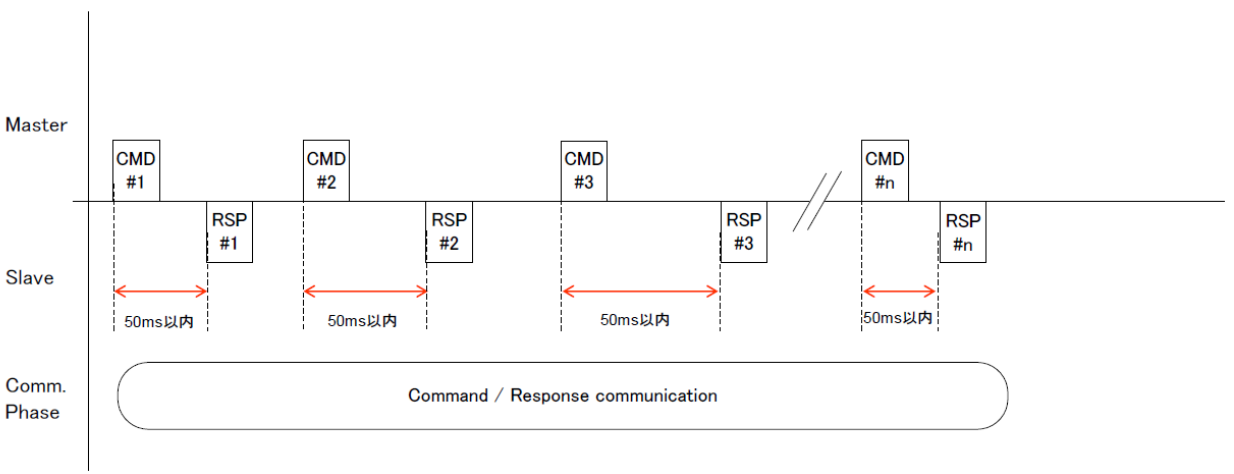
6 Mechatrolink III Supporting Devices 5
7 SORTE Supporting Devices 5
8 PRP Supporting Devices 5
9 HSR Supporting Devices 5
10 EnDat 2.2 Supporting Devices 6
11 HIPERFACE DSL Supporting Devices 6
12 Tamagawa Supporting Devices 6

http://www.ti.com/lit/sprach6

Mechatrolink III



- Cyclic communication



- Event-driven communication

Mechatrolink III – 3P's Solution

Mechatrolink III

Sitara processors currently support Mechatrolink III, as specified in Table 6. The solution is available from Systec in Japan, or Macnica for outside of Japan. For more information, contact Macnica at AtdSpl@macnica.co.jp.

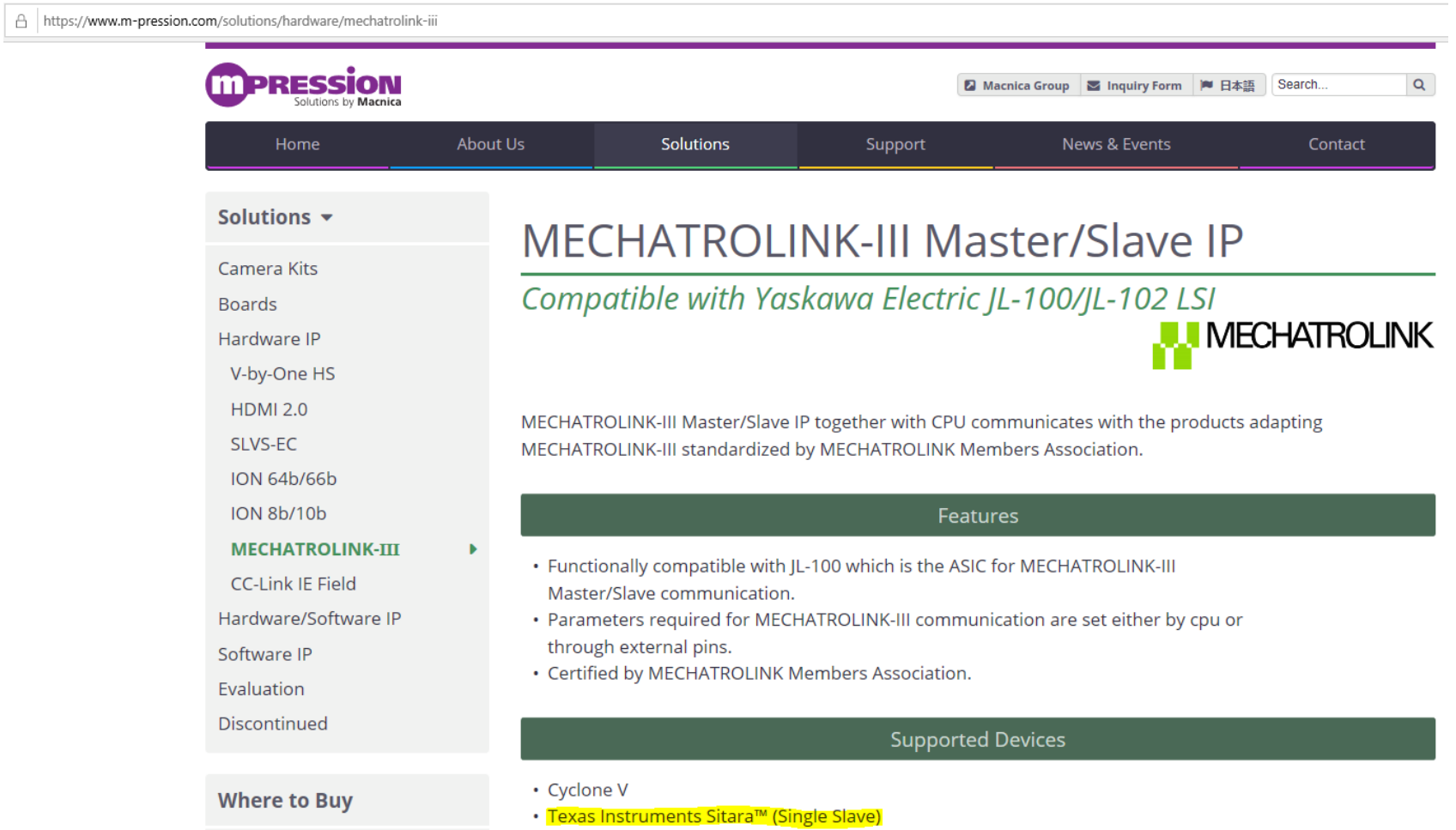
Table 6. Mechatrolink III Supporting Devices

OS		AMIC	AM335x	AM437x	AM57x	66AK2G
Linux	Master					
	Slave					
RTOS	Master					
	Slave	AMIC110				

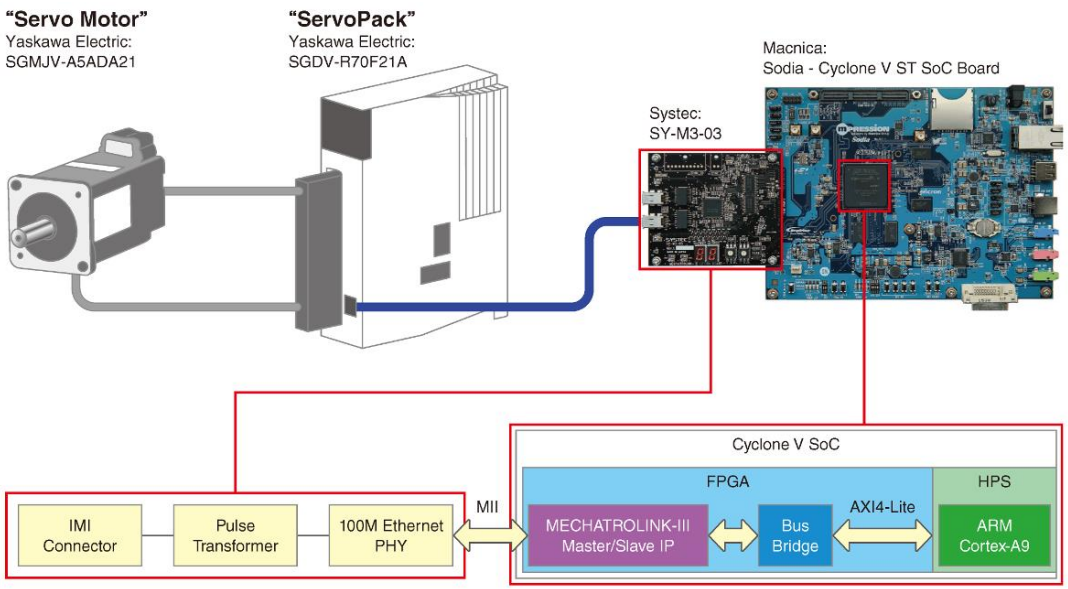
Additional Resources:

- Macnica's Mechatrolink III IP specifications

Mechatrolink III – 3P's Solution

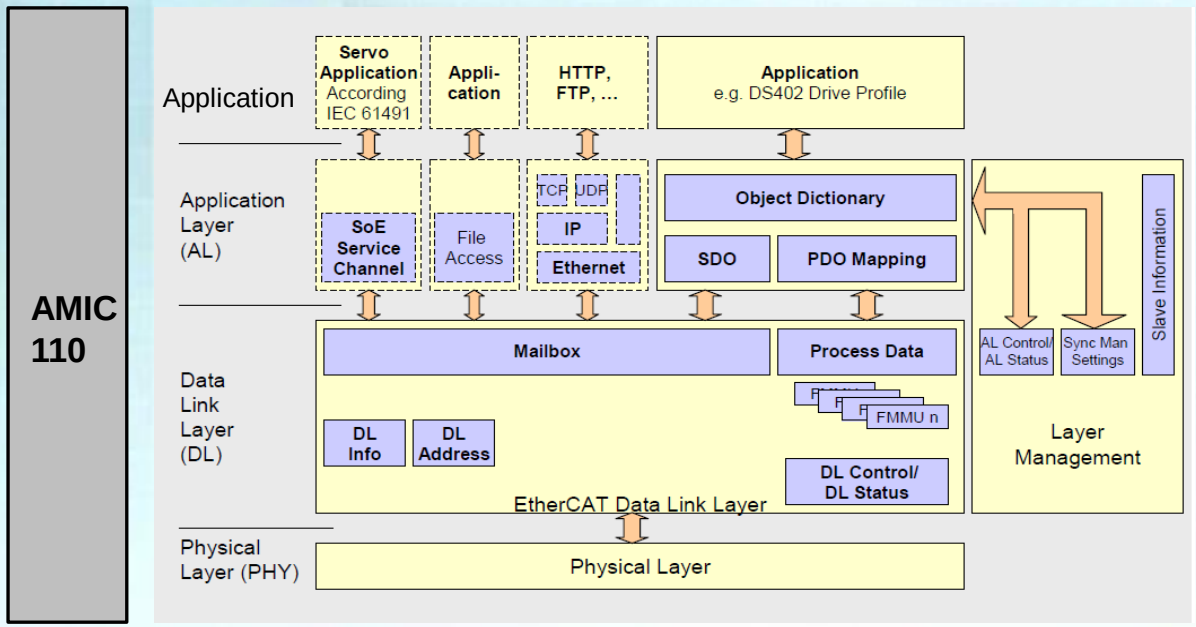


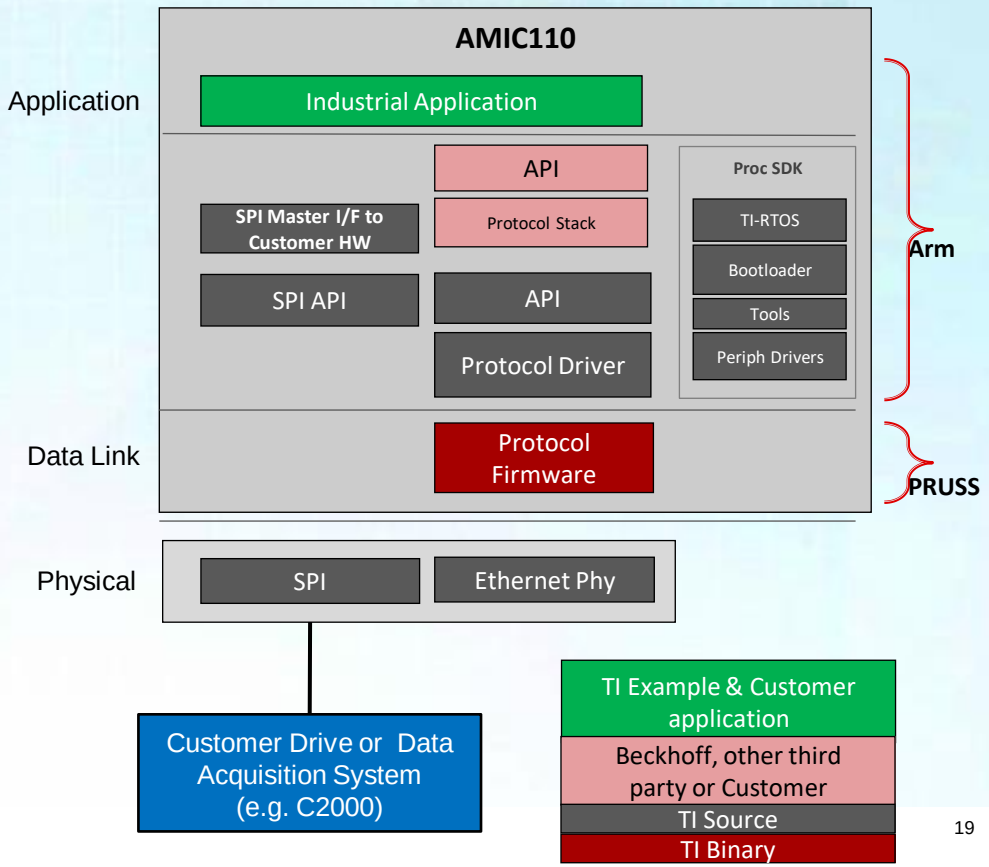
Mechatrolink III – Cyclone vs. AMIC110



DDR-less EtherCAT on AMIC110

EtherCAT slave stack code (SSC)





AMIC110: EtherCAT stack, SPI master
C2000 : Motor drive, data acquisition

19

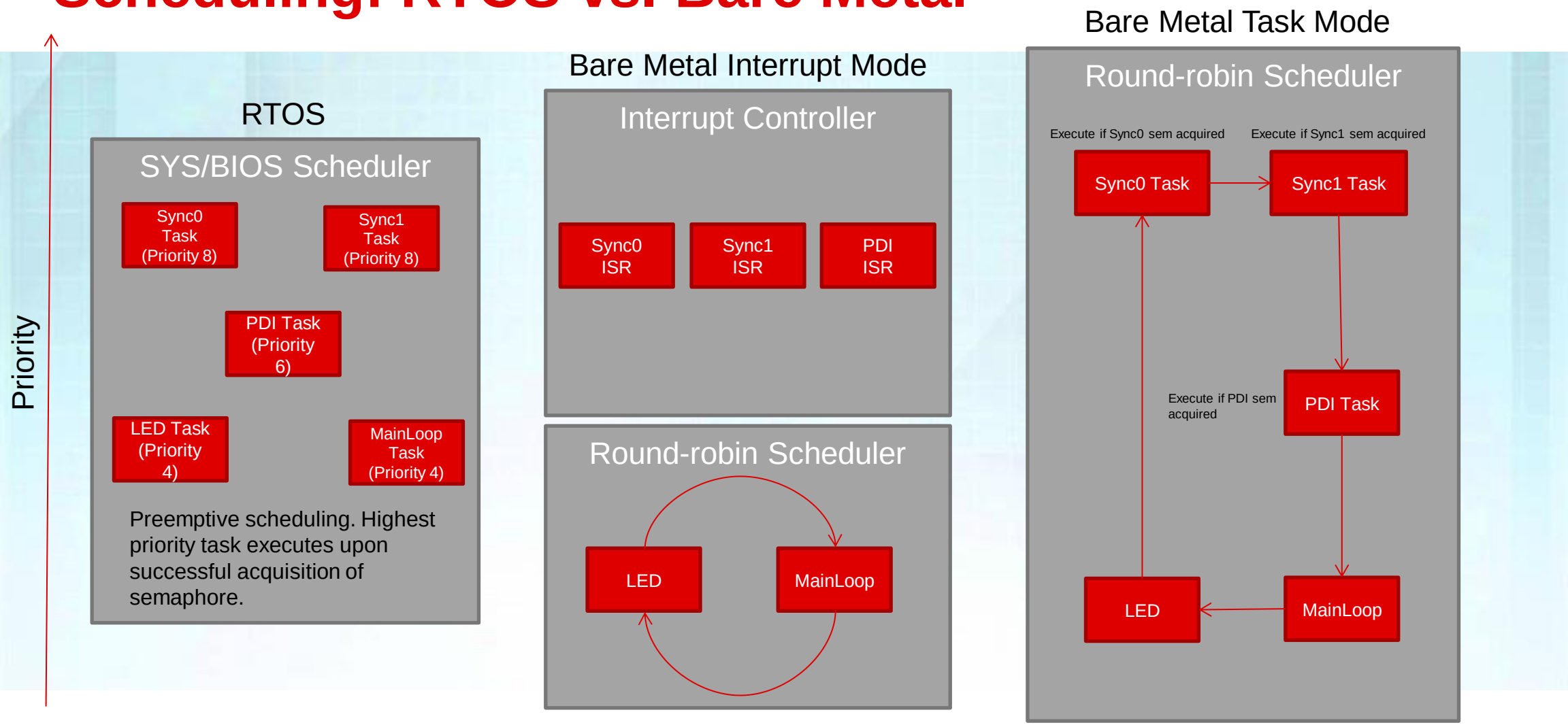
Optimization Techniques

- AMIC110 On-chip Memory

Type	Start address	Size	Description
SRAM	0x40200000	0x00010000	64kB internal SRAM
L3 OCMC	0x40300000	0x00010000	64kB L3 OCMC SRAM
M3 SHUMEM	0x44D00000	0x00004000	16kB M3 Shared Unified Code Space
M3 SUDMEM	0x44D80000	0x00002000	8kB M3 Shared Data Memory

- Optimize from AMIC110 Second Boot Loader (SBL) to Processor SDK RTOS drivers and EtherCAT protocol.
  - eliminate code support for unused features of the device
  - minimize RTOS debug and error handing components
  - eliminate any unnecessary operations and optimize the remaining functions
  - compile the code and link the code with the appropriate settings

Scheduling: RTOS vs. Bare Metal



Size Comparison

	RTOS Debug *(Arm mode, DDR, optimization off)*	RTOS Release *(Thumb mode, On-chip, optimization on)*	Bare Metal Debug *(Arm mode, DDR, optimization off)*	Bare Metal Release *(Thumb mode, On-chip, optimization on)*
Binary	236 KB	87 KB	162 KB (31% smaller)	52 KB (40% smaller)
Memory Usage	**317 KB**	**130 KB**	**242 KB (24% smaller)**	**86 KB (34% smaller)**

RTOS Debug

Memory region	Used Size	Region Size	%age Used
SRAM_LO:	0 GB	1 KB	0.00%
SRAM_HI:	0 GB	63 KB	0.00%
OCMC_SRAM:	0 GB	64 KB	0.00%
DDR3:	316736 B	512 MB	0.06%

Bare Metal Debug

Memory region	Used Size	Region Size	%age Used
DDR0:	241904 B	256 MB	0.09%
OCMCRAM:	0 GB	60 KB	0.00%
VECS:	0 GB	1 KB	0.00%

RTOS Release

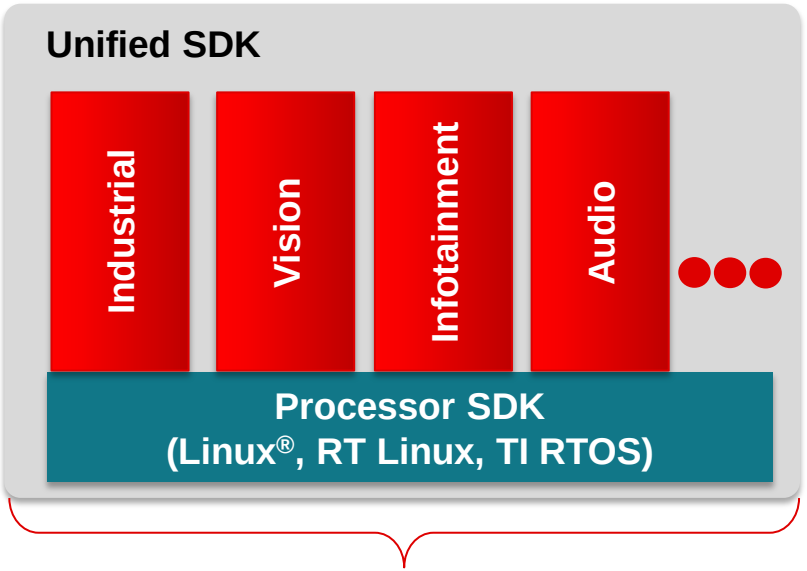
Memory region	Used Size	Region Size	%age Used
SRAM_LO:	0 GB	1 KB	0.00%
SRAM_HI0:	19184 B	21760 B	88.16%
SRAM_HI1:	88300 B	105208 B	83.93%
SRAM_HI2:	2056 B	3 KB	66.93%
SRAM_CM:	16 KB	16 KB	100.00%
SRAM_DM:	4 KB	8 KB	50.00%
DDR3:	0 GB	512 MB	0.00%

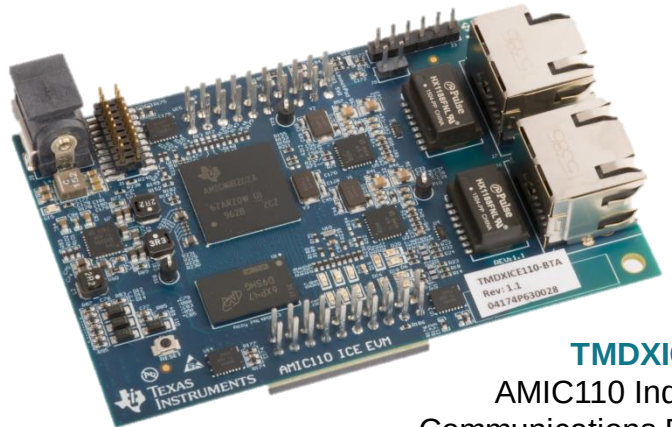
Bare Metal Release

Memory region	Used Size	Region Size	%age Used
SRAM_LO:	0 GB	1 KB	0.00%
SRAM_HI0:	7424 B	21760 B	34.12%
SRAM_HI1:	52292 B	105208 B	49.70%
SRAM_HI2:	2056 B	3 KB	66.93%
SRAM_CM:	16 KB	16 KB	100.00%
SRAM_DM:	8 KB	8 KB	100.00%
DDR3:	0 GB	512 MB	0.00%

Get started now: Dev kits, Processor SDK and more

Unmatched, scalable software and hardware experience





TMDXICE110
AMIC110 Industrial Communications Engine
$195

Online Ethernet reference designs

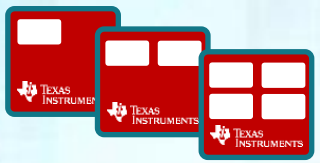
TI E2E™ community

Development documentation, guides, app notes etc.

Processor Software Test Process

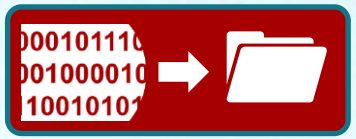
Automation enables scale and efficiency

Total Processor platform families covered



7+

Total platforms tested



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Test cases per Day

14000+

Multiple release streams supported in parallel

Designed to Scale for *100s of EVMs* and End Equipment Use Case based tests

Processor Automated Software Test Framework

Industrial Communication Partners

- **KUNBUS** – KUNBUS offers the broadest support of multiple industrial communication protocols in one package. KUNBUS offers a full suite of services and expertise related to industrial communication applications, including hardware evaluation kits, hardware modules, software customization, and certification support for Sitara processors.
- **Acontis** – Acontis offers EtherCAT master solutions for Sitara processors.
- **Matrikon** – Matrikon offers the OPC UA stack for Sitara processors on Linux RT.
- **Be.Services** – Be.Services offers openPowerlink on Sitara processors through Codesys on Linux RT.
- **CC-Link Partner Association (CLPA)** – The CLPA provides the stack for CC-Link IE Field Basic for Linux RT and RTOS.
- **Systec** – Systec offers the entire Mechatrolink III solution, including firmware and software stack on RTOS. Macnica offers these services for Systec outside of Japan. For licensing, contact AtdSpl@macnica.co.jp.
- **Molex** – Molex supplies production master stacks for PROFINET and EtherNet/IP on Sitara processors on RTOS.
- **TMG** – TMG TE supplies production slave stacks for PROFINET and EtherNet/IP on Sitara processors on RTOS. For more information on the products visit www.tmgte.de/en, or for licensing contact willems@tmgte.de.
- **CouthIT** – CouthIT offers integration of the BiSS C encoder for Sitara processors. For more information, contact Krishna@CouthIT.com.

Q&A

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