Application Report
SPRACK9–February 2019

OMAP-L13x/C674x/AM1x schematic review guidelines

Catalog Processors

ABSTRACT

This application report provides schematic review guidelines for the OMAP-L1x, C6l4x, and AM1x families of TI System-on-Chips (SoCs).

Contents

List of Figures

List of Tables

Trademarks

C6000 is a trademark of Texas Instruments.
Arm9 is a trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
All other trademarks are the property of their respective owners.

1 Introduction

This application report applies to the following devices:

- OMAP-L138
- OMAP-L137
- TMS320C6748/TMS320C6746/TMS320C6742
- TMS320C6747/TMS320C6745/TMS320C6743
- AM1810/AM1808/AM1806/AM1802
- AM1707/AM1705

For OMAP-L1x DSP + ARM9 based processors, refer to this link: OMAP-L1x based processors.

For C6000™ DSPs, refer to this link: C6x DSPs.

For Arm9™-based processors, refer to this link: ARM9 processors.

2 Recommendations Specific to OMAP-L1x/TMS320C674x/AM1x

2.1 EVM vs Data Sheet

In the event of discrepancies between the TI EVMs and the device-specific data sheet, always follow the data sheet. EVMs are often designed before the device has been fully characterized, and may contain errors which do not impact functionality on that particular board, but are not completely aligned with the data sheet specifications. Therefore, the EVMs should not be considered reference designs.

2.2 Before You Begin

2.2.1 Documentation

Make sure you have the latest version of documentation, especially the data sheet and silicon errata.

Tip: Try searching the documentation for words such as: "must," "require," "do not," "shall," "note," and so forth. Important criteria for the device will typically contain one or more of these words. This is an easy way to make sure you have not missed anything important.

Tip: On each ti.com device product folder, there is a button, "Alert me about changes to this product." Registering here enables proactive automatic notification of device errata.

2.2.2 Pinout

- Have you verified that your pin labels correspond to the correct pin numbers?
- Have you verified that the power pins are connected to the correct supply rails?
- Pull-ups/pull-downs:
  - Internal pull-up/pull-down resistors are implemented with weak transistors. As the voltage present on the I/O pin varies, the relative gate voltage for this weak transistor changes, which will cause the effective pull-up/pull-down resistance to change. Therefore, internal resistors do not have a linear response like external resistors do. The non-linearity, along with process, voltage, and temperature variations, require internal pull-up/pull-down resistors to be specified with a wide range of resistance or current sourcing/sinking.
  - The input current without a pull-up or pull-down turned on defines the input leakage without any current from internal pull resistors. The input current with a pull-up or pull-down turned on defines a combination of input leakage current and current required to force the internal pull resistors to the opposite voltage rail. For example, if an internal pull-up is turned on, the value shown represents the total current required to pull the input to VSS.
  - When deciding what value of external resistor to use, you must consider the worst case combination of all internal leakage paths of all devices connected to a signal and make sure the external resistor is able to force these internal leakage paths to a potential greater than Vih min, or less than Vil max.

2.3 Critical Connections

2.3.1 Decoupling capacitors

Voltages from traces on a printed circuit board can couple to each other in places where it is not desired, (like power supply planes). To decouple the traces, we add capacitors to absorb some of the voltage and help reduce this effect. For more information on how to correctly place decoupling caps, see the data sheet section for power-supply decoupling.

PLL and some analog supplies benefit from filters or ferrite beads to keep the noise from causing clock jitter. The minimum recommendation is a ferrite bead with a resonance at 100 MHz along with at least one capacitor on the device side of the bead. Additional recommendation is to add one capacitor just before the bead to form a Pi filter. The filter needs to be as close as possible to the device pin, with the device side capacitor being the most important thing to be close to the device pin. PLL pins close together can be combined on the same supply. PLL pins farther away from each other may need their own filtered supply.

For more information, see *General Hardware Design/BGA PCB Design/BGA Decoupling* (SPRABV2).

2.3.2 Power

- Check that the correct voltages are applied to their respective power pins on the chip, and that your power supply can provide the required current.
- If the user would like to measure power on prototype PCBs, it is recommended that they install zero-ohm resistors plus probe points for each power rail. The user can then remove the zero-ohm resistor and measure across the probe points.
- Check that power comes up in the correct sequence, per the device-specific data sheet.
- The DVDD18 I/O supply must always be connected, even when the dual-voltage I/Os are supplied with 3.3 V.
- RTC_CVDD may be connected to CVDD if no battery is used, even when using the 1.3 V core OPP.
- Verify that the PLL0 and PLL1 supplies follow the filtering requirements shown in the device-specific data sheet. Each PLL must have its own filter in order to assure noise immunity.

2.3.3 Ground

- Digital ground nodes: VSS, SATA_VSS
- Analog ground nodes: OSCVSS, PLL0_VSSA, and PLL1_VSSA
- Local ground nodes:
  - RTC_VSS - Local ground for RTC oscillator (must not be connected to the board ground)
  - OSCVSS - Local ground for oscillator
  - PLL0_VSSA and PLL1_VSSA - local ground for PLL
  - These local ground nodes must not be connected to board ground unless otherwise stated in the data sheet.

2.3.4 Clocking

Make sure your input clock/crystal meets the data sheet requirements. For example:

- Frequency
- Voltage (if using external clock source)
- ESR for crystal
- Load capacitance meets both the crystal’s and processor’s requirements
- Crystal and caps placed physically close to processor
- Double check proper voltage level for clock (some devices will use core voltage, others I/O voltage).
- If there are any PLL configuration pins make sure they are set such that the resulting frequency is within device spec. Also, having alternate population options for those PLL pins could be handy.

OSC Internal Oscillator Clock Source

Figure 1 shows the recommended crystal circuit. It is recommended that pre-production printed circuit board (PCB) designs include the two optional resistors Rbias and Rs. They may be required for proper oscillator operation when combined with production crystal circuit components.

OSC Crystal Circuit Schematics

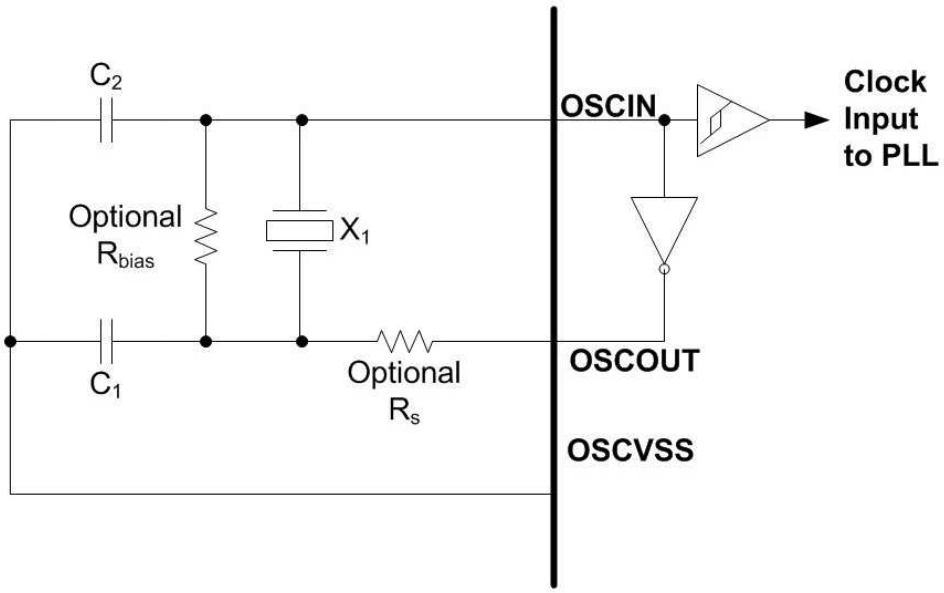

Figure 1. Crystal Circuit

In general, adding Rbias and Rs resistors improves circuit performance by reducing the long start-up time, crystal overdrive and voltage and temperature related issues. Specifically, they provide the following functionality:

- Rs helps reduce the drive level on the crystal and decreases the slew rate, which adds additional phase shift Recommended value: 50 Ω Rbias (a.k.a. the feedback resistor) is used to bias the input of the inverting amplifier and improve the loop gain Recommended value: 1M Ω

However, in most cases Rbias is not required and Rs is a 0-Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on pre-production PCBs.

For calculation of Rs and Rbias values, see www.crystek.com/documents/appnotes/Pierce-GateIntroduction.pdf.

Oscillator components (Crystal, C1, C2, optional Rbias and Rd) must be located close to the OMAPL1x package. Parasitic capacitance to the printed circuit board (PCB) ground and other signals should be minimized to reduce noise coupled into the oscillator.

- **Observation clock**

CLKOUT is a PLL observation clock output, and is provided for test and debug purposes only. It should not be used as a synchronous clock for any of the peripheral interfaces because it was not timing-closed to any other signals. This clock output was not designed to drive any time-critical external circuits that require a low-jitter reference clock. There is no characterization data for the jitter performance for CLKOUT.

2.3.5 Reset

Make sure that reset is kept asserted as the power supplies are ramping. You must not release the processor from reset until all the proper voltage/clocking is in place, as specified by the device-specific data sheet. Conversely, make sure that something on the board is actually RELEASING the device from reset once power and clocks are stable.

A useful tip is to place a 0.1 µF cap near the reset pin to help avoid ESD-induced resets.

Also, having a reset button on your board can be helpful for development.

2.3.6 Boot

- Double check that the boot configuration pins are set to the correct option.
- Use external pull resistors. Do not tie boot pins directly to ground or VDD.
- It is highly recommended to have some population options to be able to easily change the reset mode. This can be handy in a variety of circumstances. For example, if you were doing a NOR flash boot and you ever accidentally put in some bad code, you might end up in a scenario where you can't connect to the device with emulator because it is in a bad state, and you can't reprogram the flash as a result! Having an alternate boot mode can be a life saver.
- Read carefully the initialization section in the device-specific Technical Reference Manual. You may have to deal with important information that can change your design. Look for which chip select is used by default, default clock setups, bus widths, wait states, supported booting devices, initial fetch address and interrupt vector addresses, default memory map and so on.
- For OMAPL137/C6747 devices, the UART boot mode requires the input clock (OSCIN) to run at 24 MHz.

CAUTION

Be careful if *anything* external is hooked up to boot pins (such as when the pins are multiplexed with GPIO or other peripherals). You must make sure that the boot pins are at the proper levels when power-on reset occurs, such that the correct values are latched in order for the device to boot correctly.

2.3.7 Pin multiplexing

Although pin muxing is frequently software configurable, the initial configuration is often dependent upon several configuration pins (are they high or low when reset is released). Make sure that the initial pin muxing corresponds properly with your boot modes so that any interfaces necessary for boot will be available. On some devices, this could potentially be handled by the boot ROM, but to be certain you should configure the initial pin muxing appropriately.

2.3.8 Debug

- Include pullup resistors on EMU0 and EMU1 pins.
- For more information, see these recommendations when designing your JTAG interface.
- For more information, see the JTAG Connectors article when deciding which header to put on the board. Double-check the pin-out!

2.4 Peripherals

2.4.1 UART

- Install pullup resistors on the UART_TXD pins. During reset, these pins are internally pulled low, and host software may incorrectly interpret this as sending null characters.
- This peripheral is frequently hooked up incorrectly. Make sure it is connected as follows:
  - TX ---> RX
  - RX <--- TX

2.4.2 EMAC

The RMII reference clock (RMII_MHZ_50_CLK) must have a jitter tolerance of 50 ppm or less.

2.4.3 MMC/SD

Weak (~51K) pull ups on all MMC/SD lines are recommended.

2.4.4 EMIF

- Check that chip selects are connected to the proper memory devices.
- Weak pullups are recommended on chip selects.

2.4.4.1 NAND

- When booting from NAND devices, use EMA_CS[3].
- Support of NAND flashes that are not ONFI-compliant is not guaranteed. If you've selected a such a device, you must verify that it works with the bootloader before going into production.
- EMIFA does not support NAND Flash devices that require the chip select signal to remain low during the tR time for a read. Make sure that this is not required by the selected NAND flash.
- For a list of verified-compatible NAND devices, see the *Using the OMAP-L132/L138 bootloader*.

2.4.4.2 NOR

- When booting from NOR devices, use EMA_CS[2].
- Verify that address pins are connected correctly according to Appendix B.

The mapping of address pins to the memory interface is a device-specific detail that often depends on the bus width (8- or 16-bit data bus). For example, in some devices the upper address bits get mapped down to handle the least significant bit, while in other devices the pins may all "shift" depending on the width of the interface. Double check the device-specific documentation to verify that the address mapping is handled correctly.

2.4.4.3 DDR2/mDDR

- Parallel termination is not allowed on CLKP/CLKN pins.
- If termination is used, the DDR2/mDDR drive strength should be set to full strength. Otherwise, the drive strength should be set to half strength.
- No pullups or stubs are allowed on any DDR pins.
- For DQS and D net classes:
  - Routes must be point-to-point.
  - Skew matching across bytes is not needed nor recommended.
  - Skew between the two classes should not exceed 25 mil.
- Clock and DQS net class trace lengths need to be routed such that the skew between the two net classes meets the tDQSS timing parameter.

For additional guidance, see *Understanding TI's PCB routing rule-based DDR timing*.

2.4.5 SPI

When booting from SPI EEPROM or Flash devices, use SPIx_CS[0].

2.4.6 I2C

- Approximately 5K pull ups on both lines (only one set, or two sets of 10K pull ups) are recommended.
- Make sure that all devices on a given I2C bus have unique addresses (often this is configurable through a pin to enable multiple of the same device).

2.4.7 McASP

The transmit bit clock, ACLKX, can only be derived:

- From an external source via the AHCLKX pin
- Internally from the AUXCLK

ACLKX *cannot* be sourced from the AHCLKR pin. For more information about clock sourcing diagrams, see the *McASP* chapter of the device-specific TRM.

2.4.7.1 Audio

- Filter audio power rails.
- Audio ground should be single-point. This is accomplished by separating (and using different symbols for) digital and analog grounds on the schematic and then connecting them together with a 0 ohm resistor or ferrite bead in the schematic. This ensures that all audio grounds are connected to digital ground at only one point, thereby reducing the chance of ground loops.

2.4.8 USB

2.4.8.1 USB0 (USB 2.0 OTG)

Table 1. USB0 Guidelines

Pin	Question	Operating Mode							
		HS Host	FS Host	LS Host	HS Device	FS Device	LS Device	OTG A Device	OTG B Device
USB0_DM	Series or pull resistor needed?	No	No	No	No	No	No	No	No
USB0_DP	Series or pull resistor required?	No	No	No	No	No	No	No	No
USB0_VDDA33	Connect to...	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
USB0_ID	Connect to...	Ground	Ground	Ground	Floating	Floating	Floating	Direct to cable	Direct to cable
USB0_VBUS	Connect to...	Power supply & connector	Power supply & connector	Power supply & connector	Connector	Connector	Connector	Power supply & connector	Connector
USB0_REFCLKIN	Recommended frequencies...	12,24,48,19.2,38.4,13,26,20,40 MHz							
USB0_VDDA18	Connect to...	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
USB0_VDDA12	Bypass cap value	0.22 µF							
USB0_CVDD	Connect to...	1.2 V (1.32 V max)							

2.4.8.2 USB1 (USB 1.1 OHCI)

- No external pull resistors are required for the DM/DP pins.
- Connect USB_CVDD to 1.2 V (1.32 V max)

2.4.8.3 Unused USB pins

The data manual recommends connecting USB0_VDDA12 to a 0.22 µF capacitor even when neither USB port is being used. That differs from an earlier recommendation to leave USB0_VDDA12 as a no-connect in the case where neither USB port is used. That connection is not expected to be problematic for existing designs, but the recommendation moving forward is to always populate the 0.22 µF capacitor. This topic is discussed in this E2E post.

2.4.8.4 USB Board Design Guidelines

General routing and placement guidelines for USB interfaces:

1. Place the USB PHY and major components on the un-routed board first.
2. Route the high-speed clock and high-speed USB differential signals with minimal trace lengths.
3. Route the high-speed USB signals on the plane closest to the ground plane, whenever possible.
4. Route the high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.
5. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
6. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.
7. Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mils.
8. Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.

Note that USB supports hot insertion and removal, so it is very vulnerable to ESD resulting from this. External ESD protection like the TPD2E001 or TPD3E001 is recommended. For USB OTG, the recommended ESD protection is the TPD4S012. Any USB 2.0 certified ESD protection chip is acceptable as long as the USB PCB routing guidelines are followed.

For in-depth details, see the *High-speed interface layout guidelines*.

2.4.8.4.1 Cautionary note - USB PHY off while host is still powered on

When the USB PHY is powered off while still connected to a host that is powered on, the customer may notice leakage on the 3.3 V supply. This is because there is a path between VBUS and the 3.3 V supply rail that allows current to leak from the powered VBUS to the 3.3 V supply rail.

If the USB PHY remains powered off for an indefinite period of time while connected to a powered VBUS, there is a risk of long-term stress on the PHY's internal circuitry. TI therefore recommends that customers isolate the input USB0_VBUS from the VBUS until the device is powered up. This can be accomplished by implementing a discrete load switch such as TPS22913. Some example circuits are shown in Figure 2 and Figure 3.

If the SoC supports OTG Host/Device mode:

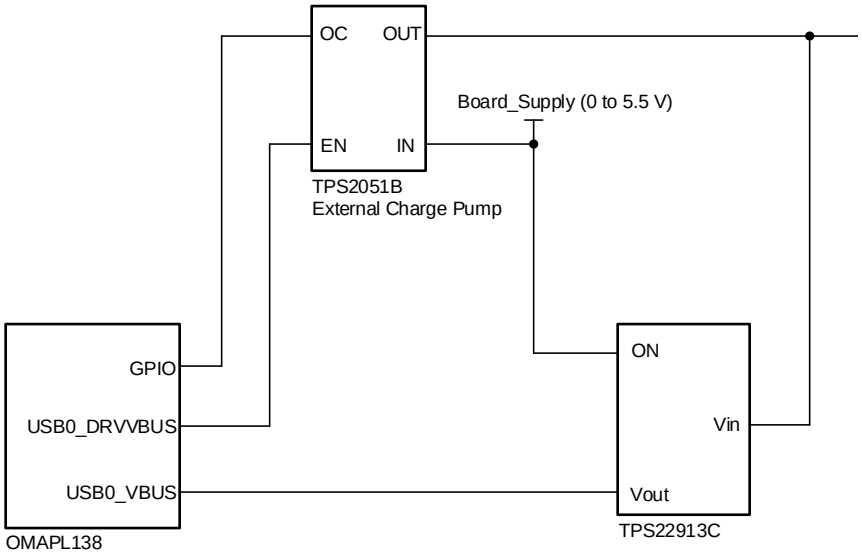

Figure 2. Isolation Circuit for OTG Host/Device Mode

If the SoC supports Device-only mode:

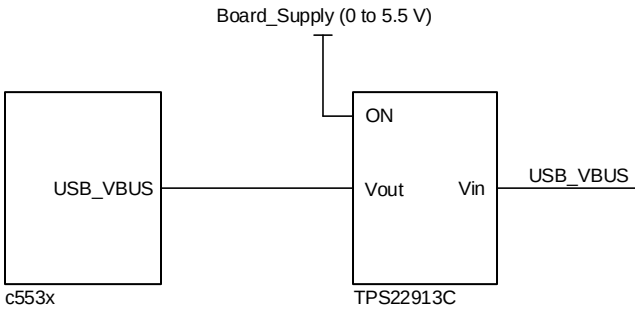

Figure 3. Isolation Circuit for Device-Only Mode

2.4.9 Other

2.4.9.1 Signal Visibility

For debugging purposes, it is often useful to be able to monitor a signal with an oscilloscope. For that purpose, it is helpful to provide access to the signals via test points, particularly with BGA devices where it might otherwise be impossible. Signals that are pulled up or down may also be probed at the resistor. Having a GPIO brought to a test point or an LED can be useful for debug, as well.

2.4.9.2 Voltage Level Changes

Can you change the supply voltage with some simple resistor changes? Sometimes a pin-for-pin compatible release is made at a higher speed, sometimes requiring higher voltage. Having this flexibility on your board can save you re-design work later.

2.4.9.3 Signal Terminations

Careful attention should be paid to any notes in the device-specific data sheet regarding the correct termination of pins. In particular, make sure to follow any instructions regarding termination instructions for reserved pins. Also, there are often pins that have special significance at the time the device reset is released. Often these are documented with something like "do not oppose this pin at reset" meaning that if there is an internal pullup or pulldown on that pin, you should not drive that pin in the opposite direction at reset. This would include not putting an opposing pullup/pulldown and also making sure that anything connected to that pin does not drive the pin opposite the intended direction.

Pay close attention to how any unused pin is terminated. Frequently, pins will default to an input state. If left floating, they can pick up noise and toggle at a high frequency. This can cause significant unwanted current consumption. Unused pins should be checked to see if they can be configured through software as outputs so they are not floating. If there is an internal pull-up/down you should configure the level of the output (high/low) to match the pull-up/down for lowest current consumption.

2.4.9.4 Ground Symbols

Ground symbols must have applicable names assigned to them. Also, the net name of each ground symbol should be displayed on the schematic in order to help a reviewer to verify that no ground connections are orphaned by mistake. Use a standard triangle ground symbol for the main digital ground. Then use a signal ground (symbol with decreasing horizontal lines) for all other grounds. Use different net names for these local grounds to allow easy review of the schematic, as well as easy referral to them in the PCB layout tools.

2.4.9.5 Power Symbols

Power symbols must have applicable names assigned to them. Also, the schematic should display the unique name for each power net. Placing a 'V' for the first character of a power supply can ease the schematic verification process since the power supply net names will appear next to each other in the view of the nets on the board.

3 BGA PCB Design

In addition to the 176-pin HLQFP (PTP) package, the devices discussed in this document are available in the following different BGA packages:

- 0.65 mm-pitch ZCE
- 0.80 mm-pitch ZWT
- 1.0 mm-pitch ZKB

For additional guidance on PCB design for BGA devices, see the *AM57xx BGA PCB Design*.

4 Power Management Solutions

For power management solutions, see the TI power management webpage: TI Power Management Solutions.

In addition, WEBBENCH designer tools provide a visual interface that delivers a complete power application in seconds WEBBENCH.

5 References

- Texas Instruments: *Using the OMAP-L132/L138 bootloader*
- Texas Instruments: *Understanding TI's PCB routing rule-based DDR timing*
- Texas Instruments: *High-speed interface layout guidelines*
- Texas Instruments: *AM57xx BGA PCB Design*

XDS Connector Design Checklist

A.1 XDS Connector Design

This checklist can be applied to any XDS connector for both JTAG and Trace applications.

Table 2. JTAG 1149.1 Port Description

PIN	XDS SignalType	Target Signal Type	NAME	CHECKLIST ITEMS
$\overline{\text{TRST}}$	O	I	Test Logic Reset	TRST- should normally be pulled down on the target card. This holds the device's JTAG/debug logic in reset when an XDS cable is not present. For all cases, this is the normal operating mode of the device. If a device does not have a $\overline{\text{TRST}}$ pin then the pin on the connector can be left disconnected. TI recommends a 4.7K pull-down but common values in the 4.7K to 10K range are acceptable.
TCK	O	I	Test Clock	The requirements for TCK are dependent on the number of devices in the JTAG serial chain and on the routing distance of the TCK signal. • Single device case AND TCK routing distance less than 6 inches - In this case, the only requirement is a series termination resistor. Normally, a value of 22 Ω is sufficient. The termination resistor should be placed physically near the XDS connector and its location noted in the schematics. • Multiple device case OR single device case and TCK routing greater than 6 inches - In this case, a buffer is required to drive TCK from the connector to the device (or all devices in the multiple device JTAG serial chain). The buffer should be series terminated near the buffer output, the size of which is dependent on the buffer selected. The buffer input should be AC terminated per the following link and pulled up to eliminate switching if the XDS is disconnected. TI recommends a 4.7K pull-up but common values in the 4.7K to 10K range are acceptable.
TMS	O	I	Test Mode Select	The requirements for TMS are dependent on the number of devices in the JTAG serial chain and on the TMS signal routing distance. • Single device case AND TMS routing distance less than 6 inches - This signal is a direct connect between the XDS connector and the device. • Multiple device case OR single device case and TMS routing greater than 6 inches - A buffer is required with a pull-up on the input. TI recommends a 4.7K pull-up but common values in the 4.7K to 10K range are acceptable. The buffered output is routed to all devices in the serial scan chain.

Table 2. JTAG 1149.1 Port Description (continued)

PIN	XDS SignalType	Target Signal Type	NAME	CHECKLIST ITEMS
TDI	O	I	Test Data Input	The requirements for TDI are dependent on the number of devices in the JTAG serial chain and on the TDI signal routing distance. • Single device case AND TDI routing distance less than 6 inches - This signal is a direct connect between the XDS connector and the device. • Multiple device case OR single device case and TDI routing greater than 6 inches - This signal is buffered from the XDS connector to the device. The buffer requires a pull-up on the input. TI recommends a 4.7K pull-up but common values in the 4.7K to 10K range are acceptable. In the single device case the output of the buffer is connected to the devices TDI pin. In the Multiple device JTAG serial chain case the buffered output is routed to the first device in the serial scan chain. TDO of each device is connected to TDI of the next device (except in the case of the last device). In any cases where the routing between devices (TDO to TDI) is greater than six inches a buffer (with a pull-up on the input) is required.
TDO	I	O	Test Data Output	The requirements for TDO are dependent on the number of devices in the JTAG serial chain and on the TDO signal routing distance. • Single/Multiple device case AND TDO routing distance less than 6 inches - This signal is a direct connect between the device (in the multiple device case the last device in the scan chain) and the XDS connector and requires a series termination resistor near the device. Normally a 22 Ω termination resistor is sufficient, but ideally matching the input impedance of the XDS cable (normally 50 Ω) will provide the most robust connection (see Non-buffered JTAG Signal Termination for details). • Single/Multiple device AND TDI routing greater than 6 inches - This signal requires a buffer between the device (in the multiple device case the last device in the scan chain) and the XDS connector. The buffer requires a pull-up on the input. TI recommends a 4.7K pull-up but common values in the 4.7K to 10K range are acceptable.

Table 2. JTAG 1149.1 Port Description (continued)

PIN	XDS SignalType	Target Signal Type	NAME	CHECKLIST ITEMS
RTCK	I	O	TCK Return	The requirements for TCK are dependent on the number of devices in the JTAG serial chain, on the routing distance of the TCK signal, and if the device supports a RTCK pin. • Single device AND the device has no RTCK pin AND TCK is not buffered - In this case a simple loop from the TCK pin to the RTCK pin of the XDS connector with a series termination resistor is all that is required. Normally a 22 Ω termination resistor is sufficient, but ideally matching the input impedance of the XDS cable (normally 50 Ω) will provide the most robust connection (see Non-buffered JTAG Signal Termination for details). • Single/Multiple devices AND none of the devices in the JTAG scan chain have a RTCK pin AND TCK is buffered - If TCK is buffered, RTCK should normally be buffered to provide the same delay to the XDS as the device (or first device) will see through the TCK buffer. When buffering RTCK a series termination resistor should be utilized. Normally a 22 Ω termination resistor is sufficient, but ideally matching the input impedance of the XDS cable (normally 50 Ω) will provide the most robust connection. For details, see the Non-buffered JTAG Signal Termination. The RTCK buffer input should be pulled-up by the same pull-up resistor that is used to pull-up TCK's buffer input. • Single device AND the device has a RTCK pin AND TCK is not buffered - This signal is a direct connect between the device and the XDS connector and requires a series termination resistor near the device. Normally a 22 Ω termination resistor is sufficient, but ideally matching the input impedance of the XDS cable (normally 50 Ω) will provide the most robust connection. For more details, see the Non-buffered JTAG Signal Termination. • Single device AND the device has a RTCK pin AND TCK is buffered - In this case RTCK is buffered from the device to the XDS connector. A series termination resistor is required on the output of the buffer. Normally a 22 Ω termination resistor is sufficient, but ideally matching the input impedance of the XDS cable (normally 50 Ω) will provide the most robust connection. For more details, see the Non-buffered JTAG Signal Termination. • Multiple devices AND the device has a RTCK pin - For details, see Multi-device Adaptive Clocking. When working with these topographies if any signal routing exceeds six inches, it is recommend you buffer the signals (with pull-ups on the inputs) and on clock signals adding series termination resistors.

1. To confirm compatibility with your XDS for signal types voltage levels, check your device-specific data sheet.

The following signals may also be present on your XDS Target Cable and are common to many XDS products.

Table 3. Additional Common Emulation Header Signal Descriptions

PIN	XDS Signal Type	Target Signal Type	NAME	DESCRIPTION
TVRef	I	O	Target Voltage Reference	Must be tied to the I/O voltage of the target device used for JTAG through a 100 Ω current limiting resistor. Used by the XDS to detect if power is active and to set JTAG signal voltage level translators (if supported by the XDS(1).
TDIS	I	O	Target Disconnect	If your XDS connector supports this signal it must be tied directly to the target's ground plane. Connecting it through a pull-down resistor may cause the XDS to NOT detect the target system and prevent normal operation.
EMU[0:n]	I/O	I/O	Emulation Port	EMU0 and EMU1 must be pulled-up on the target card. For EMU0 and EMU1, it is not recommended relying on the internal pull-ups normally provided in most devices on the EMU pins. It is recommended to connect all the XDS pins supported by your device to the XDS connector. In cases where you are connecting more than EMU0 and EMU1, follow the instructions in the *Emulation and Trace Headers Technical Reference Manual*. In cases where the device supports more than two EMU pins, these devices normally support high speed trace (either Core Trace, System Trace or both) in which case it is a requirement to utilize termination resistors per Emulation and Trace Headers Technical Reference Manual. In cases where the device has more EMU pins than the XDS supports, the general rule is to connect as many EMU signals as possible to the XDS connector. For some device families, due to packaging size limitations, EMU signals are being multiplexed with other device functional signals on a single pin. If you are not using the functional signal then simply connect the pin to the XDS connector per the instructions in the previous paragraph. If you need both the functional and EMU (trace) capabilities then TI recommends you isolate the XDS header and functional circuit from each other using a FET mux.
nRESET	O	I	Target Reset	This is an optional signal that if integrated into your application's power-up-reset circuit may be used to remotely reset the target board. This signal driven from the XDS (if supported) is open-drain and therefore requires a pull-up.

1. Some TI documents refer to TVRef as TVD, VREF_DEBUG, and VTRef (Arm's naming convention).
2. Some TI documents refer to nRESET as nSYSRST or nTGTRST.

Connecting NOR Flash to OMAP-L138

B.1 Connecting Memory Devices <32 MB

This is a standard hookup with no glue logic needed.

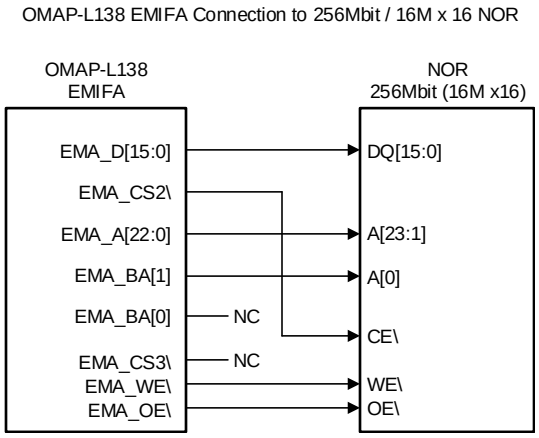

Figure 4. Hardware Connection for 16 M x 16 Device

This is a standard hookup with no glue logic needed.

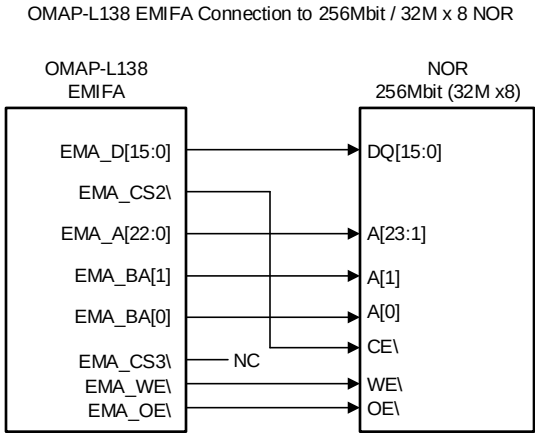

Figure 5. Hardware Connection for 16 M x 16 Device

B.2 Connecting Memory Devices >32 MB

The device memory map was designed such that each chip select could address 32 MB of external memory. In order to go beyond 32 MB, glue logic and additional software configuration is required.

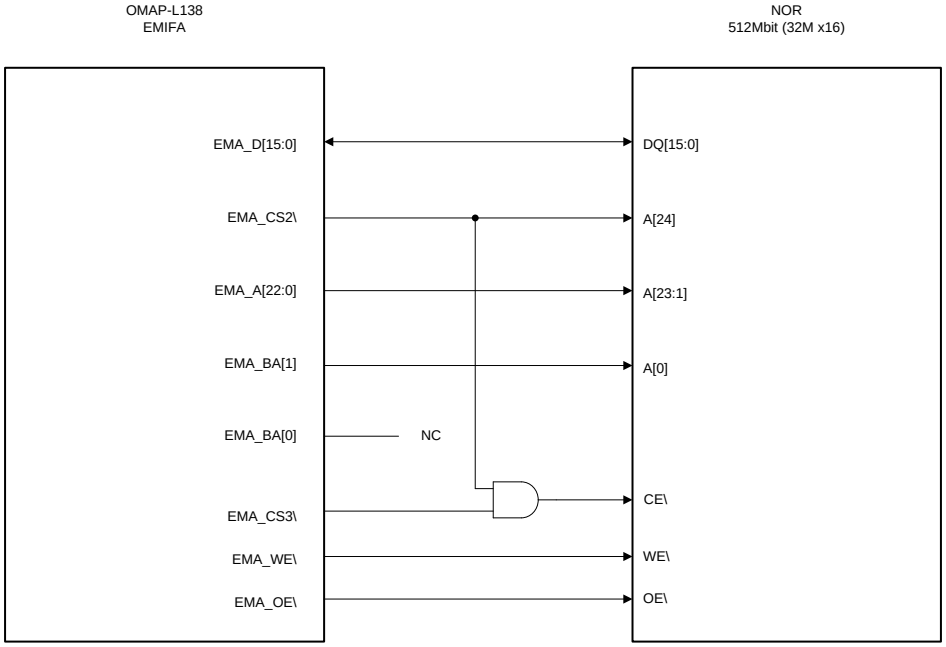

Figure 6. Hardware Connection for 32 M x 16 Device

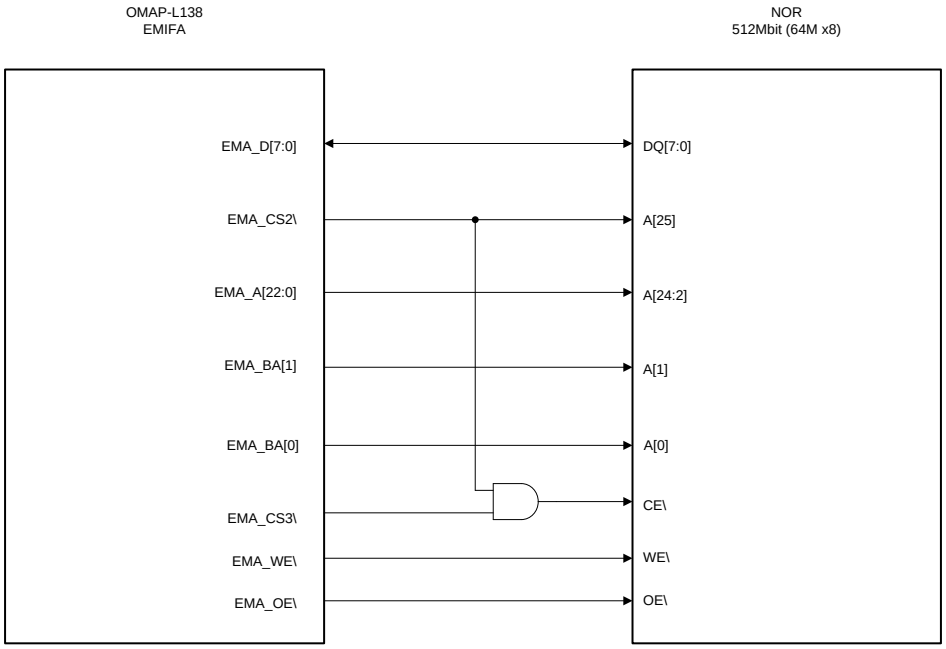

Figure 7. Hardware Connection for 64 M x 8 Device

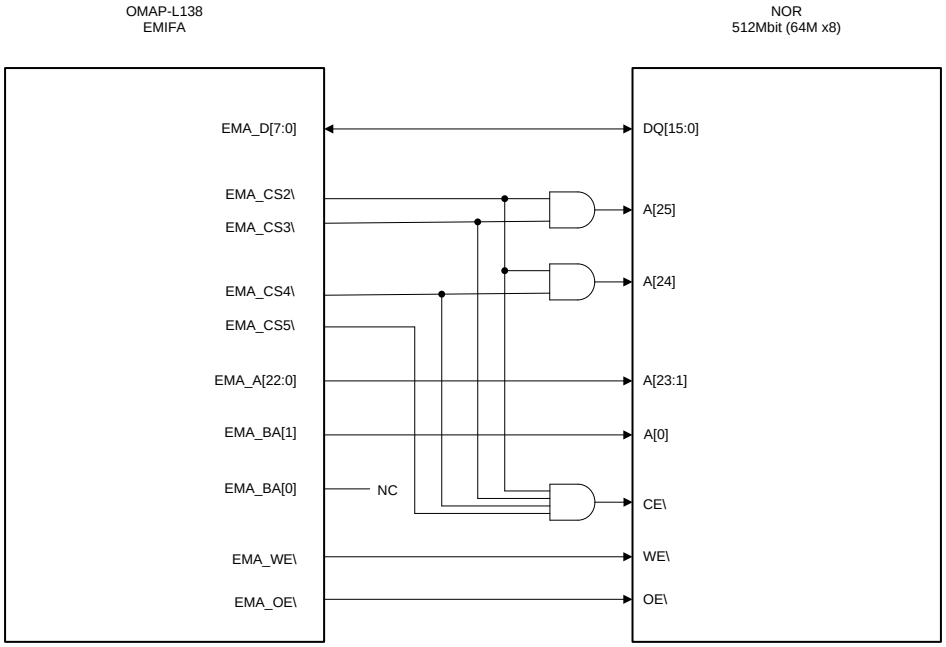

Figure 8. Hardware Connection for 64 M x 16 Device

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265