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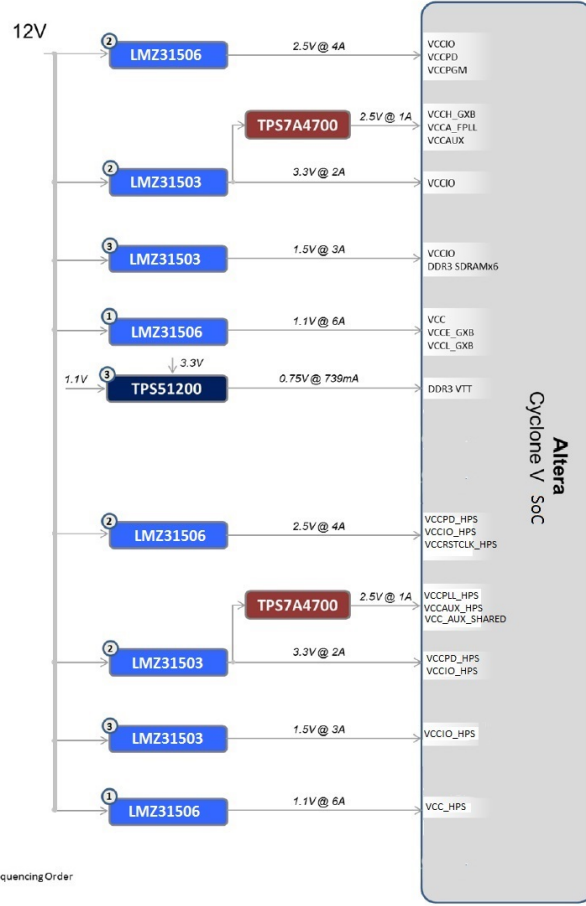
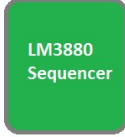
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Revision History	
Revision	Notes



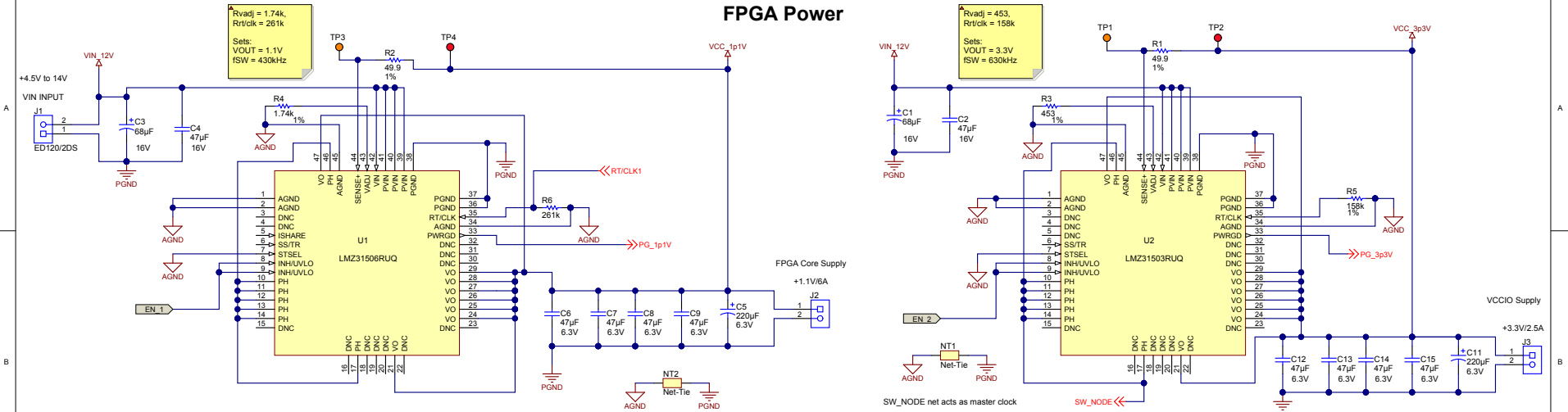
Altera Cyclone V SoC

Designed for: Public Release	Mod. Date: 7/3/2014
Project Title: Altera Cyclone V SoC	
Sheet Title:	
SVN Rev.: Not in version control	Sheet: 1 of 6
Drawn By:	File: Cover Sheet_ANSI-B_SchDoc
Engineer: Sami Sirhan	Size: B
Contact: http://www.ti.com/support	



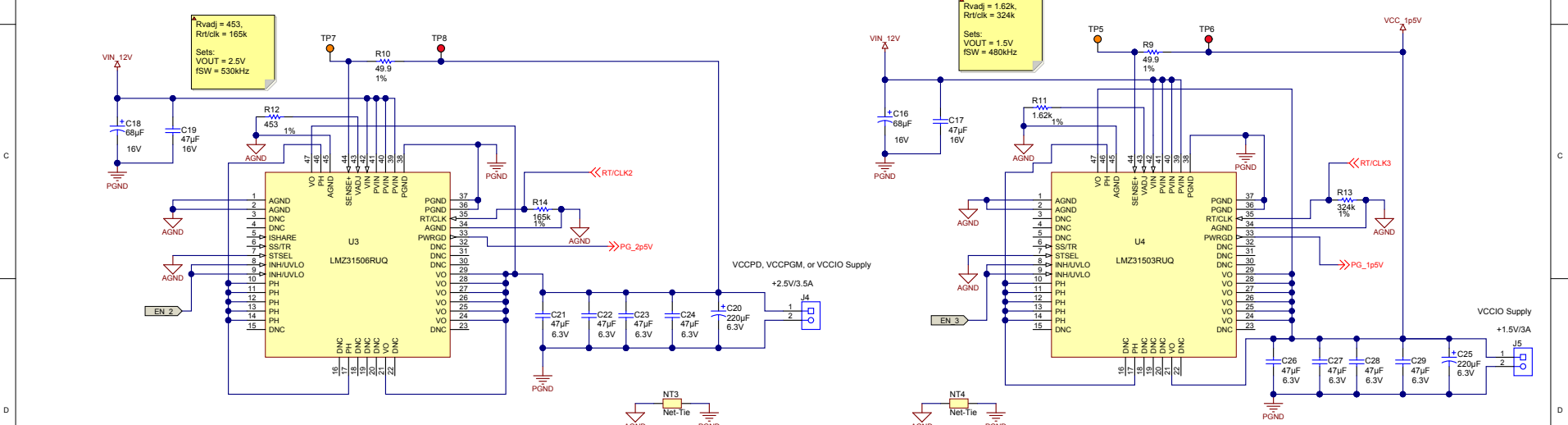
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FPGA Power



PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.

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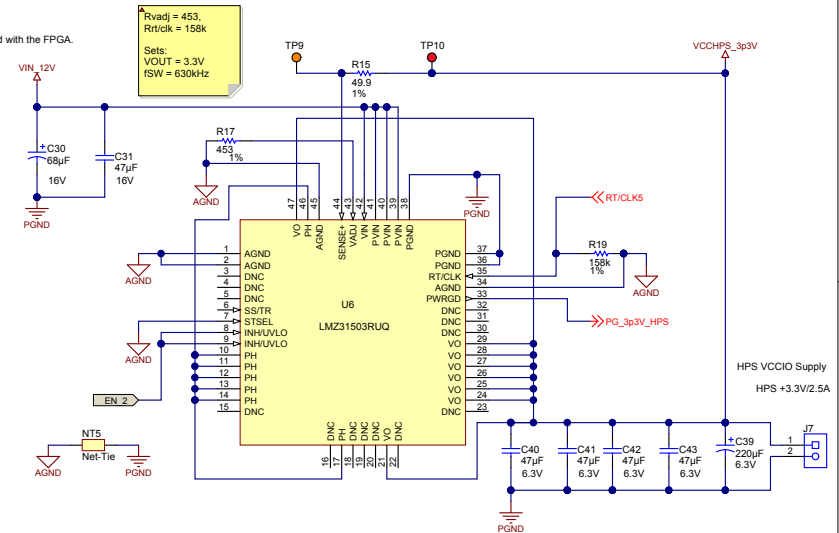
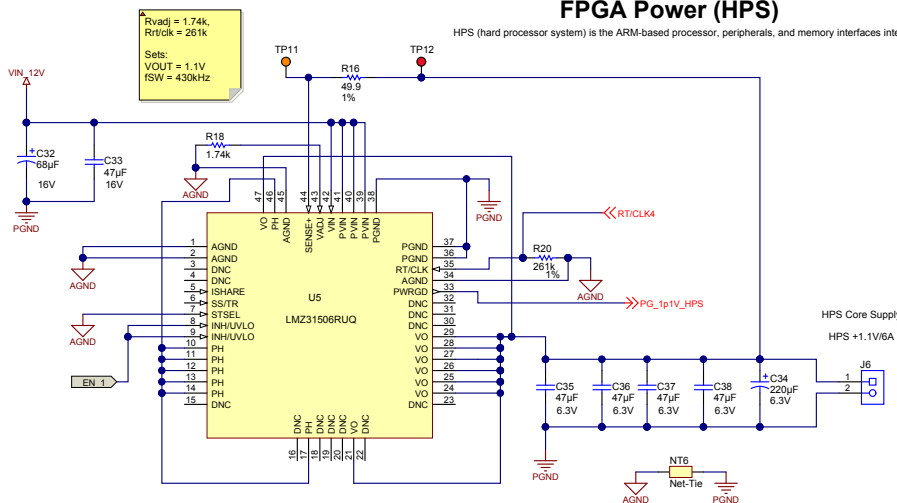


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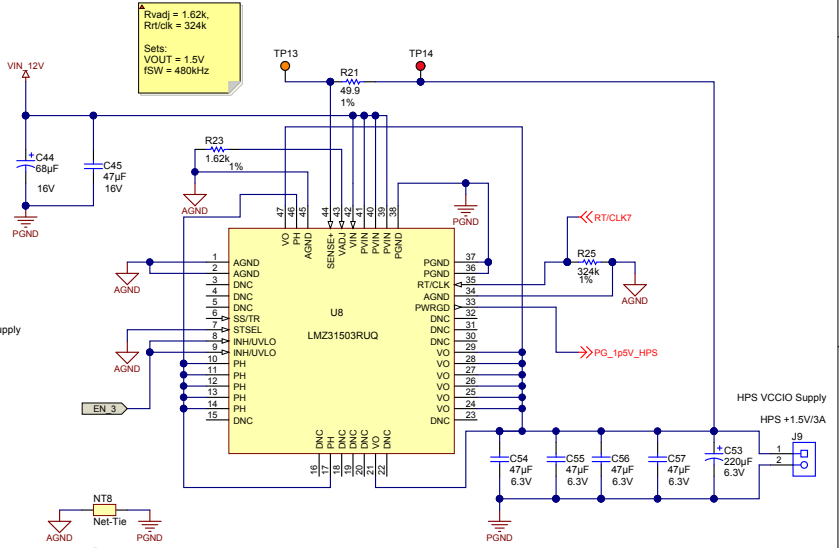
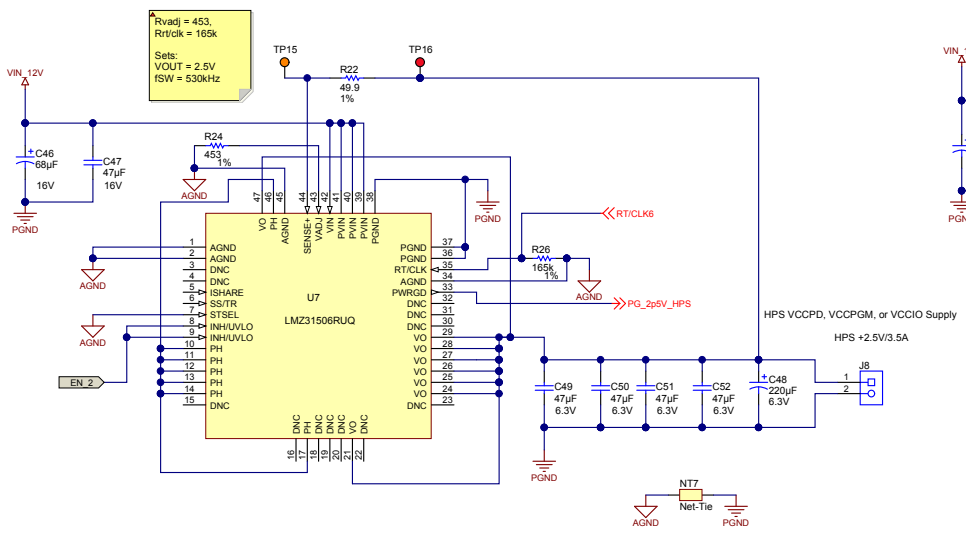
FPGA Power (HPS)

HPS (hard processor system) is the ARM-based processor, peripherals, and memory interfaces integrated with the FPGA.



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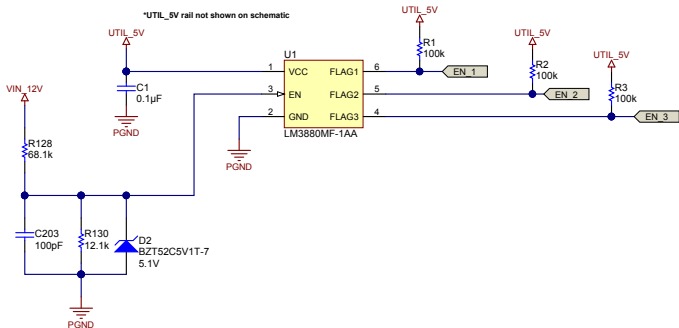
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Number: PMP9353	Rev: E1	Designed for: Public Release	Mod. Date: 7/3/2014
SVN Rev.: Not in version control	Assembly Variant: [No Variations]	Project Title: Altera Cyclone V SoC	Sheet Title:
Drawn By:	Engineer: Sami Sirhan	File: Page2_SchDoc	Sheet 3 of 6
		Contact: http://www.ti.com/support	Size: B



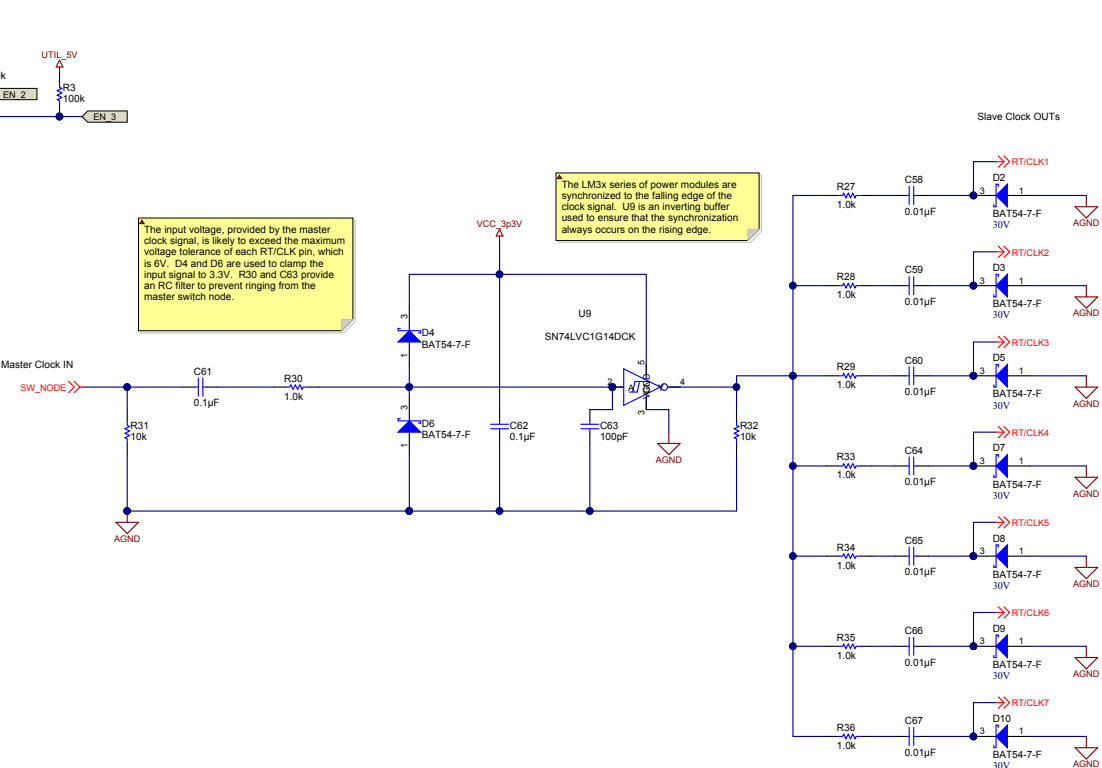
Clock Synchronization Circuit

Sequencer



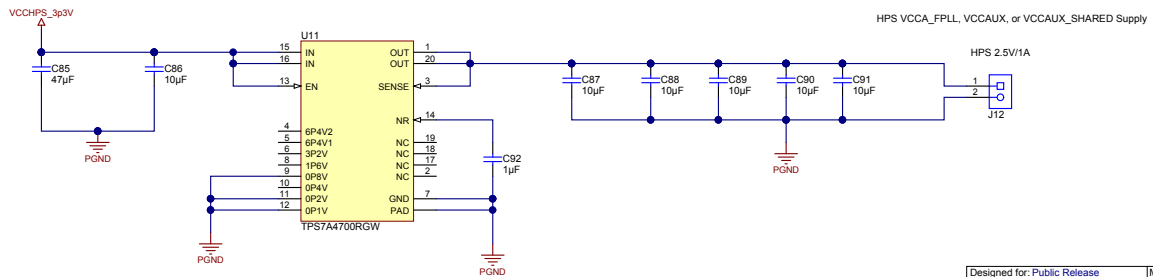
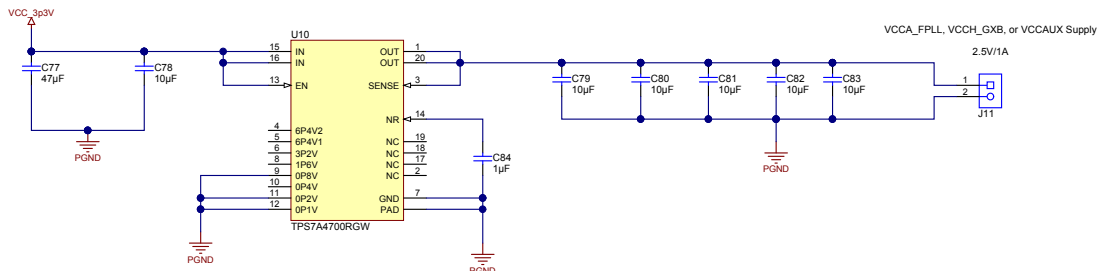
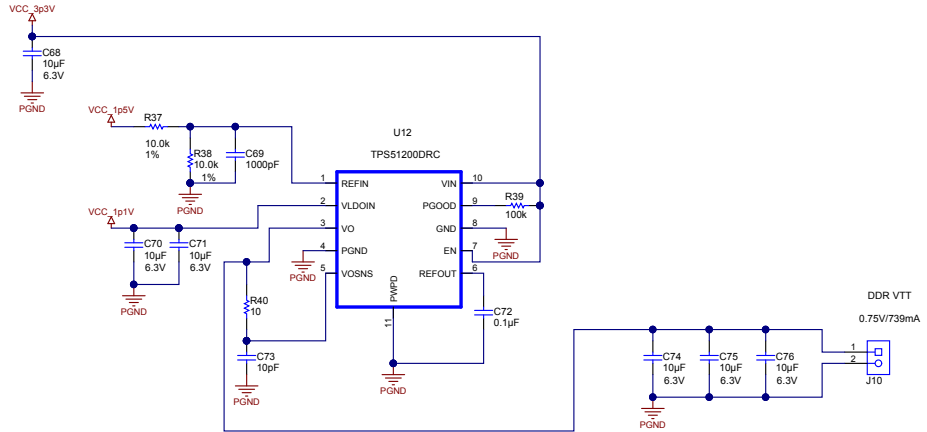
The input voltage, provided by the master clock signal, is likely to exceed the maximum voltage tolerance of each RTI/CLK pin, which is 5V. D4 and D6 are used to clamp the input signal to 3.3V. R30 and C63 provide an RC filter to prevent ringing from the master switch node.

The LM3x series of power modules are synchronized to the falling edge of the clock signal. U9 is an inverting buffer used to ensure that the synchronization always occurs on the rising edge.



Slave Clock OUTs

DDR Termination and LDOs



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Number: PMP9353	Rev: E1	Designed for: Public Release	Mod. Date: 2/19/2014
SVN Rev.: Not in version control		Project Title: Altera Cyclone V SoC	
Drawn By:		Sheet Title:	
Engineer: Sami Sirhan	Assembly Variant: [No Variations]	File: Page 4.SchDoc	
	Contact: http://www.ti.com/support	Sheet 5 of 6	Size: B



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