Ebenezer Dwobeng

TI Designs High Speed: Verified Design

Measuring Bit Errors in the Output Word of an A/D Converter

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Design Resources

Source code is available by request through the High Speed Data Converter E2E forum.

High Speed Data Converters Forum

Design Overview

For applications where there are bit errors and resulting sample errors (also called sparkle codes, word errors, or code errors), the ability to measure the Error rates caused by these bit errors is important. This application note proposes a method to accurately measure these errors over an indefinite time and provides an example of how this measurement can be done using a simple FPGA platform. Code is available for the two examples described in the application note.

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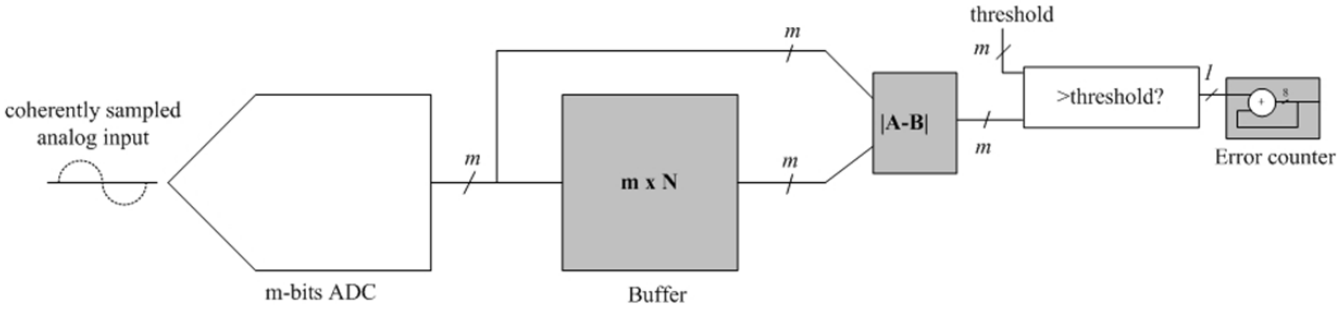

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1 Measuring Bit Errors in the Output Word of an A/D Converter

Words don't always come out of an ADC the right way.

Some bit errors in the output words of an analog-to-digital converter (ADC), such as those due to comparator metastability (sparkle codes) [1] and low frequency flicker noise, occur over a large number of ADC output words. These are not always captured in common performance metrics such as signal-to-noise ratio (SNR) or effective number of bits (ENOB), which relies on spectral analysis of a limited number of the output words over a short time interval.

The complex computations involved in Fast Fourier Transform (FFT) algorithms used in spectral analysis [2] and the large memory size required to store data, makes this method impractical for BER analysis because of the long observation window required. Expected error rates for applications such as *Bluetooth*®, WLAN, and instrumentation are depicted in Figure 1. [1]

One common method is to detect and count bit errors by comparing two successive words (or samples) out of an ADC. Because the sampling frequency and input signal are carefully chosen to ensure that there is less than one least-significant bit (LSB) change between successive samples, a bit error is detected if this difference is greater than an LSB.

In this application note, a means to continuously monitor and log bit errors by comparing samples in successive frames of the output codes of an ADC output codes is discussed. Implementation results using LatticeECP3™ FPGA on a TSW1405 data capture card [3] and TI's ADS5402 [4] and ADS4249 [5] ADCs are given. The application note also briefly discusses coherent sampling and the confidence level of a BER measurement.

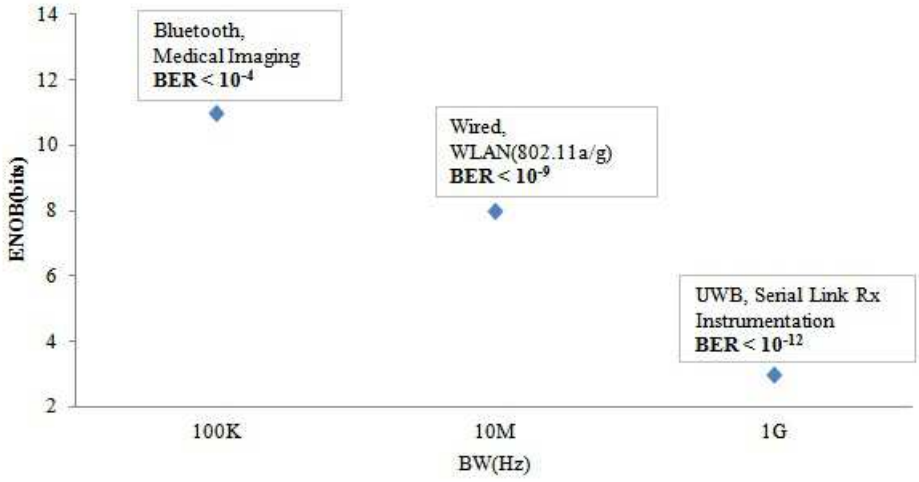

Figure 1. BER Requirements of Some Common Applications

2 Confidence Level of a BER Measurement

Bit-error rate is the ratio of the number of erroneous bits observed to the total number of bits in a bit stream. When applied to ADCs, the bit-error rate measures the number of erroneous samples expected at the output within a given time interval. Because the occurrence of bit errors is a random process, a large number of samples must be observed over a long period (ideally infinite) to accurately determine the error rate. However, in a real world measurement, the number of observable samples is limited by finite test time. Thus, the actual value for the BER cannot be determined with 100% certainty.

The confidence level (*CL*) gives the probability that a measured BER value is less than or equal to the actual BER value if the bits where observed over an infinite time. The *CL* is related to the number of bits that are transmitted (or received) through a system without any errors (*n*) and the actual value of the BER if the bit stream is observed for an infinite time (*p*) by Equation 1 [6]:

$$n = \frac{\ln(1 - CL)}{p} \quad . \tag{1}$$

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Thus, to determine if the BER of a system is less than *p* at a confidence level of *CL*, it should be possible to transmit (or receive) at least *n* total bits through the system without any error. As an example, to determine if the actual BER value is less than 10^{-10} (*p*) with a 95% certainty (*CL*), the total number of bits to transmit without errors (*n*) evaluates to 2.996×10^{10} bits (from Equation 1). For a 14-bit ADC running at 100 MSPS, this means that the ADC should be able to run for approximately 22 seconds without any bit error (or sample error).

3 Concept of ADC BER Estimation

A continuous time signal is generally represented by Equation 2.

$$y = \sin(2\pi f_{in} t) \tag{2}$$

When the continuous time signal in Equation 2, with a frequency f_{in} is sampled at a rate f_s, the duration of sampling is related to the number of cycles (N_{cycle}) of the continuous signal and the number of samples (*N*) by Equation 3:

$$\text{Sampling time} = \frac{N}{f_s} = \frac{N_{cycle}}{f_{in}} \tag{3}$$

If the number of cycles of the continuous time signal (N_{cycle}) is a positive integer, then the frequency pair f_{in} and f_s are coherent frequencies. Coherency ensures that every group of N_{cycle} cycles of the continuous signal has exactly N discrete samples and every group of N discrete samples is the same ($[y_0, y_1 ... y_{N-1}] = [y_{Nm}, y_{Nm+1} \ldots y2_{Nm-1}]$, m is a positive integer)

The resulting discrete time signal obtained after sampling is given by Equation 4.

$$y(n) = \sin\left(2\pi \frac{f_{in}}{f_s} n\right) = \sin\left(2\pi \frac{N_{cycle}}{N} n\right)$$

$$n = \mathbb{Z}^+ \text{ (positive integer)} \tag{4}$$

The least value of *n* after which the discrete samples start repeating is the period of the discrete signal. From Equation 4, when N_{cycle} is a prime number, the discrete signal y(n) will only start repeating when *n* equals to *N*. Consequently, from Equation 3, if f_{in}, f_s, and *N* are chosen to ensure that N_{cycle} is a prime integer, then the resulting discrete time signal is ensured to have *N* unique discrete samples.

As shown conceptually in Figure 2, all the *N* unique output words (or samples) in one period of the discrete time signal from an m-bits ADC are captured and stored in a buffer of size $m \times N$. These samples are then compared with the next *N* samples out of the ADC. If the sampling frequency and input signal frequency are coherent and the number of the continuous time signal cycles after *N* discrete time samples is a prime number, then sample numbers *n* and $n + N$ are equal if there are no bit errors. However, if there are bit errors in the ADC's output codes, the difference between these two samples is non-zero. The magnitude of this difference depends on the error bit position. Thus any non-zero value resulting from subtracting the corresponding samples *n* and $n + N$ is flagged as a bit error. The magnitude of the error is compared with a threshold value to determine the bit position where the error is located and then counted by an error counter.

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3.1 Double Counting

Every ADC output word is compared twice; once with the corresponding sample in the frame before it and also with the corresponding sample in the frame after it. To avoid counting word errors twice, the output of the error counter is divided by 2.

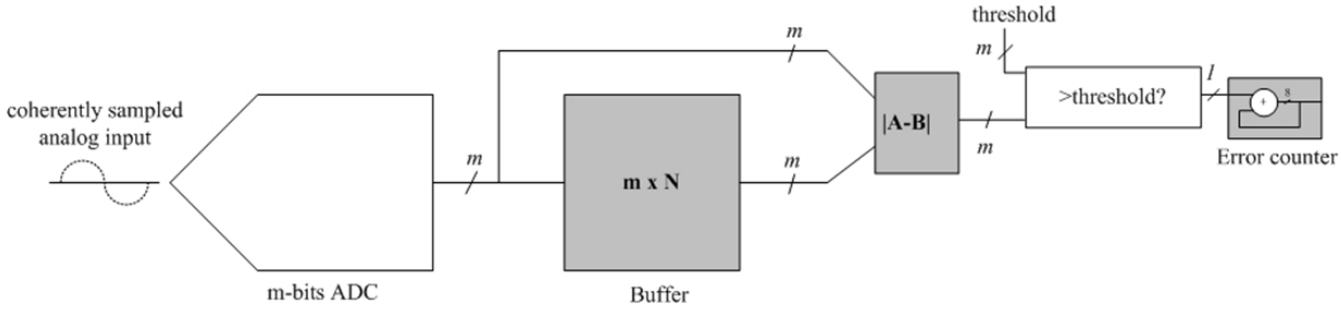

Figure 2. Conceptual Diagram of Module used to Detect and Count ADC Word Errors

The value of *N* (or the frame size) must be chosen to ensure that all the ADCs output codes are tested for bit errors. This requires that the total number of samples in a period (*N*) of the discrete time signal must be at least equal to $2^{\text{ADC resolution}}$.

3.2 Implementation

The module shown in Figure 3 detects and counts the bit errors in the output of the ADC. The module consists of an interface block to receive data from the ADC, a double-clock FIFO (dclk FIFO), single-clock FIFO (sclk FIFO), a subtractor and an error counter. Data is represented in 2's complement format.

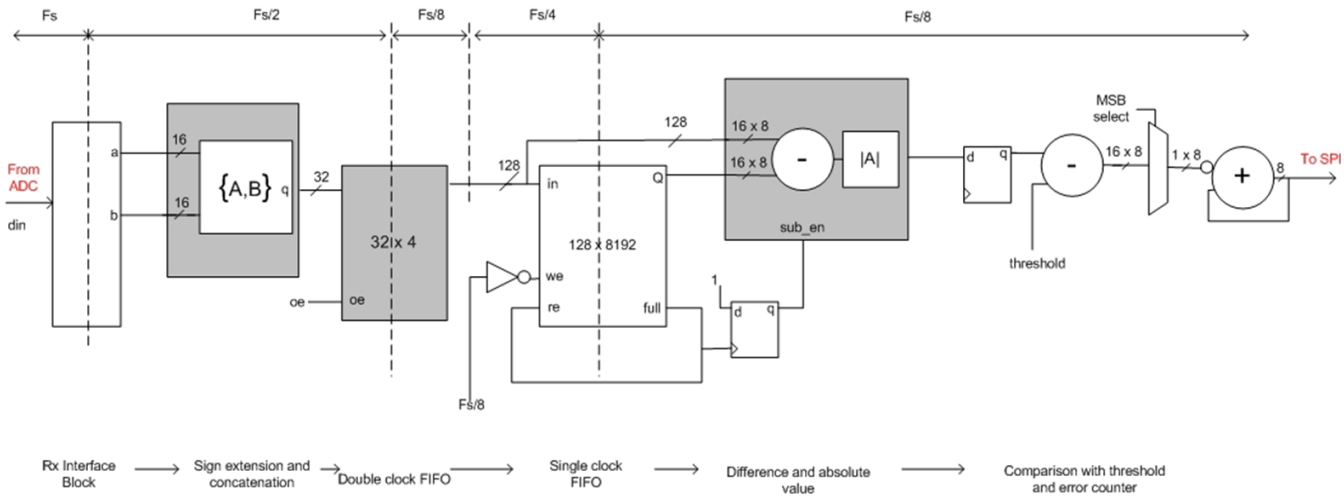

Figure 3. Module for Measuring Word Errors of an ADC

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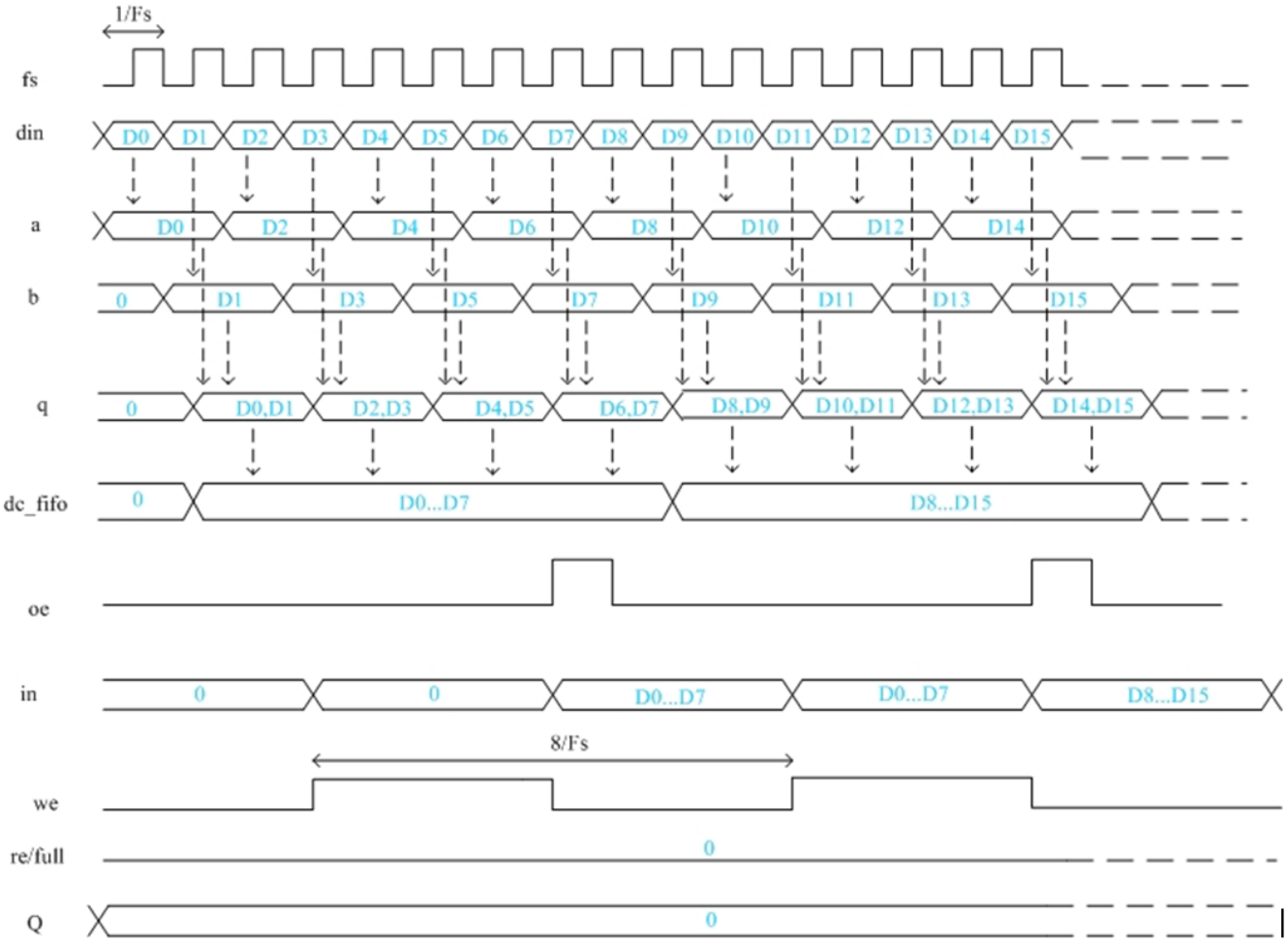

Figure 4. Timing Behavior for First 64k Samples Before the Full Flag of sclk FIFO is Asserted

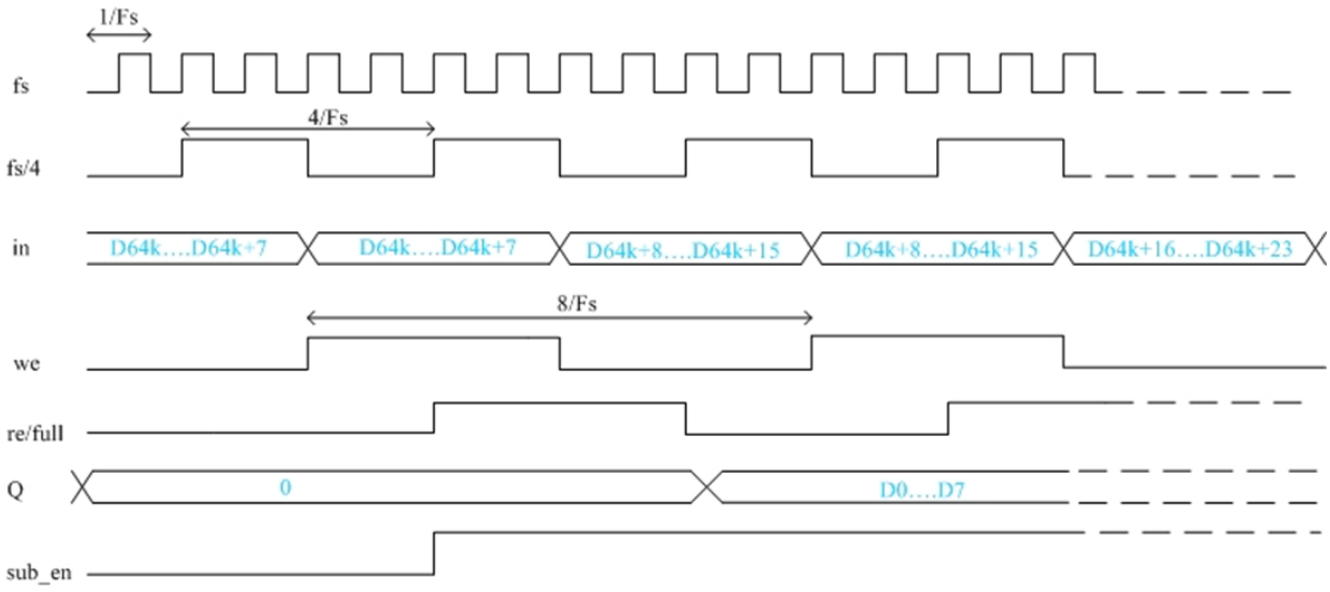

Figure 5. Timing Behavior After First 64k Samples When the Full Flag of sclk FIFO is Asserted

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The interface block receives data coming in from the ADC. This data is either double data rate (DDR) or single data rate (SDR). All the major FPGA vendors include this module as part of their IP library. For implementation on a LatticeECP3 FPGA, use the IDDRX2D1 [7] primitive when interfacing to a DDR ADC.

The module after the interface block extends the sign bit (or MSB) of the m-bit two's complement data from the ADC into a 16-bit word (if m < 16). The module also concatenates two consecutive samples into one 32-bit word for the dclk FIFO.

The dclk FIFO block accumulates up to 8 samples of the ADC, each 16-bits wide, and outputs 128-bit wide data at 1/8th the input clock speed. This enables the logic following this block to run at a lower speed.

The sclk FIFO block holds one frame of samples from the ADC (up to 64k, 16-bit wide samples on a LatticeECP3 FPGA). Anytime a sample, *n* (*n* is any positive integer), is available at the input of this block, the sample *n* mod 64k inside the FIFO is popped out and the sample, *n*, is written to the end of the FIFO. After this block is reset at startup, the FIFO starts filling with data on the positive edge of clock Fs / 4 when the write enable (*we*) signal is high. Because *we* toggles at a rate of Fs / 8, data is effectively written at this rate until the FIFO fills up and the full flag is asserted. Upon assertion of the full flag, the FIFO read operation is enabled and the first ADC word that was written into the FIFO is popped to the output port (Q). Following the read operation, the full flag is de-asserted just in time for the first word of the next period of 64k samples to be written to the end of the FIFO at the next rising edge of the write clock. Timing diagrams for these signals are found in Figure 4 and Figure 5.

The subtractor block is an asynchronous block that computes the absolute value of the difference between the current sample available at the input of the sclk FIFO and the corresponding sample from the previous frame popped out of the FIFO. The subtractor block enables (sub_en) at the first rising edge of the full flag of sclk FIFO (after it is filled with the first 64k samples from the ADC). The output of this block is always zero if there are no bit errors and the input signal and sample clock frequencies to the ADC are coherent. If there are bit errors, the magnitude of the output depends on the bit position of the error.

The error counter counts the data at the output of the subtractor block that are greater than or equal to a specified threshold value. Data at the output of the subtractor block is latched into the error counter block at a rate of Fs / 8 and the threshold value is subtracted from it. If the difference is negative then the threshold value is greater than the latched data and vice versa. For 2's complement data, the MSB is 1 for negative numbers and 0 for non-negative numbers. Consequently, the counter is incremented by the inverse of the MSB.

3.3 Measured Results

This section describes results from measurements with TI's ADS4249 and ADS5402 ADCs.

3.3.1 ADS4249

Measured results for the ADS4249, a 2-channel, DDR, 14-bit, 250-MSPS ADC are given below. Measurements were carried out over 24 hours at a sample rate of 245.76 MHz and input signal level of –1 dBFs. An appropriate coherent frequency for the input signal was chosen as follows:

minimum frame size (*N*) = $2^{\text{ADC resolution}} = 2^{14}$ ADC words

Because a LatticeECP3 FPGA holds up to 2^{16} of 16-bit words in the internal FIFO, the frame size is set to 2^{15} for each channel.

Desired Input frequency (f_{in})=15.5 MHz

Sample rate (f_s) = 245.76 MHz

$$\text{Number of cycles } \left(N_{cycle}\right) = \frac{N f_{in}}{f_s}$$

$$\text{Number of cycles } \left(N_{cycle}\right) = \frac{2^{15}\left(15.5M\right)}{245.76M} = 2066.6667$$

N_{cycle} is set to 2069, the prime number nearest 2066.6667

$$\text{Coherent frequency} = \frac{2069\ \left(245.76M\right)}{2^{15}} = 15.5175 \text{ MHz}$$

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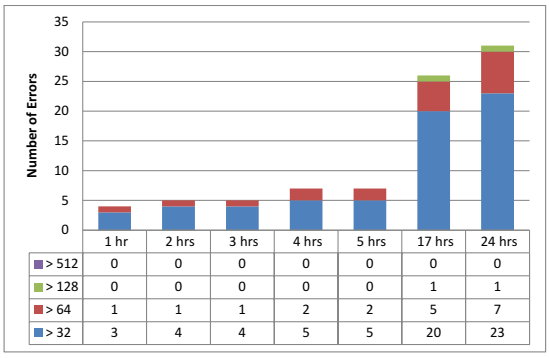
Thus, the frequency of the input signal is set to 15.5175 MHz for a sampling clock frequency of 245.76 MHz. This frequency pair ensures that the samples of the discrete signal only repeats after every 2^{15} samples or after every 2069 cycles of the input signal.

Also threshold values are set at 32, 64, 128, and 512 to determine the magnitude of the errors at the ADC output. Based on these threshold values, the distribution of the error magnitudes after 24 hours of measurements is shown in Figure 6.



	1 hr	2 hrs	3 hrs	4 hrs	5 hrs	17 hrs	24 hrs
> 512	0	0	0	0	0	0	0
> 128	0	0	0	0	0	1	1
> 64	1	1	1	2	2	5	7
> 32	3	4	4	5	5	20	23

Figure 6. Measured Word Errors for ADS4249 ADC Over 24 Hours (hrs)

After 24 hours of measurement:

Total ADC words (in 24 hrs) = 245.76×10^6 $(24 \times 60 \times 60) = 21.2337 \times 10^{12}$

Thus, out of the 21.2337×10^{12} words out of the ADC, 23 were erroneous and the distribution of the magnitude of the errors is as follows:

32 ≤ error magnitude < 64 = 15

64 ≤ error magnitude < 128 = 6

128 ≤ error magnitude < 512 = 1

error magnitude ≥ 512 = 0

3.3.1.1 *BER Estimate for ADS4249 at 95% Confidence Level*

A 95% cofidence level (*CL*) means that if the BER measurements are repeated multiple times, 95% gives results that are either equal to or better than the result presented here.

From Equation 1:

$$n = \frac{\ln(1-CL)}{p}$$

Because no bit errors are observed above 10 LSBs (or error magnitude greater than 512):

$$p = -\frac{\ln(1-CL)}{n} = \frac{\ln(1-0.95)}{21.2337 \times 10^{12}} = 141.08 \times 10^{-15}$$

Consequently, if these measurements are repeated 100 times for ADS4249, 95 times out of the 100 times gives a BER value that is either equal to or less than 141.08×10^{-15} for bits greater than or equal to 10 LSBs.

3.3.2 ADS5402

Measured results for the ADS5402, a 2-channel, DDR, 12-bit, 800-MSPS ADC are given below. Measurements were carried out over 48 hours at a sample rate of 737.28 MHz and input level of –1 dBFs. An appropriate coherent frequency for the input signal was chosen as follows:

minimum frame size (*N*) = $2^{\text{ADC resolution}} = 2^{12}$ ADC words

Because the total available memory on the LatticeECP3 FPGA is $2^{16}$of 16-bit words and the device has two channels, the frame size is set to 2^{15} for each channel.

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Desired Input frequency $(f_{in}) = 15.5$ MHz

Sample rate $(f_s) = 737.28$ MHz

Number of cycles $\left(N_{cycle}\right) = \frac{2^{15}(15.5M)}{737.28M} = 688.8889$

N_{cycle} is set to 691, the prime number nearest 688.8889

Coherent frequency $= \frac{691\ (737.28M)}{2^{15}} = 15.5475$ MHz

Thus, the frequency of the input signal is set to 15.5475 MHz for a sampling clock frequency of 737.28 MHz. This frequency pair ensures that the samples of the discrete signal only repeats after every 215 samples or after every 691 cycles of the input signal.

Also, threshold values are set at 16, 32, and 64 to determine the magnitude of the errors at the ADC output. Based on these threshold values, the distribution of the error magnitudes after 48 hours of measurements is shown in Figure 7.

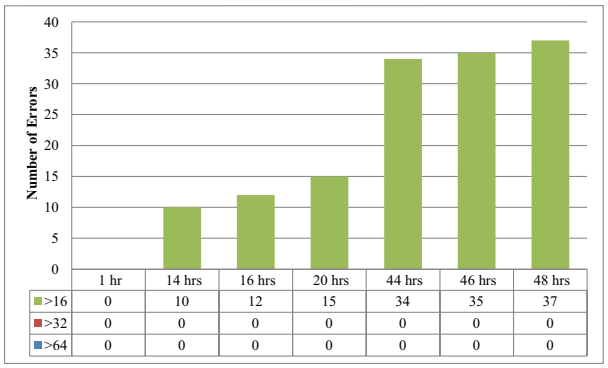

Figure 7. Measured Word Errors for ADS5402 ADC Over 48 Hours (hrs)

After 48 hours of measurement:

Total ADC words (in 48 hrs) = 737.28×10^6 $(48 \times 60 \times 60) = 127 \times 10^{12}$

Thus, of the 127×10^{12} words out of the ADC, 37 were erroneous and the distribution of the magnitude of the errors is as follows:

16 ≤ error magnitude < 32 = 37

32 ≤ error magnitude < 64 = 0

error magnitude ≥ 64 = 0

3.3.2.1 BER Estimate for ADS5402 at 95% Confidence Level

From Equation 1:

$$n = \frac{\ln(1-CL)}{p}.$$

Because no bit errors are observed above 6 LSBs (or error magnitude greater than 32):

$$p = -\frac{\ln(1-CL)}{n} = \frac{\ln(1-0.95)}{127 \times 10^{12}} = 23.588 \times 10^{-15}$$

Consequently, if these measurements are repeated 100 times for ADS5402, 95 times out of the 100 gives a BER value that is either equal to or less than 23.588 $\times 10^{-15}$ for bits greater than or equal to 6 LSBs.

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4 Conclusion

Because of the limitations in the sample size that can be used in spectral analysis, some of the bit errors in the output word of an ADC may not be captured in commonly used performance metrics such as SNR or ENOB. For such errors which occur over a large number of output samples, a means to continuously monitor the output of the ADC for errors is required. One such method, based on comparing output frames of the A/D converter was discussed and implemented in this application note. The results from such measurements can be used alongside FFT based metrics to properly quantify the performance of an ADC.

5 References

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