A Design Review of a Full-Featured 350-W Offline Power Converter

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ABSTRACT

Equipping devices with at least one microcontroller is becoming more popular. The flexibility of such devices is enormous and makes them unique. Switch-mode power supplies can be pure analog, pure digital or mixed designs. Mostly, the power is still controlled by an analog controller, but other tasks like monitoring, safety functions and interfacing are handled by microcontrollers. This paper will show a complete, state-of-the-art, high-performance and high-efficient analog power-supply system with full monitoring by a microcontroller.

I. INTRODUCTION

A. Specifications

Table 1 lists the system specifications. This kind of power supply is typically needed for RF transceivers.

For this design, the main challenges are:

- High bandwidth needed on the output to cover huge load steps caused by the transceiver's power demand (from standby to full power and vice versa).
- Low noise to avoid any disturbances in the receiver system (clean electric power, low audio noise).
- Monitoring and changing certain parameters on the fly.

To avoid any audible noise, a fan for active cooling is undesirable. Additionally, the housing and thermal interface were already defined, so the necessary overall efficiency could be as high as 90 percent.

When talking about noise and noise propagation in a system, there is one additional point worthy of discussion. If several converters are working at the same or similar switching frequencies and are not synchronized, subharmonic oscillations will occur.

Input	Universal AC input voltage range 85 to 265 VAC at 50 or 60 Hz
Output	12- to 14-VDC adjustable 25-A continuous, 30-A peak Voltage ripple < 12-mV peak to peak at 20-MHz bandwidth measured Load step 2% to 90% with a voltage deviation of < 1%
Mechanics	Silent power = no forced air → Overall efficiency has to be > 90% Slimline housing with a height of < 2 inches/50 mm
Extras	Hold-up time > 20 ms for harsh environments All converters synchronized to the same switching frequency Switching frequency-selectable (170 kHz ± 10%) Full monitoring with a microcontroller → Analog design with digital monitoring

Table 1 – System specifications.

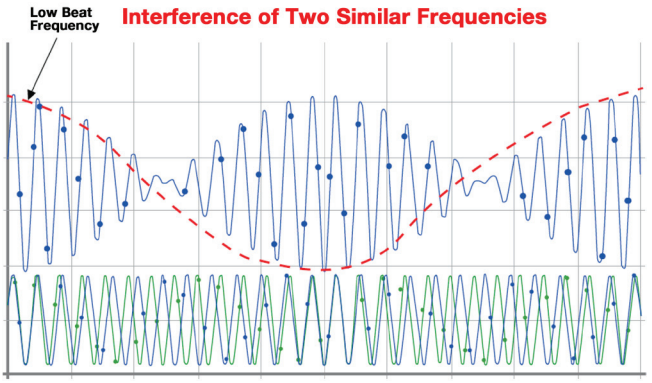


Figure 1 – Subharmonic oscillation.

In Figure 1, two converters are running at almost the same switching frequency but are not synchronized to each other. The two sinusoidal waveforms on the bottom are the input currents drawn by two converters in a power-supply system. This leads to subharmonic oscillation, shown in the waveform at the top. The envelope of that waveform is called "low beat frequency."

It is very difficult to filter such a low frequency and it causes trouble with sensitive circuits like phase-locked loops. The way to eliminate this interference is to synchronize all converters to the same switching frequency. Depending on the demands, the converters can work in phase or with a phase shift of 180°, which reduces the input current ripple.

However, on the frequency spectrum of that signal there is still a visible peak at the switching frequency. This can cause system performance degradation if the peak is at or near the receiver's frequency. Therefore, it is necessary to change the switching frequency slightly to shift the spectrum away from the sensitive frequency.

For monitoring purposes, various voltages, temperatures and other parameters have to be gathered and made visible, necessitating a microcontroller with a human-machine interface.

B. Overview

Figure 2 shows a simplified block diagram of the power-supply system.

The box at the top of Figure 2 represents the analog power path. An EMI filter is placed on the input, followed by an AC rectifier and a power-factor-correction (PFC) stage. An isolated downstream converter generates the output voltage, which is additionally filtered by an output EMI filter. The digital microcontroller circuit collects data like voltage, current and temperature. Furthermore, it generates a clock (CLK) signal for synchronization of all converters, a signal to set the output voltage, and provides a human-machine interface.

An auxiliary power supply supplies both the analog and digital parts of the system.

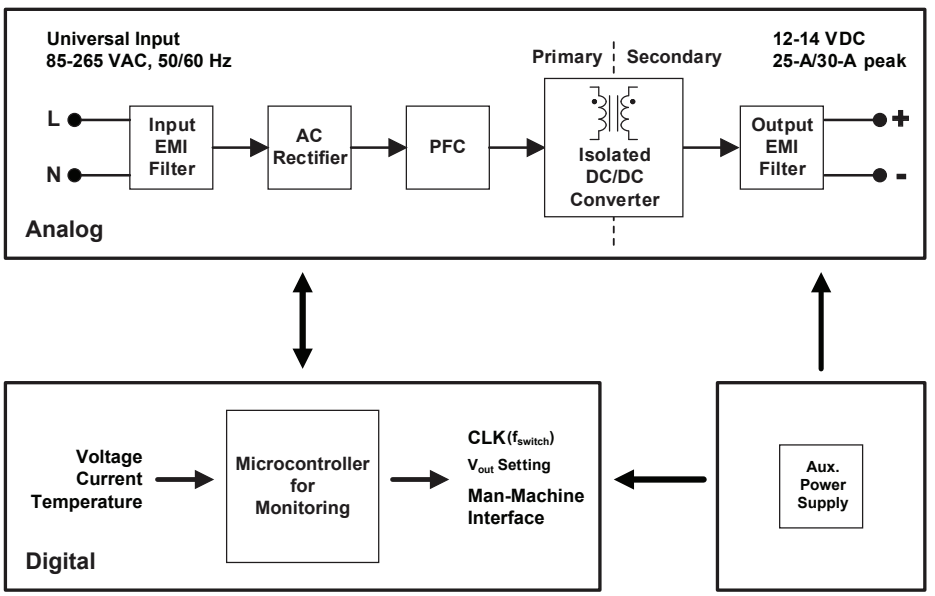


Figure 2 – Simplified system block diagram.

II. Power Board

A. EMI Input Filter

All switch-mode power supplies have one common issue: noise. Therefore, a very important block in the system is the input EMI filter. From a system-level point of view, you need a filter on each input and output of a device. The quality of these filters is well-defined in industry standards.

Apart from that, the process of designing filters is mostly an iterative process combined with a lot of tests and measurements.

For this system, we chose to install a two-stage differential and two-stage common-mode filter, shown in Figure 3.

The differential filter is made up of L1, L4, C3 and C4. Inductor L4 is placed in the return path to make it symmetrical for the common-mode filter.

Ferrite beads are placed directly on the input to the line and neutral. To reduce the DC resistance and optimize the footprint, three of the beads are in parallel.

The first part of the common-mode filter consists of L2, C1 and C5. It is dimensioned for a higher-frequency range (> 5 MHz). Inductor L2 needs to have a higher saturation current compared to standard ferrite cores, with approximately 20 mA.

The second part, made up of L3, C2 and C6, is for the lower-frequency range (< 5 MHz). All capacitors connected to ground (through the chassis, which has ground potential) have to be Y-types due to safety regulations.

If for any reason the system is not absolutely symmetrical, the common-mode chokes will go very easily into saturation and lose their filter functionality.

The same chokes – made with nanocrystalline materials instead of ferrite – have a higher saturation current in the range of 100 mA. This is very important when too much noise is coupled to the chassis or injected from outside (higher EMI/EMC requirements) and stresses the chokes. To suppress independent noise, L1 and L4 are placed in both lines.

While a single varistor is sufficient, two smaller varistors are placed in parallel to optimize the footprint and protect the converter.

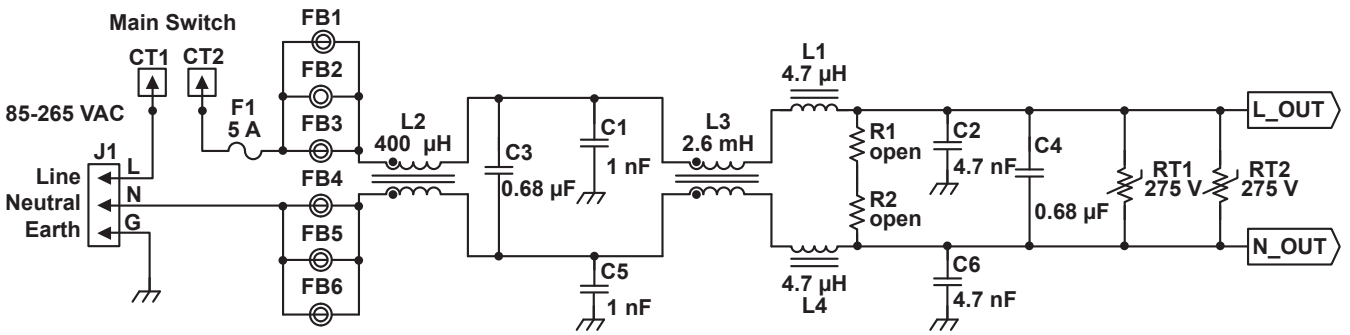


Figure 3 – Input EMI filter.

B. AC/DC Rectifier

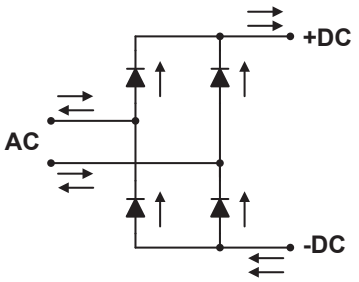
A bridge rectifier rectifies the AC input voltage and supplies the PFC stage with a positive voltage. Let's explore this implementation.

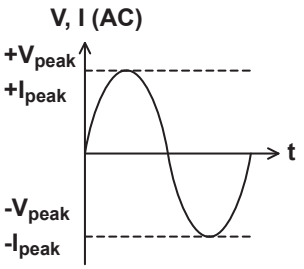
A standard bridge rectifier for single-phase systems consists of four diodes. The diodes are interconnected in such a way that the output current generated has a fixed direction of flow. In the majority of cases, the rectified AC voltage is smoothed out even further by capacitors so that the output voltage exhibits a low ripple.

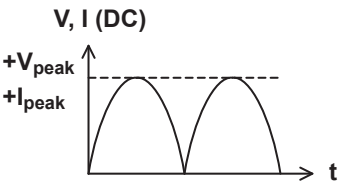
Figure 4 shows the path of current in the bridge rectifier; the form of the input voltage, output voltage and current; and the mathematical relationships for the effective and average values. As the current follows the path of the voltage in an ideal system, the specified formulas are also valid for currents.

A bridge rectifier is also called a "full-wave rectifier," as both the positive and negative half-waves of the AC voltage are rectified. A "half-wave" rectifier uses only one diode and only the positive half-wave. Therefore, the average voltage is only half of a full-wave rectifier.

Power losses are caused by non-ideal diode behavior ($V_{forward} \neq 0$ and $r_{diode} \neq 0$). Static losses are caused by forward-voltage and dynamic losses, which are in turn caused by the dynamic resistance of the diode. The dynamic resistance can be calculated using two points from the linear region of the diode characteristic shown in Figure 5. ΔV divided by ΔI results in the dynamic resistance.







Sinusoidal, without rectification:

$$V_{effective,\ AC} = +V_{peak} \times \frac{1}{\sqrt{2}}$$

$$V_{average,\ AC} = 0\ V$$

Sinusoidal, with full rectification:

$$V_{effective,\ DC} = +V_{peak} \times \frac{1}{\sqrt{2}}$$

$$V_{average,\ DC} = +V_{peak} \times \frac{1}{\pi}$$ **Half-Wave Rectifier**

$$V_{average,\ DC} = +V_{peak} \times \frac{2}{\pi}$$ **Full-Wave Rectifier**

Figure 4 – Four-diode bridge rectifier.

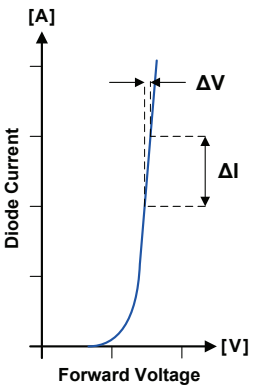


Figure 5 – Diode forward characteristic.

The total losses on a diode can be calculated with Equation 1:

$$P_{Diode} = V_{Forward} \times I_{Diode,\,avg} + R_{Diode} \times I^2_{Diode,\,rms} \quad (1)$$

The first summand represents the static losses; the second represents the dynamic losses. The calculation model for multiple diodes connected in parallel is shown in Equation 2.

$$P_{Diode,\,n} = n \times \left(V_{Forward} \times \frac{I_{Diode,\,avg}}{n} \right) + n \times \left(R_{Diode} \times \left(\frac{I_{Diode,rms}}{n} \right)^2 \right) \quad (2)$$

This equation can be simplified further:

$$P_{Diode,\,n} = V_{Forward} \times I_{Diode,\,avg} + R_{Diode} \times \frac{I^2_{Diode,\,rms}}{n} \quad (3)$$

The difference between Equation 1 and Equation 3 – shown in Equation 4 – illustrates the influence of the parallel connection on dynamic losses:

$$P_{Diode} - P_{Diode,\,n} = R_{Diode} \times I^2_{Diode,\,rms} \times \left(1 - \frac{1}{n} \right) \quad (4)$$

If, for example, 10 diodes were connected in parallel, the dynamic losses correspond to only 10 percent of the losses of an individual diode. The static losses, however, remain the same.

A good rectifier diode has the following characteristics:

- Component number: 1N5406.
- Reverse voltage: 600 V.
- Continuous current: 3.0 A.
- Threshold voltage: 0.6 V at 0.2 A.
- Dynamic resistance: 80 mΩ.

The forward voltage is the threshold voltage. It is almost constant and current-independent from approximately 0.2 A on for this diode. The only significant influence on the threshold is temperature.

A bridge rectifier with this diode on a 110-VAC input generates significant losses. Using Equations 1-4 shows this clearly.

- Input: 110 VAC at 60 Hz.
- Load: 13.8 V at 25-A load, 90 percent efficiency considered.
- Current per diode: 1.7-A RMS, 1.6-A average, 4.9-A peak.

$$P_{Diode} = 0.6\,V \times 1.6\,A + 80\,m\,\Omega \times (1.7\,A)^2 = 1.0\,W + 0.2\,W = 1.2\,W$$

$$P_{Bridge\ rectifier} = 4 \times P_{Diode} = 4 \times 1.2\,W = 4.8\,W$$

The conclusion is obvious:

- Diode losses only result from static losses.
- A parallel connection of several diodes does not generate any real improvement.
- The static losses of the diode can only be reduced by an element with a lower voltage drop or by eliminating the need for a diode.
- In general, paralleling of diodes is difficult, as the threshold voltage highly depends on the junction temperature with a negative temperature coefficient. Therefore, the diodes need very good thermal coupling to each other; otherwise the hottest diode takes the most current, gets hotter, takes more current, etc.

i. Diode vs. Synchronous Rectifiers

The solution to reduce losses is to put a metal-oxide semiconductor field-effect transistor (MOSFET) in parallel to each diode, like in Figure 6.

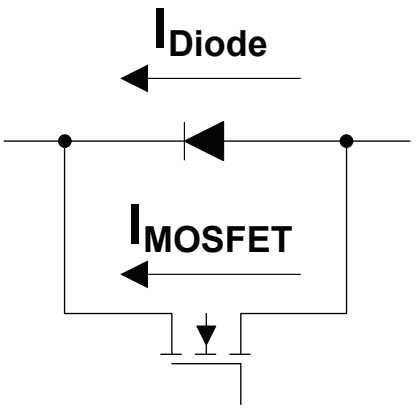


Figure 6 – MOSFET and diode in parallel.

Any modern MOSFET with low drain-source on-resistance would be suitable. Here's an example:

- Component number: IPW60R041C6.
- Drain-source voltage: 600 V.
- Drain current: 49 A.
- Drain-source on-resistance: 41 mΩ.
- Gate charge: 290 nC.

Static losses can be calculated with Equation 5:

$$P_{FET} = R_{DS} \times I^2_{FET,\,rms} \qquad (5)$$

As the static losses only occur in the MOSFET and not in the diode, we must assume that the diode does not conduct. And that is the situation here, as the maximum voltage drop on the MOSFET is 201 mV and the minimum switch-on threshold of the diode is 600 mV.

Power loss is recalculated with Equation 6:

$$P_{FET} = 41\ m\Omega \times (1.7\ A)^2 = 0.1\ W \qquad (6)$$

Equation 7 applies to the bridge rectifier:

$$P_{FET\ rectifier} = 4 \times P_{FET} = 4 \times 0.1\ W = 0.4\ W \qquad (7)$$

This is only 8 percent of the losses compared to a bridge rectifier with four diodes.

The switching and driver losses are negligible due to the low switching frequency of 50 or 60 Hz.

Even though the calculations in the example are for a 110-VAC input, the selected diode and MOSFET are optimized for a universal input (85 to 265 VAC).

For a bridge rectifier working at 110 VAC at the maximum possible power (15-A fused), the comparison is even more impressive, as shown in Table 2.

Diode Bridge Rectifier GSIB2040	**MOSFET Bridge Rectifier with IPP200N25N3G**
400 V, 20 A, 0.6-V threshold from 10-mA, 20-mΩ dynamic resistance	250 V, 64 A, 20-mΩ on-resistance
$P_{Bridge\ rectifier}$ = 4 x 5.2 W = 20.8 W	$P_{Bridge\ rectifier}$ = 4 x 1.1 W = 4.4 W
20.8 W = 1.3% of the total input power	4.4 W = 0.3% of the total input power

Table 2 – Comparison between diode and MOSFET bridge rectifiers.

The main benefit of a bridge rectifier with MOSFETs in parallel to each diode (a so-called "synchronous bridge rectifier") is not only the boost in efficiency, but the tremendous reduced losses. These losses have to be dissipated by a heat sink and well-designed thermal management. Eliminating 20-W losses requires a huge heat sink and a fan. The lower losses caused by the MOSFET solution makes even a surface-mounted device solution possible.

ii. Block Diagram

Implementing a synchronous bridge rectifier requires:

- Zero voltage detection at each of the two lines of the AC input.
- Load current measurement.
- MOSFET drivers (two on the high side, two on the low side).
- A control circuit.

The behavior of this circuit must mimic a diode bridge rectifier:

- The energy flows only in one direction, from the mains to the load.
- The MOSFET only conducts if the voltage and current are positive at the same time.
- The MOSFET must not switch under any other circumstances.

This functionality can be implemented with two different solutions. One solution is to use a bunch of logic gates, which you can find in some older designs. Another solution is to use a small low-cost MSP430F2012 microcontroller from Texas Instruments (TI) to control the whole circuit (see Figure 7). This microcontroller makes the circuitry simpler, is more flexible, and can perform additional tasks like monitoring the input voltage and load current.

For zero-voltage detection of the phase and neutral line, high-impedance voltage dividers (R1 + R2, R3 + R4) are connected directly to the logic inputs of the microcontroller. The integrated protection diodes of the microcontroller inputs clamp the voltage to the input voltage (+3.3 V), or rather to ground potential. This generates a logic rectangular signal with the same frequency as the mains frequency. Both signals have the same frequency, but a phase shift of 180°.

This is a very simple but effective method of retrieving logic signals with a higher voltage than the supply voltage of the microcontroller.

The load current is measured on a shunt resistor and amplified, filtered and read out by an analog input. This circuit is necessary to detect a current flow, as the MOSFETs are only active if a certain current is drawn.

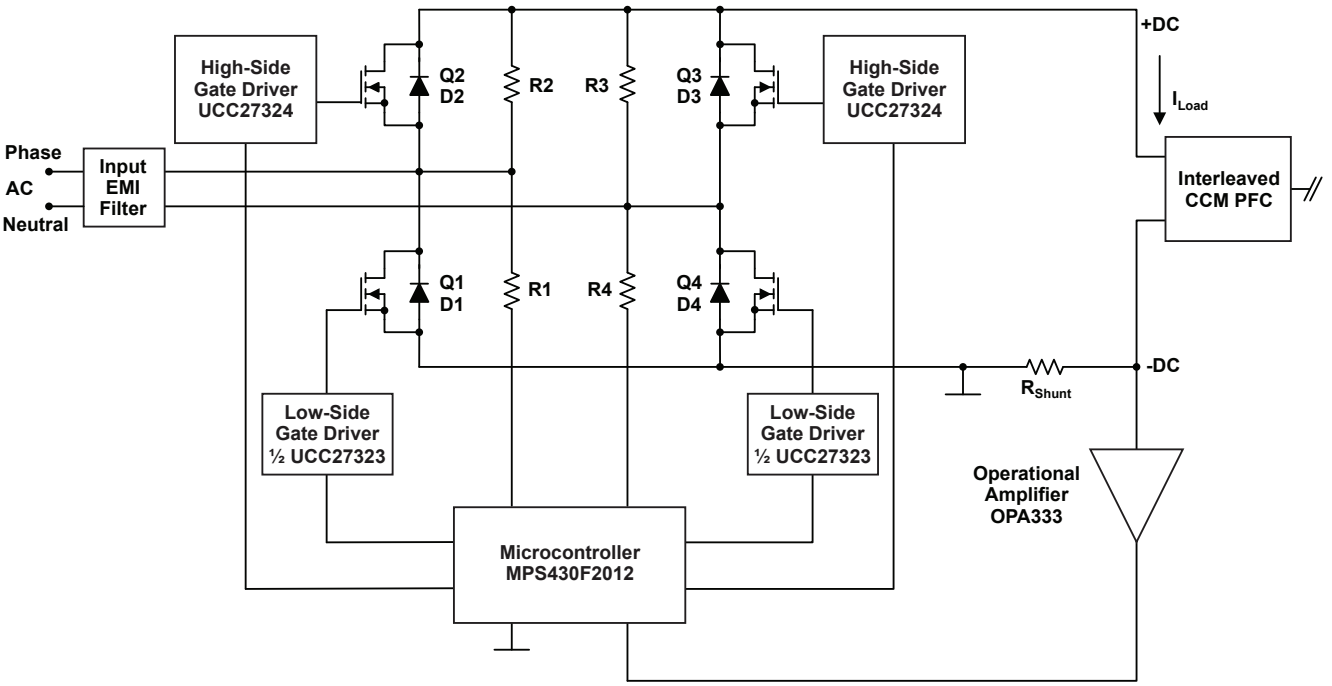


Figure 7 – Block diagram of a synchronous bridge rectifier.

iii. High-Side Gate Driver

MOSFETs Q1 and Q4 on the low side are referenced to the same potential as the microcontroller, so you can use a standard driver.

The high-side MOSFETs Q2 and Q3 are referenced to the input lines (phase, neutral) and need a special driver with galvanic isolation to the microcontroller.

For this purpose, we developed a dedicated "carrying gate driver." Figure 8 shows the schematic, where a high-frequency signal generates a static voltage to drive the MOSFETs.

A 200-kHz square wave signal generated by the TI MSP430™ microcontroller is applied to INA and INB. The two signals have a duty cycle of 50 percent and are 180° phase-shifted to each other. This is an additional benefit of using a microcontroller solution as opposed to logic gates, as the square wave signal is generated "for free."

C1 prevents saturation of the transformer if the driver output will eventually have a DC offset. Therefore, a pure AC voltage drives the transformer.

On the secondary side of the transformer, diodes D3 and D5 perform rectification and voltage clamping. As the input voltage is constant and the duty cycle is fixed, a constant voltage is applied to the MOSFET gate.

The MOSFET is switched off simply by switching off the two PWM signals. For a defined discharging of the gate, more effort is necessary.

Transistor Q2 and its circuitry are a current sink drawing a constant current of 10 mA. This current biases transistor Q1, which again discharges the gate with a constant current of approximately 300 mA. If you used only a base resistor instead of the current sink Q2, the discharge current would be dependent on the gate voltage. In this case, the discharge current is high at the beginning and is dropping lower, corresponding to the falling gate voltage. Overall, the time to discharge the gate will be much longer. The only drawback to using the constant current sink is that 10 mA are drawn continuously, even if the MOSFET is switched on.

A 10-kOhm resistor between gate and source discharges the gate further when the gate voltage has reached the threshold of about 1 V of the base-emitter voltages of Q1 and Q2 in series.

To protect the MOSFET against re-igniting caused by high Miller currents, we placed a 100-nF capacitor between gate and source. Re-ignition can occur if high dV/dt is applied on the drain, resulting in a very high capacitive current flowing into the gate and a voltage that could reach the threshold.

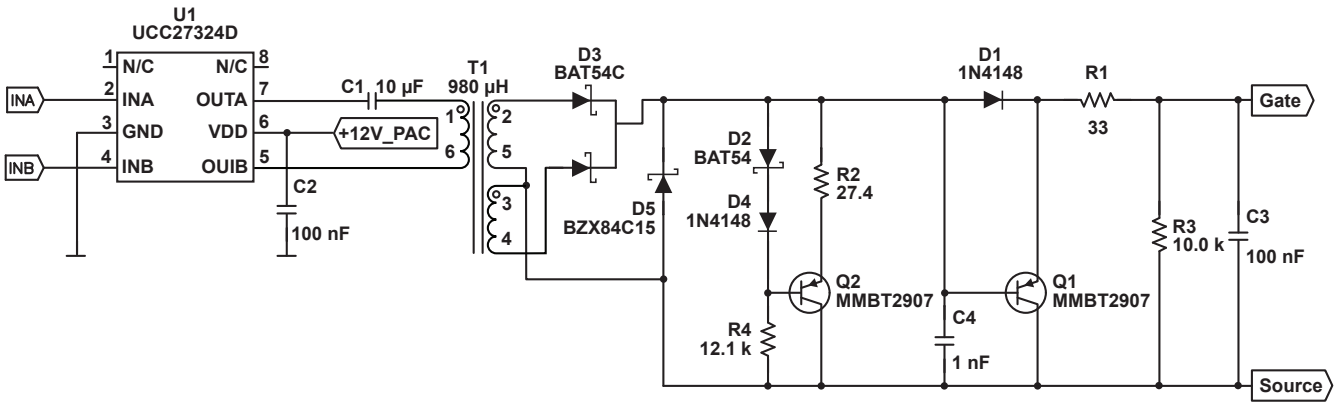


Figure 8 – Carrying gate driver.

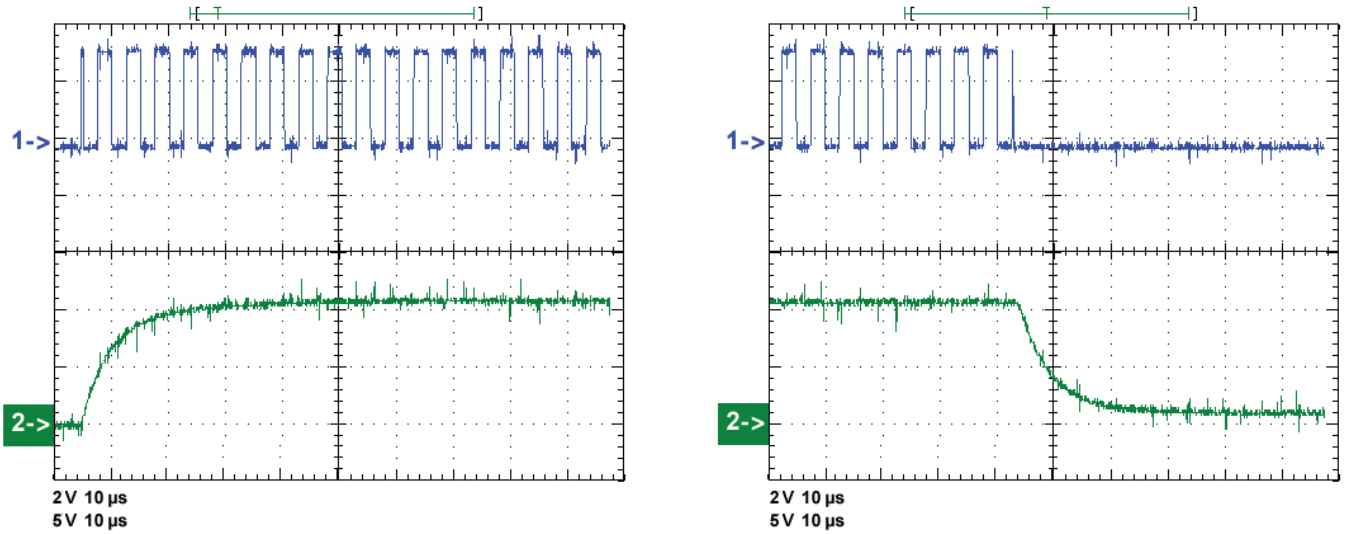


Figure 9 – Ramp-up and ramp-down of the gate-source voltage, 10 µs/div.

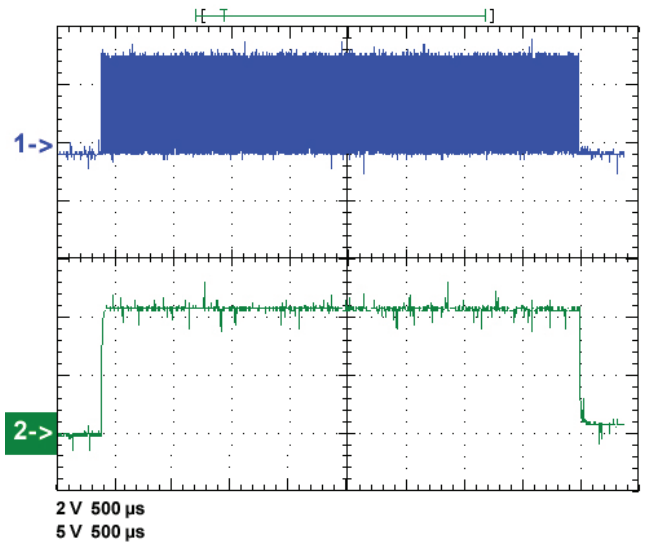


Figure 10 – Gate-source voltage, 500 µs/div.

The bottom plots of the measurements in Figure 9 show the ramp-up and ramp-down of the gate-source voltage. The rise and fall time are in the range of 10 µs. This is fast enough for the very low 50- to 60-Hz switching frequency for the MOSFETs. The curve on the top shows one square wave signal from the MSP430 microcontroller with a frequency of 200 kHz. Figure 10 shows a complete switching cycle of a MOSFET.

iv. Software

The load current and the mains voltage are sampled every 25 µs. A digital filter and a plausibility check are helpful to avoid malfunctions.

The voltage, which represents the load current, is compared to a fixed threshold value. The threshold value is selected so that a certain load current flows through the diodes. If the MOSFETs are not switched on, a higher threshold is set than when the MOSFETs are active. By having different thresholds for switching on and off, hysteresis is achieved and the system becomes more immune to noise and malfunctions.

The status of the three elements is stored in one variable each of the microcontroller's memory. If the digital input is a logic one (phase, neutral), the variable is incremented by one; if it is a logic zero, it is decremented by one.

This functionality is implemented for the load current analogous to the voltage measurement. If the converted value is higher than the threshold value, the variable is incremented by 1; otherwise it is decremented by 1. The software limits the variables to a minimum of 0 and a maximum of 3.

If a variable reaches 3, that means that a logic one state has been ascertained three times in a row. A variable value of 0 corresponds to a logic zero state on three consecutive occasions.

Only if these three variables are 0 or 3 are they are checked for plausibility; where appropriate, the MOSFETs are activated. This method, described and shown in Figure 11, ensures the establishment of a stable state, while also minimizing malfunctions.

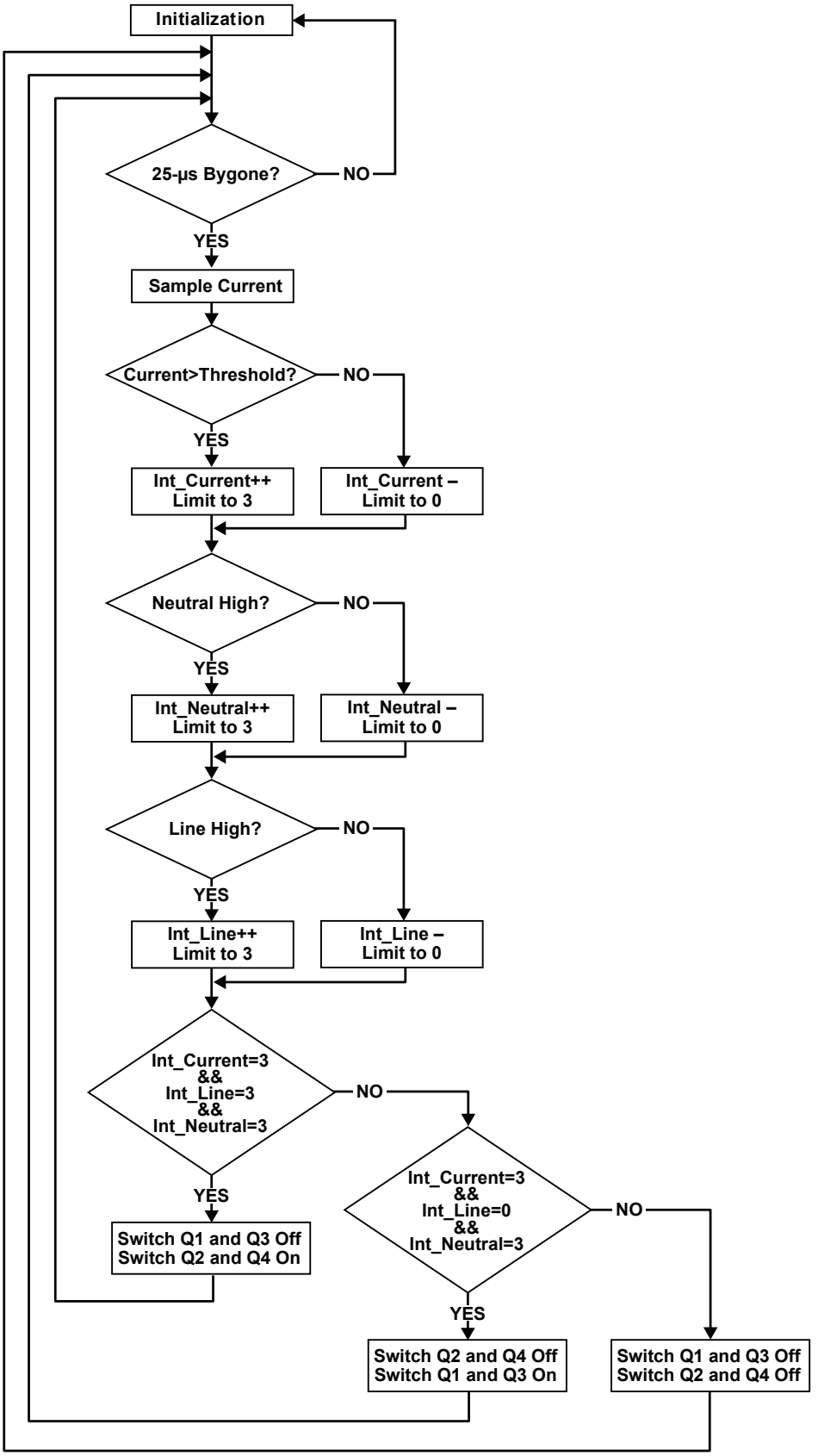


Figure 11 – Software flow chart.

There are only two status combinations allowed in which two MOSFETs may be switched on. The program ensures that the current flows from the mains to the load and that the voltage between the phase and neutral is applied correctly. The four MOSFETs must be switched off for all other combinations; Table 3 shows the various possibilities.

Implementing additional functionality, like monitoring the load current, should be a simple task.

C. PFC

After the rectifier, a PFC circuit is necessary to fulfill the norms and regulations. It has two main functionalities:

- Tracking the input current to be in the phase with the AC input voltage, thus reducing the harmonics injected to the mains and improving the power factor.
- Generating a stabilized output voltage to supply the downstream converter.

To achieve an efficiency as high as possible, we chose to use a continuous conduction mode (CCM)-interleaved PFC. In theory, a single-stage PFC can also be used for this power range. But the high current ripple on a single-stage PFC needs bulky parts like an inductor, MOSFET and diode. You would also need huge, high-ripple-rated capacitors on the input as well as the output, and a large EMI filter on the input to reject the noise caused by high peak currents.

These problems can be avoided or at least minimized by using an interleaved PFC topology.

Two power stages switching with a phase shift of 180° cause a reduction in the current ripple on the AC input. This makes EMI filtering easier and works with smaller components. Current ripple decoupling on the output is also much easier.

CCM also reduces the current stress and filtering efforts compared to a transition-mode or discontinuous-conduction-mode PFC.

You can easily scale this topology to higher power levels by using parts with a higher power range or by putting several power stages in parallel.

You need the same amount of silicon and copper to achieve the same efficiency as a single-stage PFC. But as the silicon and copper are distributed into two stages, you can use smaller parts with a low profile.

There are also two drawbacks, however. As this is a hard switching topology, you will need a fast reverse recovery diode like a silicon carbide. Unfortunately, the fast switching speed of this diode type shifts the EMI issues to much higher frequencies – in the range of 50 to 200 MHz. See the references for further descriptions and explanations of this issue.

Load Current	Line Voltage	Neutral Voltage	Conducting MOSFETs
Variable current = 3	Variable phase = 3	Variable neutral = 0	Q2, Q4
Variable current = 3	Variable phase = 0	Variable neutral = 3	Q1, Q3

Table 3 – Allowed status combinations for switching on the MOSFETs.

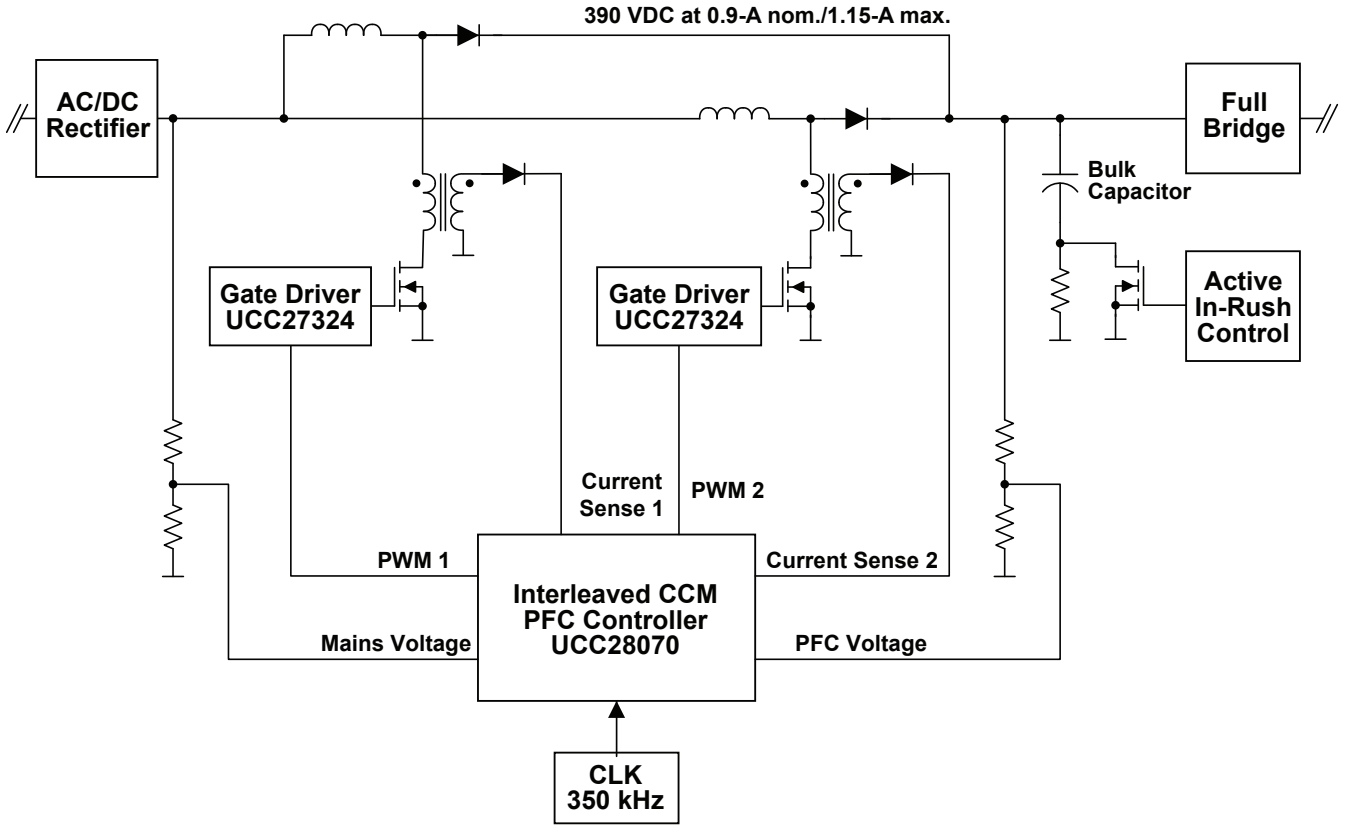


Figure 12 – Block diagram of the interleaved PFC.

i. Block Diagram

Figure 12 shows the PFC stage after the AC/DC rectifier and before the full bridge. At the top, note that the two boost power stages work with a phase shift of 180° to each other.

The controller is a TI UCC28070 synchronized to a clock frequency of 350 kHz by a microcontroller. A relatively high switching frequency for the PFC allows us to achieve the strict height restriction of < 2 inches/50 mm from the specification, as a higher switching frequency enables the use of smaller components. The two MOSFETs of the boost power stages are driven by low-side gate drivers to achieve fast switching. Both outputs are paralleled and generate a DC voltage of 390 V at 0.9-A nominal.

The bulk capacitor on the output is extended with an active in-rush current control. At the moment the power supply is switched on, the bulk capacitor is not charged. As the mains have a galvanic connection with the bulk capacitor even when the PFC is not working, a high pulse current would flow during the very first moment, charging the bulk capacitor. This means not only high stress for this capacitor and all parts inline, but it can also blow the fuse of the wall socket.

To prevent any damage, we put a resistor in series with the bulk capacitor, thus reducing the initial charge current. Before the PFC starts working, this resistor is shorted automatically by a MOSFET due to the rising voltage of the auxiliary power supply.

Adding a resistor is a very reliable and simple solution compared to other in-rush current-limiting solutions.

ii. Component Selection

The efficiency of the PFC power stage is limited by its conduction and switching losses. Conduction losses are caused by copper losses, the on-resistance of MOSFETs and the voltage drop on diodes. Switching a MOSFET on and off produces losses, as do the capacitance and reverse recovery charge of a diode. Further losses are caused by the hysteretic losses of magnetic materials.

To achieve a maximum efficiency, the parts of the power stage have to be selected carefully.

The electric lines on the PCB have to be as short as possible with a sufficient copper cross-section. A rule of thumb is to stress a line with maximum 4 A/mm^2. If the cross-section of the PCB is not enough, use additional bus bars like those seen on the phase-shifted full bridge shown in Figure 37.

The second part of the power stage is the inductor. Its RMS current is half of the AC input current because of the two interleaved power stages. The high-frequency current ripple is only ~20 percent of the maximum peak current. Basically, this value is a trade-off between the size and the price of the inductor and its losses.

These inductors also need very low distributed capacitance to lower EMI issues. The lowest capacitance is a single layer, and a single-layer inductor is best with as few windings as possible. Sometimes it is useful to stack cores to increase the effective magnetic cross-section and reduce the number of turns at the same time. For this approach, ring cores are a good choice, especially moly-permalloy powder (MPP) and high flux cores.

The third part is the MOSFET and the diode. As the CCM PFC is a hard switching topology, a fast-switching MOSFET and fast recovery diode are needed.

While the MOSFET is switched off, the diode is conducting. At the next commutation period (when the MOSFET is switched on and takes over the inductor current), the diode is reverse-biased and conducts negative current from the output through the MOSFET to ground. This occurs during "reverse recovery time," producing a lot of noise and additional losses.

To minimize these, we used a fast recovery diode like a silicon carbide. This type of diode boosts the efficiency of this kind of PFC by more than 2 percent.

For each switching cycle (switching on or off), the inductor current commutates between the MOSFET and the diode, generating reverse recovery losses. These losses depend on the current level as the input current follows the input voltage, which is a rectified 110-VAC/230-VAC sinusoidal voltage. Therefore, the losses are a function of the rectified input voltage. Charging and discharging all parasitic capacitors (C_{OSS} of the MOSFET, layout, etc.) generate additional losses.

To minimize these losses, choose transistors with low C_{OSS} and a PFC inductor with low parasitic capacitance. With a well-selected MOSFET, 50 percent of the losses should be conduction losses and 50 percent should be switching losses.

iii. Measurements

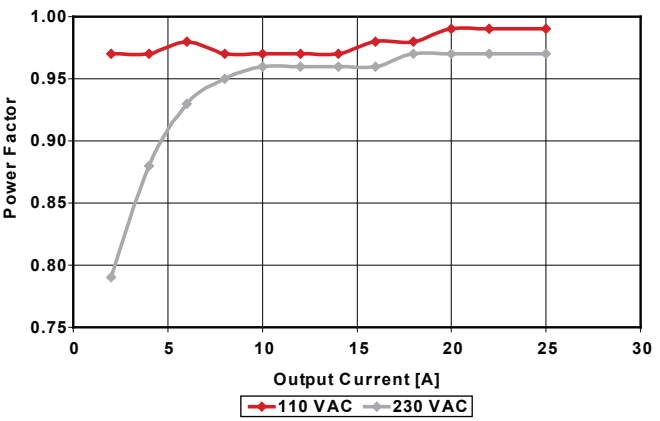


Figure 13 – Power factor of the interleaved PFC at 13.8-V output voltage.

The most desirable qualities of a PFC besides efficiency are the power factor achieved and harmonic content. Figure 13 shows the power factor at a 13.8-V output voltage and 110 VAC, as well as a 230-VAC input at different loads.

Figure 14 shows the measured harmonic content according to EN61000-3-2 Class D at a 230-V input voltage and full load.

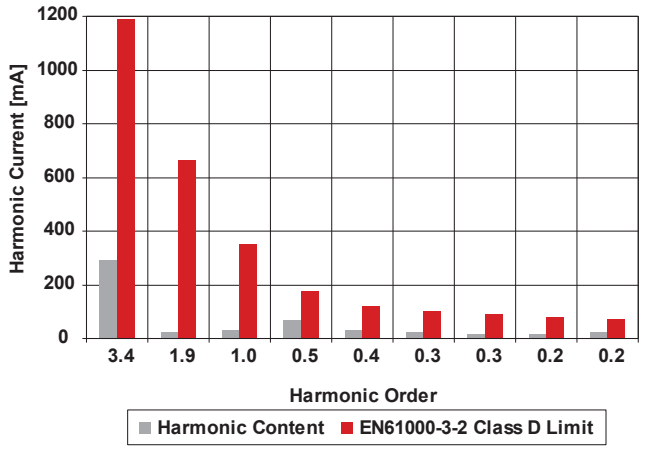


Figure 14 – Harmonic content according to EN61000-3-2.

The performance is outstanding with a power factor higher than 0.95 from 30 percent load on at 230 VAC. At 110-VAC operation, the power factor is 0.97 from 10 percent load up to maximum load.

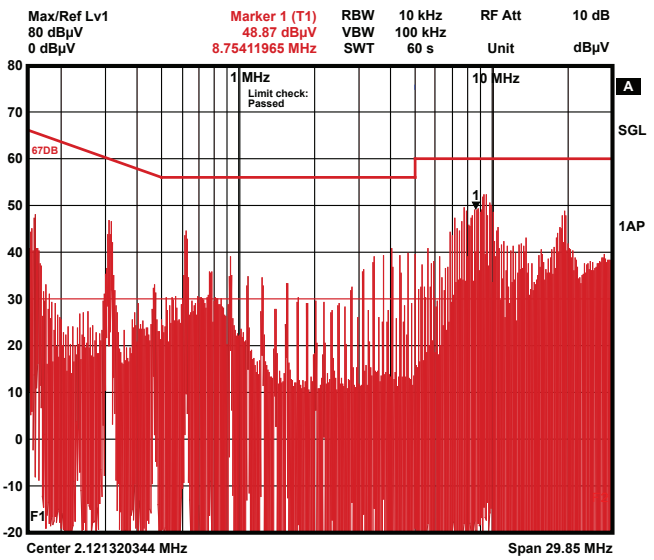


Figure 15 – Conducted emissions at 230-VAC input and 0.9-A load at 390 V.

The measurement of the conducted emission of the PFC stage at 230-VAC input and full load on the PFC output (0.9 A at 390 V) shows a result well below the limits (Figure 15).

A CCM-interleaved PFC has lower conducted emissions compared to a discontinuous- or transition-mode PFC.

The maximum efficiency of the PFC is 97.0 percent. We will discuss efficiency measurements of the complete power supply in Section V.

A bridgeless PFC will show a similar efficiency, but with much worse EMI behavior. In this case any advantages of this topology (such as higher efficiency) are eaten up by the disadvantages (higher EMI requiring a larger filter).

D. Phase-Shifted Full Bridge

The phase-shifted full-bridge topology, which is already described in various application notes (see the references), is used as downstream converter in this power supply. A synchronous rectification on the output enables fast transient response and a high loop bandwidth, which is needed to fulfill the specifications. Keeping the full bridge in CCM (with the synchronous rectifier working permanently as burst mode is disabled) allows the converter to work in two quadrants (first and second). This means that the current can flow from the primary to the secondary side, as well as from the secondary side to the primary side. This behavior is not possible with a diode rectifier and reduces voltage overshoots and undershoots caused by load steps. This is the only way to achieve fast transient response without a huge output capacitance.

Another benefit of synchronous rectification on the output is a boost in efficiency. With modern MOSFETs, the voltage drop – and therefore the losses on them – are much lower. Switching the MOSFETs off is done hard, meaning that neither current nor voltage are zero. This introduces additional switching losses and commutation noise. Therefore, you need fast-switching MOSFETs and good dead-time matching to avoid cross-conduction.

To push the loop response to the limit, the PWM controller has to be placed on the secondary side. In this case, the voltage feedback loop is closed directly on the converter's output without an optocoupler in-between.

On a normal converter, the PWM controller is placed on the primary side, so the voltage feedback loop has to cross the isolation barrier by an optocoupler or similar device. The optocoupler's low-pass behavior limits the bandwidth to about 5-kHz maximum. This is the main limitation of the bandwidth, which can only be eliminated by placing the controller on the secondary side. Only then is the maximum practical bandwidth – approximately one-fifth the switching frequency – achievable. The integrated error amplifier's bandwidth can also limit the loop response.

A PWM controller on the secondary side does have two drawbacks:

- You will need an auxiliary power supply for the controller on the secondary side or the converter cannot start up.
- More signals now have to cross the isolation barrier: four gate signals to drive the primary MOSFETs and one current-sense signal. Additionally, these circuits must be designed for high-voltage isolation.

The block diagram shown in Figure 16 shows the phase-shifted full bridge.

i. Gate Driver

The phase-shifted full-bridge topology has one big benefit compared to a standard hard-switching full-bridge topology: the duty cycle of the gate signals remains fixed at close to 50 percent all the time. Therefore, the gate-drive circuit can be optimized quite well. Either a single- or double-side-ended circuit for bipolar driving (shown in Figure 17) will work.

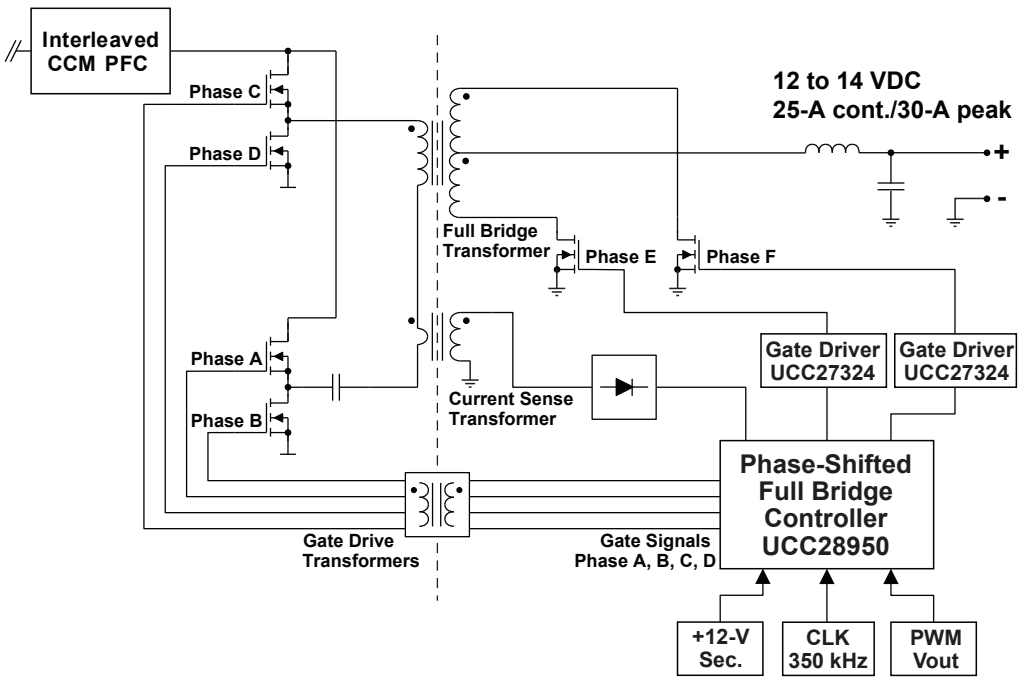


Figure 16 – Block diagram of the phase-shifted full bridge.

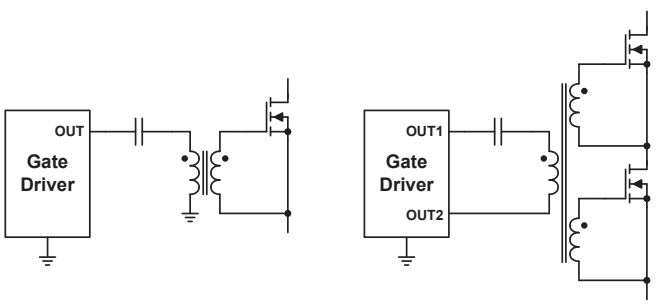


Figure 17 – Single- and double-side-ended gate-drive transformer.

Table 4 shows the advantages and disadvantages of both circuits.

	Advantages	Disadvantages
Single side-ended	Duty cycle > 50% of gate driver possible	Transformer saturation issues
Double side-ended	Low component count No transformer saturation issues High- and low-side control with one transformer possible if driver provides dead time (duty cycle < 50%)	Must be placed close to MOSFET

Table 4 – Single side-ended vs. double side-ended.

Both circuits generate a bipolar output voltage to drive the MOSFETs. The negative voltage brings faster switch-off behavior and higher noise immunity than only pulling the gate voltage down to zero during switching off. A drawback is the double power consumption of the driver circuit.

Figure 18 shows the implemented single-side-ended gate driver. It shows only one half of the driver's output, but the same circuitry around transformer T1 is connected to the output "low-drive" for a second MOSFET.

A small NPN-PNP transistor pair placed directly at the gate of the driven MOSFET minimizes leakage inductance caused by the transformer and the copper traces, and thus improves the switching behavior. Thus, the distance between the driver on the primary side and the MOSFET does not have to be as small as usual. In this application, it is important to use fast-switching bipolar transistors with very low turn-on and turn-off delay times.

Capacitor C2 in series with the primary winding of the gate-drive transformer performs DC decoupling. Its maximum capacitance is limited by the saturation current of the transformer. On the other hand, the minimum capacitance is limited by the maximum ripple voltage caused by the magnetizing current. During startup, it takes some time until C2 is charged to half the supply voltage of the primary side (duty cycle on OUTA is fixed to 50 percent). A practical value for this capacitor can be calculated using Equation 8.

$$C_{DC} = \frac{1}{R_{total} \times 5 \times f_{switch}} \tag{8}$$

R_{total} is the total DC resistance in the driver circuit; specifically, it is the output resistance of the driver, U1, and the DC resistance of the transformer's primary side. A factor of five will achieve a time constant well below the switching frequency. A value that is too low would introduce a high ripple voltage across the capacitor and decrease circuit performance.

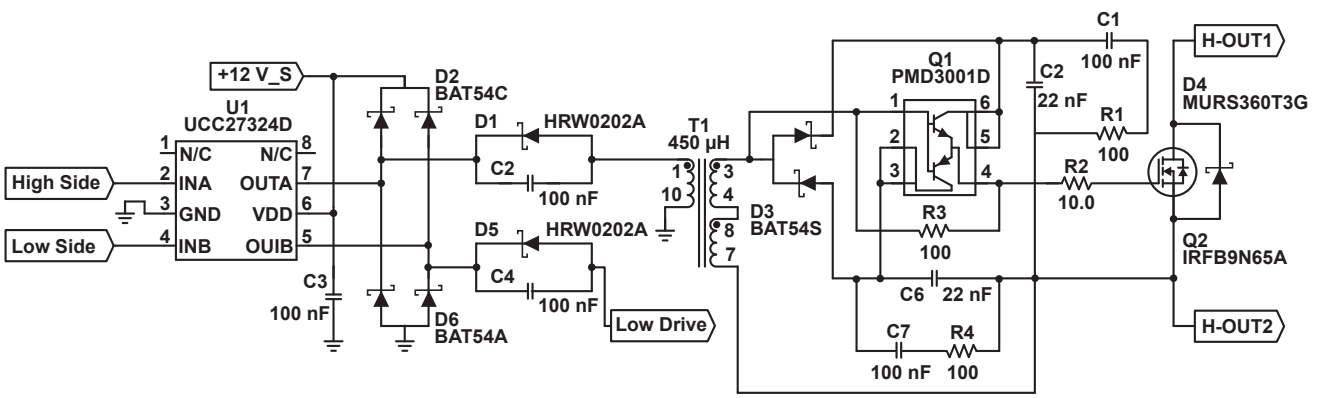


Figure 18 – Gate driver for phase-shifted full bridge.

Diode D1 in parallel discharges the capacitor during switch-off or in hiccup mode to prevent a too-high, negative DC voltage across the transformer, which leads to saturation. Discharging the capacitor also prevents oscillation in the resonant circuit formed by C2 and the transformer's inductance, which can switch on the MOSFET by accident. Therefore it is very important to use a diode with a low forward-voltage drop.

Still another resonant circuit – formed by C2 and the reflected capacitance from the secondary side and magnetizing inductance of the transformer – generates a low-frequency voltage (approximately 4 kHz) bouncing on the gate, as shown in Figure 19.

A snubber circuit (100 Ω + 100 nF) in parallel to C2 and C6 stabilizes bouncing on the gate.

$$C_{Snubber} = 4 \times C_{Bias}$$
$$R_{Snubber} \geq \sqrt{\frac{L_{Mag}}{C_{Bias}}} \qquad (9)$$

C_{Bias} in Equation 9 is the bias capacitor (22 nF) in this circuit. The resistor of the snubber is dependent on the primary magnetizing inductance, L_{Mag}, and the bias capacitor, C_{Bias}.

ii. Voltage Mode vs. Current Mode

Like many modern PWM controllers, the IC has a burst mode implemented to keep the efficiency high at light load.

Activating burst mode leads to a very low primary current and narrow duty-cycle operation on the output at light or no load. This also means that the signal on the current-sense pin is very small. High noise in the hundred-millivolt range is superimposed on top of this current signal in the millivolt range; it is coming from the switching noise. This can cause instability, because the controller tries to regulate a peak current signal that is not clean enough.

As the peak-current mode needs voltage slope compensation anyway, the only solution is to add even more slope compensation to keep the controller stable in this low load condition. But then it is moving away from a real peak-current mode to a voltage-mode regulation.

Disabling the burst mode is the right approach for this application. In this case, the synchronous rectification is working continuously and the duty cycle remains almost constant over the entire load range. But again, at light or no load conditions, the current-sense signal is still very small and also has a negative part.

The explanation is easy: The current in the output inductor has two components, an average (DC current) and an alternating (ripple current). At no load, the average current is zero. But due to synchronous rectification, the current in the inductor remains continuous and the alternating component remains present. This behavior forces the current-sense signal on the primary side to zero for each period of cycle when the current is negative (flowing back from the secondary side to the primary side). The higher the current ripple, the more negative this voltage.

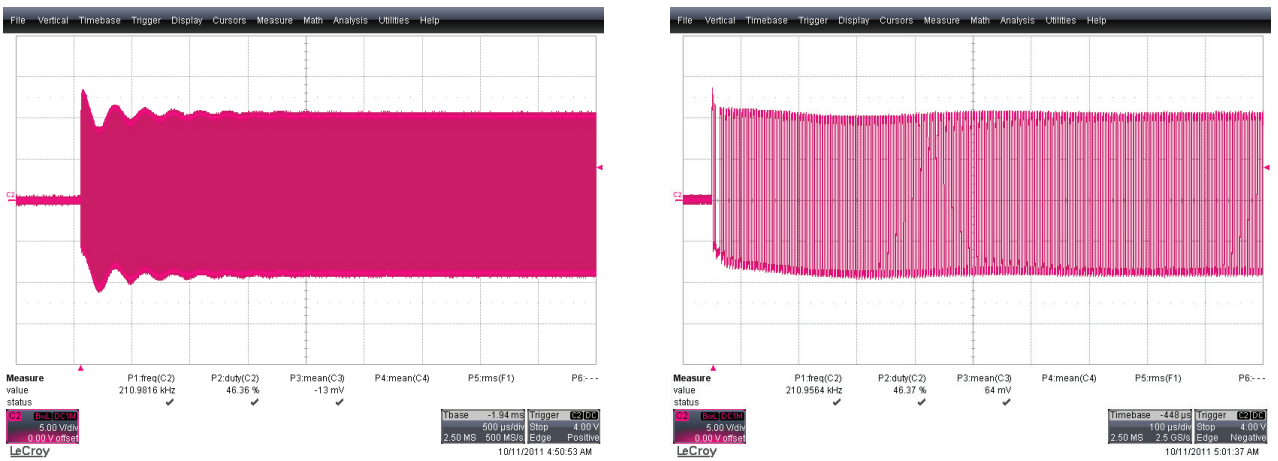


Figure 19 – Gate-source voltage with and without a snubber circuit.

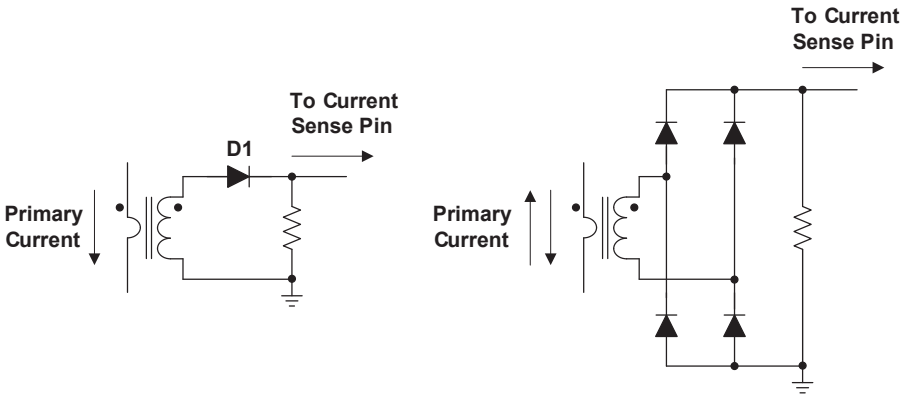


Figure 20 – Unipolar and bipolar current sense.

As the negative voltage is blocked by D1, as shown in Figure 20 (unipolar current sense), the voltage on the current-sense pin of the controller is zero. Now, if the dead time between each switching cycle is not high enough for demagnetization of the transformer, it will go into saturation.

These factors create a lot of problems and can confuse the controller, especially during huge load steps. Even high slope compensation doesn't help keep the converter stable.

Having said all this, the conclusion is that unipolar current sense with a current-sense transformer is only suitable for converters where the current flows in one direction – not bidirectionally. Using a unipolar current sense requires a high-voltage diode with very low parasitic capacitance and leakage current, as well as a clamping circuit against the energy overshoot coming from the leakage inductance caused by the current-sense transformer.

To achieve a very good transient response at huge load steps and rejections (from almost 0 to 90 percent and vice versa), not only are two-quadrant operations essential (current flowing from the primary side to the secondary side and vice versa), but two requirements also have to be fulfilled:

- The PWM controller has to work in voltage mode.
- There has to be some kind of cycle-by-cycle overcurrent protection.

The current-sense transformer has to be placed in series with the full-bridge transformer's primary winding. This ensures demagnetization even when a negative current is measured (current flowing from the secondary side to the primary side).

The easiest way to prevent saturation in voltage mode for the full-bridge transformer is to put a capacitor in series with the transformer. It blocks any DC component caused by asymmetry.

The type and value of this capacitor is defined by the accepted ripple voltage and primary peak current. Usually, 1 percent of the input voltage is allowed for the ripple voltage. A metalized polyester film capacitor is well-suited for this task.

At the lowest switching frequency of 157 kHz and an input voltage of 390 V, the capacitor needs to be 390-nF minimum, as shown in Equation 10. The next-higher standard value for MKT capacitors is 470 nF.

As explained previously, unidirectional current sensing works properly only if the current keeps the same flow direction. Bidirectional current sensing works only with alternating current.

As the current-sense transformer is placed in series with the primary winding of the full-bridge transformer and the system working in voltage mode, the demand for measuring an alternating current is fulfilled. Furthermore, the transformer is demagnetized inherently, as only AC current flows because the capacitor is in series with the full-bridge transformer. Because rectification of the current signal is not an issue anymore, you can use low-voltage Schottky diodes.

In voltage mode with bipolar current sensing, the current-sense signal is used only for protection. If it hits the threshold, the controller is going into cycle-by-cycle current limit. Slope compensation is necessary, but much less (10 to 20 percent), since a high-level voltage signal is already applied.

In summary:

- Use a topology with synchronous rectification for a high-performance and high-speed power supply. Only then is it possible to work in two quadrants and thus achieve good transient behavior.
- Disable any burst or power-safe mode and enable CCM all the time. This reduces efficiency at low or no load conditions, but it is the only way to react fast to load changes.
- Avoid any components with low-pass behavior like an optocoupler in the voltage-feedback loop. You will achieve the highest bandwidth by placing the PWM controller on the secondary side.
- Use voltage-mode control and bidirectional current sensing to avoid instabilities when current flows backwards (from the secondary side to the primary side).

$$C = \frac{I}{2 \times \pi \times f_{Switch} \times U} = \frac{1.5\ A}{2 \times \pi \times 157\ kHz \times \frac{390\ V}{100}} = 390\ nF \quad (10)$$

iii. Component Selection

Like the PFC stage, efficiency is defined by the performance of the power stage. For maximum efficiency, you will need a zero-voltage or zero current-switching topology – or a combination of both.

The phase-shifted full-bridge topology has zero-voltage switching-on. This means that switching-on is done at a low voltage across the MOSFET. According to the system parameters and load conditions, this voltage can even be close to zero. Unfortunately, the switching-off is done hard. This means that neither the voltage nor the current is low or close to zero. Let's discuss the problems this can cause.

The transformer's leakage inductance, along with the stray inductance, is forcing zero-voltage switching during switching-on. But it is also causing high-voltage overshoot on the secondary side during switching-off. The voltage across the MOSFETs on the primary side is always clamped well to the bus voltage, so the induced voltage across the leakage inductance is reflected to the secondary side as a negative voltage and multiplied by the transformer's turns ratio.

This voltage overshoot introduces additional voltage stress to the rectification MOSFETs and produces noise. To keep the overshoot within a reasonable range, you would have to use clamping and snubber networks, which unfortunately cause additional power losses.

The compromise between the threshold of zero-voltage switching and peak efficiency is finally defined by the leakage inductance of the transformer. In this design, the transformer's leakage inductance was specified in such a way that zero-voltage switching was achieved at approximately 50 percent load [6] [7].

The transformer is a critical part of this design. The most important points are:

- The transformer cross-section must be as high as possible with the lowest possible core volume. RM and P pot cores are well-suited for this and guarantee low EMI.
- Litz-wire and single-layer windings minimize skin and proximity effect tremendously compared to standard copper wire.
- On a well-designed transformer, 50 percent of the total losses are caused by the copper losses and 50 percent by the core losses.

In this topology, all connections of the transformer are hot. In other words, no one connection is connected to a fixed potential like input voltage or ground; all are switched between different potentials. As with all forward topologies like this one, it needs a well-coupled transformer, which typically introduces high interwinding capacitance. Thus the noise coupling from the primary side to the secondary side is much higher than with other comparable topologies.

The only way to effectively attenuate this noise is to use a static screen inside the transformer (Figure 21). It is a copper foil placed in-between the primary- and the secondary-side winding and connected to ground on the primary side.

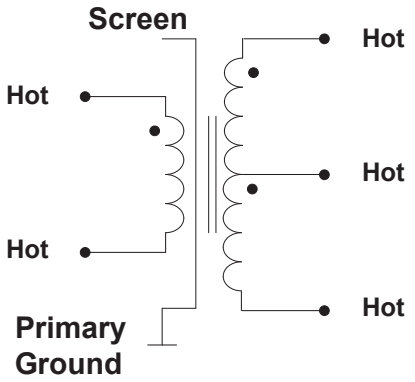


Figure 21 – Transformer with integrated screen.

This kind of shielding between the two windings adds an additional noise attenuation of about 20 dB.

A further improvement would be a second screen, well-isolated from the first one and connected to ground on the secondary side.

On the primary side, you must use MOSFETs with a moderate switching speed. If the switching speed is too high, they can destruct themselves due to the high dV/dt. Another problem with very fast MOSFETs on the primary side (in combination with the high input voltage) is the generated EMI level.

At the same time, for the synchronous rectification on the secondary side, you need fast MOSFETs to keep the transition time between the MOSFETs and the losses as small as possible.

The output inductor needs to have a low equivalent series resistance (ESR) for best efficiency. Flat-wire inductors with ferrite core are the best choice.

The main reason to increase the loop bandwidth is to get a better response to a load step and to decrease the required output capacitance. The output capacitance not only codetermines the transient response but also the output ripple voltage and thus necessitates a combination of different capacitor types. Usually electrolytic and ceramic capacitors are put in parallel. This leads to a complex output impedance, which is a function of parameters like switching frequency, temperature, DC bias voltage, tolerances, aging and so on, and makes any precise calculations almost impossible. Therefore, let's show how to define the output capacitance and still get a good output filter.

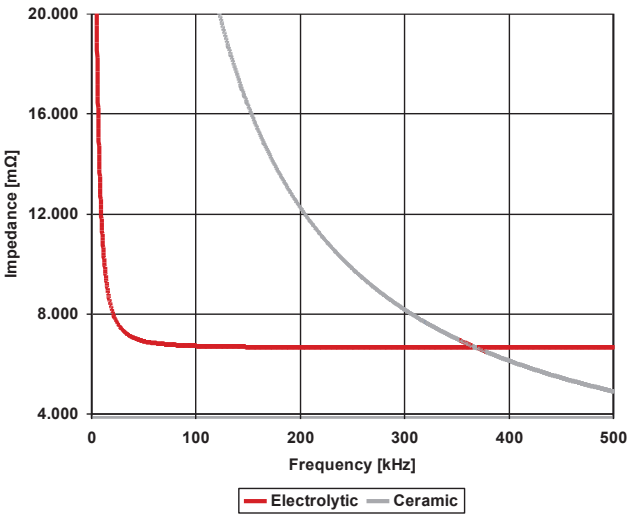


Figure 22 – Impedance vs. switching frequency.

Figure 22 plots the impedance curve of two different types of capacitors:

- Electrolytic: Three 680-µF capacitors in parallel, ESR = 17 mΩ per capacitor.
- Ceramic: Ten 10-µF X7R capacitors in parallel, ESR = 2 mΩ per capacitor.

The impedance of the electrolytic capacitor drops at approximately 50 kHz down to the value of its ESR. For higher-switching frequencies, the ESR dominates massively over the reactance and the impedance equals the ESR of the capacitor.

The crossing point where the impedance of the ceramic capacitor hits the impedance of the electrolytic capacitor is at about 370 kHz and is called the "critical frequency." At this frequency, the current load in the electrolytic capacitor is equal to the current load in the ceramic capacitor. Moving to higher frequencies, the ceramic capacitor is taking over the bigger part of the current.

Because the impedance of the electrolytic capacitor is going down very fast, the critical frequency is obviously pretty high. If intense harmonic current components at higher frequencies are present, a lot of ceramic output capacitance is

needed to bypass these current parts with its low impedance. This is seen in flyback converters, for example.

As the ESR of electrolytic capacitors changes a lot with temperature (the higher the temperature, the lower the ESR), this also influences the critical frequency. That can cause problems as the ripple current switches from the ceramic capacitors to the electrolytic capacitor. Basically, the output impedance is defined by the load step and ripple voltage requirements. For CCM, the calculation of the ripple voltage is shown in Equation 11.

$$V_{Ripple,\,peak\text{-}peak} = I_{Ripple,\,peak\text{-}peak} \times Z_{Cout}(f_{Ripple}) \tag{11}$$

$$Z_{Cout}(f) = \sqrt{R_{ESR}{}^2 + X_{Cout}{}^2} \tag{12}$$

$$X_{Cout}(f) = \frac{1}{2 \times \pi \times f \times C_{out}} \tag{13}$$

$I_{Ripple,peak\text{-}peak}$ is the peak-to-peak value of the current ripple. f_{Ripple} is the frequency of the current ripple, which is not necessarily the switching frequency.

Equation 12 shows that impedance comprises a resistive part (caused by the ESR) and a capacitive part (caused by the capacitor's reactance). The dominating part can be figured out using Figure 22. The impedance of a capacitor depends on the frequency as well as its capacitance, as shown in Equation 13.

If the measured ripple voltage is a triangular wave form, the impedance is resistive-dominated ($R_{ESR} >> X_{Cout}$). If the ripple caused by the reactance is dominant, it looks like a sine wave form ($X_{Cout} >> R_{ESR}$). The impedance also has an influence on the compensation network. As a rule of thumb, if the output capacitors have a very low ESR, you will need a type-3 compensation in voltage mode. If the ESR is significant, a type-2 compensation can be sufficient.

In general, several capacitors need to be put in parallel. This increases the capacitance and decreases the ESR of such a capacitor block, which is shown in Equation 14.

$$C_{Out,\,parallel} = n \times C_{Single}$$
$$R_{ESR,\,parallel} = \frac{R_{ESR,\,single}}{n} \tag{14}$$

C_{Single} and $R_{ESR,single}$ are the capacitance and ESR, respectively, of a single capacitor and n amount of capacitors put in parallel.

For a specified transient behavior to a load step, the maximum impedance of such a capacitor block has to be calculated with Equation 15.

$$\Delta V = \Delta I \times Z_{Cout}(f_{Crossover}) \tag{15}$$

ΔI is the current change during a load step (low to high or vice versa). ΔV is the voltage deviation during the load step and $Z_{Out(f)}$ is the output impedance of the capacitor at the crossover frequency, which is basically the loop bandwidth of the converter assuming a linear system.

When a system has a high loop bandwidth of several tenths of kilohertz and a dominant electrolytic capacitor, the load-current step response becomes a function of only the ESR (Z_{Cout} at $f_{crossover} \approx R_{ESR}$) of the output capacitor.

The voltage deviation is specified as 1 percent (ΔV = 138 mV). This means that the voltage under- or overshoot during a load step from 0.5 A (2 percent load) to 22.5 A (90 percent load) – or vice versa – must be equal to or smaller than 138 mV (measured with AC coupling).

$$R_{ESR} = \frac{\Delta V}{\Delta I} = \frac{138\,mV}{22\,A} \leq 6.3\,m\Omega$$

The output capacitance is built with three 680-µF/25-V electrolytic capacitors with an ESR of 20 mΩ each. This results in a total capacitance of 1,734 µF and an ESR of 6.7 mΩ, with all tolerances already taken into account.

With a conventional approach placing the PWM controller on the primary side and an optocoupler in the voltage feedback path, the bandwidth would be around 4 kHz, which requires approximately three times as much capacitance as this design.

Ceramic capacitors are also placed on the output. The impedance of the 10-µF/25-V ceramic capacitors at the frequency of the current ripple ($2x\ f_{Switch} \approx 350$ kHz) is the same as for the electrolytic capacitors. The current ripple is covered about one-half each by the electrolytic capacitors and by the ceramic capacitors. Therefore the ripple voltage is very small, as the overall impedance is much lower.

Adding additional capacitors with lower capacitance (100 nF, 1 nF) creates a "capacitor ladder." This results in a low impedance over a broad frequency range (up to several megahertz) to filter even higher frequency noise.

iv. Measurements

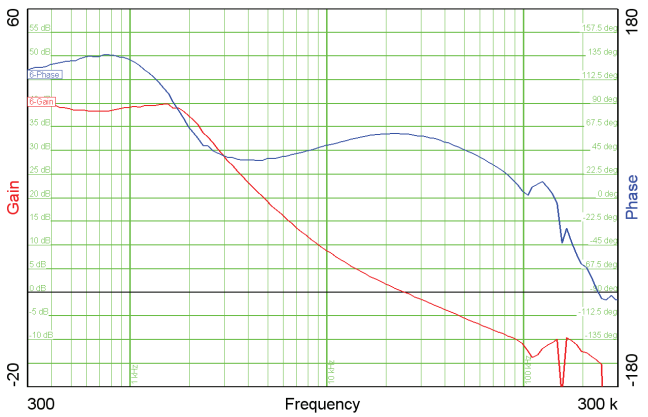


Figure 23 – Bode plot of the control loop.

The Bode plot of the control loop is shown in Figure 23. It shows a remarkable bandwidth of 24 kHz at a 61° phase margin for an isolated converter. The gain margin is about 15 dB.

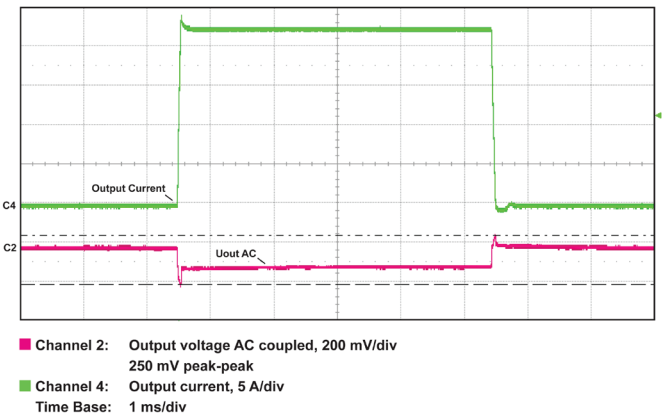


Figure 24 – Load step from 2 to 90 percent load.

Due to the high bandwidth, the transient response during a load step is also excellent (Figure 24). The undershoot when the load steps up from 0.5 A to 22.5 A is 132 mV. The overshoot back from 22.5 A to 0.5 A is even lower at 110 mV.

At 22.5-A load, the output voltage shows a constant deviation. This is caused by the output filter, as the voltage for sensing the output voltage is tapped before and not after the output filter. This deviation is approximately 100-mV additional.

At the end, the total deviation of this load change is 250-mV peak-to-peak (1.8 percent of 13.8-V output voltage).

The measured maximum efficiency of the phase-shifted full bridge is 96.6 percent. An efficiency measurement of the complete power supply can be found in Section V.

E. Auxiliary Power Supply

As the controller for the phase-shifted full bridge is located on the secondary side, it needs an auxiliary power supply; otherwise it would never start up. Additionally, the system requires various voltages – with galvanic isolation between each other – as shown in Figure 25.

The flyback converter is fed by the output voltage of the PFC: nominal 390 VDC. Because the auxiliary has to start at 85 VAC and works nominally at 390 VDC (worst case up to 420 V), this stage is not as efficient as it could be.

All converters are synchronized by a microcontroller to the same switching frequency to prevent subharmonic oscillations. As the microcontroller is placed on the secondary side and the flyback controller is connected to the PFC output voltage on the primary side, the synchronization signal has to have galvanic isolation. This is done by a digital isolator like the TI ISO7520, which has significant advantages compared to an optocoupler-based solution, as described in Section III-B.

The flyback transformer has three output windings, which are isolated to each other and supply different circuits on the board. The capability of these outputs is shown in Table 5.

The auxiliary power supply is also supplied by the mains, even when the PFC has not yet started up. This is caused by the diodes of the synchronous bridge rectifier and the diodes of the PFC in boost configuration, which have a galvanic connection to the mains even if any of these circuits are inactive and therefore charge the PFC's output capacitors. As the mains voltage is connected to the power supply when it is switched on by the line switch, the PFC capacitors are charged with the in-rush current control active. At a certain level, the auxiliary power supply starts up, disables the in-rush current control circuit, and supplies the PFC controller and all other circuits.

The feedback loop is connected to the +12-V primary output; the flyback controller has the same reference. The other outputs are unregulated and not as accurate as this voltage. Critical loads are supplied by post regulators.

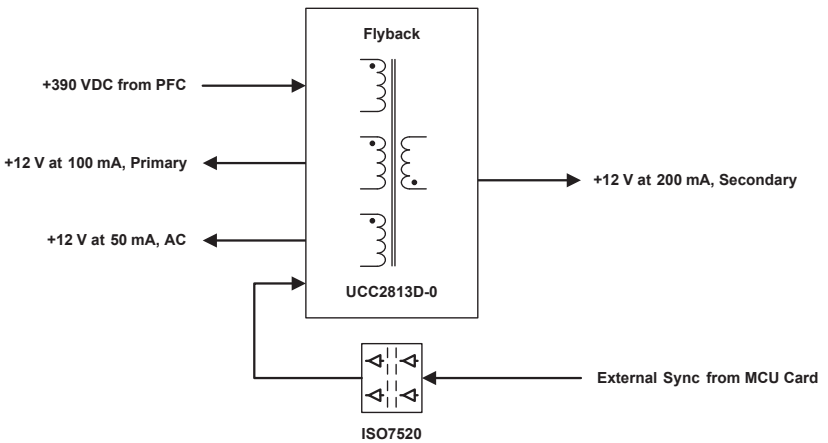


Figure 25 – Auxiliary power supply.

Output Voltage	Usage
+12 V at 50 mA, AC	Synchronous bridge rectifier
+12 V at 100 mA, primary	All circuits on the primary side: PFC controller, ADC card primary side
+12 V at 200 mA, secondary	All circuits on the secondary side: Full bridge controller and date driver, MCU card, ADC card secondary side

Table 5 – Outputs of the auxiliary power supply.

III. Analog-to-Digital Converter (ADC) Card

A. Overview

For monitoring purposes, the mains voltage as well as the output voltage of the PFC are read in by a microcontroller. The PFC's switching frequency has to be synchronized to a clock signal generated by the same microcontroller. This microcontroller is placed on the secondary side and is connected to the ground potential of the output voltage.

The mains and PFC voltage and the PFC IC are referenced to another potential on the primary side of the converter. Therefore, a direct galvanic connection of these two voltages with the microcontroller is not possible.

The connection between the primary side and the microcontroller on the secondary side has to be separated by a galvanic isolation in some way. Let's discuss the advantages and disadvantages of various circuitries based on different methods.

B. Optocoupler vs. ISO752x

The first decision is whether the signal of the mains and PFC voltage should be transferred to the microcontroller as a digital signal or an analog signal. The two voltages can be scaled down by a voltage divider and fed into an isolation amplifier. This is basically an operational amplifier with an optocoupler circuit included, which implements the galvanic isolation.

These devices are very accurate, offer high isolation voltage, and eliminate the need for an additional operational amplifier for scaling or filtering. Discrete solutions based on optocouplers, which transfer an analog voltage, are also possible. They achieve almost the same performance but are much bulkier.

The big disadvantage of both solutions is the transferred parameter: a pretty small voltage signal in the range of several hundred millivolts, sensitive to noise, that can be easily disturbed by various switch-mode power supplies (PFC, full bridge, auxiliary supply).

A more robust approach is to transfer the data to the microcontroller as a digital signal by placing an ADC with a digital interface on the primary side near the PFC. Again, the output signal (I^2C, SPI) has to be isolated between the primary side and the secondary side where the microcontroller is located. In this case, the output is purely digital, which makes things easier and more robust against noise. For the ADC card, we chose an ADS1015 12-bit sigma-delta ADC from TI, which offers an I^2C interface. Two digital signals have to be transferred: clock (SCL) and data (SDA).

An obvious approach is to use discrete, standard optocouplers for the galvanic isolation. Plenty of application notes show how to implement the bidirectional functionality needed for the data line and the unidirectional functionality needed for the clock line. If bidirectional functionality is needed (clock stretching) for the clock line, you can use the same circuit as for the data line.

Another way to transfer digital signals is to use TI's ISO752x digital isolator parts. The circuitry around and the number of channels compared to the optocoupler approach is the same, but the isolators offer much better performance in all areas.

First, optocouplers are subject to aging. The current transfer ratio drops throughout its lifetime, which is something to consider during design. In general, higher bias currents are needed to compensate for this drop.

A second problem is the tolerance of the thresholds, which leads to problems during ADC card development. Under some conditions, the circuit is not within the specifications for high and low logic levels by the ADC and the microcontroller.

Digital isolators offer much tighter thresholds as well as a push-pull output that causes almost no voltage drop. Furthermore, their signal rating is up to 1 Mbps. The I^2C "fast mode" defines transfer rates up to 400 kbps, which we tested without any problems on this system. Those speeds can only be realized with special optocouplers optimized for digital data transfer.

An isolation rating of 5-kV RMS (reinforced) also offers benefits compared to an optocoupler-based solution.

The CLK signal for synchronizing the switching frequency of the PFC converter has to have galvanic isolation. Here, the same advantages apply to an ISO752x-based solution.

Independent of the approach (isolation amplifier, optocoupler, digital isolator), a voltage supply on both sides of the isolation barrier is essential, which is provided by the auxiliary power supply.

C. Block Diagram and Signal Chain

Figure 26 gives an easy understanding of the design of the ADC card as well as its integration in the complete system.

The left side represents the primary side, which is referenced to the mains. The secondary side represents the secondary side of the power supply, referenced to the ground of the output voltage. The ADC card handles the scaling of the input and output signals as well as the galvanic isolation in-between.

The MCU card generates the CLK signal for synchronizing the PFC's switching frequency. The signal is then fed into the ADC card, galvanic-isolated, scaled and connected to the SYNC input (RDM, pin 2) of the PFC controller. The microcontroller's output is a square wave signal with a 50 percent duty cycle. As the PFC controller needs a synchronization signal with a maximum 50 percent duty cycle, the square wave signal is coupled by a capacitor to the input of a single Schmitt-trigger buffer. This generates a square wave signal with the same frequency, but a much smaller duty cycle on the output. Some margin is gained compared to a 50 percent duty-cycle signal according to the maximum value in the data sheet. Additionally, the CLK signal as well as all other signals are passed through a common-mode filter, explained in detail later on.

Starting from left to right, the signal path of the voltage measurement is visible in Figure 26. The two voltages (mains and PFC) are connected to high-impedance voltage dividers. They scale down the input voltages to a range that the ADC card can handle. These signals are fed into a single-supply dual operational amplifier wired as a buffer, followed by a passive RC-low pass filter (3.3-Hz bandwidth). The low bandwidth filters the signals effectively and reduces noise significantly.

The two voltages are applied to a 12-bit ADC with integrated reference. The output of the ADC is an I^2C interface. One bidirectional ISO7521 is needed for the data signal (SDA) to enable bidirectional communication. The diodes on each side represent the additional circuitry needed to enable this feature.

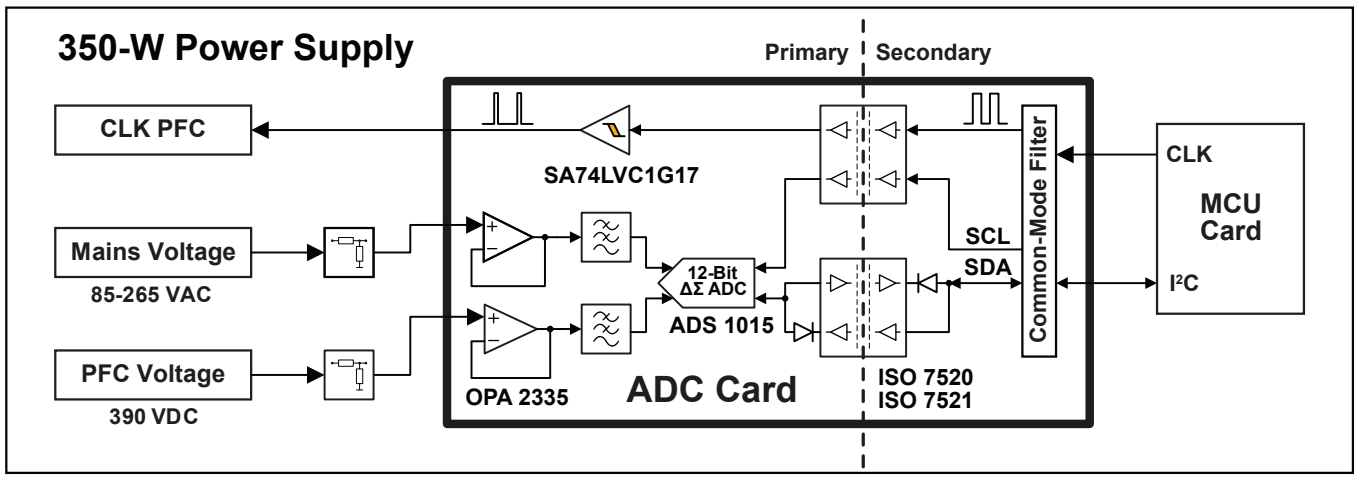


Figure 26 – Block diagram of the ADC card.

The clock signal (SCL) is always generated by the master, represented by the MCU card in this application. Therefore, you only need a unidirectional path from the microcontroller to the ADC. The same ISO7520 with two independent unidirectional channels is used for the SCL of the I^2C bus and the CLK for synchronizing the PFC switching frequency of the PFC (Figure 27).

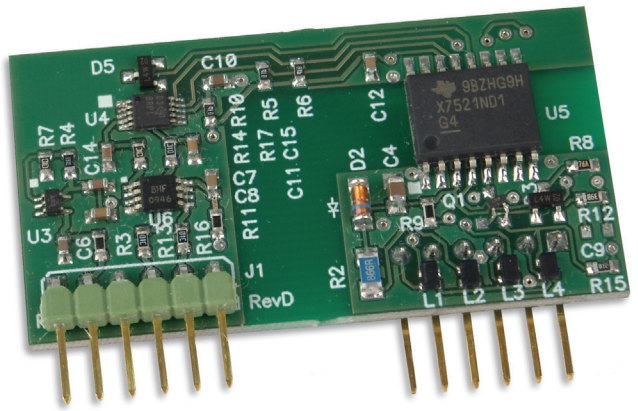


Figure 27 – Photo of the ADC card.

D. Common-Mode Filter

Galvanic isolation is the physical separation of two current paths to avoid any direct current flow between them. However, there is still a parasitic capacitance between them, made up of the parasitic capacitance of the components used to pass the galvanic isolation (such as the transformer) and stray capacitance caused by the layout and system geometry.

If dV/dt is applied to one side of the galvanic isolation, a high-frequency current flows across the isolation barrier because of the parasitic capacitance. This can be the noise of a switch-mode power supply or even switching the power supply on by the main switch. The exact propagation path of this current, called "common-mode current," is usually unknown and hard to figure out.

A switching system (a PFC stage for example) near a component passing the galvanic isolation generates common-mode noise, which is injected to the other side of the galvanic isolation. This causes common-mode currents flowing from the primary side to the secondary and back, which may cause high-voltage noise on sensor and communication lines. In practice, it is often difficult to localize the source of common-mode noise and determine if it is caused by the E- or H-fields.

During development, we encountered problems with the I^2C communication when the power supply was working at a certain load level. Communication was disturbed and no more data was transferred. With no load applied on the output, however, communication between the MCU card and the ADC card worked properly.

Investigations showed that this problem was caused by the PFC stage, which is near the ADC card. Tests with screening the ADC card showed no improvement; it even got worse. This was a clear indicator that common-mode currents were causing the trouble.

Placing common-mode chokes in each signal and supply line, as shown in Figure 28, attenuated the common-mode currents effectively – without changing the signal integrity.

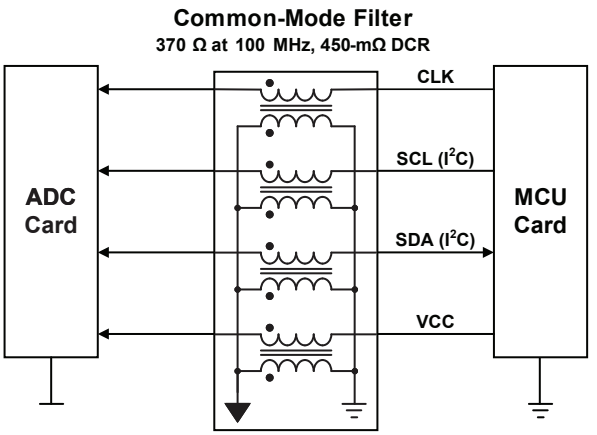


Figure 28 – Common-mode filter on the ADC card.

To save space, the ADC card is populated on both sides and mounted horizontally on the power board.

IV. MCU Card

A. Overview

Two microcontrollers are used for different tasks in this power supply. The first microcontroller controls the synchronous AC/DC bridge rectifier, first described in Section II-B.

The second microcontroller is used as a human-machine interface for displaying information about the system's state, handling user inputs and overall monitoring.

B. Block Diagram and Interfaces

Figure 29 shows the MSP430F2255 microcontroller and its peripherals on the MCU card. The user interface is built by a backlit liquid crystal display with 2 x 16 characters and four push buttons.

The temperature inside the chassis is measured by a surface-mounted negative temperature coefficient (NTC) thermistor, which is populated on the MCU card. A screw-in NTC in each of the heat sinks measures the temperature of the MOSFETs (PFC, full bridge).

The I^2C interface is connected to the ADC card to transfer the values of the mains and PFC voltage to the microcontroller. The Spy-Bi-Wire interface of the microcontroller is used for programming and debugging purposes. It needs fewer pins compared to a standard JTAG interface and therefore saves places.

A digital output enables and disables the full bridge. During startup, all converters (PFC, auxiliary supply) besides the full bridge start automatically. The full bridge is always disabled

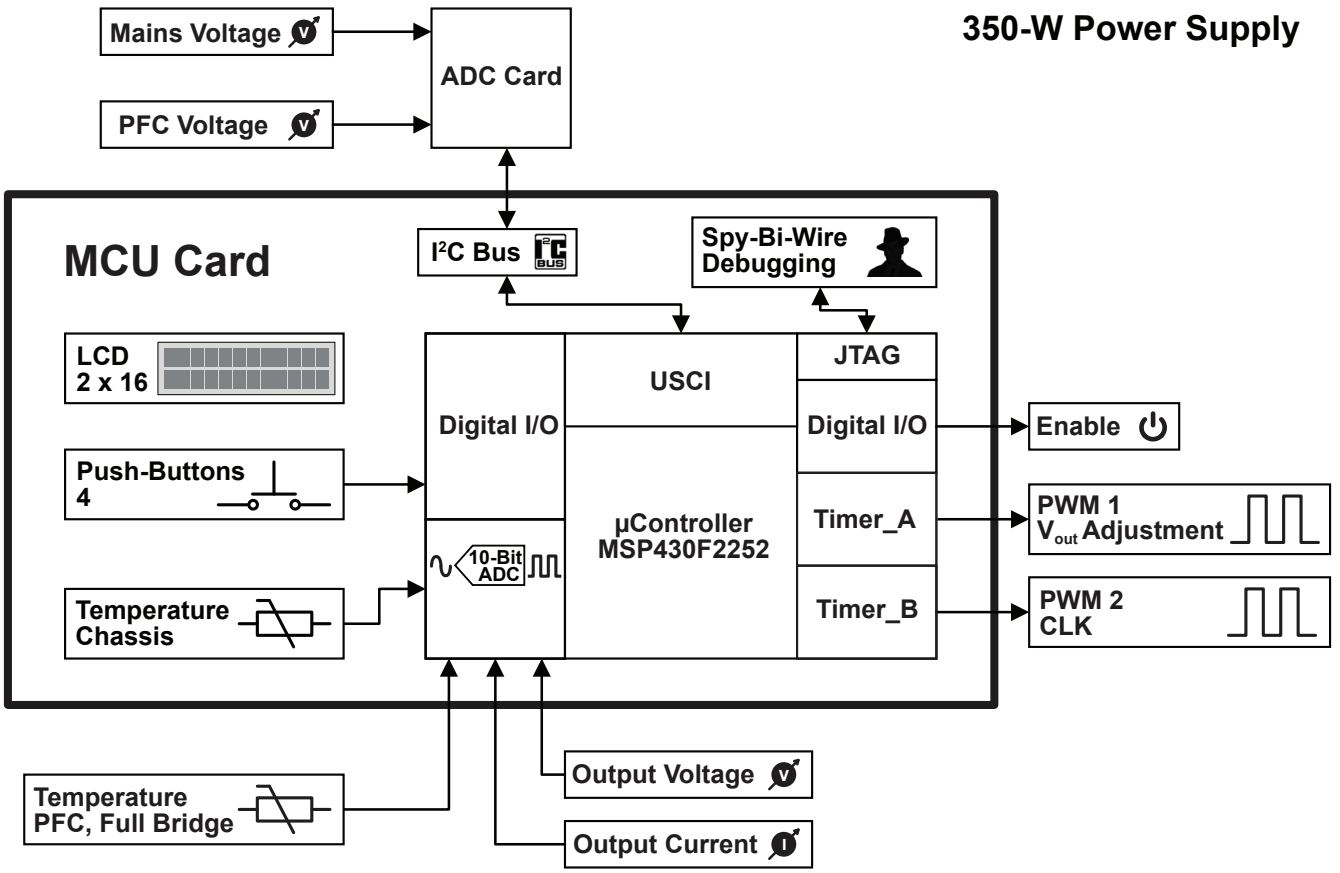


Figure 29 – Block diagram of the MCU card.

until the user presses the Enable push button. If all parameters are in range, the MSP430 MCU activates it.

A PWM signal is used to set the output voltage in the range of 12 to 14 V. The error amplifier of the full-bridge controller is connected as shown in Figure 30. The inverting input of the error amplifier is connected to the output voltage of the full bridge by a voltage divider, like almost every power supply. The output voltage changes by modulating the reference voltage of the error amplifier through a PWM signal.

One specific feature of the UCC28950 is that the reference voltage and the reference input of the error amplifier lead out to pins. The reference voltage is connected to the noninverting input of the error amplifier by a voltage divider. The PWM signal connected to Q_1 connects R_1 cyclic to ground. This reduces the average voltage on the noninverting input, as R_1 is put in parallel to R_3 and R_2. Thus the output voltage is reduced as the reference voltage is reduced. The higher the duty cycle of the PWM signal, the lower the output voltage.

Capacitor C_1 filters the voltage to achieve a clean reference voltage and a stable output voltage.

This principle is applicable to every switch-mode power supply even when the reference voltage and the noninverting input are not accessible, in which case an additional, external operational amplifier and a reference must be used. The output of this amplifier has to be connected to the inverting input of the internal error amplifier.

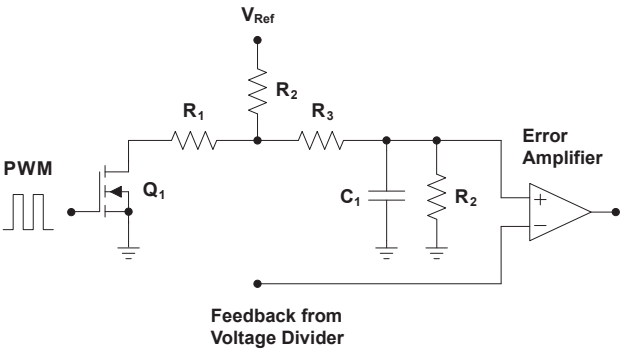


Figure 30 – Modulation of the reference voltage for an error amplifier by a PWM signal.

A second PWM signal generates a signal for synchronizing the switching frequencies of the converters (PFC, full bridge, auxiliary supply) and preventing subharmonic oscillations in the system. The switching frequency is user-adjustable in four discrete steps (178, 170, 163 and 157 kHz). The step size is limited by the timer resolution of the microcontroller. When the microcontroller has a high-resolution timer, like Timer_D in the TI MSP430F517x, dithering can be implemented. This means that the switching frequency always changes slightly. It doesn't reduce the overall noise generated by switch-mode power supplies, but it does broaden the spectrum and makes it easier to pass a certification measurement.

The MCU card shown in Figure 31 is an element of the front panel and plugs into the power board.

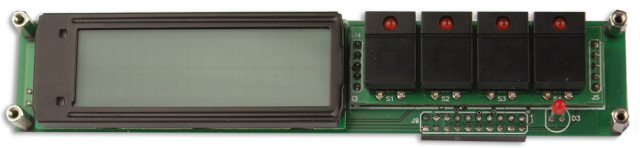


Figure 31 – MCU card.

C. Software

Figure 32 summarizes the software functionality in a flow-chart format.

The software is written in TI's Code Composer Studio™ software using C language. All functions are separated into single libraries (timer, menu, LCD) and well-commented to keep the source code clear, serviceable and easy reusable for other projects.

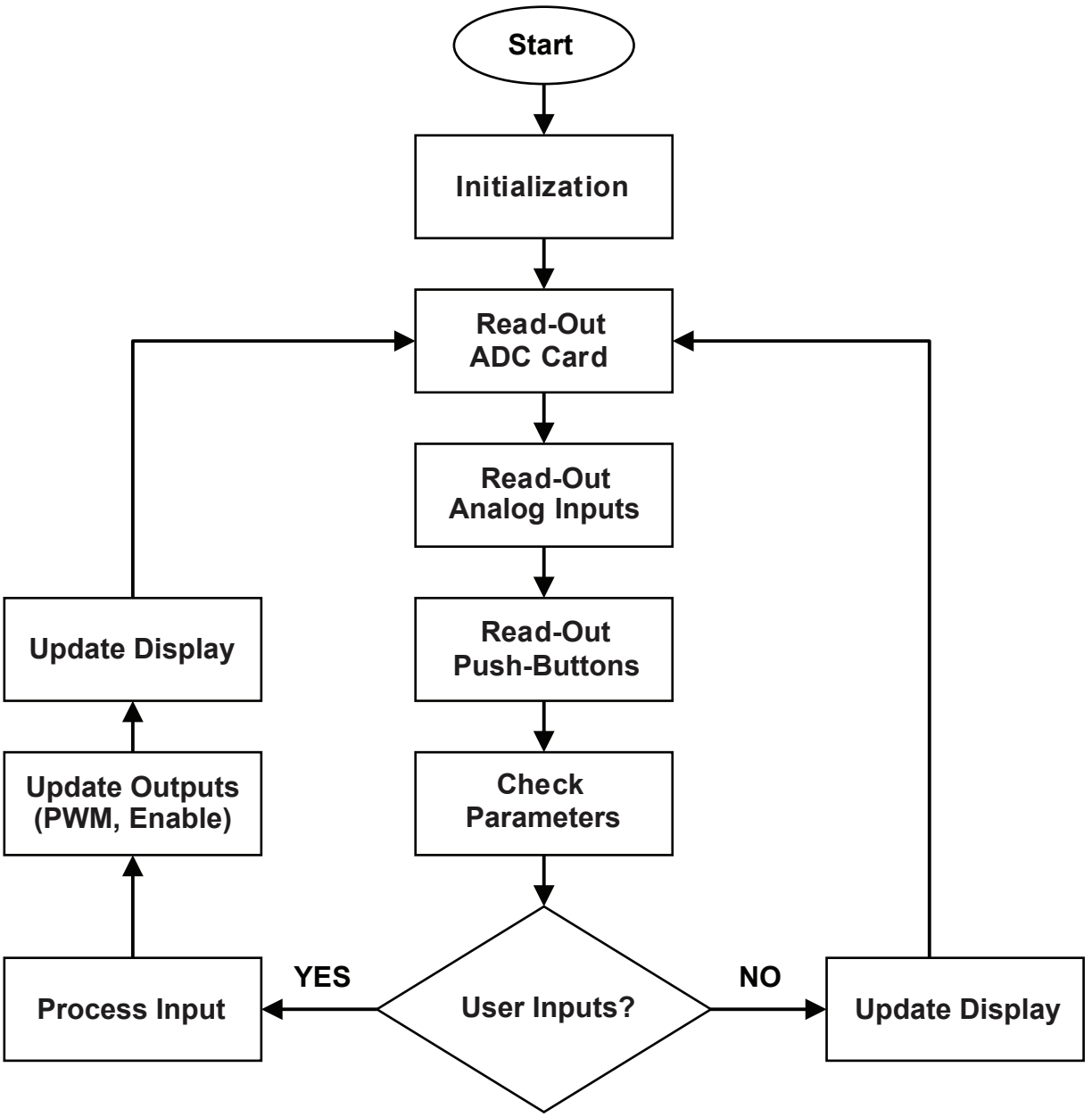


Figure 32 – MCU card software flow chart.

V. Conclusion

This paper described the unique synchronous bridge rectifier, the interleaved PFC stage, the high-speed phase-shifted full-bridge converter and the monitoring capability enabled by a MSP430 microcontroller for a 350-W, state-of-the-art power supply. Each building block can be used separately and is easy scalable to higher power levels. You can easily synchronize several converters to the same switching frequency using digital isolators.

Using synchronous rectification on the full bridge and placing the controller on the secondary side enable a bandwidth and load response far better than the potential of a standard converter that uses an optocoupler for the feedback path, even with much more output capacitance.

Figure 33 shows the plug-to-plug efficiency of the power supply at 110-VAC and 230-VAC input voltages and a 13.8-V output voltage. The efficiency goal from the specification of >90 percent is clearly achieved.

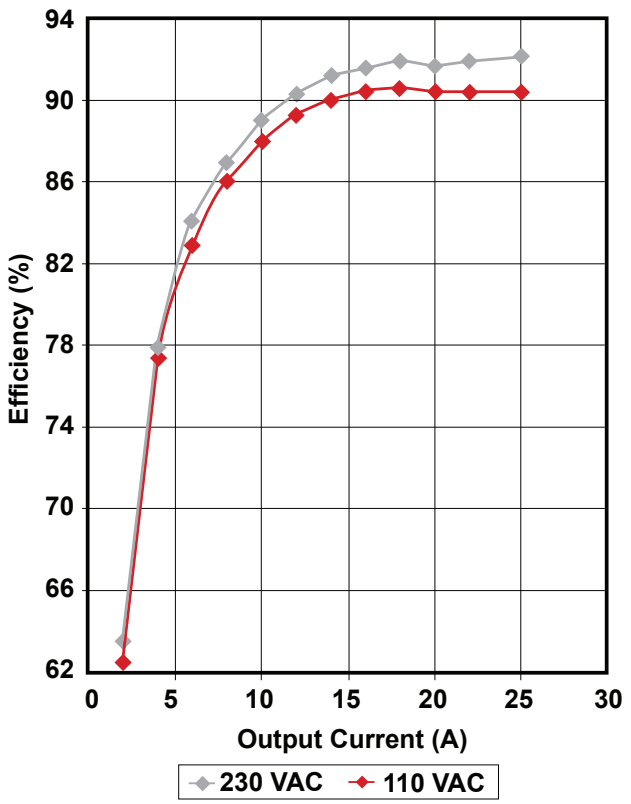


Figure 33 – Plug-to-plug efficiency at 13.8-V output voltage.

The peak efficiency at 110 VAC is 90.4 percent; at 230 VAC it is 92.2 percent. The slightly lower efficiency at the 110-VAC input is caused by the dropping efficiency of the PFC stage.

The flat efficiency curve from 12 A to 25 A is an indicator of a well-designed power stage. Besides this, the high efficiency speaks for the topologies used and their correct implementation.

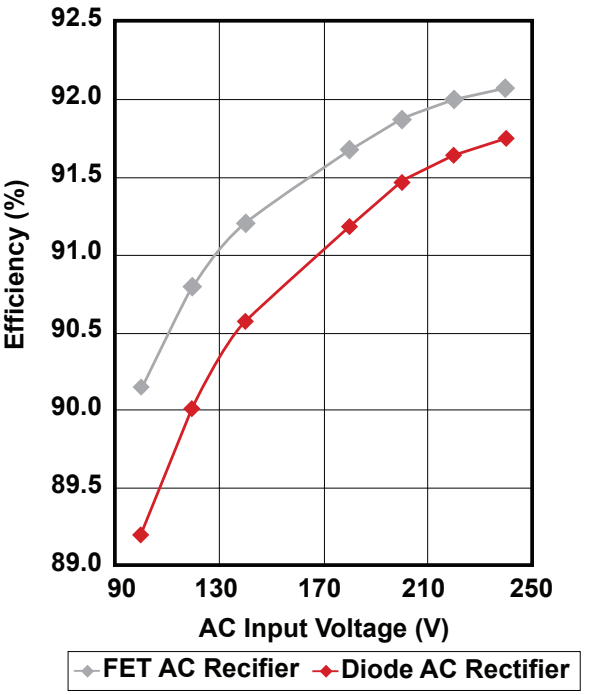


Figure 34 – Efficiency diode bridge rectifier vs. synchronous rectifier.

Using a synchronous bridge rectifier with MOSFETs instead of diodes boosts the overall efficiency at the 110-VAC input by 0.9 percent, as shown in Figure 34. At 230 VAC, the boost is lower at 0.3 percent because of the lower input current. Without that, a >90 percent efficiency wouldn't have been possible.

At higher power levels, the benefit is not only the reduced losses but the relaxed thermal interface.

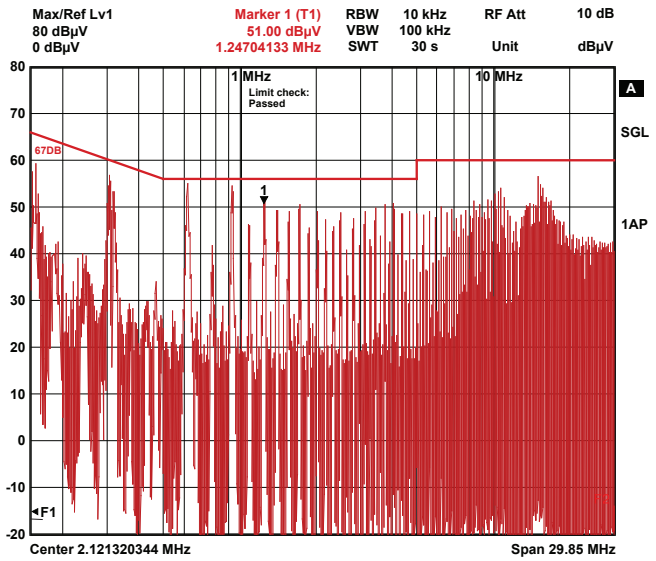


Figure 35 – Conducted emissions at 230-VAC input and 25-A load at 13.8 V.

The measurement of the conducted emission in Figure 35 gives feedback about the noise performance of the system. With all circuits running and a load of 25 A at 13.8 V attached, the emissions are well below the limits.

The detailed block diagram and the connections between all sections of the system are shown in Figure 36. They include:

- The power path.
- Control and sense signals.
- Synchronization signal (switching frequency).
- Auxiliary power supply.
- An isolated gate driver.

The base of the power supply is the power board, first described in Section II. It carries four additional boards: two carrying gate drivers for the AC/DC rectifier, the ADC card and the MCU card.

During start up, the auxiliary power supply starts first; it then supplies all other circuits. Next to start is the PFC stage, which works at the beginning without synchronization of the switching frequency. When the MCU card is ready, it automatically applies the synchronization signal to the PFC and auxiliary power supply.

When the user presses the ENABLE button, the full bridge starts up, also with its switching frequency synchronized.

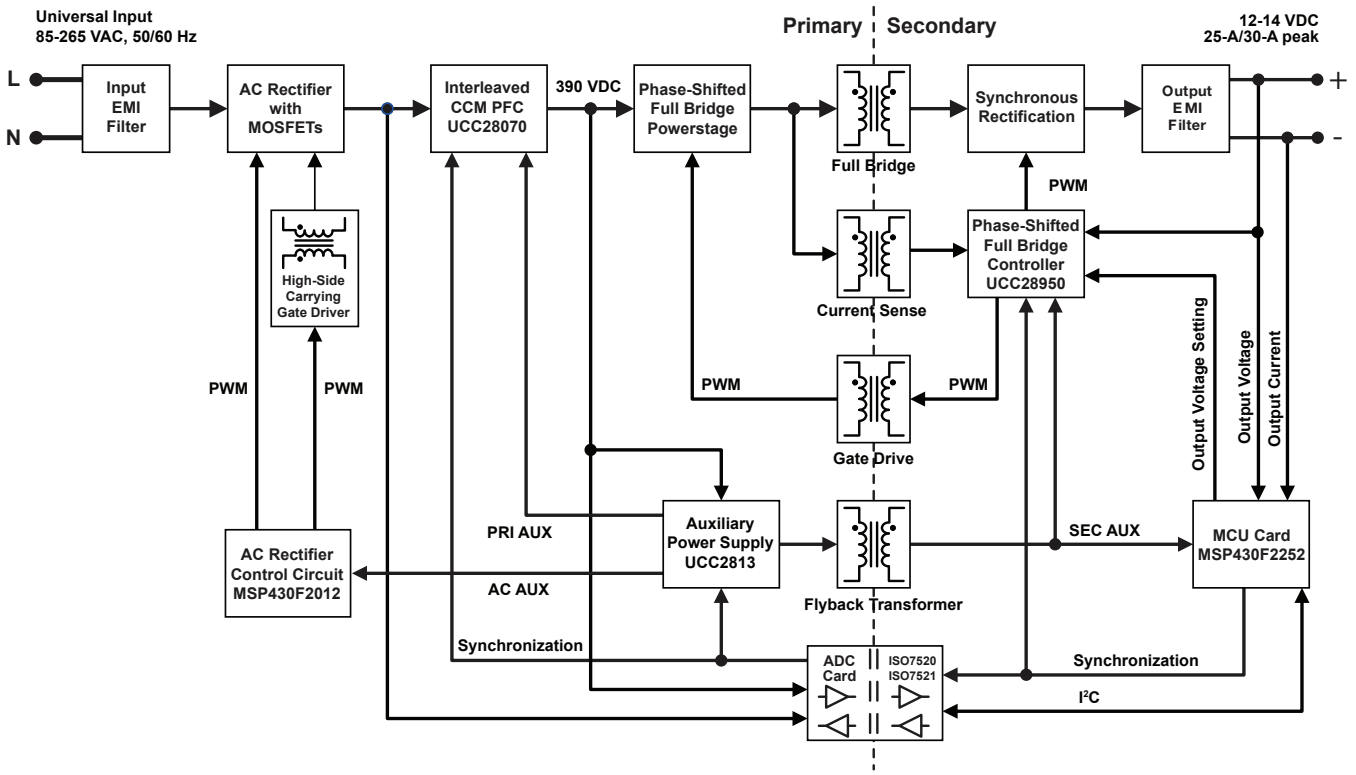


Figure 36 – Detailed block diagram of the system.

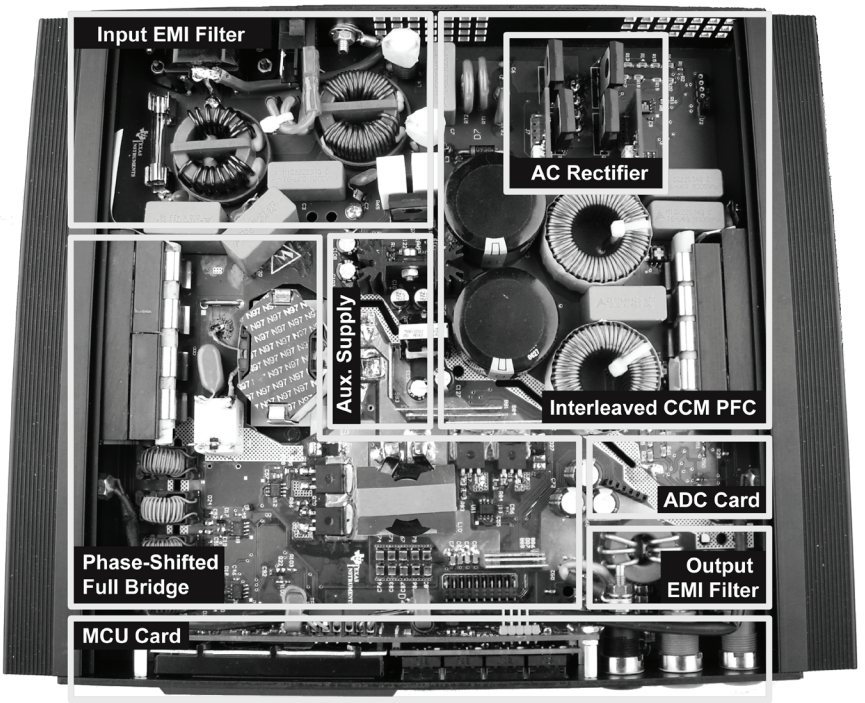


Figure 37 – Top view of the power supply.

The dimension of the housing containing the power supply is 10.8 x 9.1 inches/275 x 230 mm with a height of 1.7 inches/44 mm. A photo of the power supply with its main sections highlighted is shown in Figure 37.

All specifications from Section I-A in Table 1 are fulfilled, repeated here as Table 8.

The complete high-efficient, high-performing 350-W power supply, including hardware and software, was developed at TI's Design Services Europe in Freising, Germany. The project name is PMP5568 and documentation is available on TI.com using the keyword "PMP5568."

Input	Universal AC input voltage range	✔
	85 to 265 VAC at 50 or 60 Hz	
Output	12- to 14-VDC adjustable	✔
	25-A continuous, 30-A peak	✔
	Voltage ripple < 12-mV peak-to-peak at 20-MHz bandwidth measured	✔
	Load step 2% to 90% with a voltage deviation of < 1%	✔
Mechanics	Silent power = no forced air → Overall efficiency has to be > 90%	✔
	Slimline housing with a height of < 2 inches/50 mm	✔
Extras	Hold-up time > 20 ms for harsh environments	✔
	All converters synchronized to the same switching frequency	✔
	Switching frequency-selectable (170 kHz ± 10%)	✔
	Full monitoring with a microcontroller → Analog design with digital monitoring	✔

Table 8 – System specifications.

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