1 Introduction

This document provides a report of the tests that were carried out to validate the EM1401 rev A2 5 amp Active Balance BMS board.

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2 AFE Accuracy

2.1 Hardware Requirements

The AFE analysis required the voltages of the batteries attached to the EM1401 to be accurately measured and then compared to measurements taken by the EM1401 itself.

To provide an accurate reference of the input voltages (battery) applied to the EM1401, an Agilent 34970A Data Acquisition Switch was connected across the EM1401 BATTERY_16 connector board main connector to record the battery voltages being input to the board. The results were uploaded to Agilent software on the bench PC. The 34970A was set to sample the input every 2 seconds.

The raw output data was collected at the bench PC via the output from the CAN communication interface and the BMSView GUI. The AFE sampling time per channel was observed to be ~200us and a complete set of channel reading uploaded to PC every second. Measurements were taken with the oversampling set to 32 and 1 (effectively disabled) to focus on single sample performance.

All tests were conducted with ~3.3V cell in mid stack and assumes mismatch between cells of <100mV.

2.2 Typical System Accuracy

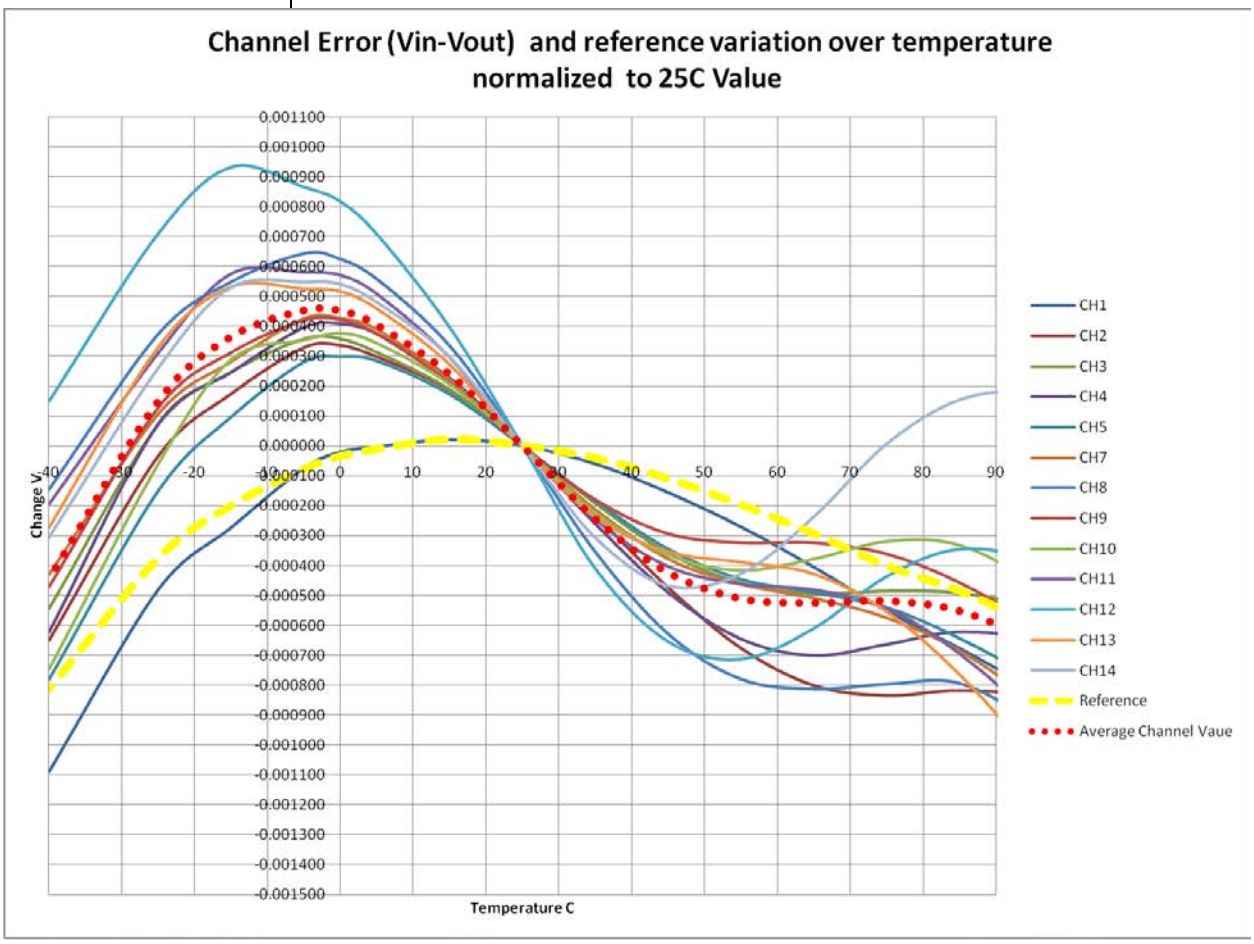
2.2.1 DC and Random Noise Errors Combined

- Included random noise based on measured system data
- DC error includes gain and offset errors calculated from AFE, ADC and REF measured device data

	Single Sample	32 Oversamples	Units
-40°C			mV
25°C	0.9	0.7	mV
85°C			mV

2.2.2 Measured System Static DC Error over Temp

- Normalized to 25C



3 Battery Stack Protection

3.1 Threshold accuracy

These tests measure the threshold error of the trip voltage versus the LTH, the HTH and AUXTH (Temperature sensing) settings on EMB1433.

Definition:

- ΔLTH is the under-voltage trip point (UVfalling) - LTH
- UVhys is the under-voltage trip point hysteresis = (UVrising) - (UVfalling)
- ΔHTH is the over-voltage trip point (OVrising) - HTH
- OVhys is the over-voltage trip point hysteresis = (OVrising) - (OVfalling)
- ΔAUX is the thermal sense trip point (AUX-Up) – AUXTH
- AUXhys is the thermal sense trip point hysteresis = (AUXrising) - (AUXfalling)

3.1.1 Test Setup

A battery box comprising 14 batteries in series is used to supply the input voltage to the EM1401 board. Except the bottom and the top connection wires, all wires connecting individual battery to the board were switched open. An adjustable DC supply is being used to create an under-voltage or over-voltage condition at the battery connector on the EM1401 board. The dc supply has an adjustable resolution of 1mV.

3.1.2 Configuration

The following EMB1433 circuit connections were used for this test.

- VM is supplied by a linear regulated -5V1.
- VP and CHPVP are supplied by a linear regulated +5V_2.
- Each channel has a 5.6V zener diode clamp at the sense pin, and has a 100 ohm resistor in series with the sense pin.

3.1.3 Test Results

The results below are a summary of the UV, OV and AUX threshold error versus the setting of LTH, HTH and AUXTH, respectively.

These tests was performed on 02/01/2010 by Stephen Holland
All measurements were acceptable and considered a PASS.

	Voltage at connector (mV)
Δ LTH	±6
UVhys	8
Δ HTH	±5
OVhys	12
Δ AUX	±3
AUXhys	5

3.2 PING/Fault Bus Operation

The PING/Fault bus protection circuitry was tested for survival of hot-plug in a stacked arrangement. The stack was comprised of 3 boards, attached to 14 cell (4P14S) battery modules comprised of 26650 2.5Ah A123 cells.

These tests was performed on 12/14/2011 by Stephen Holland
All measurements were acceptable and considered a PASS.

A basic diagram of the test setup is shown in Figure 1.

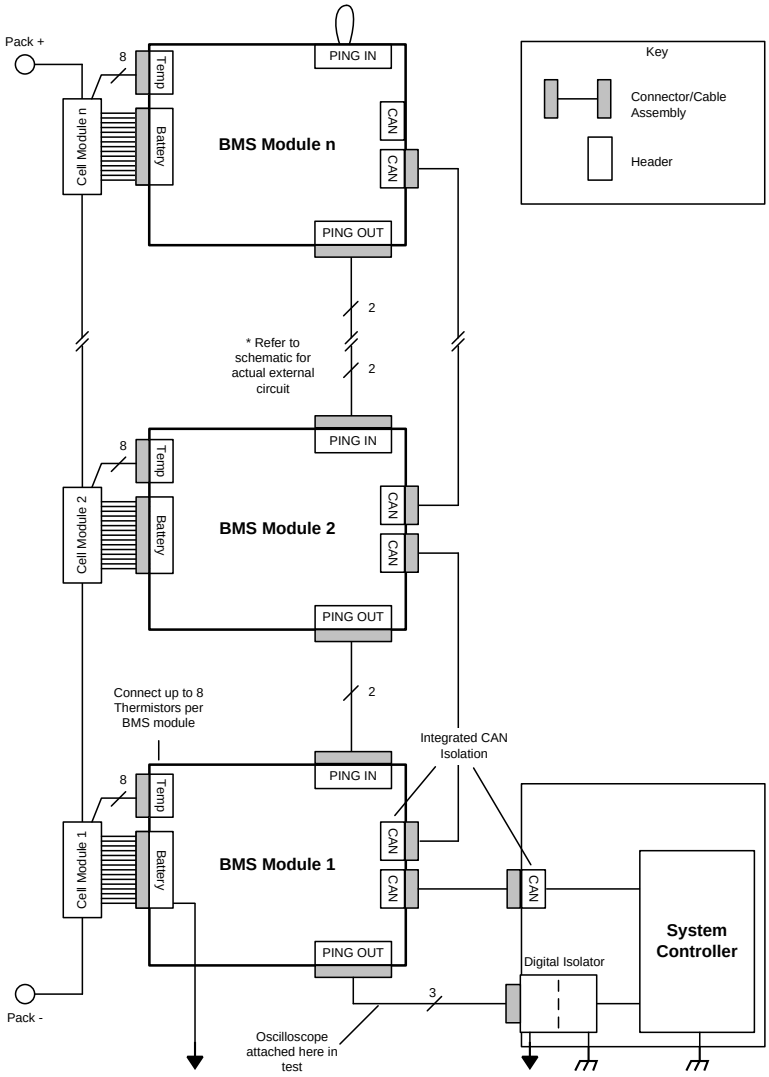


Figure 1 - Test Setup

The connection sequence of batteries and PING bus connectors were varied in the following patterns to ensure any connection sequence can be accommodated. In all cases, CAN bus communications to all

modules were made first, then power applied to the isolated CAN circuit. The OV, UV and AUX (OT) thresholds were configured to provide no faults.

Pattern #1:
1. Top battery
2. Middle battery
3. Bottom battery
4. PING termination on top module
5. Top Module PING_OUT to middle module PING_IN
6. Middle Module PING_OUT to bottom module PING_IN

Pattern #2:
1. PING termination on top module
2. Top Module PING_OUT to middle module PING_IN
3. Middle Module PING_OUT to bottom module PING_IN
4. Top battery
5. Middle battery
6. Bottom battery

Pattern #3:
1. PING termination on top module
2. Top Module PING_OUT to middle module PING_IN
3. Middle Module PING_OUT to bottom module PING_IN
4. Bottom battery
5. Middle battery
6. Top battery

Pattern #4:
1. Top Module PING_OUT to middle module PING_IN
2. Middle Module PING_OUT to bottom module PING_IN
3. Bottom battery
4. Middle battery
5. Top battery
6. PING termination on top module

Pattern #5:
1. Bottom battery
2. Middle battery
3. Top battery
4. Top Module PING_OUT to middle module PING_IN
5. Middle Module PING_OUT to bottom module PING_IN
6. PING termination on top module

Pattern #6:
1. Middle Module PING_OUT to bottom module PING_IN

2. Bottom battery
3. Middle battery
4. Top battery
5. Top Module PING_OUT to middle module PING_IN
6. PING termination on top module

In all connection patterns, the result was a successful transmission of the heart beat pulse across the stack, and monitored on the bottom module PING_OUT header. Figure 2 shows the HEART signal at the bottom PING_OUT connector (pin 7) at first connection of the batteries, with PING bus connections already made. Figure 3 shows the HEART signal at the middle module on PING_IN (pin 2).

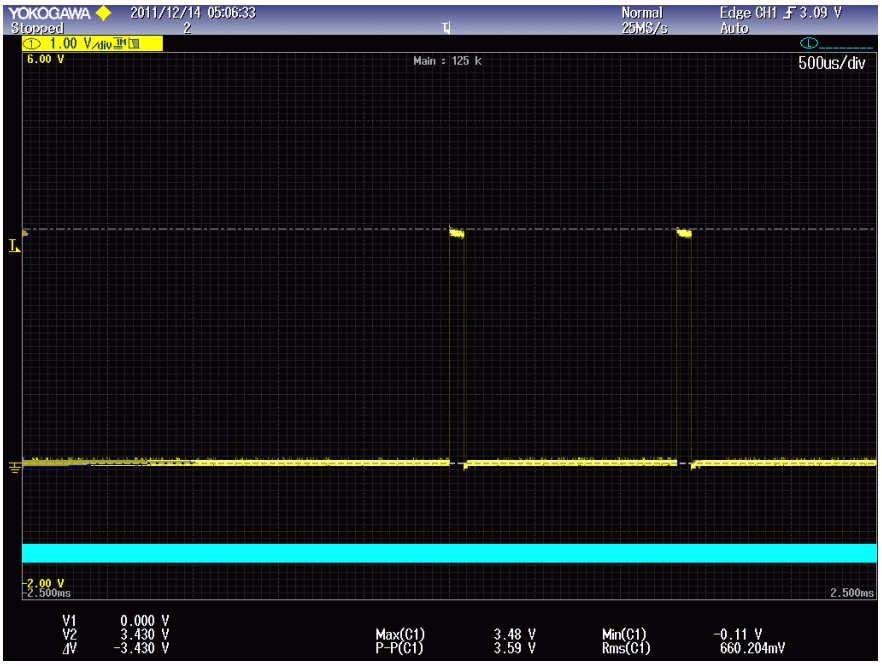


Figure 2 - HEART signal, bottom module to oscilloscope (or microcontroller)

Figure 3 - HEART signal, middle DIN_LS

4 Cell Balance Operation

4.1 Fault detection

There are several different conditions that will trigger a fault in the EMB1499. Ideally, when a fault condition occurs, the chip will shut itself down and latch a 3 bit "fault code" into its "Fail" output pins. The "Done" output will also latch high. These outputs will remain latched until the next time the EMB1428 asserts the "Enable" signal.

When a fault occurs, the "Done" signal and fault code are sent to the EMB1428 for processing. The transaction between the EMB1499 and EMB1428 should proceed as follows:

1. A fault condition occurs, causing the EMB1499 to latch a fault code to its "Fail" output pins. This fault code is sent directly to the EMB1428.
2. After about 10us, The "Done" signal is asserted high, and the chip stops switching. It is still technically enabled, but the charging action is stopped.
3. If the EMB1428 receives a "Done" command while the EMB1499 is enabled, it assumes a fault has occurred. It immediately drops the "Enable" signal to the EMB1499, shutting down the chip. It also reads the 3 bit fault code.
4. The EMB1428 then communicates the fault information to the microcontroller.

For reference, the 3 bit code for each fault is listed here:

000 – No fault
001 – Primary side current limit
010 – Secondary side current limit
101 – Cell under-voltage (UVP)
110 – Cell over-voltage (OVP)

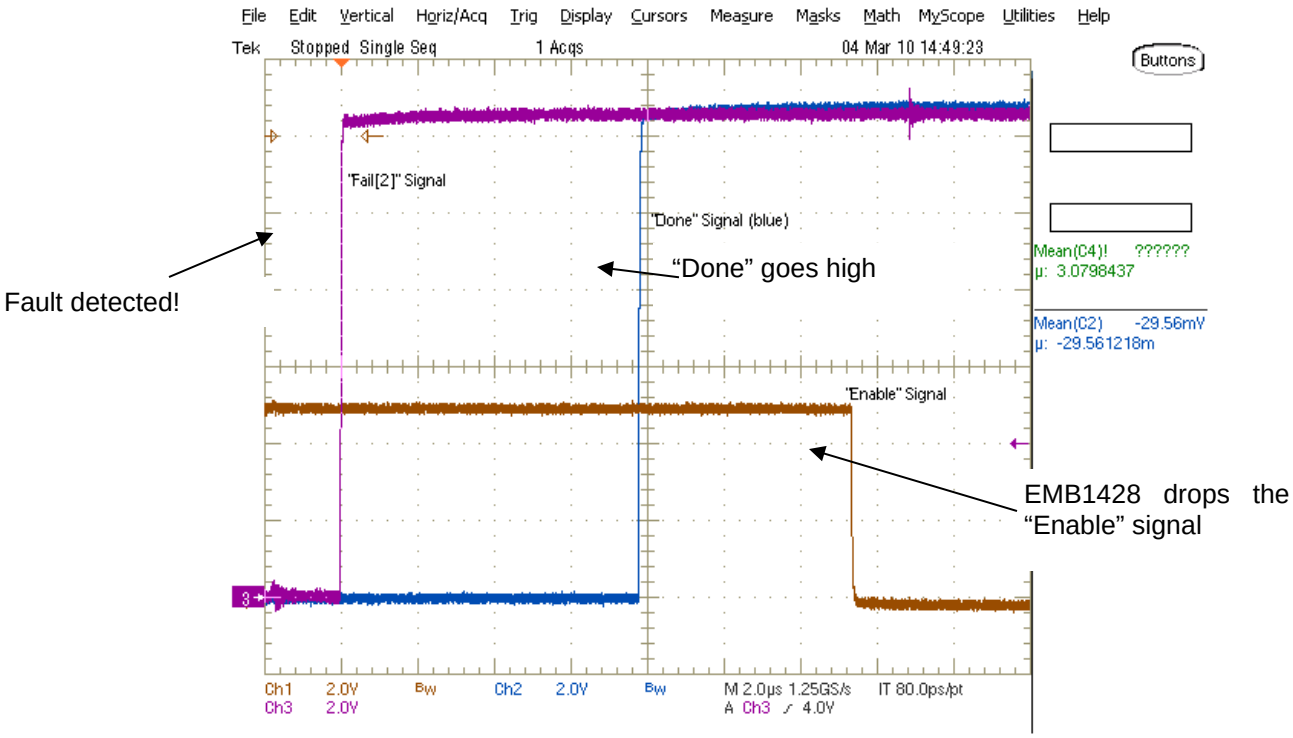
These tests was performed on 03/04-05/2010 by John Kirchoefer
All measurements were acceptable and considered a PASS.

4.2 Communication Between EMB1499 and EMB1428 During a Fault

This section provides scope plots of the transaction between the EMB1499 and EMB1428 when a fault condition occurs.

The first figure shows this transaction in the event of a non-specific fault. For this waveform, the cell was disconnected while charging to create an “OVP” fault, but this particular transaction is independent of the specific fault type. For reference, a scope probe was put on the MSB of the fault code (“Fail[2]”). Note that about 8us after the fault is detected (“Fail[2]” goes high), the “Done” signal is asserted. The EMB1428 sees this, and disables the EMB1499 by dropping the “Enable” signal. This takes about 5us.

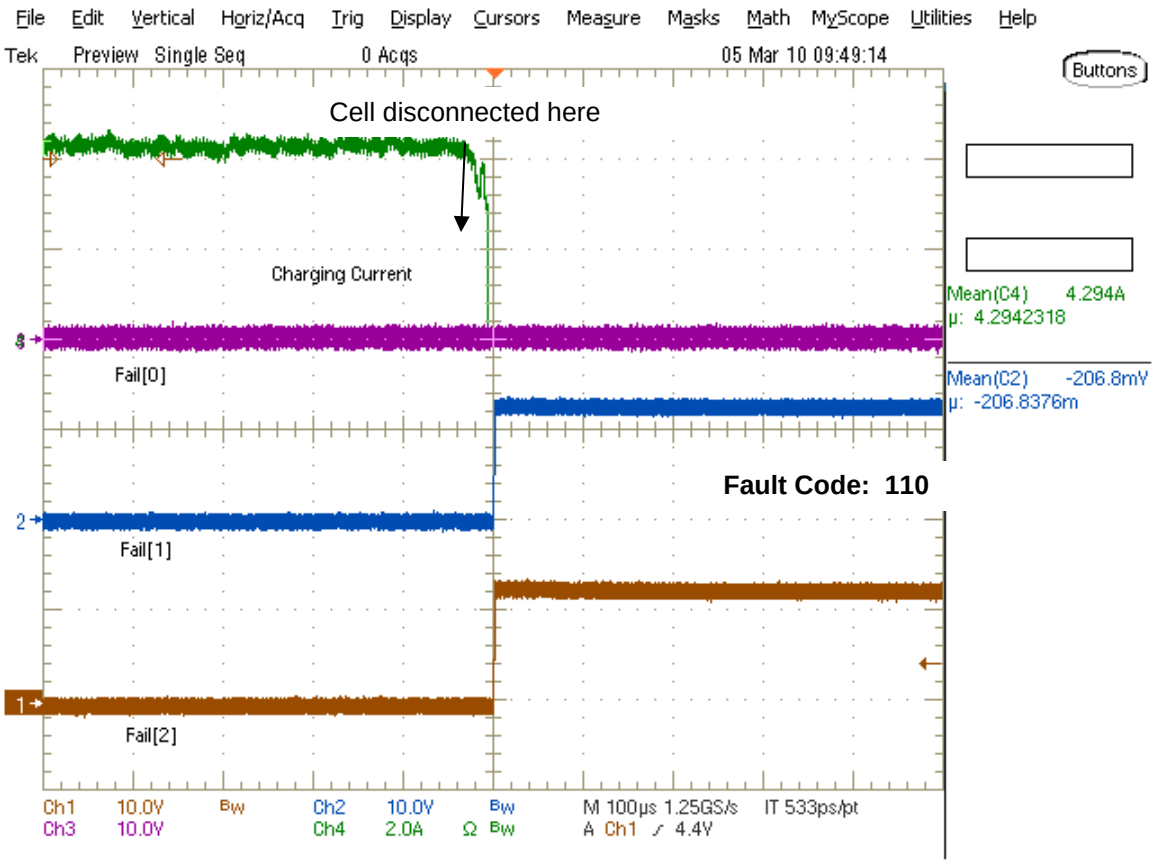
4.2.1 Fault transaction between EMB1499 and EMB1428:



4.3 Individual Failure Modes

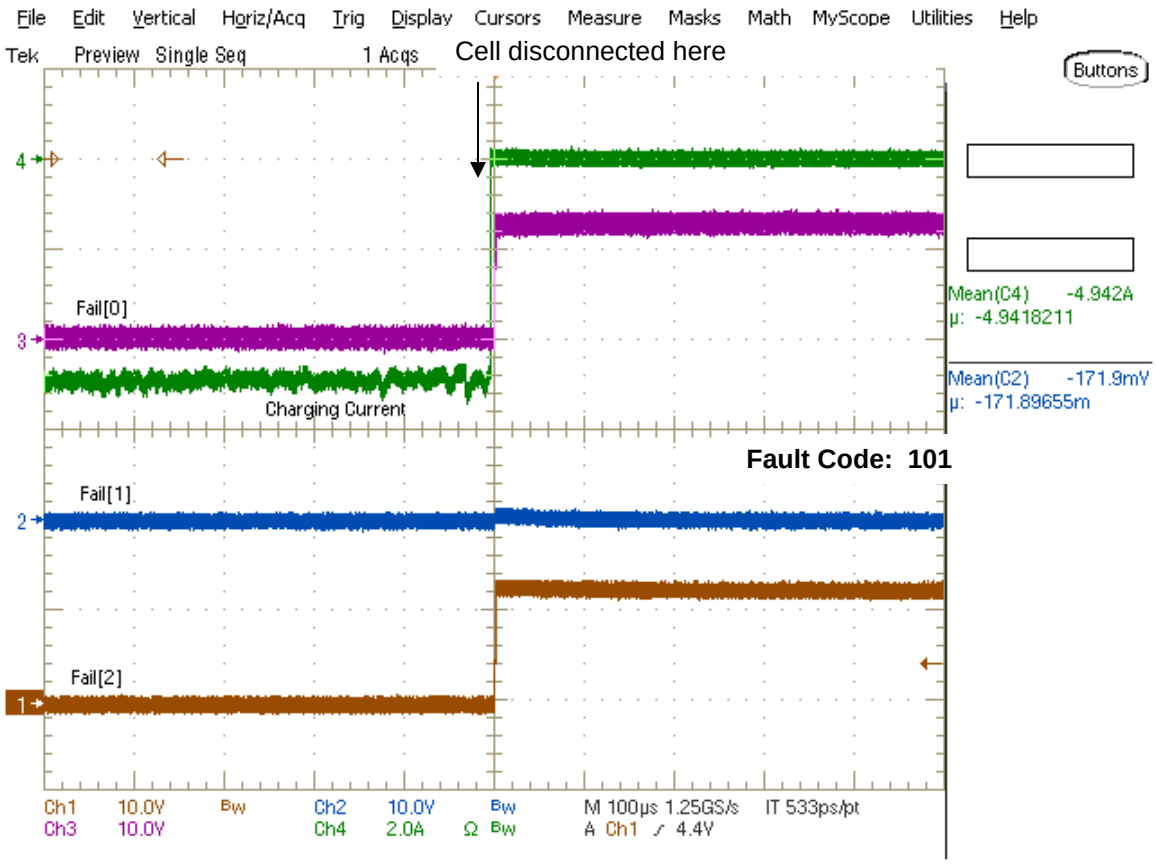
4.3.1 Over-voltage Failure (Open cell while charging)

To test this failure, the connection to the cell was broken while charging at 5A. This causes the voltage at the output of the converter to fly up, tripping the over-voltage protection. From the plot, it can be seen that the charge current drops immediately to zero and the correct fault code (110) is output:



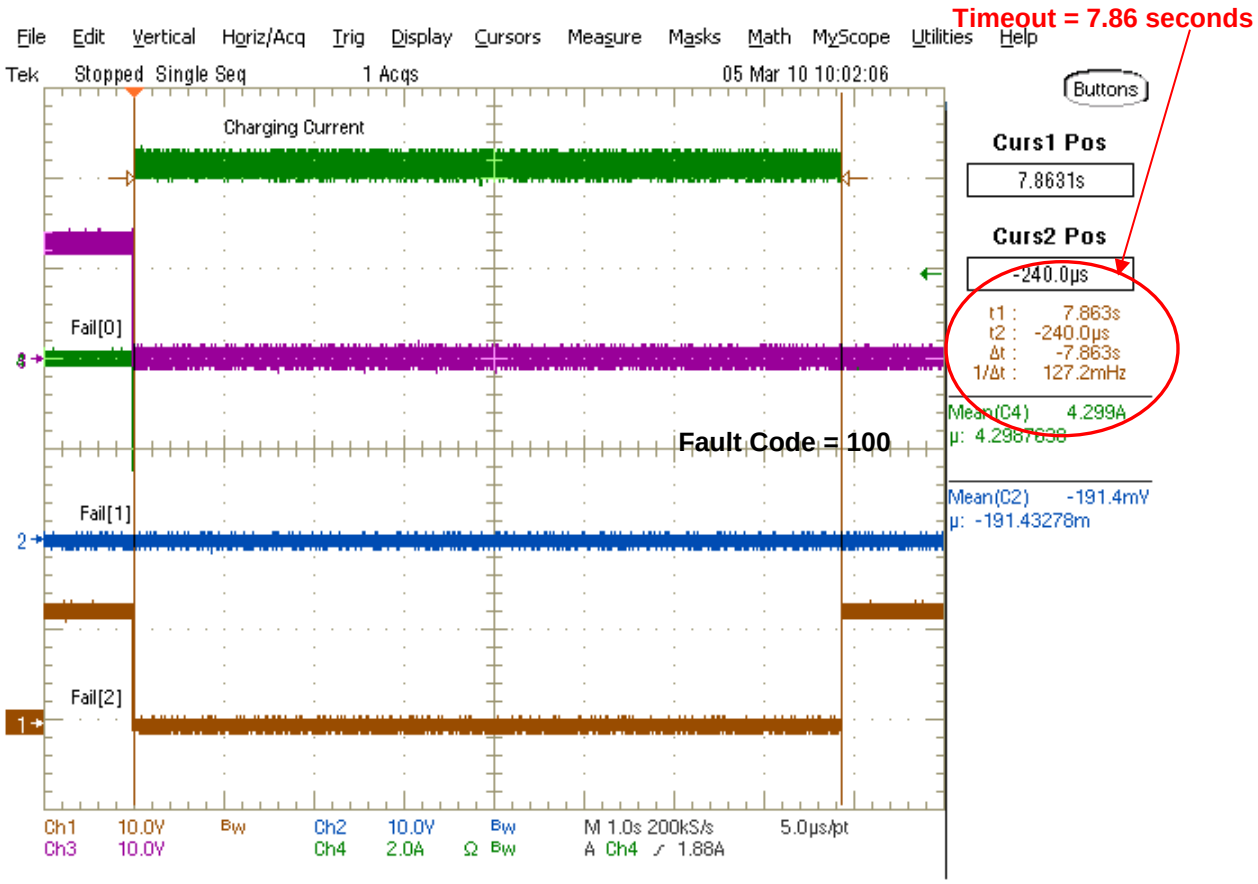
4.3.2 Under–voltage Failure (Open cell while discharging)

To test this failure, the connection to the cell was broken while discharging at 5A. This causes the voltage at the output of the converter to fly down, tripping the under-voltage protection. From the plot, it can be seen that the discharge current drops immediately to zero and the correct fault code (101) is output:



4.3.3 Watchdog Timeout:

To test this failure mode, the board was set up to charge at 5A for 10 seconds. The internal watchdog timer in the EMB1499 was designed for a maximum charge time of 8 seconds. From the scope plot below, it can be seen that the EMB1499 faults out after 7.86 seconds, and outputs the correct fault code (100).



5 Cell Balance Efficiency

5.1 Test Purpose

This test uses a 14-cell battery simulator, with the target cell adjusted to the desired cell voltage and module voltage (all 14-cells) adjusted to the desired cell voltage x 14, while a manual cell transfer is being performed at the desired current.

The current is measured to the cell, and to the module, and the derived power calculations are used to calculate efficiency. To derive the raw converter efficiency, the resistance of the switch matrix (sum of trace resistance to the connector, Rdson of switch matrix FETs) is measured and used to calculate the power loss in the switch matrix, and the board power consumption with all cell balancing circuits active is measured to calculate the power loss in the board overhead circuits.

Using a battery simulator ensures that the cell and module voltage remain stable while current measurements are made. The actual cell and module voltages are also measured and used in the efficiency calculations to ensure the highest accuracy.

5.2 Efficiency Equations

The following equations were used:
eff_conv_charge = 100*(Pcell+Pmatrix) / (Pcell+Pmatrix+Pconv_charge)
eff_conv_discharge = 100*(Pcell-Pmatrix-Pconv_discharge) / (Pcell-Pmatrix)
eff_system_singlecharge = 100*(Pcell) / (Pcell+Pmatrix+Pconv_charge+Pboard)
eff_system_singledischarge = 100*((Pcell-Pmatrix-Pconv_discharge-Pboard)/Pcell)
eff_system_dualcharge = 200*Pcell / (2Pcell + 2Pmatrix + 2Pconv_charge + Pboard)
eff_system_dualdischarge = 200*Pcell / (2Pcell + 2Pmatrix + 2Pconv_discharge + Pboard)
eff_system_chargedischarge = 200*Pcell / (2Pcell + 2Pmatrix + Pconv_charge + Pconv_discharge + Pboard)

where:
Pcell = measured current to/from converter x measured cell voltage
PModule = measured current to/from module x measured module voltage
Pmatrix = measured current to/from cell^2 x switch matrix resistance (82mΩ on EM1400 rev A4)
Pboard = measured current to cell 14 when all cell balancing circuits are active, but no current balancing
Pconv_charge = Pmodule – Pboard – Pmatrix – Pcell
Pconv_discharge = Pcell – Pboard – Pmatrix - Pmodule

14 cell, dual converter efficiency was measured at:

- 42, 46.2, 52.5 and 58.8V module voltage, with 3, 3.3, 3.75 and 4.2V (respectively) cell voltage
- 3, 3.5, 4, 4.5 and 5A cell charge and discharge current

5.3 Hardware Requirements

This test requires a 14-cell Battery Simulator (TI designed and built). For current measurements, a Tektronix TCPA300 Current Probe Amplifier was used with a TCP312 30A DC Current Probe and a Yokogawa DLM2054 Mixed Signal Oscilloscope. An Agilent 34410A 6.5 Digit Multi-meter was used for voltage measurements.

5.4 Cell Balance Efficiency Test Results

The test results below are excerpted from the full test results in file Cheetah_efficiency_RA4_030911.xlsx.

This test was performed on 03/09/2011 by Stephen Holland
All measurements were acceptable and considered a PASS.

Cell Voltage (V)	Charge Current (A)	Converter Efficiency (%)		Board Efficiency (%)				
		Charge	Discharge	Single Charge	Single Discharge	Dual Charge	Dual Discharge	Charge /Discharge
3	5	85.75	82.70	71.53	64.36	73.40	75.61	74.49
3	4.5	85.56	82.17	71.79	64.16	73.90	75.77	74.82
3	4	85.05	81.97	71.71	64.10	74.09	76.04	75.05
3	3.5	84.36	81.01	71.35	63.02	74.04	75.82	74.92
3	3	83.13	80.03	70.36	61.42	73.43	75.45	74.43
3.3	5	86.55	83.51	73.17	66.54	75.00	76.76	75.87
3.3	4.5	86.33	83.66	73.37	66.94	75.42	77.24	76.32
3.3	4	86.03	83.06	73.42	66.50	75.74	77.27	76.50
3.3	3.5	85.31	82.53	72.98	65.82	75.62	77.24	76.42
3.3	3	84.63	81.33	72.39	64.08	75.42	76.73	76.07
3.75	5	87.92	85.60	75.43	70.03	77.27	78.75	78.01
3.75	4.5	87.25	85.19	75.20	69.85	77.24	78.89	78.06
3.75	4	86.70	84.99	74.97	69.68	77.26	79.08	78.16
3.75	3.5	86.24	84.23	74.67	68.71	77.28	78.88	78.07
3.75	3	84.67	82.85	73.29	66.77	76.23	78.19	77.20
4.2	5	87.40	86.41	76.08	72.28	77.79	80.02	78.89
4.2	4.5	87.36	86.01	76.33	72.10	78.24	80.13	79.17
4.2	4	86.48	85.69	75.79	71.77	77.92	80.22	79.06
4.2	3.5	85.66	84.74	75.18	70.64	77.58	79.86	78.71
4.2	3	84.36	83.37	73.99	68.76	76.72	79.14	77.91

6 Hi-Pot

Hi-pot testing verifies the integrity of high-voltage isolation components and PCB layout features in a system to ensure that it is safe to operate. When done properly, this test will expose short circuit conditions or weak components that could compromise electrical safety and create a higher than normal risk of human electrical shock. Again, this test checks only the high voltage DC isolation of a system.

The test method is simple: apply a very high voltage potential (thus the name “hi-pot”) between the two sides of the isolation boundary and monitor the system for excessive current flow. A properly wired and isolated system will have negligible current flow during this test.

The isolation in the EM1400 is required in the communications subsystem as it is required to provide isolated communications to between all modules stacked a large battery pack. The isolation has been designed for 2.5kV.

The Module-to-module balancing subsystem also has the same isolation requirements, but testing of this subsystem is not included in this report as it not a supported product feature.

6.1 Hardware Requirements

This test was performed on a Quadtech Sentry 20 PLUS AC/DC Hi-Pot Tester, with the following programming:

- DC mode
- 2.5kV test voltage
- 2.999mA high current limit
- 60 seconds test time
- 0.015mA Low current limit
- 0.0002mA (0.2uA) arc current limit
- 5 seconds ramp time
- 60 seconds dwell time
- 5 seconds fall time
- In-rush current limit disabled

All pins on one side of U5 (SI8431BB pins 1-8) were connected to one test lead, and all pins on the other side of U5 (SI8431BB pins 9-16) were connected to another test lead. The test leads were then connected to the hi-pot tester inputs. The entire board and test leads were placed in an isolated enclosure with safety interlock attached to the hi-pot tester.

This test was performed on 05/09/2010 by Stephen Holland
All measurements were acceptable and considered a PASS.

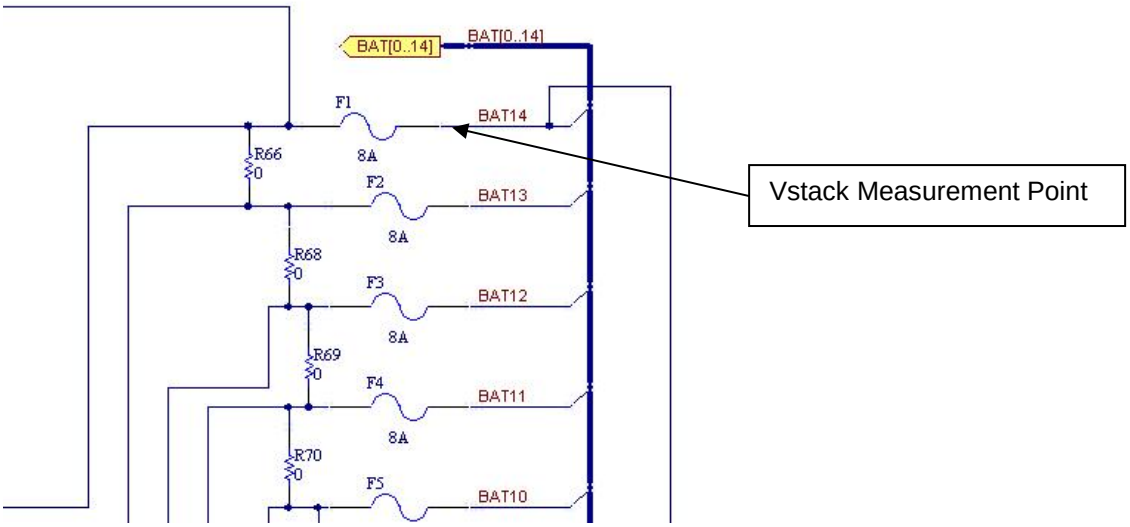
7 System Functional

7.1 Power Consumption Analysis

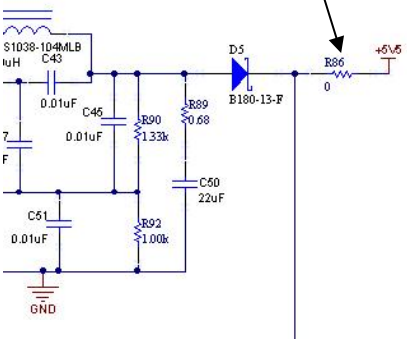
EM1400 rev A4 provides a lot of flexibility in what supplies can be enabled or disabled dynamically to help reduce power consumption. The current consumption of various power supply rails was measured, while the power supply rails were enabled or disabled.

In addition, the overall board current consumption was measured. This represents the total consumption of all housekeeping and external circuits in the EM1400 rev A4 board.

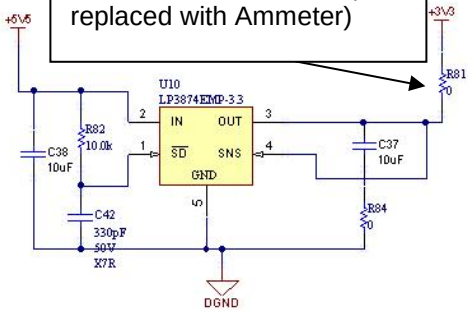
7.1.1 Measurement points

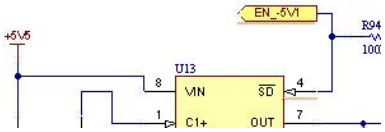


5V5 Measurement (R86 replaced with Ammeter)

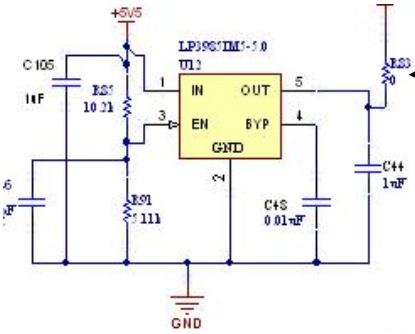


3V3 Measurement (R81 replaced with Ammeter)

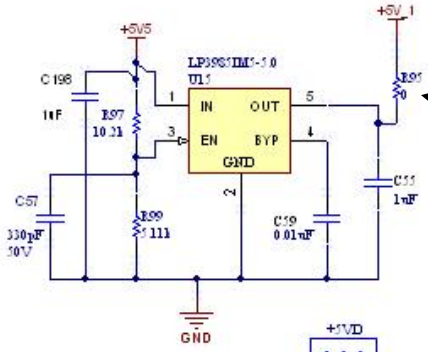




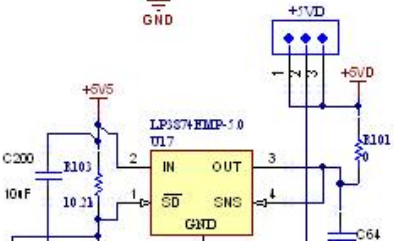
5V_2 Measurement (R83 replaced with Ammeter)

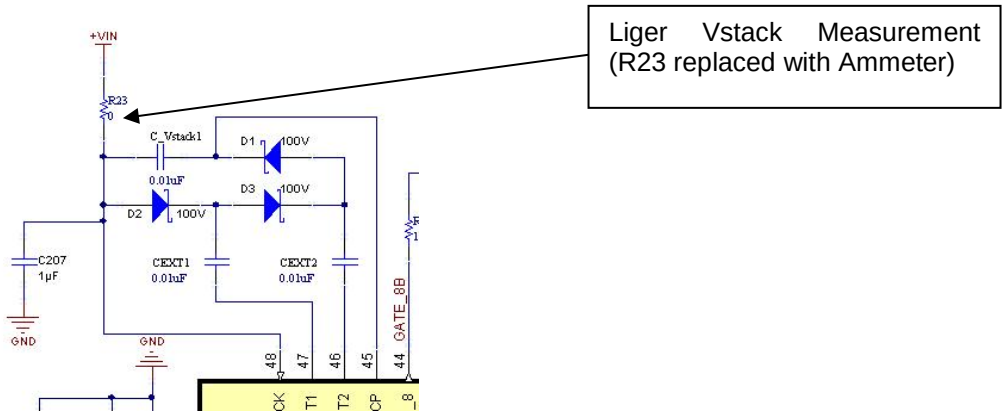


5V_1 Measurement (R95 replaced with Ammeter)



5VD Measurement (R101 replaced with Ammeter)





7.1.2 Power Consumption of Various Rails

The following results were measured with module voltage set at ~56.38V.

This test was performed on 09/03/2010 by Stephen Holland
All measurements were acceptable and considered a PASS.

State	Vstack Current	5V5 Current (at R86)	3V3 Current (at R81)	5VD Current (at R101)	5V_1 Current (at R95)	Liger Vstack Current (at R23)
After Power Up Flyback (U34) enabled	20.9mA	66.6mA	42.5mA	7.35mA	3.56mA	1.45uA
Switcher (U11) on Flyback (U34) disabled -5V1 (U33) off	10.72mA	59.7mA	38.8mA	7.35mA	3.36mA	1.45uA
AFE measurement Switcher (U11) on, Flyback (U34) off, -5V1 (U33) on	10.72 – 12.5mA	60.3 – 63.3mA	38.8 – 40.8mA	7.35mA	3.36 – 3.56mA	-
AFE measurement Switcher (U11) on, Flyback (U34) off, -5V1 (U33) off, AFE Chargepump on				7.6mA	3.61 – 3.64mA	-
ACB enabled (1A)	20.7mA	63.3mA	65.8 – 66.9mA	7.33mA		1.45uA – 1.52mA

7.1.3 Overall Board Current Consumption

The BMS is in idle mode any time active cell balancing is disabled, a manual cell charge transfer is not being performed, or during measurement or relaxation period when active cell balancing is enabled.

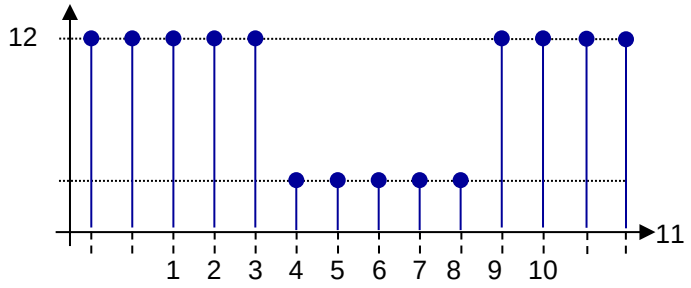
This test was performed on 03/09/2011 by Stephen Holland
All measurements were acceptable and considered a PASS.

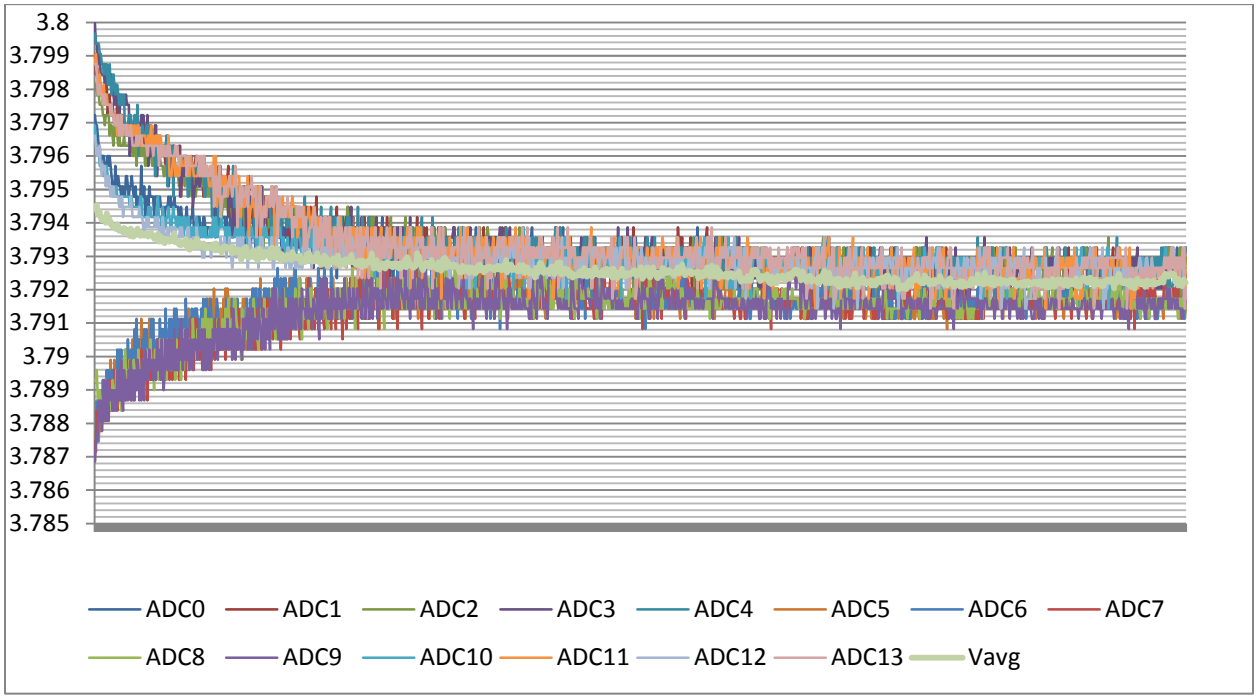
Module Voltage		Board current (active mode)
42V		25.69mA
46.2V		22.2mA
52.5V		22.73mA
58.8V		20.75mA

7.2 Stack tests

The following stack tests were performed with 5 modules (14s4p A123, unless otherwise stated) stacked, with and without charge/load on ABC150:

- Communications
  - Tested by Zane Zhu on 10/13/2010
  - PASS
- AFE operation
  - Tested by Zane Zhu on 10/13/2010
  - No ABC150 load
  - Multiple broadcast and discrete commands sent
  - PASS
- ACB operation
  - Test #1
    - Tested by Zane Zhu on 10/13/2010
    - No ABC150 load
    - ACB CAN Hacker script (20sec on, 10sec off)
    - PASS
  - Test #2
    - Tested by Zane Zhu on 10/13/2010
    - No ABC150 load
    - Multiple broadcast and discrete ACB commands sent
    - PASS
  - Test #3
    - Tested by Zane Zhu on 10/13/2010
    - ABC150 load enabled (profile is cycle of -2A (50sec), +5A(60sec), -10A(30sec), +20A(30sec), -50A(10sec), +20A(10sec)
    - ACB CAN Hacker script (20sec on, 10sec off)
    - Run for 48hrs
    - PASS
  - Test #4
    - Tested by Stephen Holland on 4/06/2010
    - ACB enabled from BMSView GUI
    - Cell balance threshold = 2mV
    - Cell hysteresis threshold = 5mV
    - Sanyo LiNiCoMn 2.5Ah 14s4p (10Ah)
    - Pattern (as shown below)
    - Run until balanced
    - PASS





8 Module-to-Module Balance (MMB)

Module-to-Module balancing testing was performed but is not included in this report as it not a supported product feature.

9 Revision History

This section records a brief summary of changes to each revision of this document.

Revision	Date	Author	Description of Changes from Previous Revision
0.1	01/04/2012	Stephen Holland	First release
1.0	01/05/2012	Stephen Holland	Added additional test information
1.1	05/22/2014	Stephen Holland	Removed NDA restriction

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

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