设计指南：TIDA-010038
峰值效率达到 94% 且采用 CC/CV 的 150W 标称值、240W 峰值工业交流/直流电源参考设计

说明

该参考设计是用于工业交流/直流电源的紧凑型、高效率、24V 直流、150W 标称值、240W 峰值输出（230VAC 时）参考设计。该电路包括基于 UCC28056 的前端转换模式 (TrM) 功率因数校正 (PFC) 电路，后跟基于 UCC256301、用于隔离式直流/直流转换器的强劲 LLC 级。为满足高效率的需求，同步整流可与 UCC24624 兼容。此设计无需额外的辅助电源即可实现无负载消耗。该设计可实现 94% 的峰值效率，并能让系统在没有强制冷却的情况下工作。该设计具备恒定电流 (CC) 和恒定电压 (CV) 反馈环路，适用于电池充电应用。

资源

TIDA-010038	设计文件夹
UCC28056	产品文件夹
UCC256301	产品文件夹
UCC24624	产品文件夹
TL103WA	产品文件夹
CSD19533Q5A	产品文件夹

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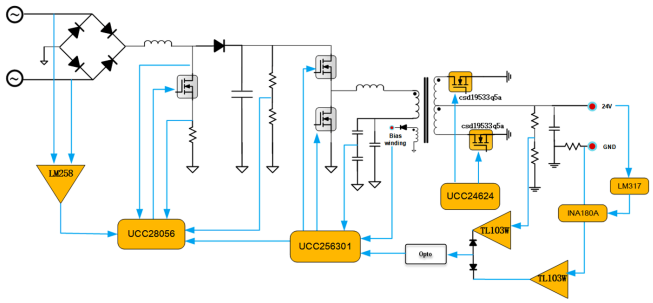
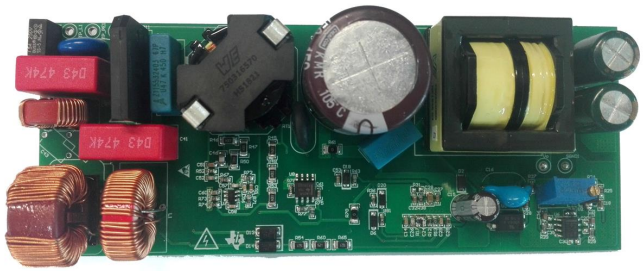
特性

- 90V 至 265V 交流的宽工作输入电压范围，可在整个范围内实现全功率
- 230V 交流时峰值总体效率为 94.4%，115V 交流时为 93%，可实现自然对流冷却
- 提供高达 6.25A 的持续电流和 3 秒高达 10A 的峰值电流
- 可调节输出电压范围为 22V 至 28V
- 无负载功耗极低，小于 400mW
- 针对过流、短路和过压故障的系统保护可确保满足安全需求
- 具备恒压和恒流反馈环路

应用

- 工业交流/直流电源
- DIN 轨电源
- 电池充电器





1 System Description

Industrial AC/DC power supplies are used in various applications such as process control, data logging, machinery control, instrumentation, factory automation, and security systems. These AC/DC supplies provide a convenient means for powering DC-operated devices including programmable logic controllers (PLCs), sensors, transmitters and receivers, analyzers, motors, actuators, solenoids, relays, and so forth. These supplies are convection cooled and need to support features like power boost, where it supplies an increased output load for a short duration. The supplies operate over a wide input range from 85- to 265-V AC, delivering full load for entire input voltage range. The output voltages from these supplies range from 5 to 56 V with power ratings from 7.5 to 480 W. Many of these supplies can be connected in parallel for higher power applications.

This reference design is a high-efficiency, 150-W AC/DC converter. The circuit consists of a front-end transition mode (TrM) power factor correction (PFC) circuit, followed by an LLC-based isolated DC/DC power stage. The design uses the UCC28056 controller for the PFC stage and the UCC256301 controller for LLC stage to achieve a compact and robust control structure. Synchronous rectification based on the UCC24624 and low RDS(on) FETs CSD19533 from Texas Instruments help in achieving higher efficiencies.

The converter is designed for a wide input voltage range of 85-V to 265-V AC with full power delivery over the entire range and single DC outputs of 24 V, which have a peak power output of 240 W, delivering a maximum current of 10 A at 230-V AC. The design has an operating peak efficiency of approximately 94.4% with 230-V AC and 93% with 115-V AC at full load. The design has a high power factor of greater than 0.94 at 230-V AC from a 50% to 100% load. The design form factor (55 mm × 140 mm) is compact for the power level of 150 W. The system also has some robust protections built in (OVP and OCP), which make the converter more secure and reliable. The EMI filter is designed to meet EN 55022 class-B conducted emission levels.

The design meets low standby power of 500 mW without needing additional auxiliary power. This reference design is fully tested and validated for various parameters such as regulation, efficiency, EMI signature, output ripple, startup, and switching stresses. Overall, the design meets the key challenges of industrial power supplies to provide safe and reliable power with all protections built in, while delivering high performance with low power consumption and low bill of material (BOM) cost.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Input voltage		85	230	265	VAC
Frequency		47	50	63	Hz
No load power				500	mW
OUTPUT CONDITIONS					
Output voltage		22	24	28	V
Output current	VO = 24-V		6.25	10	A
Line regulation	VO = 24-V			0.3	%
Load regulation	VO = 24-V			0.5	%
Output voltage ripple	VO = 24-V, Peak-Peak			240	mV

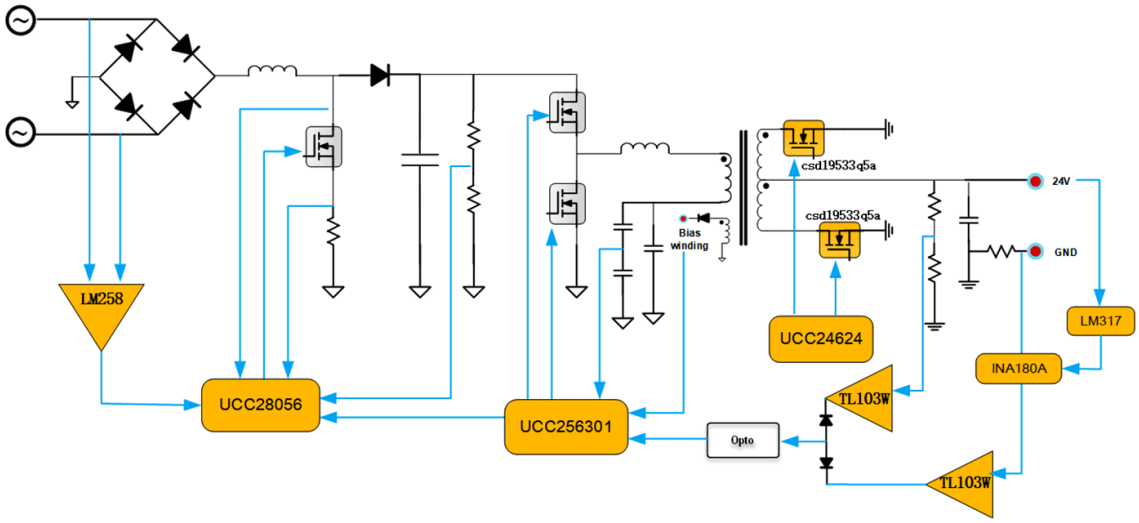
表 **1. Key System Specifications (continued)**

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Output power (nominal)				150	W
Output power (power boost)	Vin = 230-V AC RM, Vo=24-V			240	W
SYSTEM CHARACTERISTICS					
Efficiency	Vin = 230-V AC RMS and full load at 24-V output		94		%
	Vin = 115-V AC RMS and full load at 24-V output		92.5		%
Power factor	Vin = 230-V AC RMS and full load at 24-V output		0.98		
	Vin = 115-V AC RMS and full load at 24-V output		0.99		
Protections	Output overcurrent				
	Output overvoltage				
	Output undervoltage				
Operating ambient	Open frame	-10	25	55	°C
Standards and norms	Power line harmonics (THD)	IEC 61000-3-2 Class A			
	Conducted emissions	EN 55022 Class B			
	EFT	As per IEC 61000-4-4			
	Surge	As per IEC 61000-4-5			
Board form factor (FR4 material, 2 layer)	Length × Breadth × Height	140 × 55 × 30			mm

2 System Overview

2.1 Block Diagram

图 1. TIDA-010038 Block Diagram



2.2 Highlighted Products

The following highlighted products are used in this reference design. These sections also highlight the key features for selecting the devices for this reference design. For the complete details of these highlighted devices, see the respective product data sheet.

2.2.1 UCC28056

The UCC28056 is a high-performance, small-size, 6-pin, fully featured PFC controller offering excellent light load efficiency and standby power. The UCC28056 controller simplifies the design of a PSU, requiring good power factor that must also be capable of meeting modern tough standards for efficiency and standby power. At a full load, the UCC28056 operates the PFC power stage at maximum switching frequency in TrM. At a reduced load, the part transitions seamlessly into discontinuous conduction mode (DCM), automatically reducing switching frequency for maximum efficiency. At a light load, DCM operation is combined with burst mode operation to further improve light load efficiency and standby power. The UCC28056 integrates all the features necessary to implement a high performance and robust PFC stage into a 6-pin package and requires a minimal number of external components to interface with the power stage. This device maximizes the BOM savings by eliminating need of aux winding.

Key specifications for this device include:

- Innovative DCM control law to prevent valley jumping
- Superior no-load and light-load efficiency
- Robust protection: Fast response second OVP on a dedicated pin
- Soft-start and soft recovery after OVP
- Input voltage brownout detection
- Eliminates need of aux winding

• Innovative DCM control law to prevent valley jumping

• Strong drive capability: –1.0 A and +0.8 A This controller is a companion device to be used with the UCC256301 LLC controller to achieve the best no-load standby power performance.

2.2.2 UCC256301

LLC resonant converter is one of the most widely used topologies for implementing medium to high power, isolated, DC/DC power stages in industrial power supplies. These converters are popular due to their ability to achieve soft-switching (ZVS turn on) for the high-voltage MOSFET and hence improving the overall efficiency of the system. LLC converters in industrial power supplies do face some specific requirements. Some industrial power supplies need to support an over load (up to 1.6 times the nominal load) for a short period of time. Ensure that the LLC converter does not enter capacitive (ZCS) region during the overload operation; otherwise, it can be catastrophic. The UCC256301 with its ZCS avoidance feature can ensure that the system does not enter the ZCS region under all operating conditions and hence ensures the safety of the system. Apart from the overload (also known as power boost) functionality, industrial power supplies typically need a tunable output voltage with a wide range. For example, for a 24-V nominal output voltage, this can range from 22 V to 28 V. The UCC256301 provides a wide operating frequency range from 35 kHz to 1MHz to make it easier to design wide output voltage range using an LLC converter. With its unique hybrid hysteretic control, the UCC256301 provides excellent line and load transient response, minimizing the need for output filter capacitors. Its wide frequency range can reduce the PFC bulk capacitor required to meet the holdup time requirement in the industrial power supplies. With the integrated high-voltage gate drive, X-Cap discharge function, and additional output OVP, the UCC256301 reduces the amount of external discreet components required to implement a high efficiency industrial PSU.

2.2.3 UCC24624

The UCC24624 high-performance synchronous rectifier (SR) controller is dedicated for LLC resonant converters to replace the lossy diode output rectifiers with SR MOSFETs and improve the overall system efficiency. Two independent SR control channels are integrated into the single package to minimize the external components and allow for easy PCB layout.

The UCC24624 SR controller uses drain-to-source voltage sensing method to achieve on and off control of the SR MOSFET. Proportional gate drive is implemented to extend the SR conduction time, minimize the body diode conduction time and improve efficiency. To compensate for the offset voltage caused by the SR parasitic inductance, the UCC24624 implements an adjustable positive turn-off threshold to accommodate different SR MOSFET packages. UCC24624 has a built-in 450-ns minimum on-time blanking and a fixed 650-ns minimum off-time blanking to avoid SR false turn-on and -off. UCC24624 also integrates a two-channel interlock function that prevents the two SRs from being on at the same time.

With the built-in standby mode detection based on average switching frequency, UCC24624 enters the sleep mode automatically without using external components. The low standby mode current of 175 μA supports meeting modern no-load standby power requirements such as CoC, and DoE regulations.

With 1.5-A peak source and 4-A peak sink driving capability, UCC24624 is able to support LLC converters up to 1-kW. With 230-V voltage-sensing pins and 26-V maximum VDD rating, it can be directly used in converters with output voltage up to 26 V. The internal clamp allows the controller to support 36-V output voltage easily by adding an external current limiting resistor on VDD.

UCC24624 can be used with the UCC25630x LLC and UCC28056 PFC controllers to achieve high efficiency while maintaining excellent light load and no-load performances.

2.2.4 CSD19533Q5A

To achieve high-efficiency synchronous rectification, TI's power MOSFET CSD19533Q5A has been employed in this reference design. The CSD19533 is 100-V NexFET™ power MOSFET device available in SON5x6 package. Its ultra-low resistance minimizes conduction losses, while its ultra-low Qrr minimize reverse recovery losses in this high frequency system.

Key specifications for this device include:

- Drain-to-Source on resistance at 10 V : 7.8 mΩ
- Gate charge total at 10 V (Qg): 27 nC
- SON 5-mm x 6-mm Plastic Package

2.2.5 TL103W

The TL103W and TL103WA combine the building blocks of a dual operational amplifier and a fixed voltage reference – both of which often are used in the control circuitry of both switch-mode and linear power supplies. OP AMP1 has its noninverting input internally tied to a fixed 2.5-V reference, while OP AMP2 is independent, with both inputs uncommitted.

For the A grade, especially tight voltage regulation can be achieved through low offset voltages for both operational amplifiers (typically 0.5 mV) and tight tolerances for the voltage reference (0.4% at 25°C and 0.8% over operating temperature range).

2.3 System Design Theory

This reference design provides universal AC mains powered 150-W output at 24 V and 6.25 A. The UCC28056 controls a PFC boost front end, while the UCC256301 LLC resonant-half bridge converts the PFC output to isolated 24 V. The total system efficiency is 94% with a 230-V AC input and over 92.5% with a 110-V AC input at full load. In addition, several protections are embedded into this design which includes output over protection, output over current protection and over temperature protection. Low EMI, high efficiency, high power factor, and reliable power supply are main focus of this reference design for targeted applications.

2.3.1 PFC Stage Design

PFC circuit shapes the input current of the power supply to maximize the real power available from the mains. In addition, it is important to have the PFC circuit comply with low total harmonic distortion (THD) regulatory requirements. Currently, two modes of operation have been widely used to implement PFC. For higher power circuits greater than 300 W, the topology of choice is the boost converter operating in continuous conduction mode (CCM) and with average current mode control. For lower power applications less than 250 W, typically the Transition Mode (TrM) or Critical Conduction Mode (CrCM) boost topology is used. For low power levels, such as 150 W, TI recommends using TrM operation as it offers inherent zero-current switching of the boost diodes (no reverse-recovery losses), which permits the use of less

expensive diodes without sacrificing efficiency. In addition, variable frequency operation results in distributed EMI spectrum and low emissions. The design process and component selection for this design are illustrated in the following sections. To make the designing easier, use the Excel® design calculator in the product folder of this reference design. The design can also be simulated and designed in WEBENCH®.

2.3.1.1 Circuit Parameters Design

表 2. Design Parameters for PFC Stage

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
INPUT					
Input voltage	V_{AC}	85	230	265	VAC
Input frequency	f_{LINE}	47	50	63	Hz
Power factor	PF		0.98	0.99	
Hold up time	t_{holdup}			16	ms
OUTPUT					
Output voltage	V_O		400		VDC
Output power	P_{DCBUS}		150		W
Line regulation				5	%
Load regulation				5	%
Minimum switching frequency	f_{SW}	56			kHz
Targeted efficiency	η_{PFC}	95	97		%

2.3.1.2 Current Calculation

The input fuse and bridge rectifier are selected based upon the input current calculations. The boost voltage is designed to regulate at 400-V DC for an input AC voltage range of 85-V to 265-V AC operation. The boost PFC converter is designed for output power of 156 W, considering the downstream DC/DC converter operating at more than 95% efficiency.

Determine the maximum input power (P_{IN}) averaged over the AC line period using 公式 1:

$$P_{IN} = \frac{P_{DCBUS}}{\eta_{PFC}} = \frac{156W}{0.95} = 164.2W \quad (1)$$

Determine the maximum RMS input current ($I_{IN\_RMS\_max}$) using 公式 2:

$$I_{INS\_RMS\_max} = \frac{P_{IN}}{V_{IN\_min} \times PF} = \frac{164.2W}{85V\,AC \times 0.99} = 1.951A \quad (2)$$

Determine the maximum input current (I_{IN_max}) and the maximum average input current ($I_{IN\_AVG\_max}$) based upon the calculated RMS value, assuming the waveform is sinusoidal using 公式 3 and 公式 4, respectively:

$$I_{IN\_max} = \sqrt{2} \times I_{IN\_RMS\_max} = \sqrt{2} \times 1.951A = 2.76 \quad (3)$$

$$I_{IN\_AVG\_max} = \frac{2}{\pi} \times I_{IN\_max} = \frac{2}{\pi} \times 2.76A = 1.757A \quad (4)$$

Determine the maximum average output current (I_{DCBUS_max}) using 公式 5:

$$I_{DCBUS\_max} = \frac{P_{DCBUS}}{V_{DCBUS(mix)}} = \frac{156W}{400V} = 0.39A \quad (5)$$

2.3.1.3 Bridge Rectifier

The maximum input AC voltage is 265-V AC, so the DC voltage can reach voltage levels of up to 375-V DC. Considering a safety factor of 30%, select a component with voltage rating greater than 500-V DC. The input bridge rectifier must have an average current capability that exceeds the input average current ($I_{IN\_AVG\_max}$). To optimize the power loss due to diode forward voltage drop, a higher current bridge rectifier is recommended. This reference design uses the 600-V, 6-A diode GBU6J for input rectification.

2.3.1.4 Boost Inductor Design

For a detailed list of equations, see the Boost Inductor Design section of the UCC28056 6-Pin Single-Phase Transition-Mode PFC Controller data sheet.

For the boost inductance value required to ensure that the maximum load can be delivered from the minimum line voltage, use 公式 6:

$$L_{PFCO} = \frac{V_{LIN\_RMS\_mix}^2}{110\% \times P_{DCBUS}} \times \frac{T_{ONMAX0}}{2} = 269.46uH \tag{6}$$

According to the UCC28056 6-Pin Single-Phase Transition-Mode PFC Controller data sheet, the PFC inductor value will limit the maximum output power. To realize the power boost function, PFC needs a smaller inductor. 公式 7 shows the 200-uH PFC inductor which can realize 240-W peak output power at 230-V AC and 196-W peak output power at 115-V AC.

$$L_{PFC} = 200uH \tag{7}$$

Once the PFC inductor is chosen, the peak current at minimum input voltage can be calculated using 公式 8:

$$I_{LPK\_max} = \frac{V_{LIN\_RMS\_min} \times \sqrt{2} \times T_{ONMAX0}}{L_{PFC}} = 7.693A \tag{8}$$

The maximum current in the power components will flow while delivering maximum load when supplied from minimum Line voltage. In this condition, the UCC28056 operates in transition mode (TrM). The maximum RMS current of the boost inductor occurs at the minimum line voltage and maximum input power.

$$I_{LRMS\_max} = \frac{I_{LPK\_max}}{\sqrt{6}} = 3.141A \tag{9}$$

2.3.1.5 Boost Switch Selection

The maximum RMS current in the switch occurs at the maximum load and minimum line.

$$I_{MOS\_RMS\_max} = \frac{110\% \times P_{DCBUS}}{V_{LIN\_RMS\_min}} \times \sqrt{\frac{4}{3} - \frac{32 \times \sqrt{2} \times V_{LIN\_RMS\_min}}{9 \times \pi \times V_O}} = 2.012A \tag{10}$$

Select a MOSFET for the boost switch on the following basis:

- The voltage rating must be greater than the maximum output voltage. Under transient or line surge testing, the output voltage can rise well above its normal regulation level. For this design example, a MOSFET voltage rating of 600 V is chosen to support a regulated output voltage of 390 V.
- Based upon an acceptable level of conduction loss in the MOSFET, the R_{DSON} value required can be calculated from the maximum RMS current.

• For best efficiency, use a MOSFET that incorporates a fast body diode. Operating with a discontinuous inductor current (DCM) from a low input voltage incurs an additional switching power loss if a MOSFET with slow body diode is used.

2.3.1.6 Boost Diode Selection

The maximum RMS current in the boost diode occurs at the maximum load and minimum line.

$$I_{Dio\_RMS\_max} = \frac{4}{3} \times \frac{110\% \times P_{DCBUS}}{V_{LIN\_RMS\_min}} \times \sqrt{\frac{2 \times \sqrt{2}}{\pi} \times \frac{V_{LIN\_RMS\_min}}{V_O}} = 1.177A \quad (11)$$

Conduction power loss in the boost diode is primarily a function of the average output current.

$$I_{Dio\_AVG\_max} = \frac{P_{DCBUS}}{V_O} = 0.39A \quad (12)$$

Select a boost diode on the following basis:

• The boost diode requires the same voltage rating as the boost MOSFET switch.

• The boost diode must have average and RMS current ratings that are higher than the numbers calculated in 公式 11 and 公式 12.

• Diodes are available with a range of different speed and recovery charge. With a low reverse recovery charge, fast diodes typically have a higher forward voltage drop. Therefore, fast diodes have a higher conduction loss but lower switching loss. With high reverse recovery charge, slow diodes typically have a lower forward voltage drop. Therefore, slow diodes have a lower conduction loss but higher switching loss. Maximum efficiency is achieved when the diode speed rating matches the application.

This reference design uses the STTH5L06B diode from ST. This diode has a voltage rating of 600 V and an average current rating of 5 A. The STTH5L06B diode has a forward voltage drop of around 1.05 V.

2.3.1.7 Output Capacitor Selection

The hold-up time is the main requirement in determining the output capacitance. ESR and the maximum RMS ripple current rating can also be important, especially at higher power levels. The holdup time is 16 ms. The holdup voltage is considered as 340 V for continuous operation of the downstream DC/DC converter.

$$C_{OUT\_min} \geq \frac{2 \times P_{DCBUS} \times t_{holdup}}{V_O^2 - V_{holdup}^2} = 112.4uF \quad (13)$$

Considering the 20% tolerance, the actual value used in this reference design is 150 μF.

Use 公式 14 to calculate the maximum RMS ripple current flowing in the output capacitor.

$$I_{COUT\_RMS\_max} = \sqrt{I_{Dio\_RMS\_max}^2 - \left(\frac{P_{DCBUS}}{V_O}\right)^2} = 1.111A \quad (14)$$

2.3.1.8 Output Voltage Set Point

Select the divider ratio of R_{FBtop} and $R_{FBbottom}$ to set the V_{REF} voltage to 2.5 V at the desired output voltage. The current through the divider is reduced to a minimum to keep the no load power loss as small as possible. Consider the pullup resistor R_{FBtop} to be 9.9 MΩ. Using the internal 2.5-V reference (V_{REF}), the bottom divider resistor ($R_{FBbottom}$) is selected to meet the design goals of the output voltage.

$$R_{FBbottom} = \frac{V_{REF} \times R_{FBtop}}{V_O - V_{REF}} = 62.3k\Omega \quad (15)$$

A 120-kΩ resistor and a 130-kΩ resistor are paralleled for $R_{FBbottom}$ which results in a nominal output voltage set point of 399 V.

A small capacitor on the VOSNS pin must be added to filter out noise. Limit the value of the filter capacitor such that the RC time constant is limited to approximately 100 μs so as not to significantly reduce the control response time to output voltage deviations.

$$C_{VOSNS} = \frac{150us}{R_{FBbottom}} = 2402pF \quad (16)$$

The closest standard value of 2200 pF is used on the VOSNS pin.

2.3.2 LLC Stage Design

The DC/DC stage in an industrial AC/DC converter needs to support a wide output voltage range and a hold up time greater than 20 ms. Combined with the need to meet the short time power boost feature, the LLC-based DC/DC stage needs to be designed with sufficient gain and proper operating point to maximize efficiency.

Because this DC/DC stage supports a nominal output power of 150 W and a peak output power of 240 W, designing the DC/DC stage for 240-W operation does not give an optimum performance at 150 W. While designing for 150 W, take care in dimensioning the resonant tank components such that the system does not enter into the capacitive region of operation at 240 W.

The hybrid hysteretic mode control and ZCS avoidance of the UCC256301 helps in developing a robust LLC power stage for use in these applications.

2.3.2.1 Circuit Parameters Design

表 **3. Design Parameters for LLC Stage**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
INPUT					
Input voltage	V_{INDC}	340	396	410	VDC
OUTPUT					
Output voltage	V_{OUT}	22	24	28	VDC
Output power limit	P_{OUT_Max}			240	W
Max output power	P_{OUT}		150		W
Nominal switching frequency	f_{SWNOM}		150		kHz
Line regulation				0.3	%
Load regulation				0.5	%
Targeted efficiency			97		%

2.3.2.2 Determine Mg

The transformer turns ratio is determined by 公式 17:

$$n = \frac{\frac{V_{DCIN\_nom}}{2}}{V_{OUT}} \quad (17)$$

From the specifications, the nominal values for input voltage and output voltage are 396 V and 24 V, respectively, so the turns ratio can be calculated as:

$$n = \frac{\frac{396}{2}}{24} = 8.25 \tag{18}$$

No additional diode drop needs to be accounted for because a synchronous rectifier is used. The value used for turns ratio (n) for further calculations is 8.5.

2.3.2.3 LLC Gain Range Mg_{min} and Mg_{max}

Mg_{min} and Mg_{max} can be determined by using 公式 19 and 公式 20, respectively:

$$M_{g\_min} = n \times \left(\frac{V_{OUT\_min}}{\frac{V_{DCIN\_max}}{2}} \right) = 8.5 \times \left(\frac{24V}{\frac{410V}{2}} \right) = 0.995 \tag{19}$$

$$M_{g\_max} = n \times \left(\frac{V_{OUT\_max}}{\frac{V_{DCIN\_min}}{2}} \right) = 8.5 \times \left(\frac{24V}{\frac{340V}{2}} \right) = 1.2 \tag{20}$$

2.3.2.4 Determine Equivalent Load Resistance (R_E) of Resonant Network

To determine the equivalent load resistance at nominal and peak load under nominal output voltage and peak output voltage, use 公式 21:

$$R_E = \frac{8 \times n^2}{\pi^2} \times \left(\frac{V_{OUT_{nom}}}{I_{OUT_{nom}}} \right) = \frac{8 \times 8.5^2}{\pi^2} \times \left(\frac{24}{6.25} \right) = 224.9\Omega \tag{21}$$

2.3.2.5 Select L_M/L_R Ratio (L_N) and Q_E

L_N is the ratio between the magnetizing inductance and the resonant inductance.

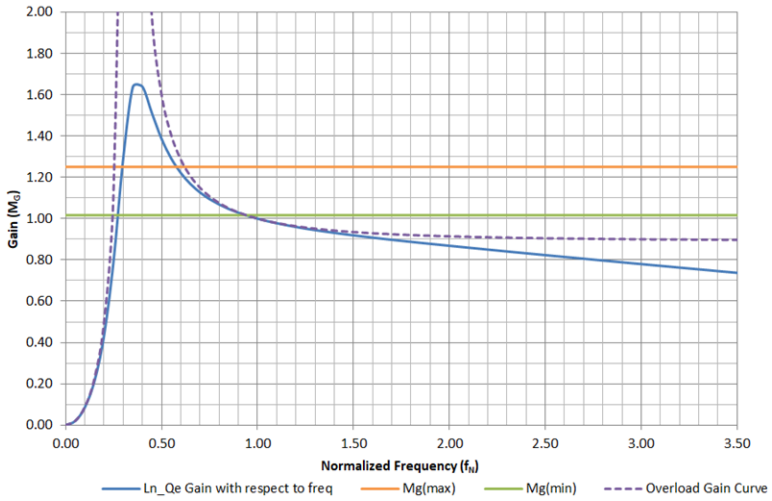
$$L_N = \frac{L_M}{L_R} \tag{22}$$

Q_E is the quality factor of the resonant tank.

$$Q_E = \frac{\sqrt{\frac{L_R}{C_R}}}{R_E} \tag{23}$$

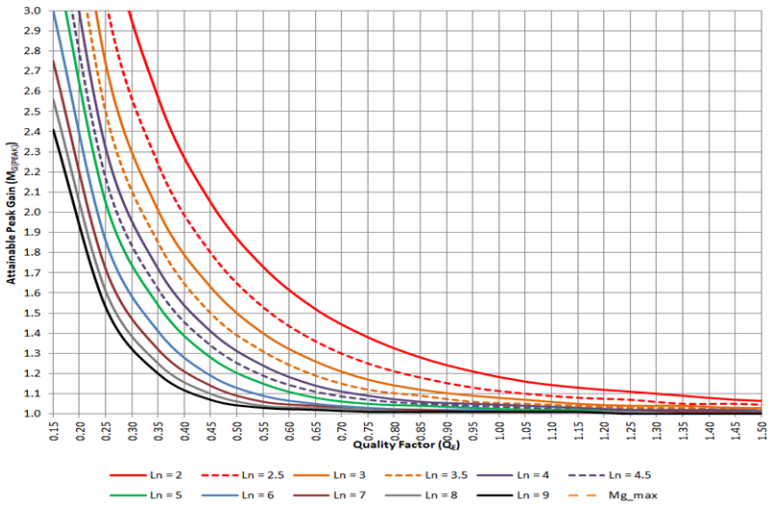
Selecting L_N and Q_E values must result in an LLC gain curve, as shown in 图 2, that intersects with $M_{G(min)}$ and $M_{G(max)}$ traces. The peak gain of the resulting curve must be larger than $M_{G(max)}$.

图 2. LLC Gain Curve for Selected L_N and Q_E



The relationship between $M_{G(peak)}$ and Q_E with respect to L_N is shown in 图 3:

图 3. $M_{G(peak)}$ and Q_E With Respect to L_N



L_N = 8

Q_E = 0.24

Use the spreadsheet to get optimized values of L_N and Q_E.

2.3.2.6 Switching Frequency

The wide switching frequency of the UCC256301 is from 35 kHz to 1 MHz, which makes this reference design more flexible. To make the transformer and inductor with a smaller size and LLC converter, work under resonant frequency with a 24-V DC output at full load. The second resonant frequency is chosen to be 150 kHz.

$f_0 = 150kHz$ (24)

2.3.2.7 Determine Component Parameters for LLC Resonant Circuit

The resonant tank parameters can be calculated using the following equations:

$$C_R = \frac{1}{2\pi \times Q_E \times f_0 \times R_E} = \frac{1}{2 \times 0.24 \times 150kHz \times 224.9\Omega} = 0.02uF \quad (25)$$

$$L_R = \frac{1}{(2\pi \times f_0)^2 \times C_R} = \frac{1}{(2\pi \times 150kHz)^2 \times 0.02uF} = 56.3uH \quad (26)$$

$$L_M = L_N \times L_R = 8 \times 56.3uH = 450uH \quad (27)$$

After the preliminary parameters are selected, find the closest actual component value that is available, recheck the gain curve with the selected parameters, and then run the time domain simulation to verify the circuit operation. This results in the following resonant tank parameters:

$$C_R = 0.022uF \quad (28)$$

$$L_R = 51uH \quad (29)$$

$$L_M = 480uH \quad (30)$$

Based on the final resonant tank parameters, the resonant frequency can be calculated as follows:

$$f_0 = \frac{1}{2\pi \times \sqrt{C_R \times L_R}} = \frac{1}{2\pi \times \sqrt{0.022uF \times 51uH}} = 15.03kHz \quad (31)$$

2.3.2.8 LLC Primary Side Currents

The primary-side RMS load current (I_{pri}) with at full load is determined using 公式 32:

$$I_{pri} = \frac{\pi}{2\sqrt{2}} \times \frac{I_O}{n} = \frac{\pi}{2\sqrt{2}} \times \frac{1.1 \times 6.25A}{8.5} = 0.898A \quad (32)$$

The RMS magnetizing current (I_m) at $f_{SW(min)}$ = 82.6 kHz is determined using 公式 33:

$$I_m = \frac{2\sqrt{2}}{\pi} \times \frac{n \times V_{OUT}}{2\pi \times f_{SW(min)} \times L_M} = \frac{2\sqrt{2}}{\pi} \times \frac{8.5 \times 24V}{2\pi \times 82.6kHz \times 408uH} = 0.867A \quad (33)$$

The current of the resonant circuit (I_r) is determined using 公式 34:

$$I_r = \sqrt{I_m{}^2 + I_{pri}{}^2} = \sqrt{0.867A^2 + 0.898A^2} = 1.248A \quad (34)$$

This is also the transformer's primary winding current at $f_{SW(min)}$.

2.3.2.9 LLC Secondary Side Currents

The total secondary-side RMS load current is the current referred from the primary-side current (I_{pri}) to the secondary side.

$$I_{sec} = n \times I_{pri} = 8.5 \times 0.898A = 7.633A \quad (35)$$

Because the transformer's secondary side has a center-tapped configuration, this current is split equally into two transformer windings on the secondary side. The current of each winding is then calculated using 公式 36:

$$I_{SW} = \frac{\sqrt{2} \times I_{sec}}{2} = \frac{\sqrt{2} \times 7.633A}{2} = 5.397A \quad (36)$$

The corresponding half-wave average current is:

$$I_{savg} = \frac{\sqrt{2} \times I_{sec}}{\pi} = \frac{\sqrt{2} \times 7.633A}{\pi} = 3.436A \quad (37)$$

2.3.2.10 Select the Transformer

The transformer can be built or purchased from a catalog. The specifications for this example are as follows:

- Turns ratio (n): 8.5
- Primary terminal voltage: 450-V AC
- Primary magnetizing inductance: L_m = 408 µH
- Primary winding's rated current, I_{wp} = 1.248 A
- Secondary terminal voltage: 24-V AC
- Secondary winding's rated current, I_{ws} = 5.4 A (center-tapped configuration)
- Minimum switching frequency: 82.6 kHz
- Maximum switching frequency: 158 kHz
- Insulation between primary and secondary sides: IEC 60950 reinforced insulation

2.3.2.11 Select the Resonant Inductor

The inductor can be built or purchased from a catalog with these specifications:

- Series resonant inductance, L_r = 51 µH
- Rated current, I_{Lr} = 1.412 A
- Terminal AC voltage: 48.84 V

$$V_{Lr} = \omega \times L_R \times I_r = 2\pi \times 82.6\text{kHz} \times 51\mu\text{H} \times 1.248\text{A} = 33.03\text{V} \quad (38)$$

2.3.2.12 Select the Resonant Capacitor

This capacitor carries the full-primary current at a high frequency. A low dissipation factor part is needed to prevent overheating in the part.

The AC voltage across the resonant capacitor is given by its impedance times the current.

$$V_{CR} = \frac{I_r}{\omega \times C_R} = \frac{1.248\text{A}}{2\pi \times 82.6\text{kHz} \times 0.022\text{uF}} = 109.3\text{V} \quad (39)$$

$$V_{CR(rms)} = \sqrt{\left(\frac{V_{IN(max)}}{2}\right)^2 + V_{CR}{}^2} = \sqrt{\left(\frac{410\text{V}}{2}\right)^2 + 109.3\text{V}^2} = 232.2\text{V} \quad (40)$$

$$V_{CR(peak)} = \frac{V_{IN(max)}}{2} + \sqrt{2} \times V_{CR} = \frac{410\text{V}}{2} + \sqrt{2} \times 109.3\text{V} = 359.6\text{V} \quad (41)$$

$$V_{CR(valley)} = \frac{V_{IN(max)}}{2} - \sqrt{2 \times V_{CR}} = \frac{410\text{V}}{2} - \sqrt{2} \times 109.3\text{V} = 63.4\text{V} \quad (42)$$

Rated current I_r = 1.248A

2.3.2.13 Select the Primary Side MOSFETs

Each MOSFET detects the input voltage as its maximum applied voltage: Choose the MOSFET voltage rating to be 1.5 times of the maximum bulk voltage.

$$V_{DS} = 1.5 \times V_{IN(max)} = 1.5 \times 410 = 615\text{V} \quad (43)$$

Choose the MOSFET current rating to be 1.1 times of the maximum primary side RMS current.

$$I_D = 1.1 \times I_r = 1.1 \times 1.248A = 1.373A \quad (44)$$

For LLC power stage working in ZVS, the turnon losses can be neglected. The choice of the MOSFET must be based on R_{DSON} and C_{oss}. Optimizing the Coss helps in minimizing the dead time required for achieving ZVS, thereby minimizing duty cycle loss.

This reference design uses the TK290P65Y MOSFET. The feature that optimizes the adaptive dead time of the UCC256301 helps in maximizing the duty cycle, thereby improving efficiency.

2.3.2.14 Select the Secondary Side MOSFETs

The secondary-side rectifier voltage rating is determined using 公式 45:

$$V_{DS\_sec} = 1.2 \times 2 \times V_{OUT\_max} = 1.2 \times 2 \times 24V = 57.6V \quad (45)$$

The current rating of the secondary-side MOSFET is determined using 公式 46:

$$I_{D\_sec} = 3.436A \quad (46)$$

This reference design uses TI's 100-V NexFET CSD19533Q5A with its low R_{DSON} (7.8 mΩ) and Q_g (27 nC). The very low R_{DSON} of the TI NexFET helps in reducing the overall loss in the synchronous rectifier.

2.3.2.15 LLC Output Capacitors

The LLC converter topology does not require an output filter, although a small second-stage filter inductor can be useful in reducing peak-to-peak output noise. Assuming that the output capacitors carry the full wave output current of the rectifier, the capacitor ripple current rating is:

$$I_{RECT} = \frac{\pi}{2\sqrt{2}} \times I_O = 1.11 \times 6.25 = 6.875A \quad (47)$$

Use a 35-V rating for a 24-V output voltage:

V_{LLCcap} = 35V

The RMS current rating of the capacitor is:

$$I_{C(out)} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times I_O\right)^2 - {I_O}^2} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times 6.25A\right)^2 - 6.25A^2} = 3.02A \quad (48)$$

The ripple current rating for a single capacitor may not be sufficient, so multiple capacitors are often connected in parallel.

$$ESR_{max} = \frac{V_{OUT(pk-pk)}}{I_{RECT(pk)}} = \frac{0.24V}{2 \times \frac{\pi}{4} \times 6.25A} = 24.446m\Omega \quad (49)$$

The capacitor specifications are:

- Voltage rating: 35 V
- Ripple current rating: 3.02 A
- ESR is less than 24.446 mΩ

2.3.2.16 Soft Start

During startup, the softstart capacitor is charged using the 25-μA current source internally. The UCC256301 exits soft start when the closed loop control takes over or when the voltage on the soft-start capacitor reaches 7 V. The value of the soft-start capacitor is selected using 公式 50.

$$C_{SS} = T_{SS} \times \frac{25uA}{7V} \tag{50}$$

Using a 47-nF soft-start capacitor gives the longest possible soft-start time as 13 ms.

2.3.2.17 BLK Pin Voltage Divider

The BLK pin senses the LLC input voltage and determines when to turn on and off the LLC converter. Different versions of the UCC256301 have different BLK thresholds. Choose the bulk startup voltage at 340 V, then the BLK resistor divider ratio can be calculated using 公式 51:

$$K_{BLK} = \frac{340V}{3.05V} = 111.47 \tag{51}$$

The desired power consumption of the BLK pin resistor is P_{BLKsns} = 10 mW. The total value of the BLK sense resistor is given by 公式 52:

$$R_{BLKsns} = \frac{V_{IN(nom)}^{2}}{P_{BLK(sns)}} = \frac{396^{2}}{0.01} = 15.68M\Omega \tag{52}$$

The lower BLK divider resistor value is given by:

$$R_{BLKlower} = \frac{R_{BLKsns}}{K_{BLK}} = \frac{15.68M\Omega}{111.47} = 140.68k\Omega \tag{53}$$

The actual value used is 142.1 kΩ The higher BLK divider resistor value is given by:

$$R_{BLKUPPER} = R_{BLKsns} - R_{BLKlower} = 15.54M\Omega \tag{54}$$

Actual value used is 15.3 MΩ.

2.3.2.18 Current Sense Circuit (ISNS Pin)

The ISNS pin sets the over current protection level. OCP1 is peak current protection level; OCP2 and OCP3 are average current protection levels. The threshold voltages are 0.6 V, 0.8 V, and 4 V, respectively. Set OCP3 level at 150% of full load. Thus, the sensed average input current level at full load is given by:

$$V_{ISNSfullload} = \frac{0.6V}{150\%} = 0.4V \tag{55}$$

The current sense ratio can then be calculated using 公式 56:

$$K_{ISNS} = \frac{V_{ISNSfullload}}{\frac{P_{OUT}}{\eta} \times \frac{1}{V_{DCBUS\_nom}}} = \frac{0.4V}{\frac{150W}{0.97} \times \frac{1}{396V}} = 1.024\Omega \tag{56}$$

Select a current sense capacitor first because there are fewer high-voltage capacitor choices than resistors.

C_{ISNS} = 150 pF

Then calculate the required ISNS resistor value:

$$R_{ISNS} = \frac{K_{ISNS} \times C_R}{C_{ISNS}} = 150.23\Omega \quad (57)$$

To realize power boost function, current sense resistor need to be smaller. The actual value of the current sense resistor used is 100 Ω.

2.3.2.19 CC and CV Feedback Loop

This reference design has two feedback loop, CC loop and CV loop, which can realize constant current output or constant voltage output. This feature is designed for battery charger application. As I calculated, the constant output current is around 6.3A. The constant output voltage value can be adjusted by R_{42} from 22V to 28V.

2.3.2.20 Auxiliary PSU

This reference design does not need an additional auxiliary PSU. The UCC256301 includes a high-voltage startup JFET to initially charge the VCC capacitor to provide the energy needed to start the PFC and LLC power system. Once running, power for the PFC and LLC controllers is derived from a bias winding on the LLC transformer.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 Testing Conditions

- Input conditions: VIN: 85-V to 265-V AC. Set the input current limit to 3 A.
- Output conditions: Electronic load, 0 to 30 V, 300 W

3.1.2 Equipment Needed

- Isolated AC source
- Single-phase power analyzer
- Digital oscilloscope
- Multimeters
- Electronic load

3.2 Testing and Results

3.2.1 Efficiency and Regulation

3.2.1.1 Performance Data

This section shows the efficiency, power factor, iTHD, and load regulation results at 115-V and 230-V AC input conditions.

表 4 shows the data for VIN = 115-V AC.

表 4. Efficiency and Regulation at 115-V AC

VINAC (V)	IINAC (A)	PINAC (W)	PF	iTHD (%)	VOUT (V)	IOUT (A)	POUT (W)	EFF (%)
114.68	1.43	162.1	0.99	9.42	24.06	6.250	150.375	92.77
114.74	1.28	145.8	0.99	10.08	24.07	5.625	135.394	92.86
114.81	1.14	129.6	0.99	10.92	24.07	5.000	120.350	92.86
114.87	1.00	113.5	0.99	11.97	24.07	4.375	105.306	92.78
114.93	0.86	97.5	0.98	15.73	24.08	3.750	90.300	92.61
115.00	0.72	81.7	0.98	9.29	24.08	3.125	75.250	92.11
115.05	0.59	65.9	0.97	9.60	24.09	2.500	60.225	91.39
115.12	0.45	50.1	0.96	9.35	24.09	1.875	45.169	90.16
115.18	0.32	34.3	0.93	8.75	24.09	1.250	30.113	87.79

表 5 shows the data for VIN = 230-V AC.

表 5. Efficiency and Regulation at 230-V AC

VINAC (V)	IINAC (A)	PINAC (W)	PF	iTHD (%)	VOUT (V)	IOUT (A)	POUT (W)	EFF (%)
230.38	0.72	159.5	0.98	6.38	24.06	6.250	150.399	94.29
230.40	0.65	143.6	0.98	6.36	24.07	5.625	135.394	94.29
230.42	0.59	127.8	0.98	5.93	24.07	5.000	120.350	94.17
230.44	0.52	112.1	0.97	5.91	24.08	4.375	105.350	93.98
230.46	0.46	96.3	0.96	5.96	24.08	3.750	90.300	93.77
230.49	0.40	80.7	0.94	5.73	24.08	3.125	75.250	93.25
230.51	0.34	65.1	0.92	6.25	24.09	2.500	60.225	92.51
230.52	0.29	49.4	0.88	7.36	24.09	1.874	45.145	91.37
230.56	0.24	33.7	0.78	8.62	24.09	1.249	30.088	89.28

表 6 shows the standby power consumption at VIN = 115-V AC and 230-V AC.

表 6. Standby Power

INPUT VOLTAGE	STANDBY POWER
115-V AC	316 mW
230-V AC	335 mW

3.2.1.2 Performance Curves

The following figures show the graphs for efficiency, power factor, iTHD, and load regulation, respectively.

图 4. Efficiency

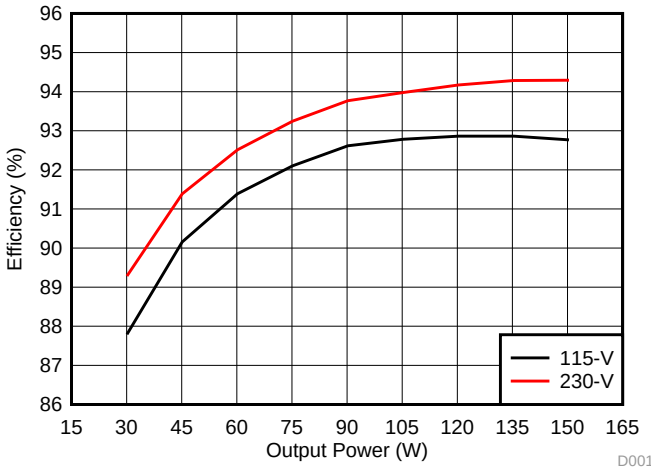


图 5. Power Factor

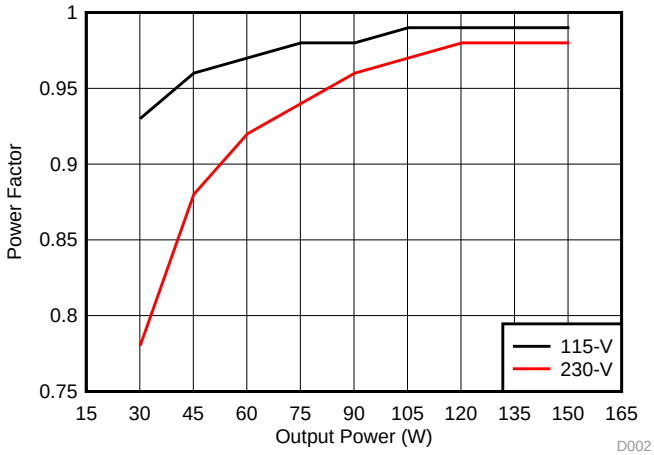


图 6. iTHD

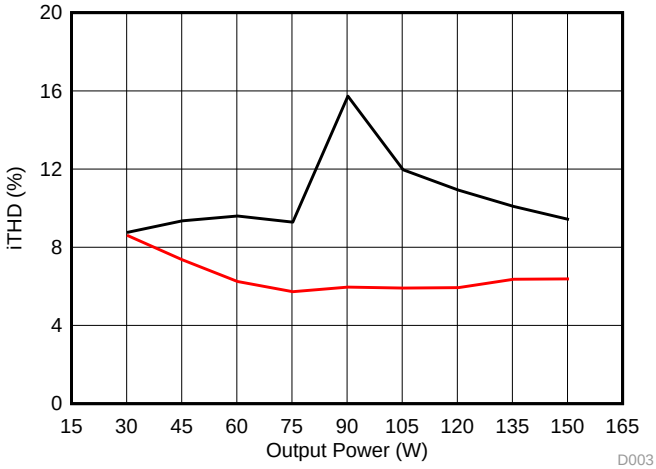
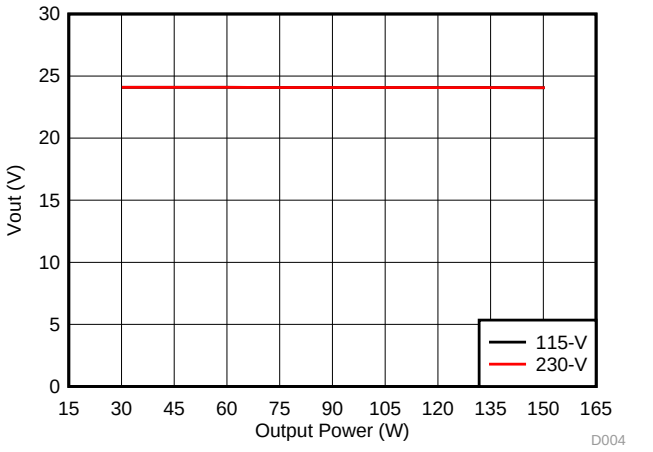


图 7. Load Regulation



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3.2.2 Switching Waveforms

3.2.2.1 PFC Stage Switching Waveforms

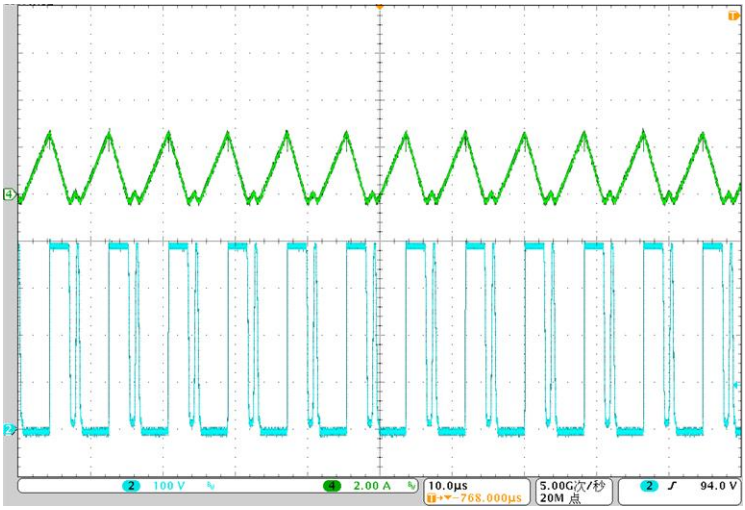
This section shows the PFC stage switching waveforms at an input voltage of 115-V AC and 230-V AC at different load conditions.

注: CH2: PFC switch node voltage (100 V/div, bandwidth: 20 MHz);

CH4: PFC inductor current (2 A/div, bandwidth: 20 MHz);

Test condition: VIN = 115-V AC/60 Hz; IOUT = 50% load

图 **8. PFC Inductor Current and Switching Node Waveform at 115-VAC, Half Load**

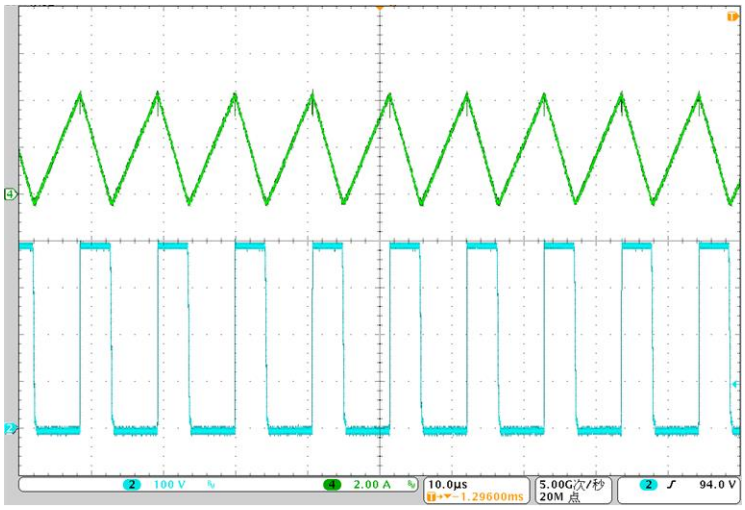


注**:** CH2: PFC switch node voltage (100 V/div, bandwidth: 20 MHz);

CH4: PFC inductor current (2 A/div, bandwidth: 20 MHz);

Test condition: VIN = 115-V AC/60 Hz; IOUT = 100% load

图 **9. PFC Inductor Current and Switching Node Waveform at 115-VAC, Full Load**

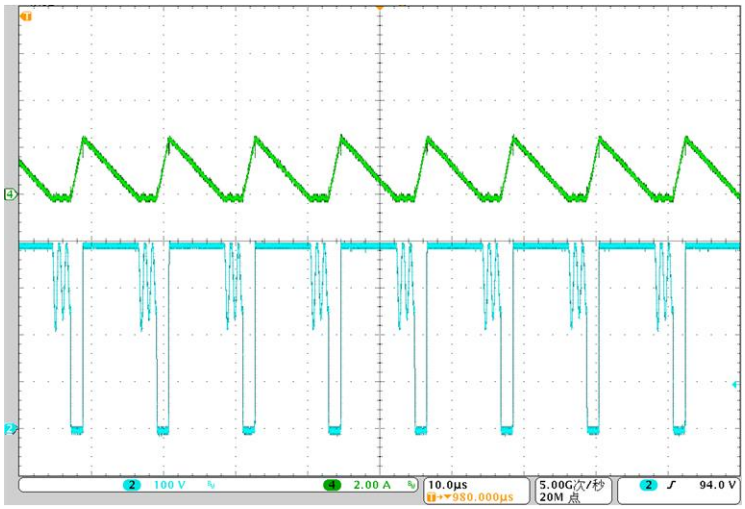


注**:** CH2: PFC switch node voltage (100 V/div, bandwidth: 20 MHz);

CH4: PFC inductor current (2 A/div, bandwidth: 20 MHz);

Test condition: VIN = 230-V AC/60 Hz; IOUT = 50% load

图 **10. PFC Inductor Current and Switching Node Waveform at 230-VAC, Half Load**

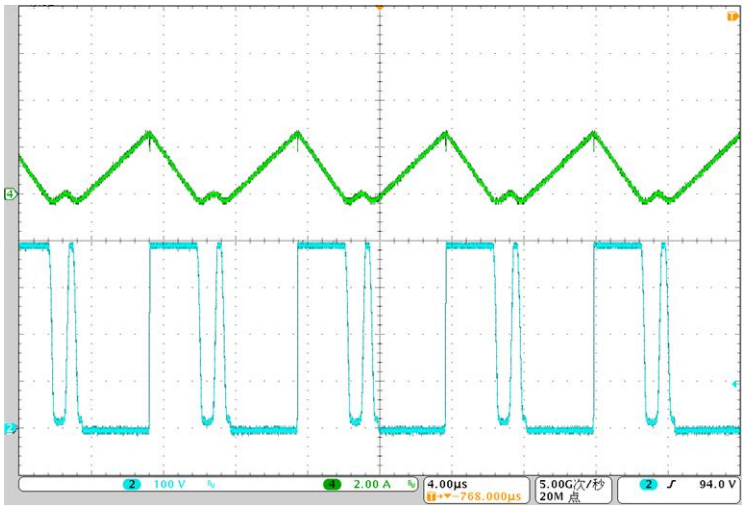


注: CH2: PFC switch node voltage (100 V/div, bandwidth: 20 MHz);

CH4: PFC inductor current (2 A/div, bandwidth: 20 MHz);

Test condition: VIN = 230-V AC/60 Hz; IOUT = 100% load

图 **11. PFC Inductor Current and Switching Node Waveform at 230VAC, Full Load**



3.2.2.2 LLC Stage Switching Waveforms

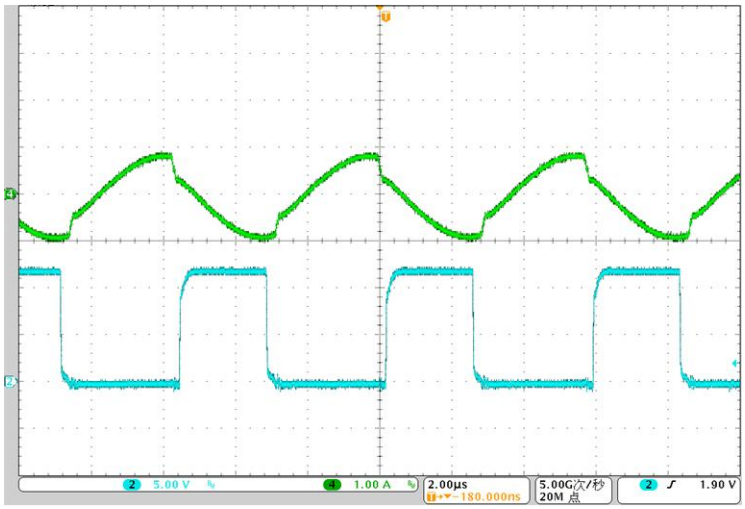
This section shows the LLC stage primary side switching waveforms at an output voltage of 24-V AC at different load conditions.

注: CH2: Low side PWM (5 V/div, bandwidth: 20 MHz);

CH4: LLC resonant current (1 A/div, bandwidth: 20 MHz);

Test condition: VIN = 115-V AC/50 Hz; IOUT = 50% load

图 **12. Low Side PWM and Resonant Current at Half Load**

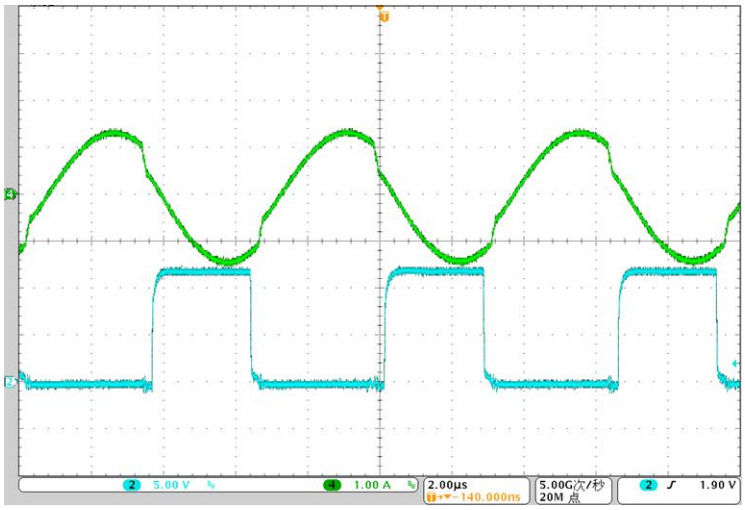


注: CH2: Low side PWM (5 V/div, bandwidth: 20 MHz);

CH4: LLC resonant current (1 A/div, bandwidth: 20 MHz);

Test condition: VIN = 115-V AC/50 Hz; IOUT = 100% load

图 **13. Low Side PWM and Resonant Current at Full Load**



3.2.2.3 LLC Secondary Side Synchronous Drive Waveform

The synchronous drive output waveforms and the resonant current are shown in the following figures.

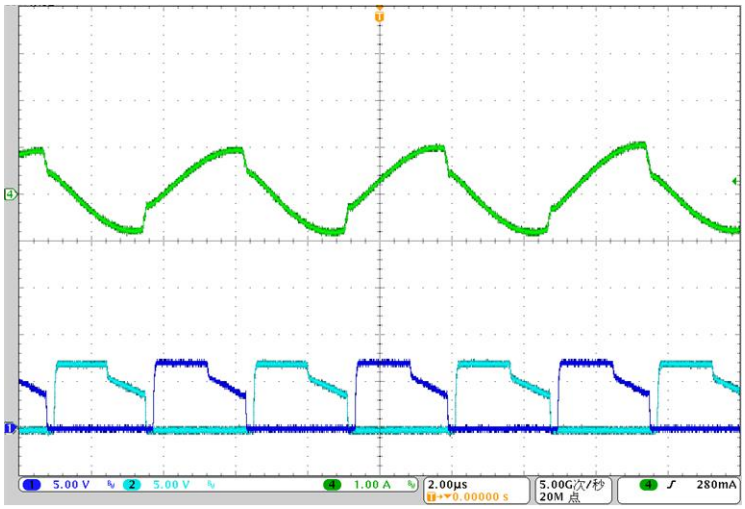
注: CH1: Gate driver of SR1 (5 V/div, bandwidth: 20 MHz);

CH2: Gate driver of SR2 (5 V/div, bandwidth: 20 MHz);

CH4: LLC resonant current (1 A/div, bandwidth: 20 MHz);

Test condition: VIN = 115-V AC/60 Hz; IOUT = 50% load

图 **14. SR Rectifier Gate Driver**

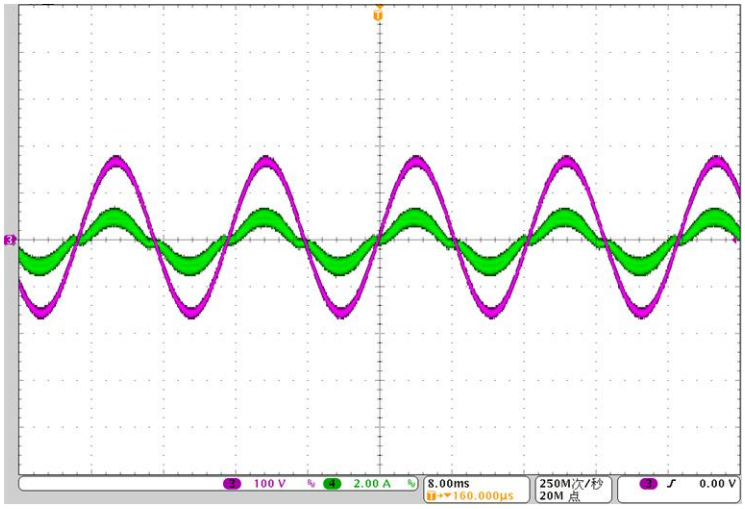


3.2.3 Input Waveforms

图 15 and 图 16 show the input current waveform at 115-V AC at half load and full load conditions, respectively.

注: CH3: Input voltage (100 V/div, bandwidth: 20 MHz);
CH4: Input current (2 A/div, bandwidth: 20 MHz);
Test condition: VIN = 115-V AC/60 Hz; IOUT = 50% load

图 **15. Input Voltage and Current at 115-VAC, Half Load**



注: CH3: Input voltage (100 V/div, bandwidth: 20 MHz);
CH4: Input current (2 A/div, bandwidth: 20 MHz);
Test condition: VIN = 115-V AC/60 Hz; IOUT = 100% load

图 16. Input Voltage and Current at 115-VAC, Full Load

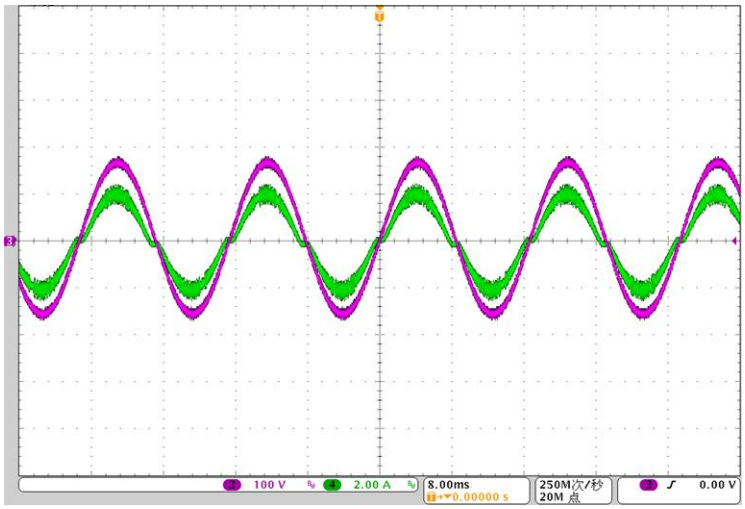
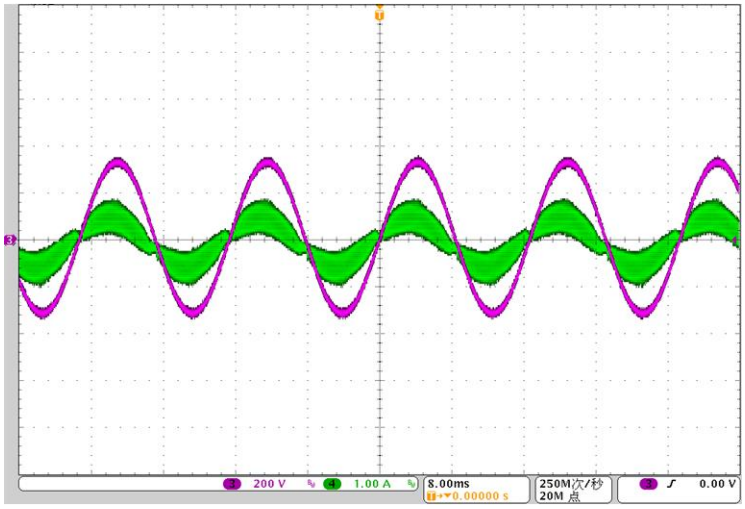


图 17 and 图 18 show the input current waveform at 230-V AC at half load and full load conditions, respectively.

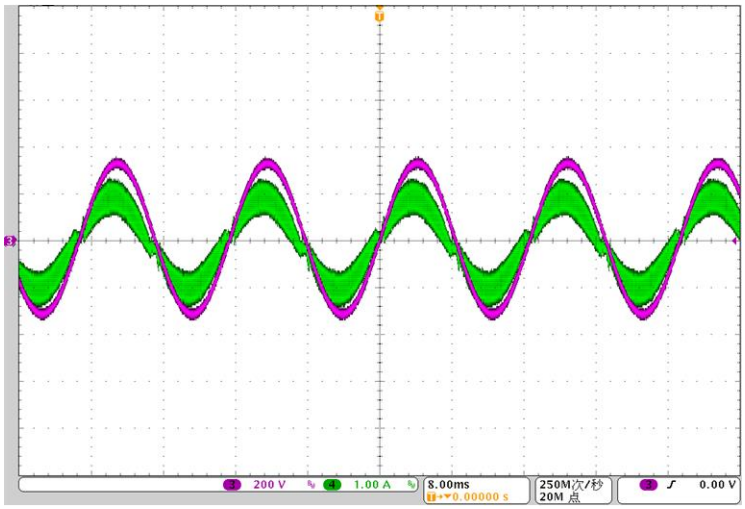
注: CH3: Input voltage (200 V/div, bandwidth: 20 MHz);
CH4: Input current (1 A/div, bandwidth: 20 MHz);
Test condition: VIN = 230-V AC/60 Hz; IOUT = 50% load

图 17. Input Voltage and Current at 230-VAC, Half Load



注: CH3: Input voltage (200 V/div, bandwidth: 20 MHz);
CH4: Input current (1 A/div, bandwidth: 20 MHz);
Test condition: VIN = 230-V AC/60 Hz; IOUT = 100% load

图 **18. Input Voltage and Current at 230-VAC, Full Load**



3.2.4 Start-up Waveforms

The startup waveform showing the 24-V output voltage and the input AC voltage.

注: CH2: Output voltage (5 V/div, bandwidth: 20 MHz);

CH3: Input voltage (200 V/div, bandwidth: 20 MHz);

Test condition: VIN = 230-V AC/60 Hz; IOUT = 0% load and 50% load.

图 **19. Startup Waveform at VINAC = 230-V AC and No Load**

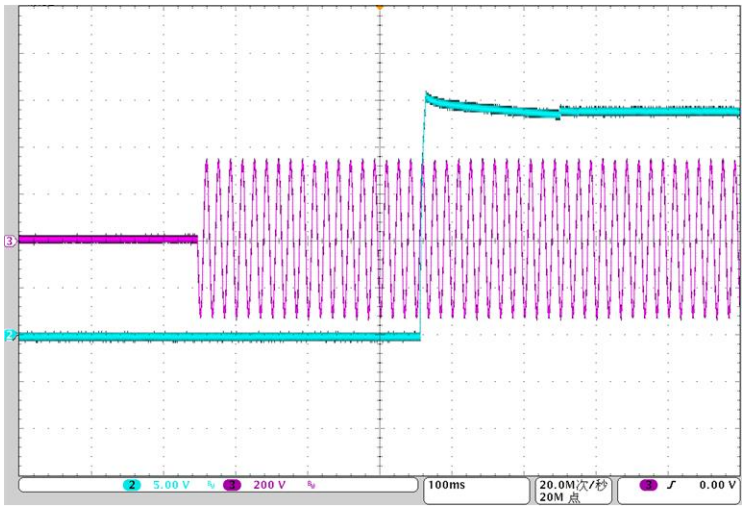
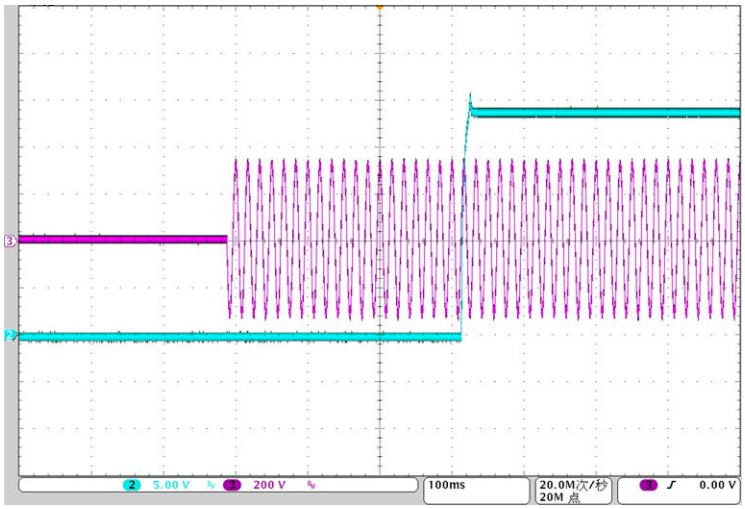


图 **20. Startup Waveform at VINAC = 230-V AC and Half Load**



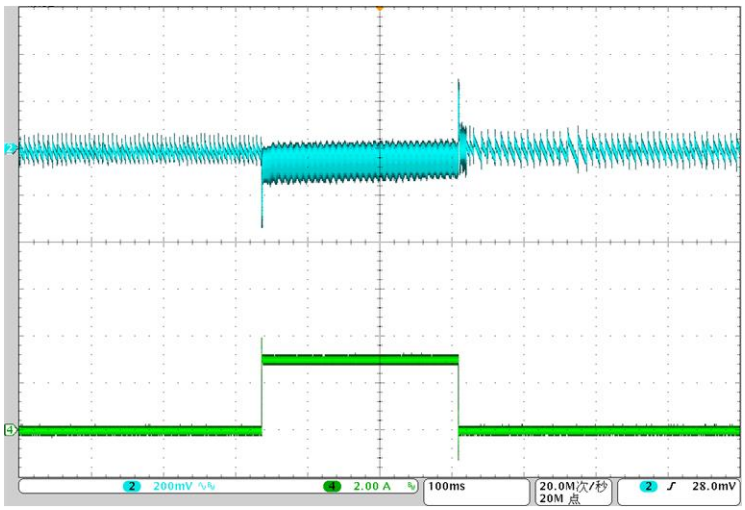
3.2.5 Dynamic Load Characteristics

Load transient performance is observed using an electronic load.

The converter is operating at an input voltage of 230-V AC and an output voltage of 24-V DC.

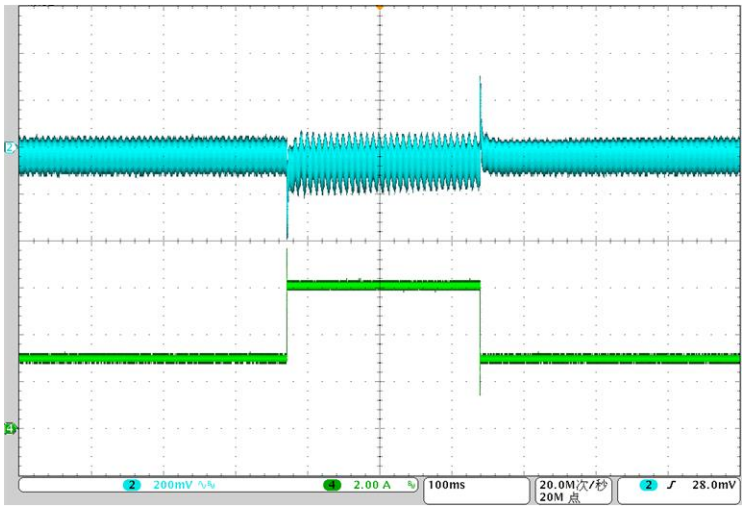
注: CH2: Output voltage in AC level (200 mV/div, bandwidth: 20 MHz);
CH4: Output current (2 A/div, bandwidth: 20 MHz);
Test condition: VIN = 230-V AC/60 Hz; IOUT = from 0% to 50% load

图 **21. Transient Response from 0% to 50% Load**



注: CH2: Output voltage in AC level (200 mV/div, bandwidth: 20 MHz);
CH4: Output current (2 A/div, bandwidth: 20 MHz);
Test condition: VIN = 230-V AC/60 Hz; IOUT = from 50% to 100% load

图 22. Transient Response from 50% to 100% load

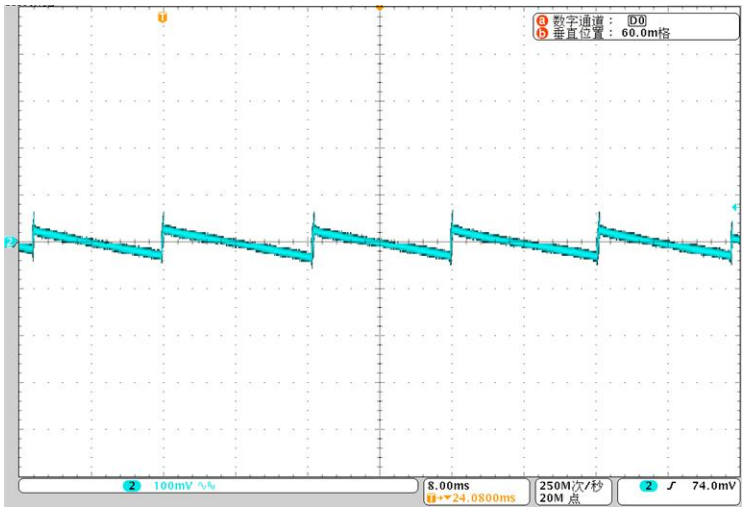


3.2.6 Output Ripple

图 23 and 图 24 show the output voltage ripple under 0-W and 150-W load conditions at a 230-V AC input, respectively.

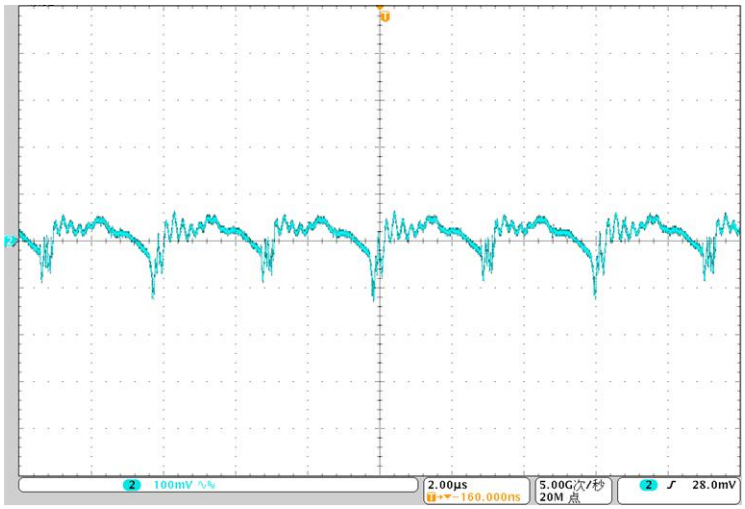
注: CH2: Output ripple (100 mV/div, bandwidth: 20 MHz);
Test condition: VIN = 230-V AC/60 Hz; IOUT = 0% load

图 23. Output Ripple With No Load at VINAC = 230-V AC



注: CH2: Output ripple (100 mV/div, bandwidth: 20 MHz);
Test condition: VIN = 230-V AC/60 Hz; IOUT = 100% load

图 24. Output Ripple With Full Load at VINAC = 230-V AC



3.2.7 Short-Time 240-W Peak Output at 230-V AC and 24-V DC

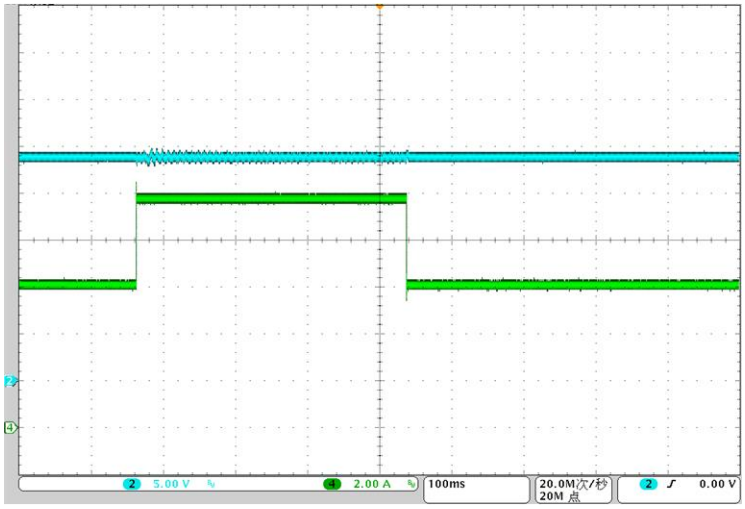
The output power capability of the short-time peak is shown in 图 25. The converter has 240-W output power capability at 230-V AC and 24-V DC condition.

注: CH2: Output voltage (5 V/div, bandwidth: 20 MHz);

CH4: Output current (2 A/div, bandwidth: 20 MHz);

Test condition: VIN = 230-V AC/60 Hz; VOUT = 24-V DC; IOUT = from 100% to 160% load

图 25. 240-W Peak Output Power Capability at 230-V AC and 24-V Output



3.2.8 Thermal Image

This section features two sets of thermal images. These thermal images are taken under room temperature with no airflow measured at the board. 图 26 shows the thermal image for both the top and bottom side of the board. The input voltage is 115-V AC, and the loads are 6.25 A for 24 V_{OUT}.

图 **26. Thermal Performance at 115-V AC With Full Load**

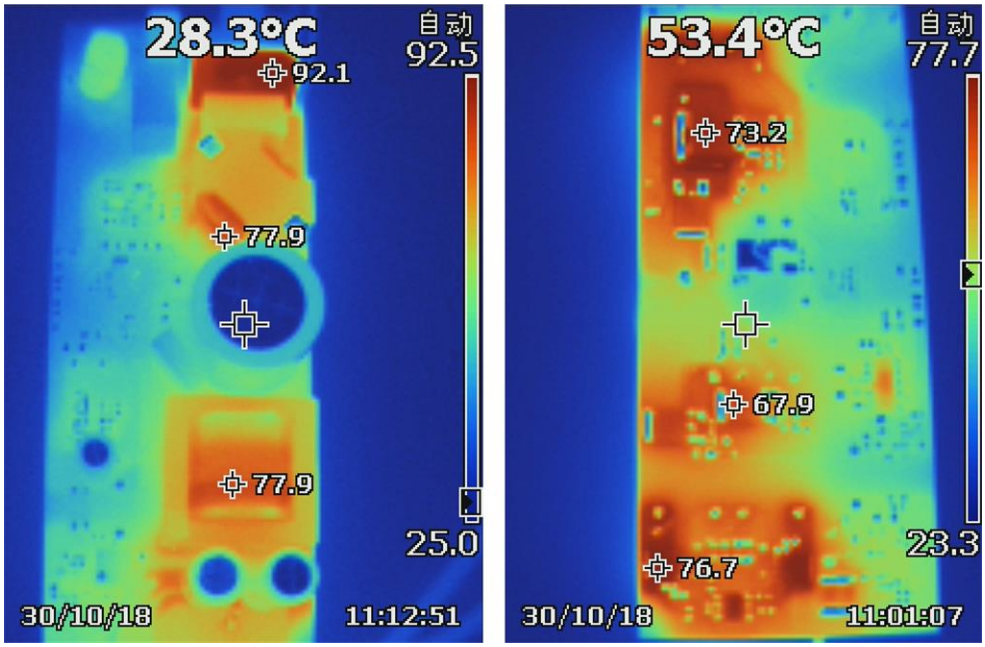
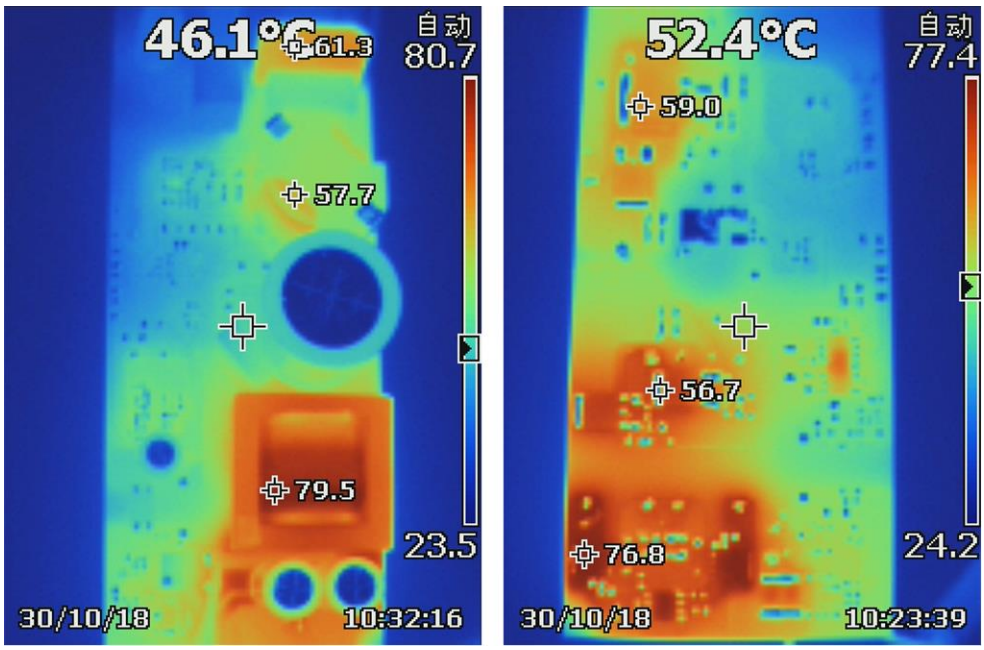


图 27 shows the thermal image for both the top and bottom side of the board. The input voltage is 230-V AC, and the loads are 6.25 A for 24 V_{OUT}.

图 **27. Thermal Performance at 230-V AC With Full Load**



3.2.9 CE Test

This section shows the CE test results. The following images and data show that it passes EN55032 Class B standard. 图 28 and 图 29 show the CE test results of L line and N line at 230-V AC. 图 30 and 图 31 show the CE test results of L line and N line at 115-V AC.

图 28. CE as per EN55032 Class B, L Line at 230-V AC

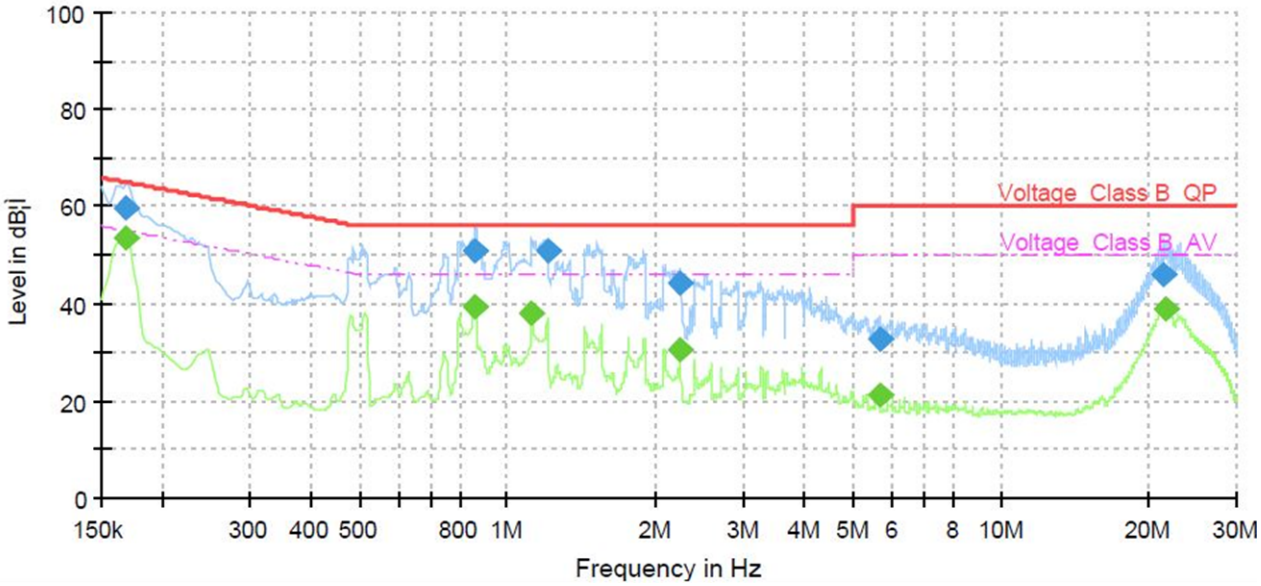


图 29. CE as per EN55032 Class B, N Line at 230-V AC

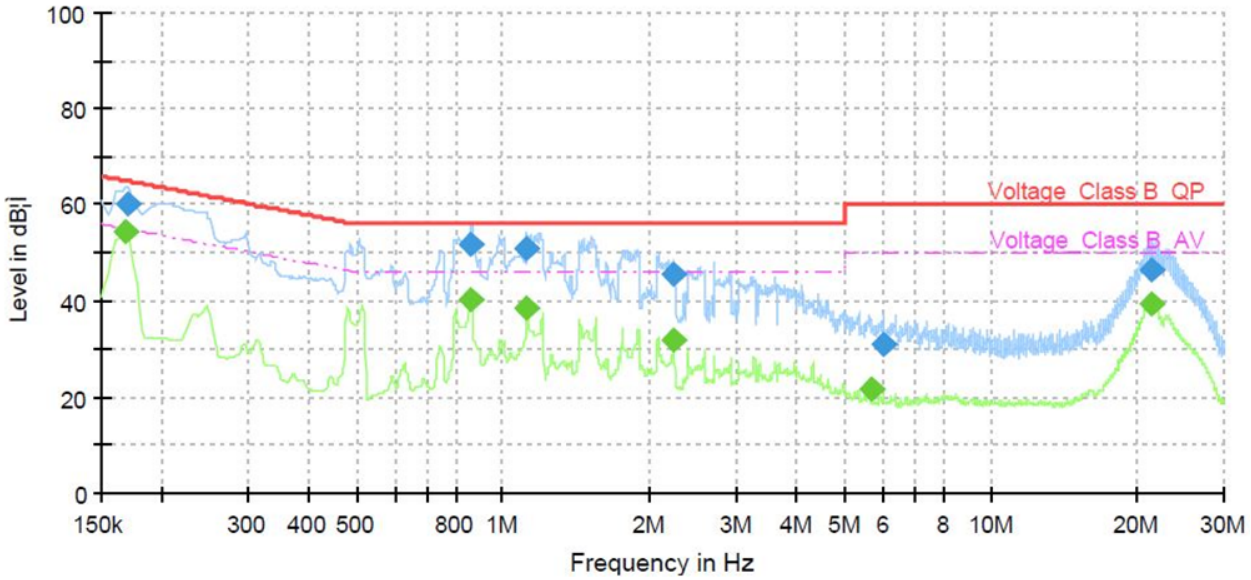


图 30. CE as per EN55032 Class B, L Line at 115-V AC

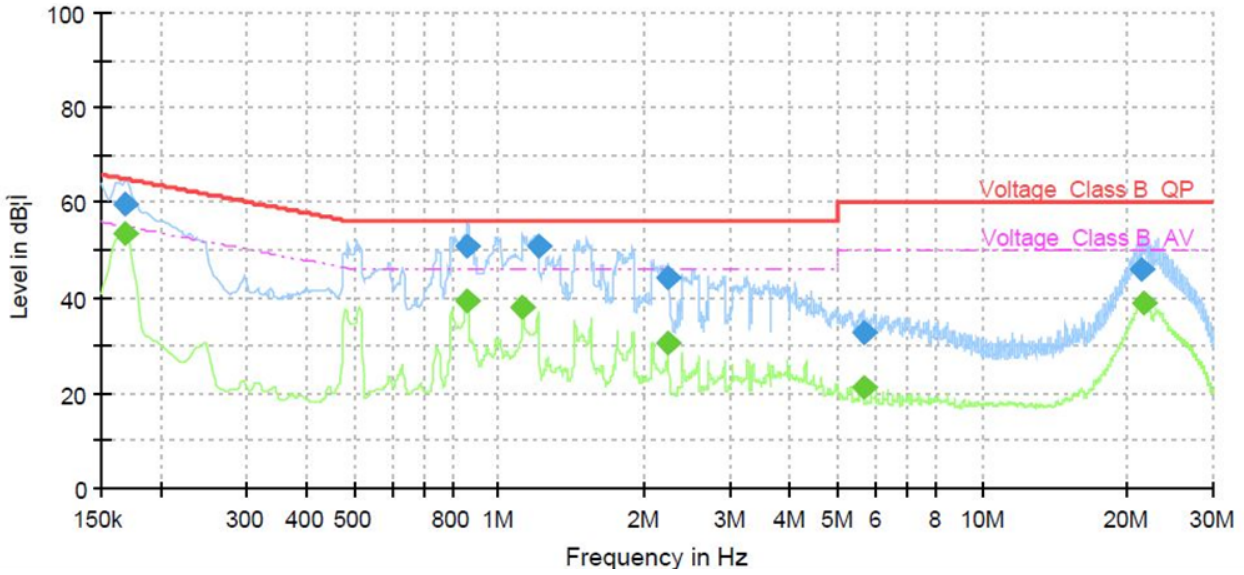
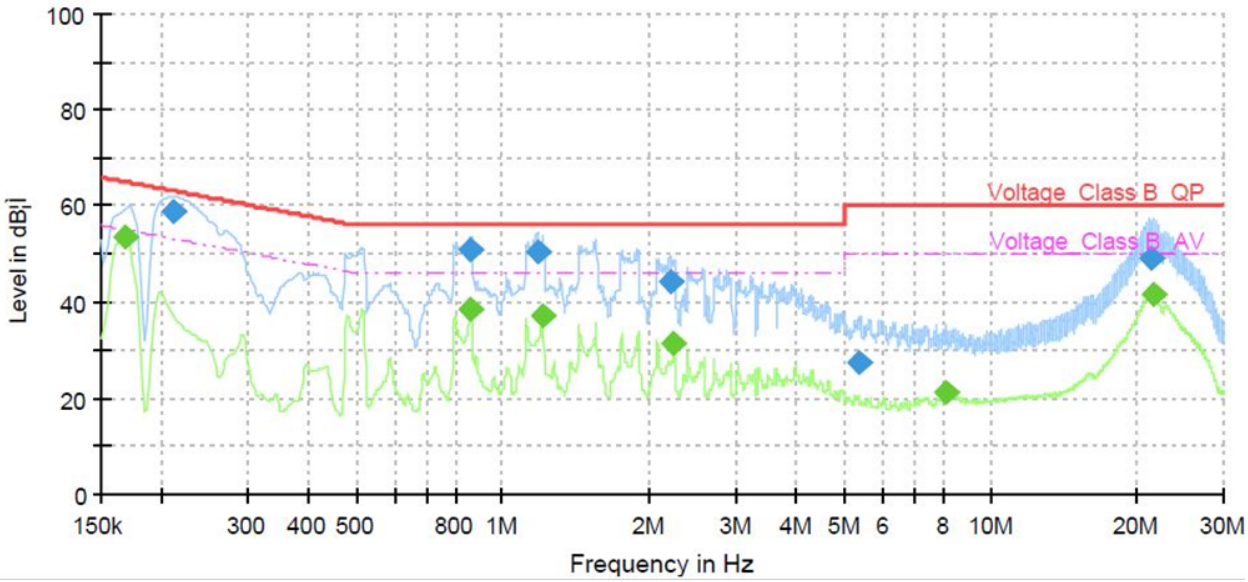


图 31. CE as per EN55032 Class B, N Line at 115-V AC



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010038.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010038.

4.3 PCB Layout Recommendations

4.3.1 Power Stage Specific Guidelines

Key guidelines for routing power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high-frequency switching currents, on both the primary and secondary sides of the converter. This helps reduce EMI and improve converter overall performance.
- Keep traces with high dV/dt potential and high dI/dt capability away from or shielded from sensitive signal.
- Keep power ground and control ground separately for each power supply stage. If they are electrically connected, tie them together at one point near DC input return or output return of the given stage correspondingly.
- When multiple capacitors are used in parallel for current sharing, the layout must be symmetrical across both leads of the capacitors. If the layout is not identical, the capacitor with the lower series trace impedance will see higher currents and become hotter.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device. The devices are intended for protection and hence need to be routed with short traces to reduce inductance.
- Choose the width of PCB traces based on acceptable temperature rise at the rated current per IPC2152 as well as acceptable DC and AC impedances. Also, the traces must withstand the fault currents (such as short-circuit current) before the activation of electronic protection such as fuse or circuit breaker.
- Determine the distances between various circuits according to the requirements of applicable standards such as the UL60950.
- Adapt thermal management to fit the end-equipment requirements.

4.3.2 Controller Specific Guidelines

For the PFC controller UCC28056:

- Locate the ROS2 and COS2 components adjacent to the VOSNS pin along with the lowest resistor(s) that comprise ROS1. High voltage drops across the resistor(s) that comprise ROS1. Allow adequate spacing around the high voltage nodes that connect to and within ROS1 to avoid air discharge across the PCB surface.

• ZCD/CS Pin Switching edge spikes imposed on the signal feeding this pin may cause the internal ESD structures to conduct, causing a voltage offset to appear on the capacitive divider feeding this pin. To limit this risk, place the voltage divider close to the ZCD/CS pin and far from the region of fast changing magnetic field. Maintain a small number of nets between the resistors and capacitors in the divider to limit capacitive pickup within the divider chain. Maintain the loop small and contain the minimum area to limit magnetic pickup. Run the connections between the current sense resistor and UCC28056 directly to the terminals of resistor and not be shared with power circuit traces. When laying out the PCB start with the ZCD/CS pin divider placement and routing to ensure that the needs of this pin come first.

• VCC Pin A local decoupling capacitor should be connected directly between the VCC and GND pins via short, dedicated, PCB traces. This capacitor supplies the high current pulses needed to charge the gate capacitance of the power MOSFET.

• GND Pin Be sure to separate the PCB traces for the GND net of the UCC28056 far from the power circuit GND net. Connect the GND pin of the UCC28056 device to the power circuit GND at only one terminal of the current sense resistor. This connection method ensures that the voltage between the UCC28056 device GND pin and the ZCD/CS pins remains equal to the voltage across the current sense resistor during the MOSFET conduction period.

• DRV Pin Avoid placing the DRV pin traces close to other high-impedance nets such as ZCD/CS or VOSNS. The fast rising and falling edges associated with the waveform on this pin may capacitively couple onto these high impedance nets causing disturbance near the switching edges.

• COMP Pin Locate the RC network attached to this pin close to the pin. Return to the GND pin should be via a short PCB trace.

For the LLC controller UCC256301:

• Put a 2.2-μF ceramic capacitor on VCC pin in addition to the energy storage electrolytic capacitor. Place the 2.2-μF ceramic capacitor as close as possible to the VCC pin.

• RVCC pin must have a bypass capacitor of 4.7 μF or more. It is recommended to add a 0.1-μF ceramic capacitor in addition to the 4.7 μF. Place the capacitors as close as possible to the RVCC pin. The RVCC cap needs to be at least fives times that of the boot capacitor.

• The minimum recommended boot capacitor is 0.1 μF. The minimum value of the boot capacitor needs to be determined by the minimum burst frequency. The boot capacitor must be large enough to hold the bootstrap voltage during the lowest burst frequency. Please refer to the boot leakage current in the electrical table

• Use large copper pour around the GND pin.

• Place the filtering capacitor on BW, ISNS, and BLK as close as possible to the pin.

• FB trace must be as short as possible.

• Place a soft-start capacitor as close as possible to the LL/SS pin.

• Use a film capacitor or C0G, NP0 ceramic capacitor on the VCR divider and ISNS capacitor for low distortion.

• It is recommended that ISNS resistor is less than 500 Ω to keep the node impedance low.

• Add necessary filtering capacitors on the BW pin to filter out the high spikes on the bias winding waveform.

• It is critical to filter out the high spikes because internally the signal is peak detected and then sampled at the low-side turnoff edge.

• Do not put any capacitors on the HV pin to ground. The layout of this pin should result in low parasitic capacitance (< 60 pF) from the HV pin to ground.

• Keep necessary high voltage clearance.

4.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-010038.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010038.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010038.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010038.

5 Related Documentation

1. Texas Instruments, *UCC25630x Practical Design Guidelines*
2. Texas Instruments, *UCC25630x Selection Guide*
3. Texas Instruments, *24V, 480W Nominal 720W Peak, >93.5% Efficient, Robust AC/DC Industrial Power Supply Reference Design*

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6 About the Author

HUIXIN WANG is a systems engineer at Texas Instruments, where she is responsible for developing reference design solutions for the power delivery, industrial segment. Huixin earned her master of technology degree in power electronics from Zhejiang University.

修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (December 2018) to A Revision **Page**

- 已更改 电路板图像 1
- 已更改 information in 表 4, 表 5, and 表 6 19
- 已更改 all graphs in 节 3.2.1.2 20
- 已添加 节 3.2.9 31

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