TI Designs：TIDM-1007
采用 C2000™ MCU 的交错式 CCM 图腾柱无桥 PFC 参考设计

说明

此参考设计阐述了一种使用 C2000™微控制器 (MCU) 和 LMG3410 来控制交错式连续导通模式 (CCM) 图腾柱 (TTPL) 无桥功率因数校正 (PFC) 功率级的方法。该电源拓扑采用氮化镓 (GaN) 器件，从而提高了效率，并降低了电源尺寸。该设计支持用于提高效率的切相和自适应死区时间，用于在轻负载下改进功率因数的输入电容补偿方案，以及瞬态时用于降低电压尖峰的非线性电压环路。可供此参考设计使用的硬件和软件可帮助您缩短产品上市时间。

资源

TIDM-1007	设计文件夹
TMS320F280049	产品文件夹
TMS320F28075	产品文件夹
LMG3410	产品文件夹
UCC27714	产品文件夹
OPA2376	产品文件夹
SN74LVC1G3157DRYR	产品文件夹
ISO7831	产品文件夹
TLV713	产品文件夹
C2000WARE-DIGITALPOWER-SDK	工具文件夹

TI E2E™ Community

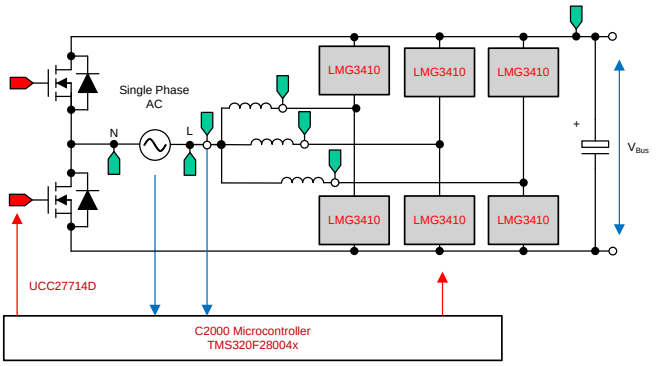
咨询我们的 E2E™ 专家

特性

- 交错式 3.3kW 单相无桥 CCM 图腾柱 PFC 级
- 100kHz 脉宽调制 (PWM) 开关
- 可编程输出电压，标称值为 380V 直流输出
- 总谐波失真 (THD) 小于 2%
- 峰值效率高于 98%
- 提供 powerSUITE™支持，以使设计轻松适应用户要求
- 具有软件频率响应分析器 (SFRA)，可实现对开环增益的快速测量
- 具有 PWM 软启动功能，可降低 TTPL PFC 中的零电流尖峰
- 对使用驱动程序库的 F28004x 的软件支持
- 在 C28x 或 CLA 上运行控制环路时保持的相同源代码

应用

- 电动汽车 (EV) 车载充电器
- 电信整流器
- 驱动器、焊接和其他工业应用



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注: 有关 LMG3410 产品和供货情况的更多信息，请参阅 http://www.ti.com.cn/product/cn/LMG3410。该器件未经 AEC-Q100 标准认证。有关更多信息，请联系 TI。

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1 System Description

Interleaved TTPL PFC is an attractive topology for EV chargers and industrial applications with the trend for higher power, higher efficiency, and higher power density. 图 1 shows the implementation of the TTPL bridgeless PFC as it is on the TIDM-1007 board.

1.1 Key System Specifications

表 1 describes the interleaved CCM TTPL PFC reference design power specifications.

表 1. Key System Specifications

PARAMETER	SPECIFICATION
Input voltage (Vin)	AC 120 Vrms VL-N, 60 Hz or AC 230 Vrms VL-N , 50 Hz
Input current (Iin)	16-A RMS maximum
Output voltage (Vout)	380-V DC bus Nominal
Output current (Iout)	10-A maximum
Power rating	1.65 KW at single phase 120 Vrms or 3.3 KW at single phase 230 Vrms
Current THD	<2% at 120-Vrms L-N rated load
Efficiency	Peak 98.7% at 230-Vrms input, peak >97.7% at 120-Vrms input
Primary filter inductor	478 µH
Output capacitance	880 µF
PWM switching frequency	100 kHz

WARNING

TI intends this reference design to be operated in a *lab environment only and does not consider it to be a finished product* for general consumer use.

TI Intends this reference design to be used only by *qualified engineers and technicians* familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

There are *accessible high voltages present on the board*. The board operates at voltages and currents that may cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

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CAUTION

Do not leave the design powered when unattended.

High voltage! There are *accessible high voltages present on the board*. Electric shock is possible. The board operates at voltages and currents that may cause shock, fire, or injury if not properly handled. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property. For safety, use of isolated test equipment with over-voltage and over-current protection is highly recommended.

TI considers it the user's responsibility to confirm that the voltages and isolation requirements are identified and understood before energizing the board or simulation. *When energized, do not touch the design or components connected to the design*.

Hot surface! Contact may cause burns. Do not touch!

Some components may reach high temperatures >55°C when the board is powered on. The user must not touch the board at any point during operation or immediately after operating, as high temperatures may be present.

2 System Overview

Interleaved TTPL PFC is an attractive topology for EV chargers with the trend for higher power, higher efficiency, and higher power density. 图 1 shows the implementation of the TTPL bridgeless PFC as it is in this reference design.

2.1 Block Diagram

图 1 shows the block diagram of this reference design with key TI components highlighted.

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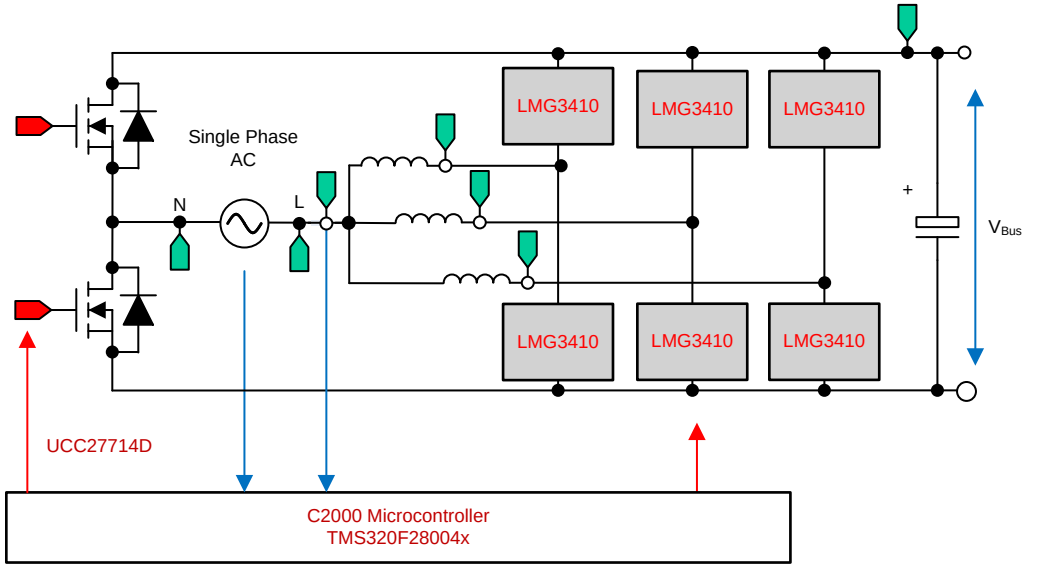

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图 1. Power Topology Block Diagram

2.2 Design Considerations

The following detail the sensing circuit that is on this design. One can also refer to the *calculations.xlsx* file, which is available under the C2000Ware Digital Power SDK Install directory at *<install_location>\solutions\tidm_1007\hardware* for details on sensing circuit.

2.2.1 Input AC Voltage Sensing

The line and the neutral voltages are sensed by resistor divider to the ground of the board as shown in 图 2. The two readings are subtracted on the controller to get the Vac sensing.

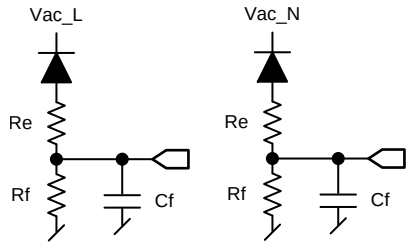

图 2. Input AC Voltage Sensing

2.2.2 Bus Voltage Sensing

Similarly the bus voltage is sensed by a resistor divider network as shown in 图 3.

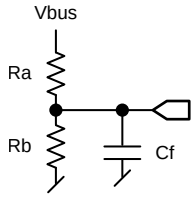

图 3. Bus Voltage Sensing Circuit

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2.2.3 AC Current Sensing

A Hall effect sensor senses the total current. The Hall effect sensor has an inbuilt offset, and the range is different than what ADC can measure. Hence, the voltage is scaled to match the ADC range using the circuit as shown in 图 4.

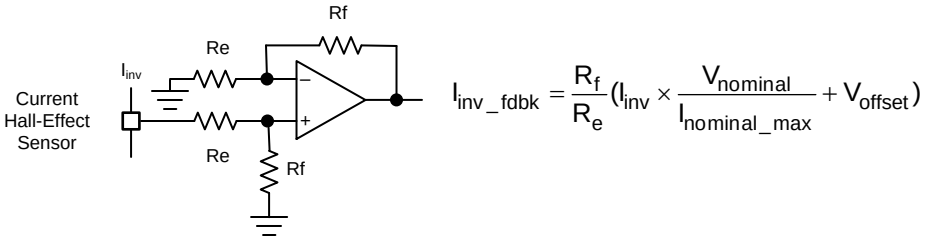

图 4. Current Sensing Using Hall Effect Sensor

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2.2.4 Sense Filter

An RC filter filters the signals before connecting to the controller. A common RC filter is used for all the sensing signals on this design as shown in 图 5.

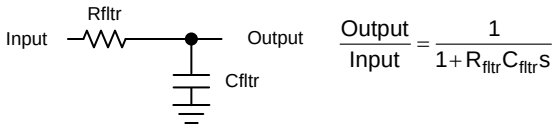

图 **5. RC Filter**

2.2.5 Protection (CMPSS)

Most power electronics converters require protection from overcurrent event. For this design multiple comparators are required, and references for the trip must be generated, as shown in 图 6.

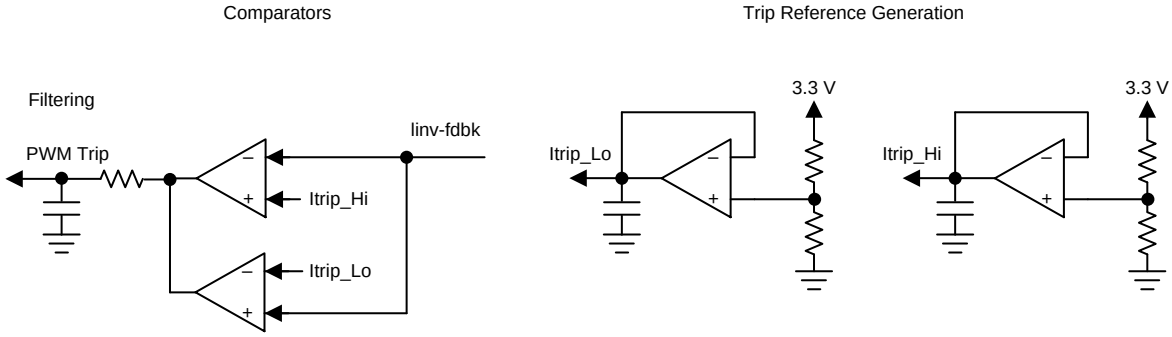

图 **6. Trip Generation for PWM Using Comparators and Reference Generators**

All this circuitry is avoided when using C2000 MCUs, such as TMS320F28377D, which have on-chip windowed comparator as part of the CMPSS that are internally connected to the PWM module that can enable fast tripping of the PWM. An on-chip windowed comparator saves board space and cost in the end application as extra components can be avoided using on-chip resources, as shown in 图 7.

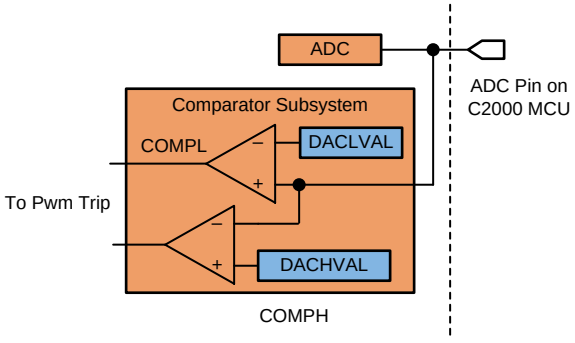

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图 **7. CMPSS Used for Overcurrent Protection**

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2.3 Highlighted Products

2.3.1 C2000™ MCU F28004x

C2000 MCUs are part of an optimized MCU family for real-time control application. Fast and high-quality analog-to-digital controller enables accurate measurement of the current and voltage signals, and an integrated comparator subsystem (CMPSS) provides protection for overcurrent and overvoltage without use of any external devices. The optimized CPU core enables fast execution of control loop. Trigonometric operations are accelerated using the on-chip trigonometric math unit (TMU). The solution also provides an option to use the control law accelerator (CLA) on the F28004x and F2837x. The CLA is a co-processor that can be used to alleviate CPU burden and enable faster-running loops or more functions on the C2000 MCU.

2.3.2 LMG3410

The LMG3410 single-channel GaN power stage contains a 70-mΩ, 600-V GaN power transistor and specialized driver in an 8-mm × 8-mm QFN package. Direct drive architecture is used to create a normally-off device while providing the native switching performance of the GaN power transistor. When the LMG3410 is unpowered, an integrated low-voltage silicon MOSFET turns the GaN device off through its source. In normal operation, the low-voltage silicon MOSFET is held on continuously while the GaN device is gated directly from an internally-generated negative voltage supply. The integrated driver provides additional protection and convenience features. Fast overcurrent, overtemperature, and undervoltage lockout (UVLO) protections help create a fail-safe system. The device's status is indicated by the FAULT output. An internal 5-V low-dropout regulator can provide up to 5 mA to supply external signal isolators. Finally, externally-adjustable slew rate and a low-inductance QFN package minimize switching loss, drain ringing, and electrical noise generation.

2.3.3 UCC27714

The UCC27714 is a 600-V high-side, low-side gate driver with 4-A source and 4-A sink current capability that is targeted to drive power MOSFETs or IGBTs. The device comprises of one ground-referenced channel (LO) and one floating channel (HO), which is designed for operating with bootstrap supplies. The device features excellent robustness and noise immunity with capability to maintain operational logic at negative voltages of up to –8 VDC on HS pin (at VDD = 12 V).

2.4 System Design Theory

2.4.1 PWM

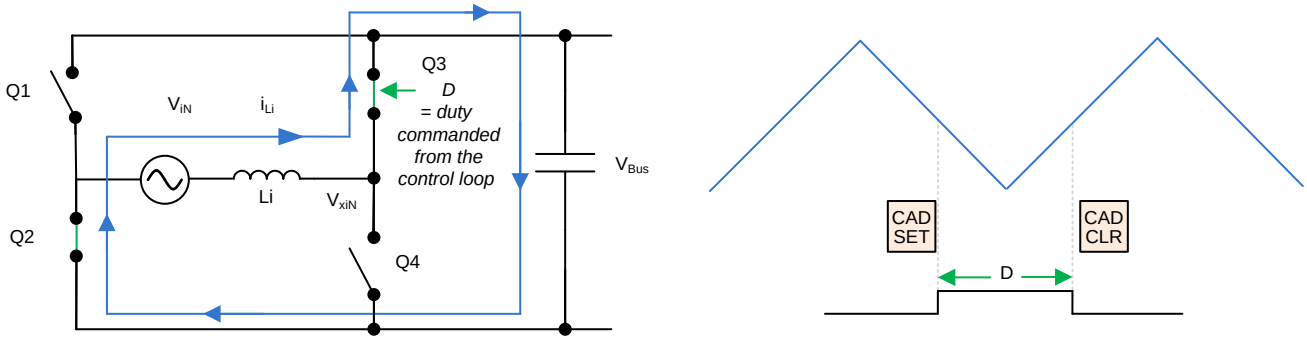

图 **8. Single-Phase Diagram of TTPL PFC**

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图 8 shows a simplified diagram of a single phase of the interleaved TTPL PFC topology. To control this rectifier the duty cycle is controlled to regulate the voltage directly. This regulation is possible if the software variable *Duty* or *D* is set so that when it is equal to 1, Q3 is always ON, and the setting makes the voltage V_{xiN} equal to the V_{bus} voltage. When *Duty* is set to 0, Q3 never turns on, and Q4 is always connected to , which makes the V_{xiN} voltage go to 0.

2.4.2 Current Loop Model

To understand the current loop model, first look at the inductor current closely. In 图 8 the Duty cycle (D) is provided to the PWM modulator, which is connected to the switch Q3 and Q4. From here, 公式 1 is written as:

$$V_{xiN} = D \times V_{bus} \tag{1}$$

注: When D is set to 1, Q3 is *on* all the time, and when D is 0, Q3 is *off* all the time.

To modulate the current through the inductor, the voltage V_{xiN} is regulated using the duty cycle control of Q3 and Q4 switches. It is assumed that the direction of current is positive in the direction from the AC line into the rectifier and that the grid is fairly stiff when using the DC bus feedforward and the AC voltage feedforward. 图 9 shows the simplified current loop, and the current loop plant model is written as 公式 2.

$$H_{p\_i} = \frac{i_{Li}^*}{D} = \frac{1}{K_{v\_gain}} \times K_{i\_gain} \times K_{i\_fltr} \times G_d \times \frac{1}{Z_i} \tag{2}$$

Where:

- K_{v_gain} is the inverse of maximum bus voltage sensed, $\frac{1}{V_{busMaxSense}}$
- K_{i_gain} is the inverse of maximum AC current sensed, $\frac{1}{I_{AC\_MaxSense}}$
- K_{i_fltr} is the response of the RC filter connected from the current sensor to the ADC pin
- G_d is the digital delay associated with the PWM update and digital control is the current command
- i_{Li}^* is the current command

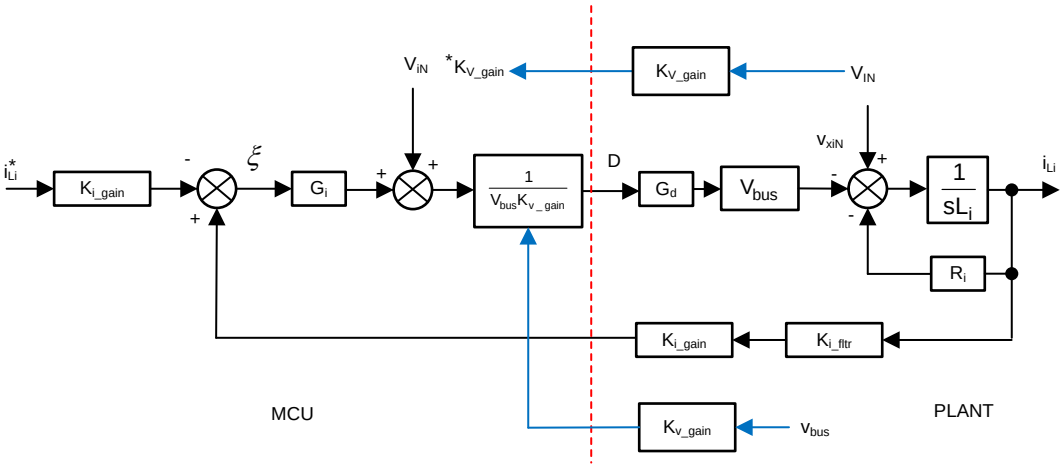

图 9. Current Loop Control Model

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注: The negative sign on the reference is because the current loop is thought to be regulating the voltage, V_{xiN} . To increase the current, V_{xiN} must be reduced—hence, the opposite sign for reference and feedback in 图 9.

This current loop model is then used to design the current compensator. A simple proportional integral controller is used for the current loop.

Now, in the case of three interleaved phases, the current is simply three times more as the same duty cycle is provided to each leg. Hence, the plant model is given as 公式 3.

$$H_{p\_i} = \frac{i_{Li}^{*}}{D} = 3 \times \frac{1}{K_{v\_gain}} \times K_{i\_gain} \times K_{i\_fltr} \times G_d \times \frac{1}{Z_i} \quad (3)$$

This model is verified on this design using the SFRA library. 图 10 shows the model versus measured open loop frequency response, which shows good correlation between the two.

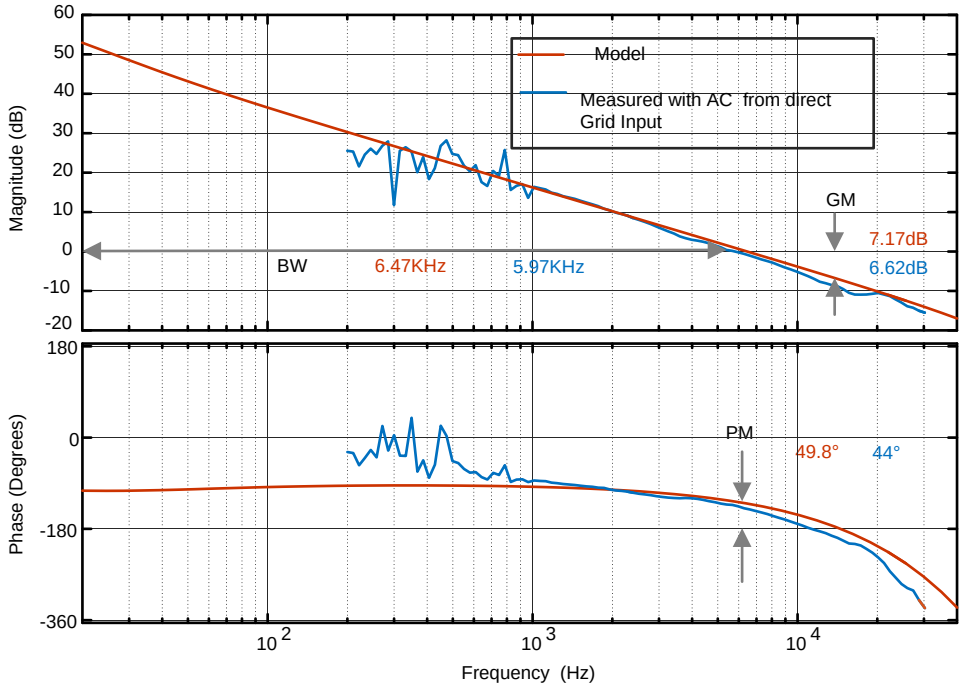

图 10. Gi, Current Open Loop Gain Measured Verus Modelled

2.4.3 DC Bus Regulation Loop

The DC bus regulation loop is assumed to provide the power reference. The power reference is then divided by the square of the line voltages RMS to provide the conductance, which is further multiplied by the line voltage giving the instantaneous current command.

Small signal model of the DC bus regulation loop is developed by linearizing 公式 4 around the operating point.

$$i_{DC} v_{bus} = \eta V_{Nrms} i_{Nrms} \rightarrow \hat{i}_{DC} = \eta \frac{\overline{V}_{Nrms}}{\overline{V}_{bus}} i_{Li} \quad (4)$$

For a resistive load the bus voltage and current are related as shown in 公式 5.

$$\hat{V}_{bus} = \frac{R_L}{1 + sR_L C_o} \hat{i}_{DC} \quad (5)$$

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The DC voltage regulation loop control model can be drawn as shown in 图 11. An additional Vbus feedforward is applied to make the control loop independent of the bus voltage, and hence, the plant model for the bus control can be written as 公式 6.

$$H_{p\_bus} = H_{load} \times \eta \times K_{i\_gain} \times K_{v\_gain} \times K_{v\_flt} \quad (6)$$

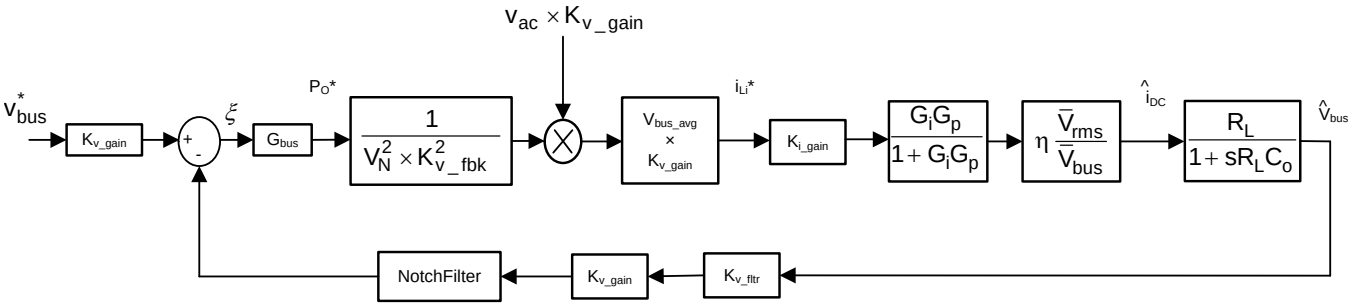

图 11. DC Voltage Loop Control Model

Using 图 11, a proportional integrator (PI) compensator is designed for the voltage loop. The bandwidth of this loop is kept low as it is in conflict with the THD under steady state.

SFRA library is used to measure the frequency response on the voltage loop and verify the model. 图 12 shows the modelled versus measured plots for the voltage loop.

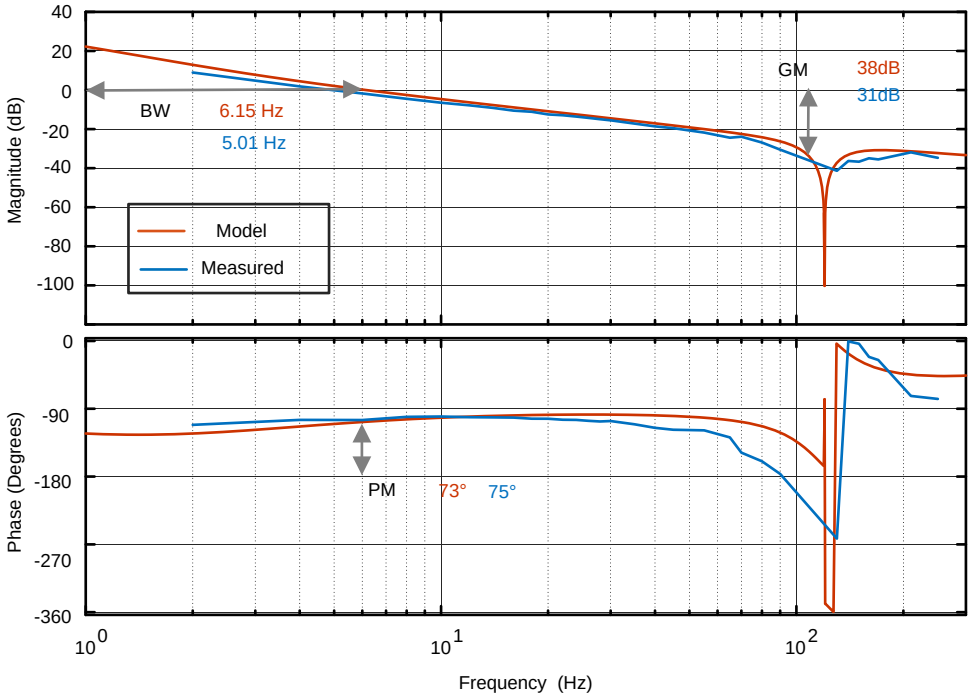

图 12. Gv, Voltage Loop Modeled Versus Measured

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2.4.4 Soft Start Around Zero Crossing for Eliminate or Reduce Current Spike

Zero crossing current spikes is a challenging issue for TTPL PFC topologies. This issue is solved by implementing a soft start scheme with a state machine to turn on and off switches in a particular sequence.

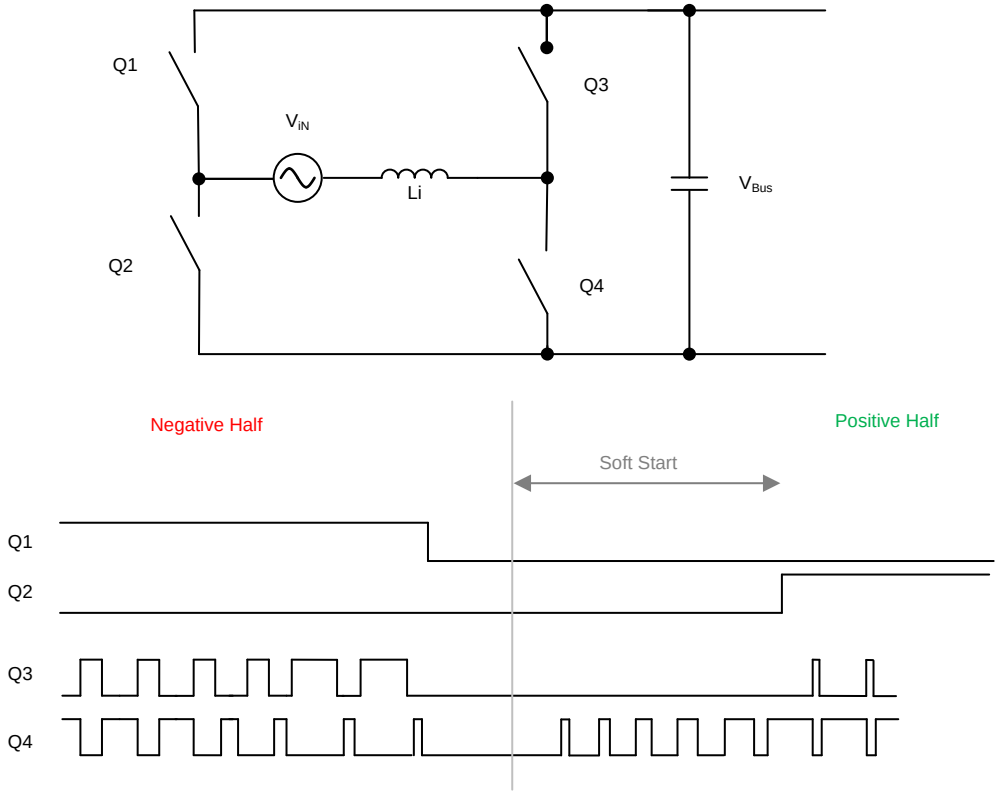

图 13. PWM Sequence With Soft Starting to Reduce Current Spike at Zero Crossing

图 13 shows the switching sequence when the AC wave goes from negative to positive. During the negative half Q1 is ON, Q3 is the active FET, and Q4 is the sync FET. During this time the voltage across Q2 is the DC bus voltage. When the AC cycle changes, Q2 must be on 100% or close to 100%. If Q2 is turned ON immediately, a huge positive spike results. Therefore, a soft-start sequence is used to turn Q4 ON as shown in 图 13. The tuning of this soft start depends on the inductance value and other power stage parameters such as device Coss.

Another reason for a negative current spike around zero crossing is the relatively low AC voltage around the zero crossing. When Q3 is turned ON, though the duty cycle is low, a high-voltage difference is applied and can result in a high negative current spike. Therefore, a sufficient delay is applied before Q3 starts switching back again.

Similarly, Q2 is turned on after some delay after the soft start has started.

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3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

This section details the hardware and the different sections on the board. If only using the firmware of the design through powerSUITE, this section may not be valid.

3.1.1.1 Base Board Settings

The design follows a HSEC control card concept, and any device for which HSEC control card is available from the C2000 MCU product family can be potentially used on this design. The key resources used for controlling the power stage on the MCU are listed in 表 2 . 图 14 shows the key power stage and connectors on the design board. 表 3 lists the key connectors and their functions. To get started:

1. Make sure no power source is connected to the design.
2. Insert the control card in the J600 slot.
3. Connect a 12-V, 1-A DC power supply at TP604. For the ground terminal, use TP606 . Do not power up the supply.
4. Connect a 5-V, 1-A DC power supply at TP608. For the ground terminal, use TP609. Do not power up the supply.
5. Turn both the 12-V and 5-V power supply ON. The LED on the control card lights up and indicates the device is powered.

> 注: The bias for the MCU is separated from the power stage, which enables safe bring up of the system in this set of instructions.

6. To connect JTAG, use a USB cable from the control card and connect it into a host computer.
7. A single phase AC power supply can be connected to the input J100. Optionally in some incremental builds a DC source may be required to test out the system safely.
8. A resistive load of approximately 500 Ω and 400 W should be connected to the output at J104.
9. Current and voltage probes can be connected to observe the input current, input voltage, and output voltages, as shown in 图 14.

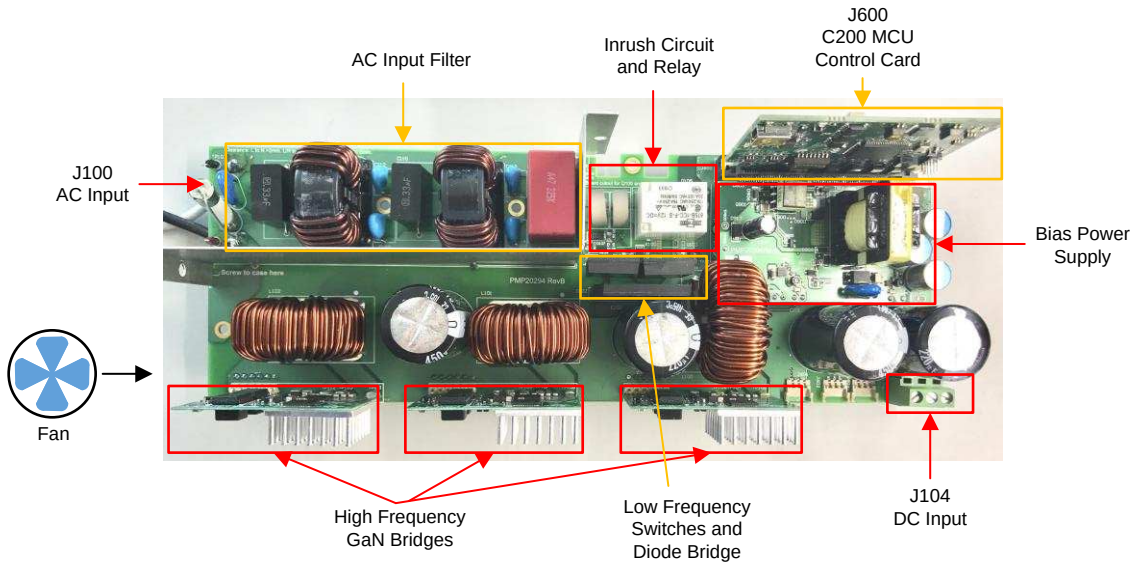

图 14. Board Overview

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表 2. Key Controller Peripherals Used for Control of Power Stage on Board

SIGNAL NAME	HSEC PIN NUMBER	FUNCTION
PWM-1A	49	PWM: low-frequency MOSFET leg, high-side switch
PWM-1B	51	PWM: low-frequency MOSFET leg, low-side switch
PWM-2A	53	PWM: high frequency GaN leg, high side switch, phase one
PWM-2B	55	PWM: high-frequency GaN leg, low-side switch, phase one
PWM-3A	50	PWM: high-frequency GaN leg, high-side switch, phase two
PWM-3B	52	PWM: high-frequency GaN leg, low-side switch, phase two
PWM-4A	54	PWM: high-frequency GaN leg, high-side switch, phase three
PWM-4B	56	PWM: high-frequency GaN leg, low-side switch, phase three
Iac	18	ADC with CMPSS: AC return current measurement
IL1	15	ADC with CMPSS : inductor current measurement Ph1
IL2	21	ADC with CMPSS : inductor current measurement Ph2
IL3	25	ADC with CMPSS : inductor current measurement Ph3
VL	20	ADC: AC voltage line
VN	17	ADC: AC voltage neutral
Vbus	24	ADC: bus voltage
In Rush Relay	57	GPIO: used to control the inrush relay
GaN Fault 1	58	GPIO: GaN fault signal phase one
GaN Fault 2	60	GPIO: GaN fault signal phase two
GaN Fault 3	62	GPIO: GaN fault signal phase three
AC Current Sense Gain Change	63	GPIO: controls the gain stage

表 3. Key Connectors and Function

CONNECTOR NAME	FUNCTION
J100	Input AC voltage
J104	Output DC bus voltage
TP604	Input bias supply, 12-VDC, 1 A
TP608	Input bias supply, 5-VDC, 1 A
TP606/TP609	GND
J600	HSEC control card connector slot

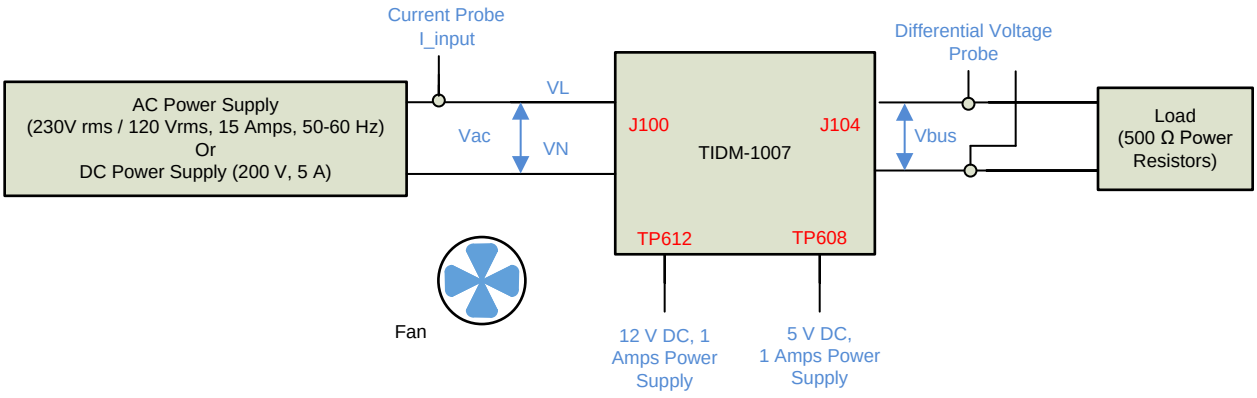

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图 15. Hardware Setup to Run Software

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3.1.1.2 Control Card Settings

Certain settings on the device control card are required to communicate over JTAG and use the isolated UART port. The user must also provide a correct ADC reference voltage. The following are the required settings for revision A of the F280049M control card. One can also refer to the info sheet located inside C2000Ware at *<install_path>\c2000ware\boards\controlcards\TMDSCNCD280049M* or alternatively get it from the document http://www.ti.com/lit/ug/spruic4/spruic4.pdf.

1. S1:A on the control card must be set on both ends to “ON (up) ” position to enable JTAG connection to the device and UART connection for SFRA GUI. If this switch is “OFF (down)” one cannot use the isolated JTAG built in on the control card nor can SFRA GUI communicate to the device.
2. J1:A is the connector for the USB cable that is used to communicate to the device from a host PC on which Code Composer Studio ™ (CCS) runs.
3. A 3.3-V reference is desired for the control loop tuning on this design. Internal reference of the F28004x is used and for this S8 switch must be moved to the left i.e. pointing to VREFHI
4. A capacitor is connected between the isolated grounds on the control card, C26:A. It is advised to remove this capacitor for the best performance of this reference design.

3.1.2 Software

The software of this design is available inside C2000Ware Digital Power SDK and is supported inside the powerSUITE framework.

3.1.2.1 Opening Project Inside CCS

To start:

1. Install CCS from the *Code Composer Studio (CCS) Integrated Development Environment (IDE)* tools folder, version 7.4 or above is recommended.
2. Open CCS. Go to *View → CCS App Center*. Under *Code Composer Studio Add-ons*, make sure GUI Composer Runtime v1.0 is installed. If not installed, install GUI Composer Runtime v1.0.
3. Install C2000Ware DigitalPower SDK at the *C2000Ware Digital Power SDK* tools folder.
   - Note: powerSUITE is installed with the SDK in the default install.
4. Close CCS, and open a new workspace. CCS automatically detects powerSUITE. A restart of CCS may be required for the change to be effective.
5. Go to *View → Resource Explorer*. Under the TI Resource Explorer, go to *C2000Ware DigitalPower SDK* .

To open the reference design software as it is (opens firmware as it was run on this design and hardware, requires the board to be exactly the same as this reference design, and does not allow modification through the powerSUITE GUI inside the project).

1. Under *C2000Ware DigitalPower SDK*, select *Development Kits → CCM Totem Pole PFC TIDM-1007*, and click on *Run <device> Project*.
2. These steps import the project, and the development kit or designs page show up. This page can be used to browse all the information on the design including this user guide, test reports, hardware design files, and so forth.
3. Click *Run <device_name> Project*.
4. This action imports the project into the workspace environment, and a cfg page with a GUI similar to 图 16shows up.
   - Note: As this project is imported from the development kit and reference design page, modifications to the power stage parameters through the GUI are not allowed.
5. If this GUI page does not appear, refer to the FAQ section under *powerSUITE* in the *C2000Ware Digital Power SDK* resource explorer.

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Open reference design software for adaptation. The user can modify power stage parameters, which are then used to create the model of the power stage in Compensation Designer and can also modify scaling values for voltages and currents for a custom design.

1. Under*C2000Ware Digital Power SDK*click on *powerSUITE* →*Solution Adapter Tool* ().
2. Select *Single Phase CCM Totem Pole PFC* from the list of solutions presented.
3. Select the device this solution must run on the next page.
4. Once the icon is clicked, a pop-up window shows up asking for a location to create the project. One can also save the project inside the workspace itself. Once the location is specified, a project is created, and a GUI page appears with modifiable options for the solution (图 16).
5. This GUI can be used to change the parameters for an adapted solution, like power rating, inductance, capacitance, sensing circuit parameters, and so forth.
6. If this GUI page does not appear, refer to the FAQ section under *powerSUITE* in the *C2000Ware DigitalPower SDK* resource explorer.

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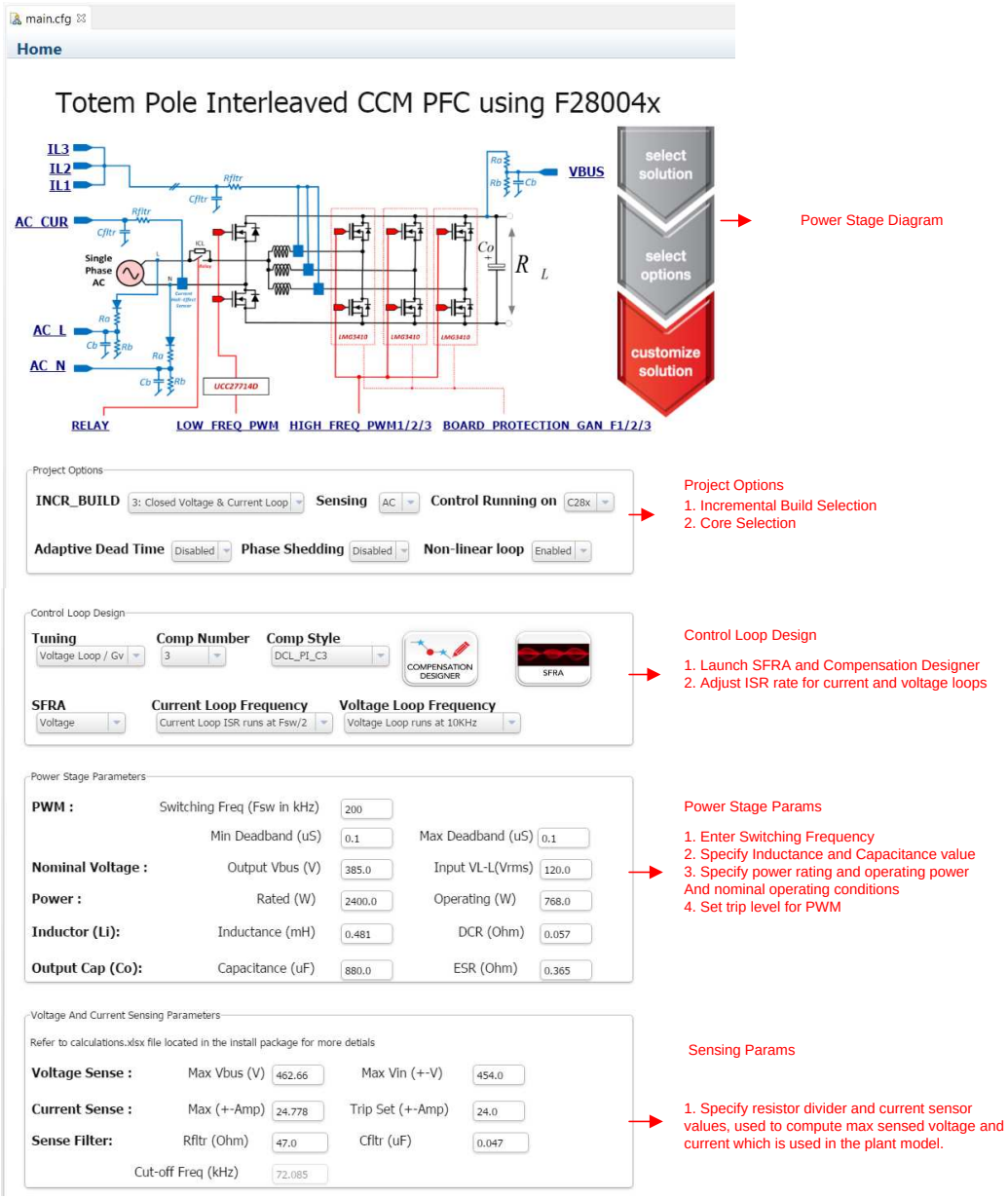

图 16. powerSUITE Page for CCM TTPL PFC Solution

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3.1.2.2 Project Structure

Once the project is imported, the project explorer appears inside CCS as shown in 图 17.

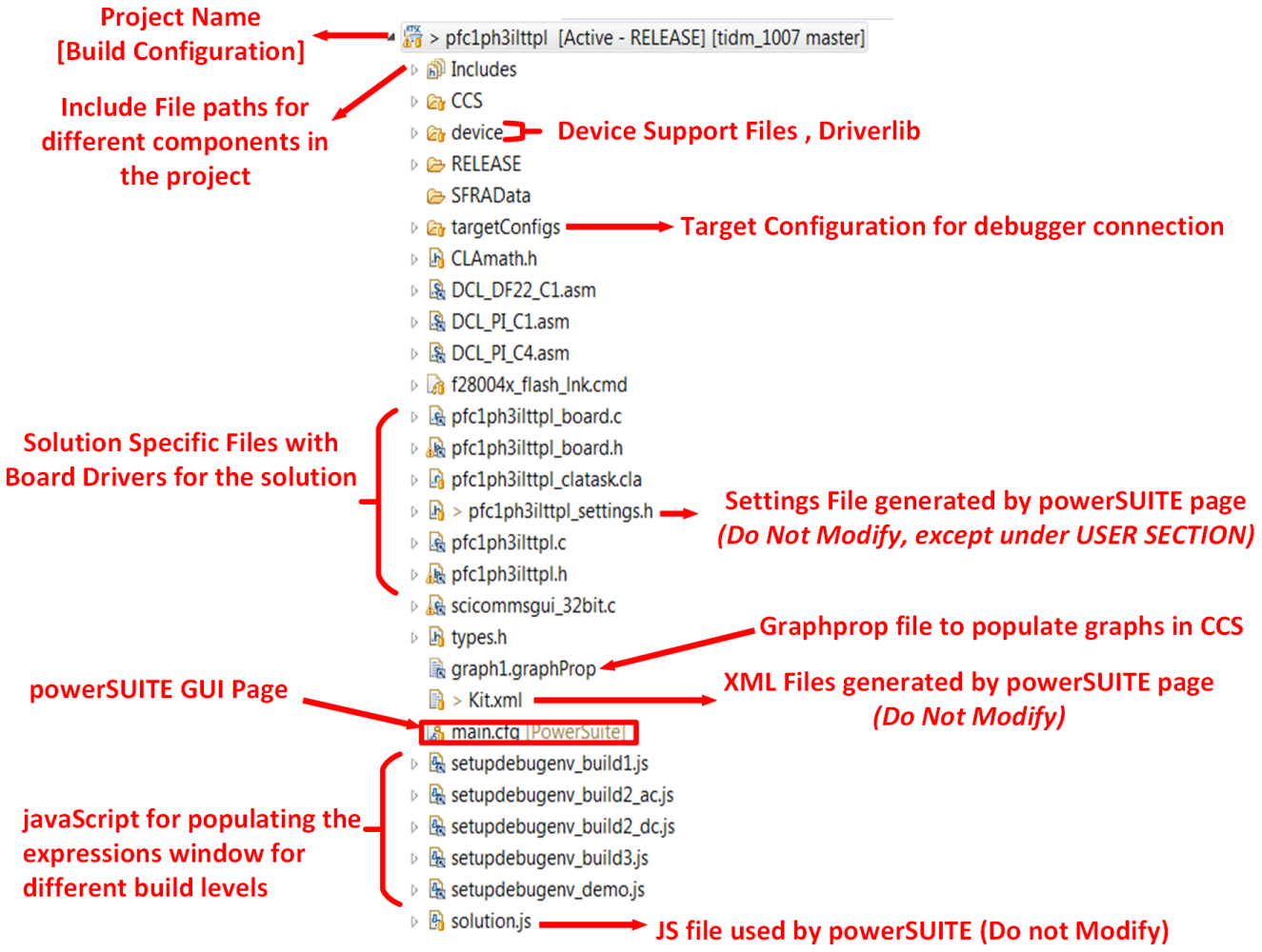

图 17. Project Explorer View of Solution Project

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The general structure of the project is shown in 图 18.

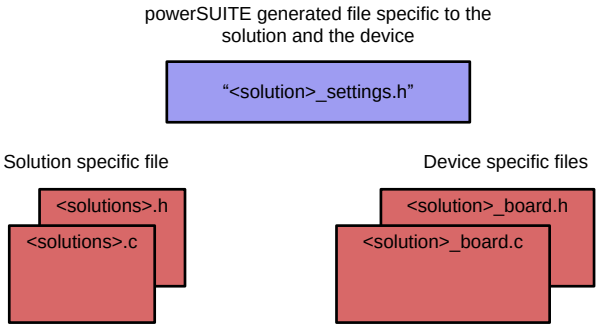

图 18. Project Structure Overview

注: 图 18 shows the project for F28004x; however, if a different device is chosen from the powerSUITE page, the structure is similar.

Solution specific and device independent files are *<solution>.c/h*. This file consist of the main.c file of the project and is responsible for the control structure of the solution.

For this design <solution> is *pfc1ph3ilttpl*.

Board-specific and device-specific files are *<solution>_board.c/h*. This file consists of device specific drivers to run the solution.

The powerSUITE page can be opened by clicking on the *main.cfg* file, listed under the project explorer. The powerSUITE page generates the *<solution>_settings.h* file. This file is the only file used in the compile of the project that is generated by the powerSUITE page. The user must not modify this file manually except under user section area, as the changes are overwritten by powerSUITE every time the project is saved.

The *Kit.xml* and *solution.js* files are used internally by the powerSUITE and must also not be modified by the user. Any changes to these files results in project not functioning properly.

The setupdebugenv_build.js are provided to autopoulate the watch window variables for different builds

The *.graphProp files is provided to auto populate settings for the data logger graph

The project consists of an interrupt service routine, which is called every PWM cycle, and a current controller is run inside this ISR. In addition to this, there is a slower ISR of approximately 10 kHz that is called for running the voltage loop and the instrumentation ISR. A few background tasks (A0-A4 and B0-B4) are called in a polling fashion and can be used to run slow tasks for which absolute timing accuracy is not required, such as SFRA background and so on.

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图 19 shows the software flow diagram of the firmware

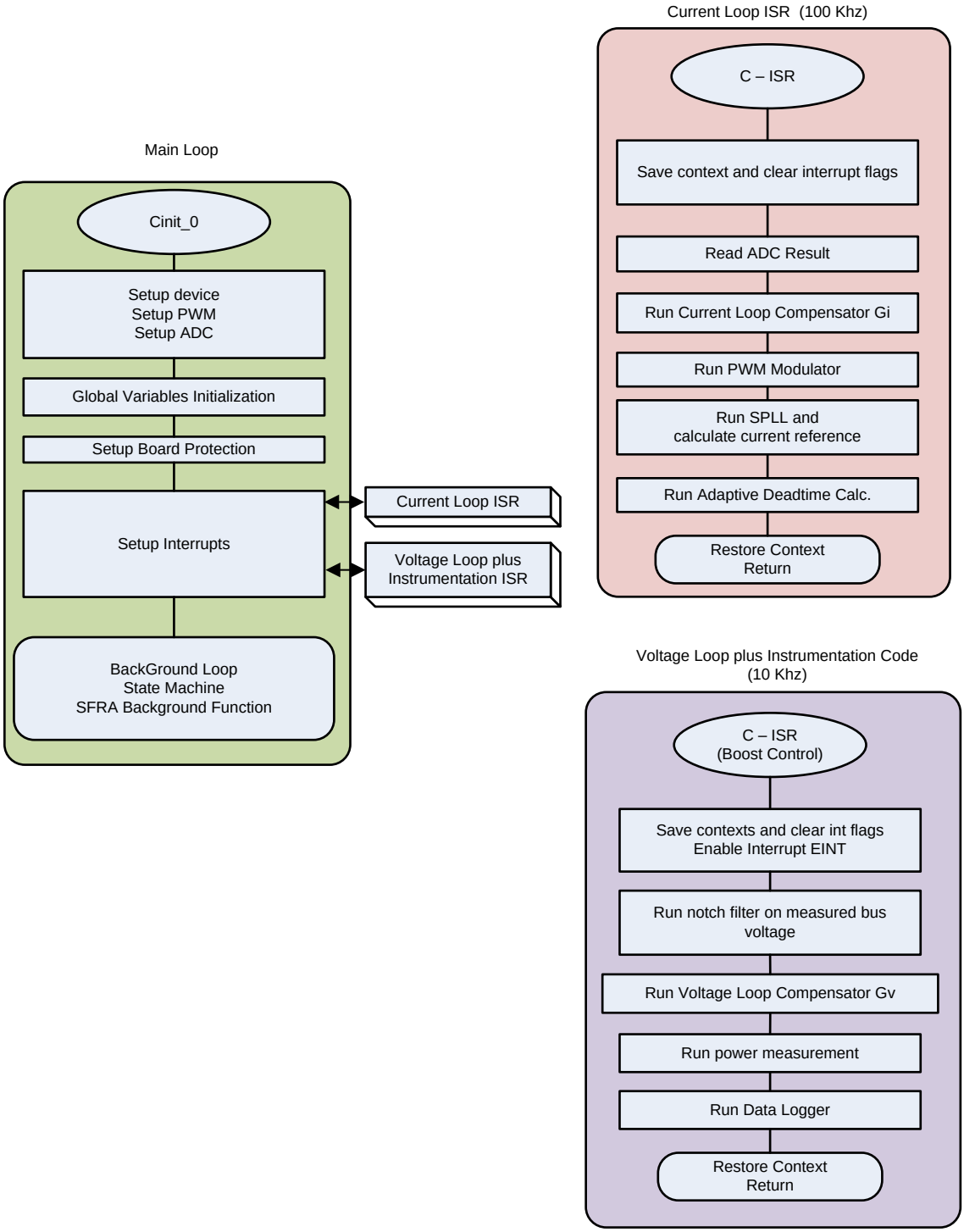

图 19. Project Structure Image

To simplify the system bring up and design the software of this reference design is organized in four incremental builds (INCR_BUILD):

- INCR_BUILD 1: Open Loop Check, DC
- INCR_BUILD 2: Closed Current Loop : DC

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- INCR_BUILD 2: Closed Current Loop : AC
- INCR_BUILD 3: Closed Voltage and Current Loop

These build levels are detailed in 节 3.1.2.4. If using the reference design hardware, make sure the hardware setup is completed as outlined in 节 3.1.1.

3.1.2.3 Using CLA on C2000 MCU to Alleviate CPU Burden

The control law accelerator (CLA) is a co-processor available on the C2000 MCU family of devices. This co-processor enables offloading the control-ISR functions from the main C28x CPU core.

To run the control ISR on the CLA for solutions supported in powerSUITE, selection is achieved through a drop-down menu on the powerSUITE CFG page. The software structure of the powerSUITE solution is designed such that offloading the task to the CLA is simply a drop-down menu selection. The code is not duplicated and a single source for the solution algorithm is maintained even when code is run on the CLA or the C28x. This configuration enables flexible debugging of the solution.

The CLA features of each device varies slightly. For example, on the F2837xD, F2837xS, and F2807x, the CLA can support only one task at a given time, and there is no nesting capability. This configuration means that the task is not interruptible. Only one ISR can be offloaded to the CLA. On the F28004x, the CLA supports a background task from which a regular CLA task can nest. This configuration enables offloading two ISRs on the CLA.

The CLA supports a background task from which it can nest into a CLA task. This configuration allows offloading two ISR functions to the CLA. For the F28004x, both the control ISR (100 kHz) for the current loop and the voltage loop and instrumentation ISR (10 kHz) are offloaded to the CLA. On the F28004x, the CPU use is approximately 42% for the 100 kHz loop (not including advanced options such as phase shedding, adaptive dead time, SFRA running, and so forth) and 11% for the 10 kHz loop that runs the voltage loop and instrumentation functions. Thus, the total CPU use is approximately 53%. With the CLA option, the CPU burden is reduced to 0% when both ISRs are offloaded to the CLA.

For more information on the CLA, visit the CLA Hands-On Workshop and the respective device technical reference manuals.

3.1.2.4 Running the Project

3.1.2.4.1 INCR_BUILD 1: Open Loop, DC

In this build the board is excited in open loop fashion with a fixed duty cycle. The duty cycle is controlled with dutyPU_DC variable. This build verifies the sensing of feedback values from the power stage and also operation of the PWM gate driver and ensures there are no hardware issues. Additionally calibration of input and output voltage sensing can be performed in this build. The software structure for this build is shown in 图 20. There are two ISR in the system: fast ISR for the current loop and a slower ISR to run the voltage loop and instrumentation functions. Modules that are run in each ISR are shown in 图 20.

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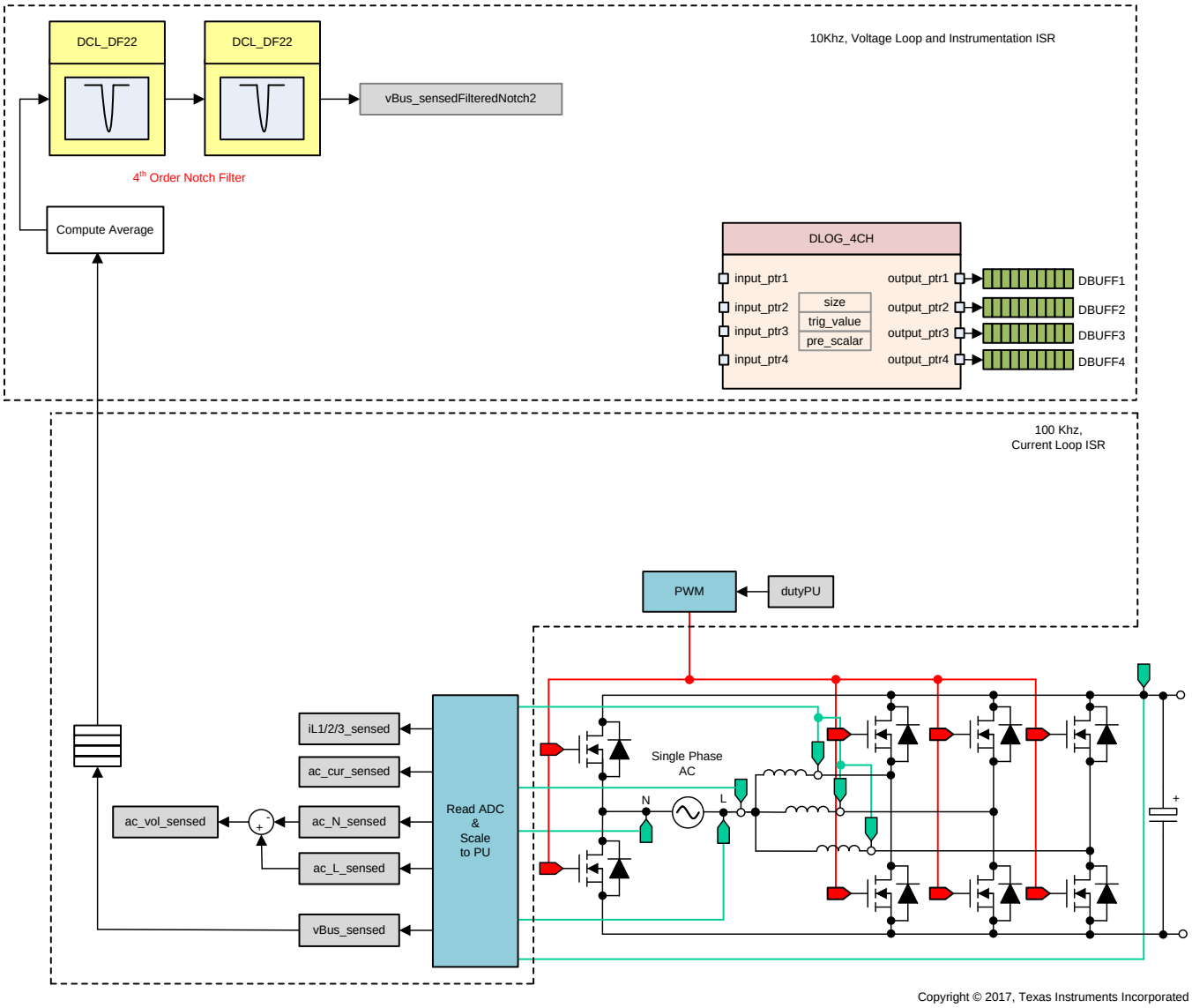

图 20. Build Level 1 Control Software Diagram: Open Loop Project

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Hardware setup is assumed to be similar to what was outline in the previous section. 图 21 recaps the hardware setup for build level 1 test.

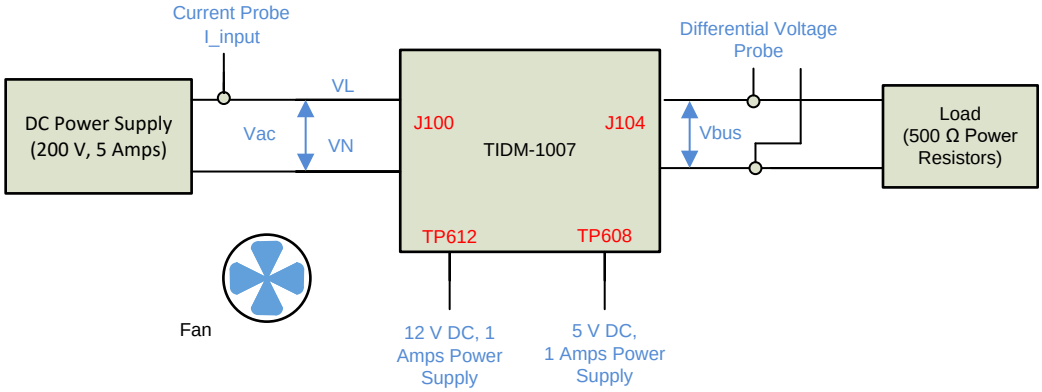

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图 21. HW Setup for Build Level 1

3.1.2.4.1.1 Setting Software Options for BUILD 1

1. powerSUITE Settings : On the powerSUITE page select under *Project Options* section:
   - Select *Open Loop* for the build level under INCR_BUILD option.
   - Select input to be DC under INPUT options
   - Also disable the other options such as *Non Linear Voltage Loop, Adaptive Deadtime and Phase shedding*
2. If this is an adapted solution, edit the setting under *Voltage and Current Sensing Parameters* . One can refer to the *calculations.xlsx* file which is available under the C2000Ware DigitalPower SDK Install directory at *<install_location>\solutions\tidm_1007\hardware* for details on sensing circuit and how max range is computed for the powerSUITE page
3. Under Power Stage Parameters specify the switching frequency, the dead band, and the power rating. Save the page.

3.1.2.4.1.2 Building and Loading Project

1. Right click on the project name, and click *Rebuild Project*.
2. The project builds successfully.
3. In the *Project Explorer* make sure the correct target configuration file is set as Active under trageteonfigs (图 17).
4. Then click *Run → Debug*. This action launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU that the debug must be performed. In this case, select CPU1.
5. The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.

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3.1.2.4.1.3 Setup Debug Environment Windows

1. To add the variables in the watch and expressions window, click *View* → *Scripting Console* to open the scripting console dialog box. On the upper-right corner of this console, click on open then browse to the *setupdebugenv_build1.js* script file located inside the project folder. This script file populates the watch window with appropriate variables required to debug the system. Click on the Continuous Refresh button on the watch window to enable continuous update of values from the controller. The watch window appears as shown in 图 22.

Variables | Expressions | Registers | Breakpoints

Expression	Type	Value	Address
buildInfo	enum enum_BuildLevel	BuildLevel1_OpenLoop_DC	0x0000A817@Data
guiVbus	float	-0.000226858858	0x0000A87E@Data
guiVin	float	-0.714660585	0x0000A876@Data
guiIi	float	0.0891165435	0x0000A874@Data
ac_cur_sensed	float	0.00343942642	0x0000A8A4@Data
clearTrip	int	0	0x0000A827@Data
EPwm1Regs.TZFLG	Register	0x0000	
EPwm2Regs.TZFLG	Register	0x0000	
dutyPU	float	0.5	0x0000A858@Data
dutyPU_DC	float	0.5	0x0000A85E@Data
vBus_sensed	float	0.0	0x0000A8C0@Data
iL1_sensed	float	-0.00341796875	0x0000A8C4@Data
iL2_sensed	float	-0.00830078125	0x0000A8C6@Data
iL3_sensed	float	-0.00732421875	0x0000A8AA@Data
Add new expression			

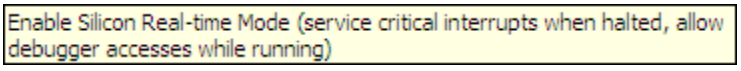
图 22. Build Level 1 Expressions View

2. Run the project by clicking on 
3. Now Halt the processor by using the *Halt* button on the toolbar (

3.1.2.4.1.4 Using Real-Time Emulation

Real-time emulation is a special emulation feature that allows windows within CCS to be updated while the MCU is running. This feature allows graphs and watch views to update but also allows the user to change values in watch or memory windows and see the effect of these changes in the system without halting the processor.

1. Enable real-time mode by hovering the mouse on the buttons on the horizontal toolbar and clicking the  button.



2. A message box may appear. If so, select *YES* to enable debug events. This action sets bit 1 (DGBM bit) of status register 1 (ST1) to a *0*. The DGBM is the debug enable mask bit. When the DGBM bit is set to *0*, memory and register values can be passed to the host processor for updating the debugger windows.

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3.1.2.4.1.5 Running Code

1. Now run the project again by clicking on  .
2. In a few seconds the inrush relay clicks, the software is programmed to do so in the build level with DC. The trip clears, and a duty cycle of 0.5 is applied.
3. In the watch view, check if the guiVin, guiVbus, guiIi, variables are updating, periodically.
   - Note: As no power is applied right now, this value is close to zero.
4. Now slowly increase the input DC voltage from zero to 120 V. The output voltage shows a boosted voltage as a steady duty cycle of 0.5 PU is applied as default setting. If a high current is drawn, verify if the voltage terminals are swapped. If true, reduce the voltage to zero first and correct the issue before resuming the test
5. Verifying the voltage sensing: Make sure *guiVin* and *guiVbus* display the correct values, for 120-V DC input, guiVbus is close to 240V. This verifies the voltage sensing of the board in some manner.
6. Verifying the current sensing: Notice the *guiIIi* for the given test condition; this value is close to 1 A.

Variables | Expressions | Registers | Breakpoints

Expression	Type	Value	Address
buildInfo	enum enum_BuildLevel	BuildLevel1_OpenLoop_DC	0x0000A817@Data
guiVbus	float	236.679321	0x0000A87E@Data
guiVin	float	117.730934	0x0000A876@Data
guiIi	float	1.01184416	0x0000A874@Data
ac_cur_sensed	float	0.0393730402	0x0000A8A4@Data
clearTrip	int	0	0x0000A827@Data
EPwm1Regs.TZFLG	Register	0x0000	
EPwm2Regs.TZFLG	Register	0x0000	
dutyPU	float	0.5	0x0000A858@Data
dutyPU_DC	float	0.5	0x0000A85E@Data
vBus_sensed	float	0.511474609	0x0000A8C0@Data
iL1_sensed	float	0.0161132813	0x0000A8C4@Data
iL2_sensed	float	0.01171875	0x0000A8C6@Data
iL3_sensed	float	0.0141601563	0x0000A8AA@Data
Add new expression			

图 **23. Build Level 1: Watch Expression Showing Measured Voltage and Currents**

7. This verifies at a basic level the PWM driver and connection of hardware, user can change the dutyPU_DC variable to see operation under various boost conditions.
8. Once finished, reduce the input voltage to zero and watch for the bus voltages to reduce down to zero.
9. This completes the check for this build, the following items are verified on successful completion of this build:
   - Sensing of voltages and currents and scaling to be correct
   - Interrupt generation and execution of the BUILD 1 code in the current loop ISR and Voltage Loop Instrumentation ISR
   - PWM driver and switching

   If any issue is observed a careful inspection of the hardware may be required to eliminate any build issues and so forth.
10. The controller can now be halted, and the debug connection terminated.
11. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the *Halt* button on the toolbar () or by using *Target* → *Halt*. Then take the MCU out of real-time mode by clicking on  . Finally, reset the MCU by clicking on  .
12. Close CCS debug session by clicking on *Terminate Debug Session* (*Target* → *Terminate all*). 

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3.1.2.4.2 INCR_BUILD 2: Closed Current Loop DC

In this build, BUILD 2, the inner current loop is closed that is the inductor current is controlled using a current compensator Gi. Both DC bus and output voltage feed forward are applied to the output of this current compensator to generate the duty cycle of the inverter, 公式 7. This makes the plant for the current compensator simple and a proportional (P) controller can be used to tune the loop of the inner current. The model for the current loop was derived in section 节 2.4.2. Complete software diagram for this build is illustrated in 图 24.

$$\text{duty1PU} = \frac{(\text{ac\_cur\_meas} - \text{ac\_cur\_ref\_inst}) \times \text{Gi} + \text{ac\_vol\_sensed}}{\text{vBus\_sensed}} \tag{7}$$

Complete software diagram for this build as illustrated in 图 24.

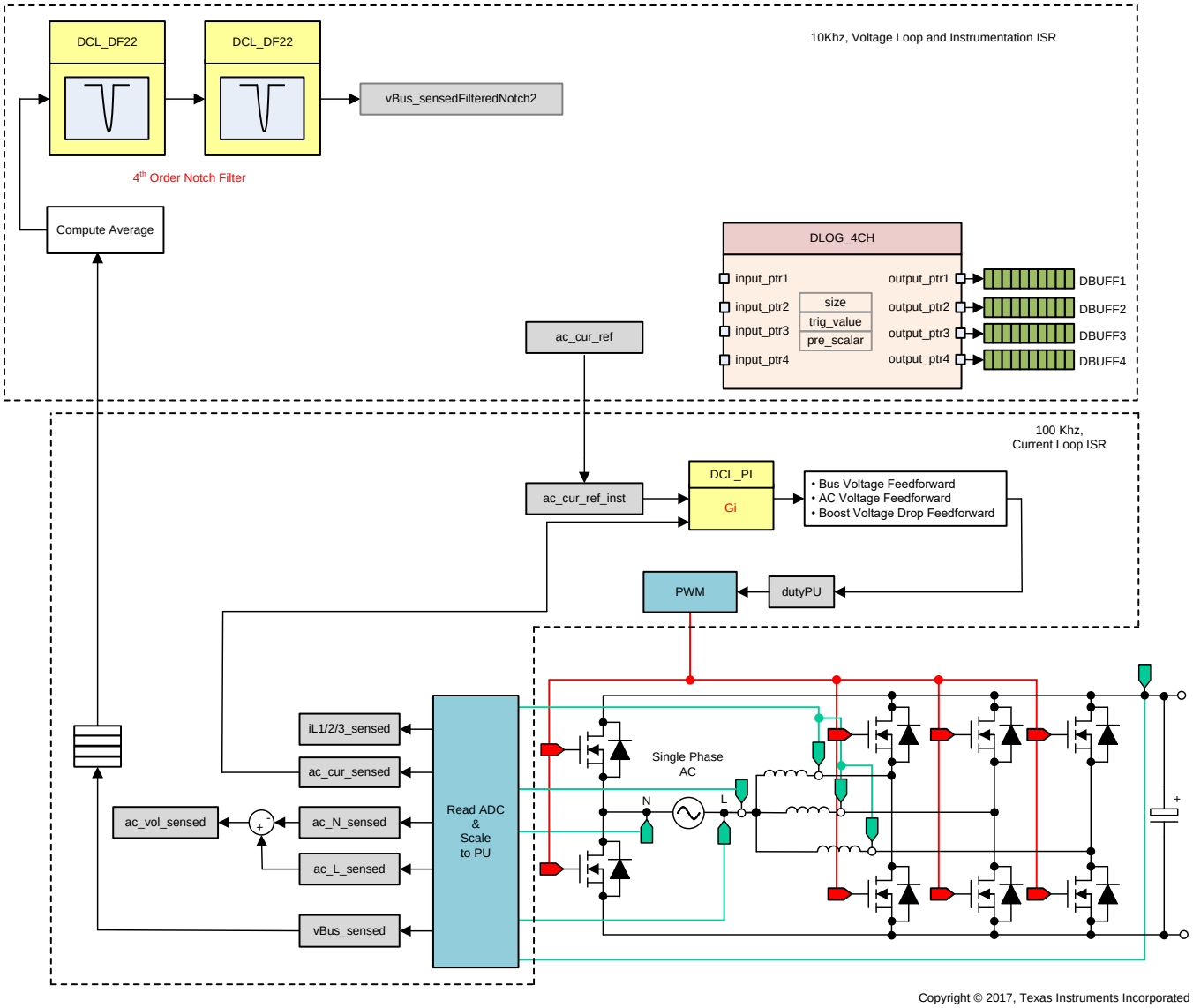

图 24. Build Level 2 Control Software Diagram: Closed Current Loop

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3.1.2.4.2.1 Setting Software Options for BUILD 2

1. Make sure the hardware is setup as outlined in 图 21 . Do not supply any high voltage (HV) power to the board yet.
2. powerSUITE Settings : On the powerSUITE page select under *Project Options* section:
   - Select *Closed Current Loop* for the build level under INCR_BUILD option.
   - Select input to be DC under INPUT options
   - Also disable the other options such as *Non Linear Voltage Loop, Adaptive Deadtime and Phase shedding*
3. Assuming all other options are same as specified earlier in 节 3.1.2.4.1.1
4. Under *Control Loop Design*, options for the current loop tuning automatically be selected (*Tuning → Current Loop → COMP1 → DCL_PI_C1*). Now click on the *Compensation Designer* icon ( ).

3.1.2.4.2.2 Designing Current Loop Compensator

1. Compensation Designer launches with the model of the current loop plant with parameters specified on the powerSUITE page. PI-based controller can be tuned from a pole zero perspective to ensure stable closed loop operation. Stability of the system when using the designed compensator can be verified by observing the gain and phase margins on the open loop transfer function plot in the Compensation Designer, as shown in 图 25.

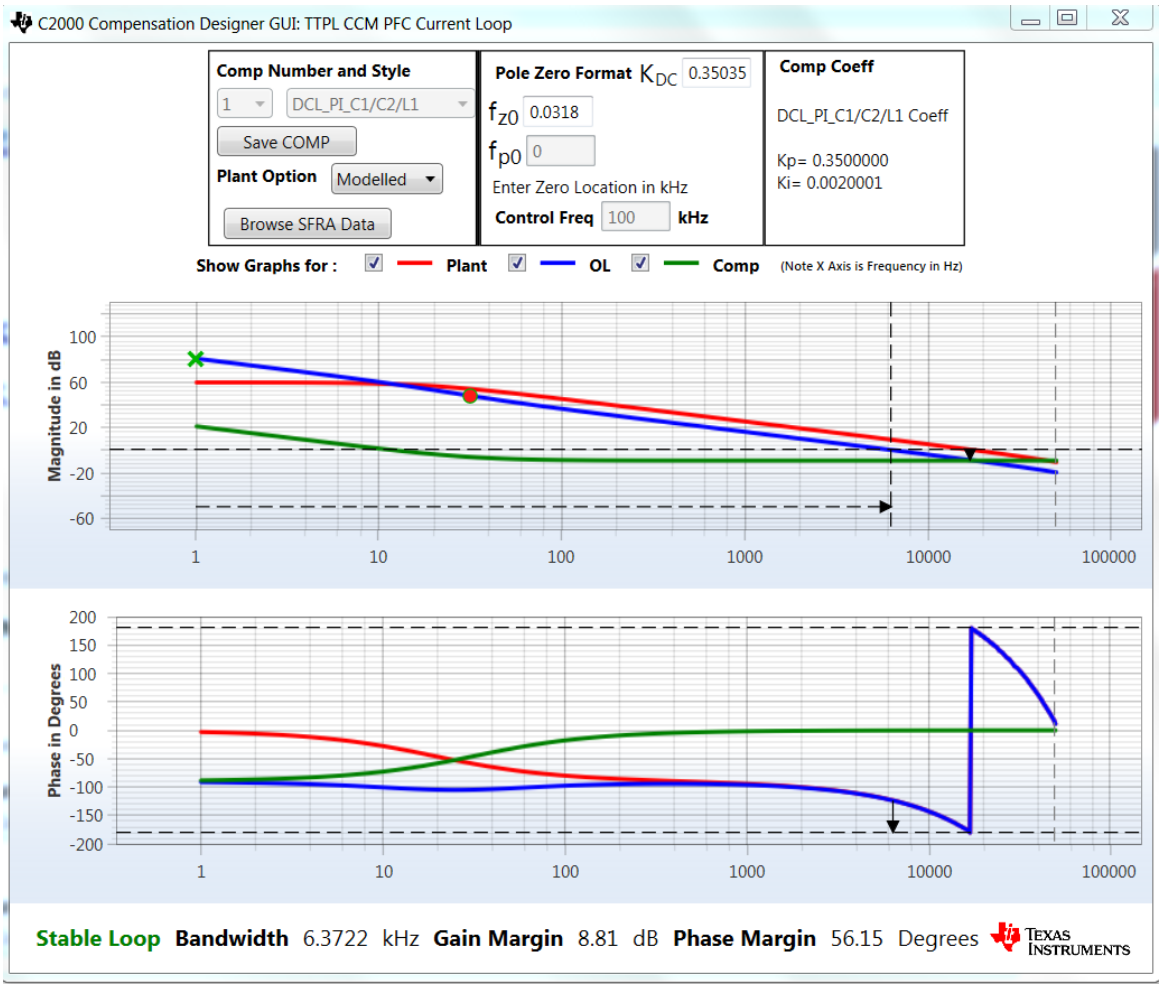

图 25. Current Loop Design Using Compensation Designer

2. Once satisfied with the open loop gain, click on *Save COMP*. This action saves the compensator values into the project.

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- Note: If the project was not selected from the solution adapter, changes to the compensator are not allowed. Select the solution through the solution adapter.

3. Close the Compensation Designer, and return to the powerSUITE page.

3.1.2.4.2.3 Building and Loading Project and Setting up Debug

1. Right click on the project name, and click *Rebuild Project*. The project builds successfully. Click *Run* → *Debug*, which launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU the debug must be performed. In this case, select CPU1. The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.
2. To add the variables in the watch and expressions window click *View* → *Scripting Console* to open the scripting console dialog box. On the upper right corner of this console, click on *Open* to browse to the *setupdebugenv_build2_dc.js* script file, which is located inside the project folder. This file populates the watch window with appropriate variables required to debug the system. Click on *Continuous Refresh* button ( ) on the watch window to enable continuous update of values from the controller. The watch window appears as 图 26.

Variables | Expressions | Registers | Breakpoints

Expression	Type	Value	Address
buildInfo	enum enum_BuildLevel	BuildLevel2_CurrentLoop_DC	0x0000A80C@Data
boardStatus	enum enum_boardStatus	boardStatus_Idle	0x0000A804@Data
clearTrip	int	0	0x0000A824@Data
closeGiLoop	int	0	0x0000A819@Data
ac_cur_ref	float	0.0299999993	0x0000A838@Data
ac_cur_sensed	float	0.0118730068	0x0000A8A4@Data
guiVbus	float	0.347434014	0x0000A846@Data
guiVin	float	-0.678055584	0x0000A86C@Data
guiIi	float	0.274688691	0x0000A86A@Data
EPwm1Regs.TZFLG	Register	0x0004	
EPwm2Regs.TZFLG	Register	0x0004	
dutyPU	float	0.00999999978	0x0000A84E@Data
dutyPU_DC	float	0.5	0x0000A84C@Data
iL1_sensed	float	-0.00537109375	0x0000A8AE@Data
iL2_sensed	float	-0.00537109375	0x0000A8AC@Data
iL3_sensed	float	-0.00634765625	0x0000A8AA@Data
autoStartSlew	unsigned long	14	0x0000A87C@Data
Add new expression			

图 **26. Build Level 2: Closed Current Loop Expressions View**

3. Enable real-time mode by hovering the mouse on the buttons on the horizontal toolbar, and clicking the button.
4. Run the project by clicking on
5. Now Halt the processor by using the *Halt* button on the toolbar (

3.1.2.4.2.4 Running Code

1. The project is programmed to drive the inrush relay and clear the trip after a set amount of time, that is, autoStartSlew==100. The software is programmed to do so in the build level with DC. An input voltage must be applied after hitting run and before this autoslew counter reaches 100. If the counter reaches 100, before voltage is applied at the input, the code must be reset. For which the controller must be brought out of real time mode, a reset performed and restarted. Repeat steps from
2. Now run the project by clicking .

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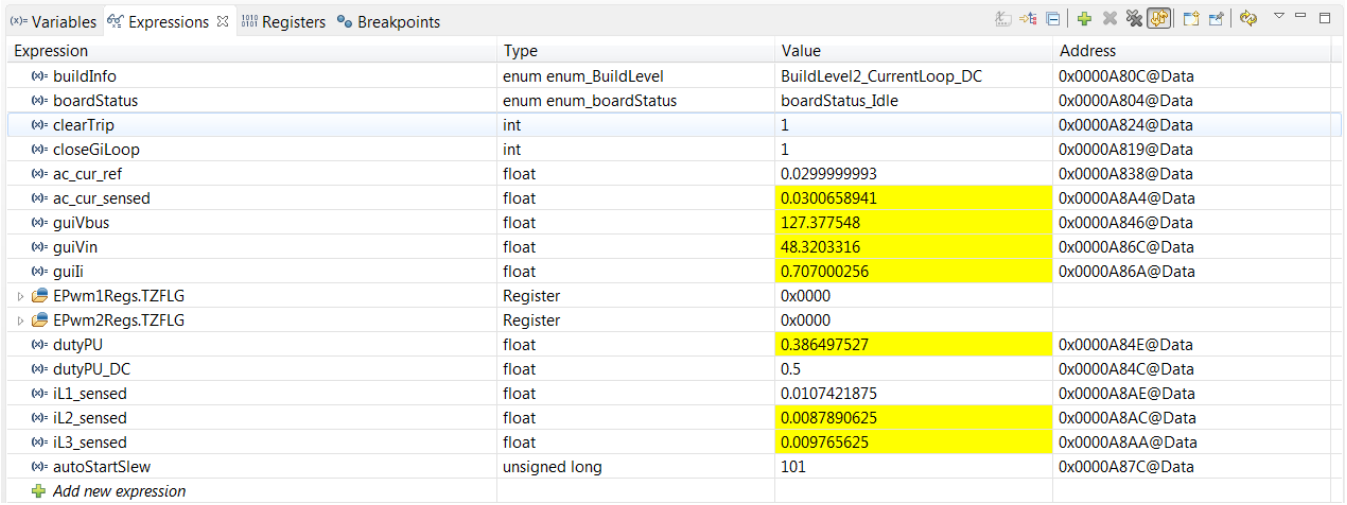
3. Apply an input voltage of approximately 50 V before the autoStartSlew reaches 100. As soon autoStartSlew reaches 100, the inrush relay is triggered, and PWM trip is cleared along with closing the current loop flag.

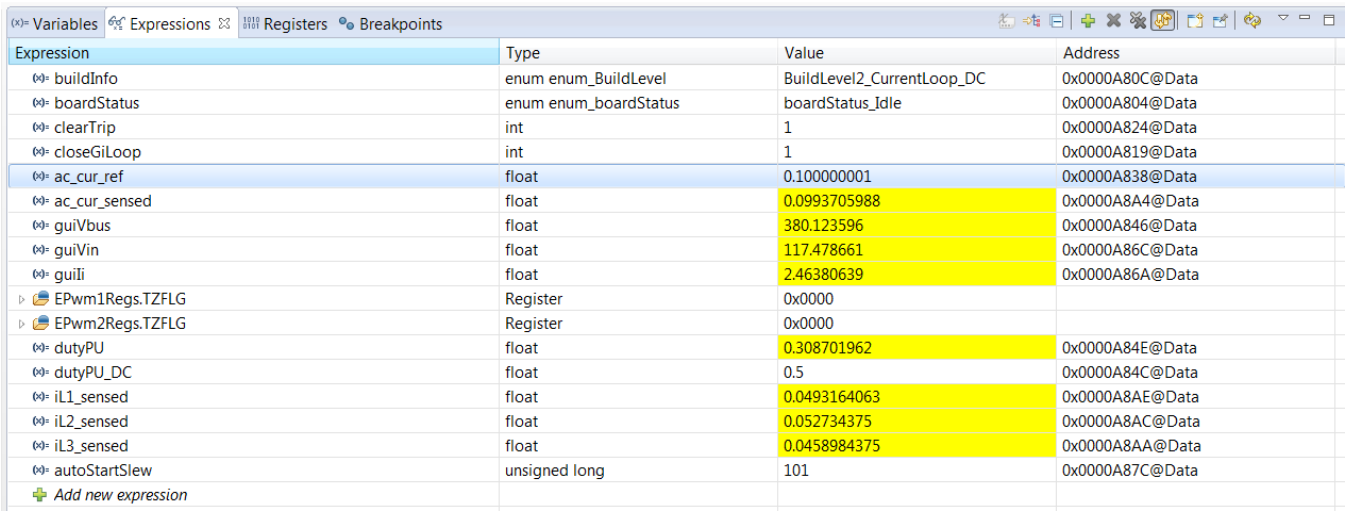


Variables | Expressions | Registers | Breakpoints

Expression	Type	Value	Address
buildInfo	enum enum_BuildLevel	BuildLevel2_CurrentLoop_DC	0x0000A80C@Data
boardStatus	enum enum_boardStatus	boardStatus_Idle	0x0000A804@Data
clearTrip	int	1	0x0000A824@Data
closeGiLoop	int	1	0x0000A819@Data
ac_cur_ref	float	0.0299999993	0x0000A838@Data
ac_cur_sensed	float	0.0300658941	0x0000A8A4@Data
guiVbus	float	127.377548	0x0000A846@Data
guiVin	float	48.3203316	0x0000A86C@Data
guiIi	float	0.707000256	0x0000A86A@Data
EPwm1Regs.TZFLG	Register	0x0000	
EPwm2Regs.TZFLG	Register	0x0000	
dutyPU	float	0.386497527	0x0000A84E@Data
dutyPU_DC	float	0.5	0x0000A84C@Data
iL1_sensed	float	0.0107421875	0x0000A8AE@Data
iL2_sensed	float	0.0087890625	0x0000A8AC@Data
iL3_sensed	float	0.009765625	0x0000A8AA@Data
autoStartSlew	unsigned long	101	0x0000A87C@Data
Add new expression			

图 27. Watch Expression, Build Level 2, DC After Closed Current Loop Operation Begins

4. The input current regulates around 0.7 A, and the output voltage boosts to approximately 128 V.
5. Now slowly increase ac_cur_ref to 0.1, that is, 2.5-A input.
6. Next slowly increase Vin = 120 V, and the output voltage will be greater than 350 V.



Variables | Expressions | Registers | Breakpoints

Expression	Type	Value	Address
buildInfo	enum enum_BuildLevel	BuildLevel2_CurrentLoop_DC	0x0000A80C@Data
boardStatus	enum enum_boardStatus	boardStatus_Idle	0x0000A804@Data
clearTrip	int	1	0x0000A824@Data
closeGiLoop	int	1	0x0000A819@Data
ac_cur_ref	float	0.100000001	0x0000A838@Data
ac_cur_sensed	float	0.0993705988	0x0000A8A4@Data
guiVbus	float	380.123596	0x0000A846@Data
guiVin	float	117.478661	0x0000A86C@Data
guiIi	float	2.46380639	0x0000A86A@Data
EPwm1Regs.TZFLG	Register	0x0000	
EPwm2Regs.TZFLG	Register	0x0000	
dutyPU	float	0.308701962	0x0000A84E@Data
dutyPU_DC	float	0.5	0x0000A84C@Data
iL1_sensed	float	0.0493164063	0x0000A8AE@Data
iL2_sensed	float	0.052734375	0x0000A8AC@Data
iL3_sensed	float	0.0458984375	0x0000A8AA@Data
autoStartSlew	unsigned long	101	0x0000A87C@Data
Add new expression			

图 28. Watch Expression, Build Level 2, DC After Closed Current Loop Operation Begins at Full Voltage

7. SFRA is integrated in the software of this build to verify the designed compensator provides enough gain and phase margin by measuring on hardware. To run the SFRA keep the project running, and from the cfg page, click on the *SFRA* icon. SFRA GUI appears.
8. Select the options for the device on the SFRA GUI. For example, for F28004x select floating point. Click on *Setup Connection*. On the pop-up window uncheck the boot on connect option, and select an appropriate COM port. Ensure *Boot on Connect* is deselected. Click *OK*. Return to the SFRA GUI, and click *Connect*.

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9. The SFRA GUI connects to the device. A SFRA sweep can now be started by clicking *Start Sweep*. The complete SFRA sweep takes a few minutes to finish. Activity can be monitored by seeing the progress bar on the SFRA GUI and also checking the flashing of blue LED on the back on the control card that indicates UART activity. Once complete, a graph with the open loop plot appears. Comparing this with the measured plots, there is good correlation between the modeled and measured as shown in 图 29. This verifies that the designed compensator is indeed stable and the model accurate. Note: the deviation at low frequency, less than 200 Hz, is expected and is a known phenomena, also the measurement shown here was taken with a DC source, if an AC source is used to emulate a DC source the output impedance of the AC source can result in deviations from the graph plotted below

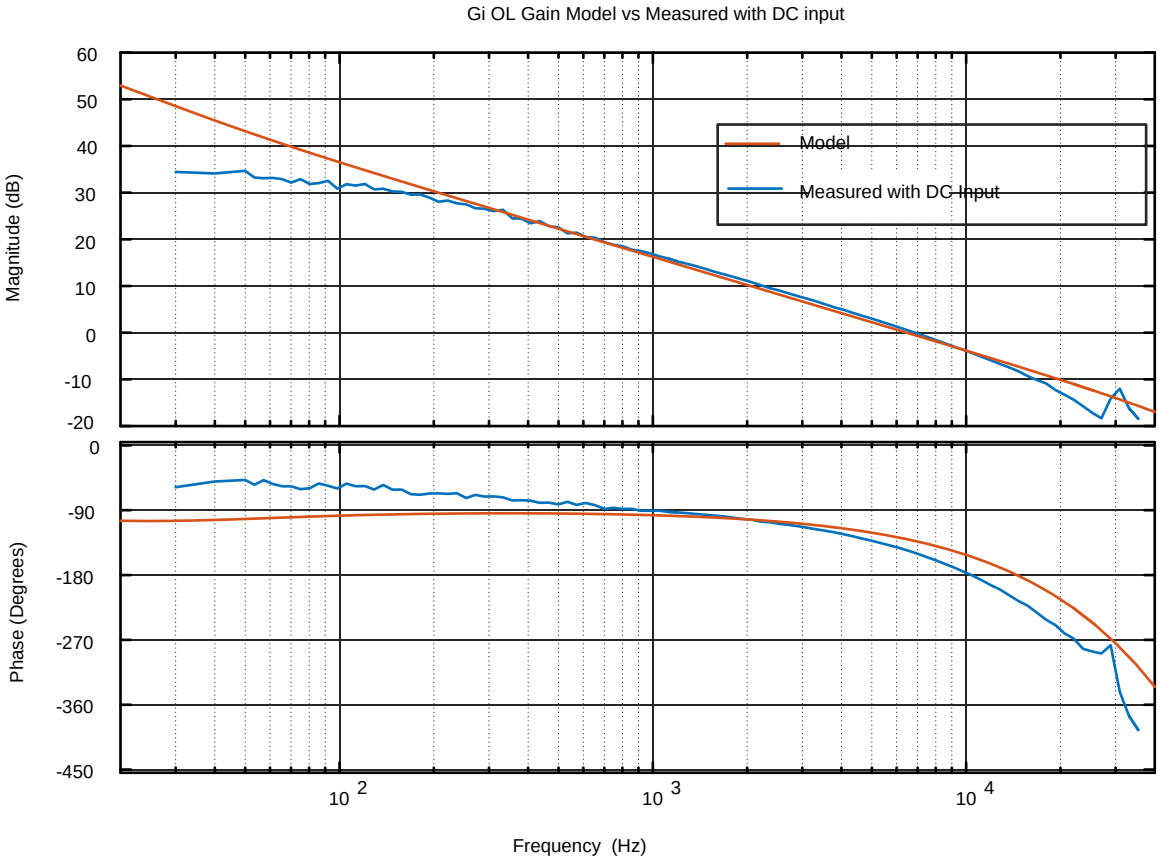

图 29. SFRA Run vs Modeled Closed Current Loop, Open Loop Gain

The frequency response data is also saved in the project folder under an SFRA data folder and is time stamped with the time of the SFRA run.

10. Optionally one can use the measured frequency response of the plant to design the current compensator by clicking on the Compensation Designer again from the CFG page and choose *SFRA Data* for plant option on the GUI. This uses the measured plant information to design the compensator. This option can be used to fine tune the compensation. By default the compensation designer points to the latest SFRA run. If a previous SFRA run plant information must be used the user can select the SFRAData.csv file by browsing to it by clicking on *Browse SFRA Data*.
11. This action verifies the current compensator design.
12. To bring the system to a safe stop, bring the input DC voltage down to zero, observe the guiVbus comes down to zero as well.
13. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the *Halt* button on the toolbar ( ) or by using *Target* → *Halt*. Then take the MCU out of real-time mode by clicking on . Finally, reset the MCU ( ) .
14. Close the CCS debug session by clicking on *Terminate Debug Session* (*Target* → *Terminate all*).

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3.1.2.4.3 INCR_BUILD 2: Closed Current Loop, AC

In this build, BUILD 2, the inner current loop is closed, that is, the inductor current is controlled using a current compensator Gi. Both DC bus and output voltage feedforward are applied to the output of this current compensator to generate the duty cycle of the inverter along with soft start for PWM around the zero crossing

Complete software diagram for this build as illustrated in 图 30.

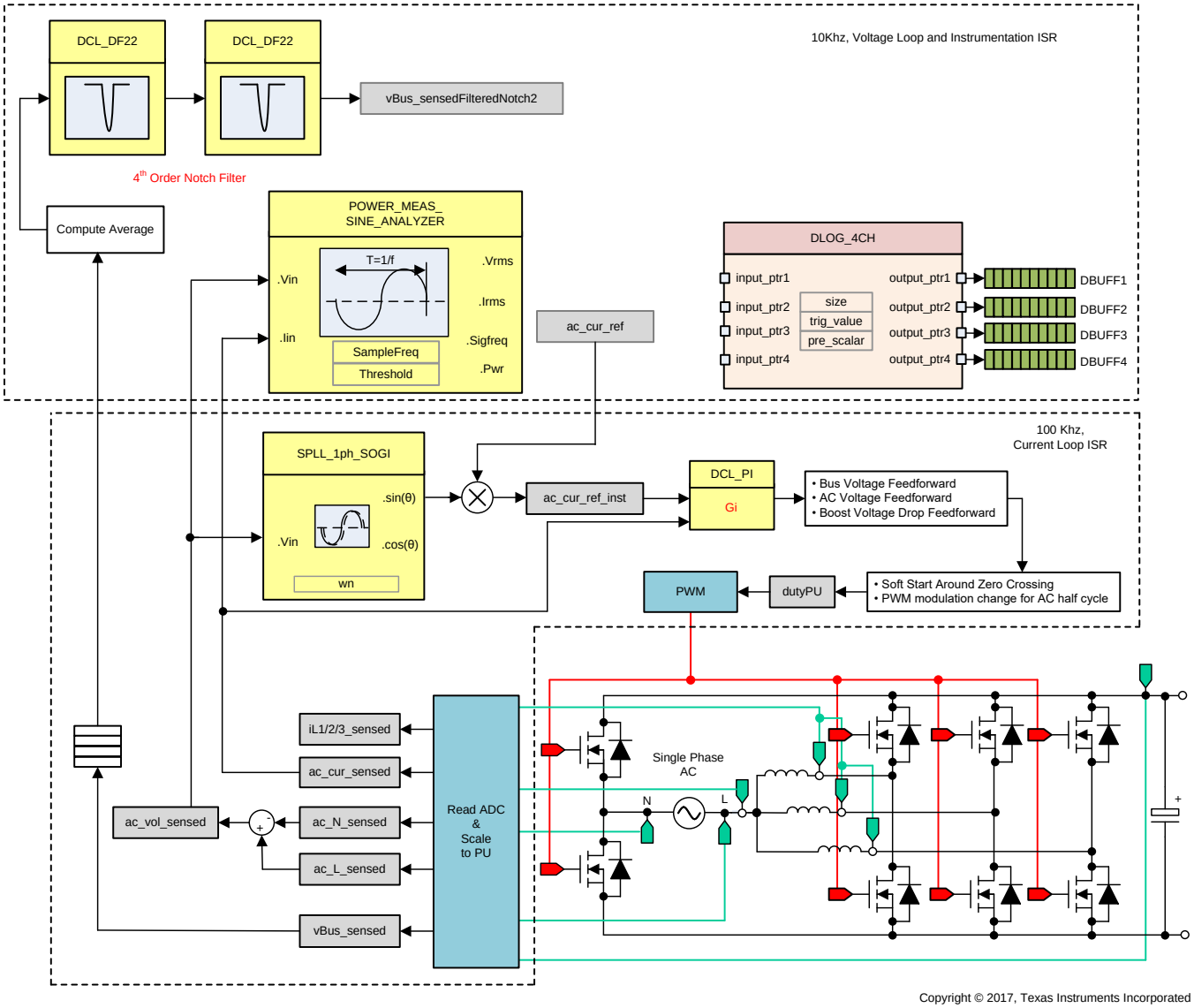

图 30. Build Level 2 Control Software Diagram: Closed Current Loop AC

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To run this build level make sure the hardware is setup as shown in 图 31. Do not supply any HV power yet to the board.

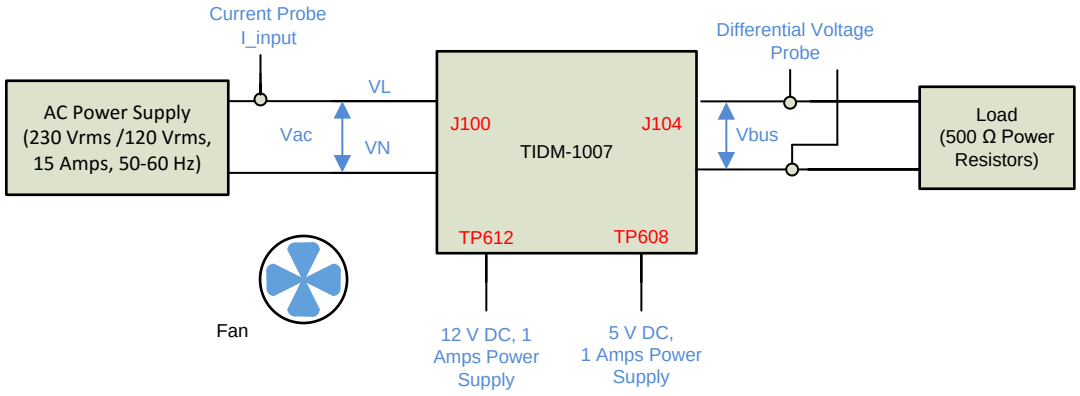

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图 31. HW Setup for AC Input

3.1.2.4.3.1 Setting Software Options for BUILD 2

1. powerSUITE Settings: On the *powerSUITE* page assuming options were selected at outlined in under *Project Options* section, select *Closed Current Loop* and AC input for the build level. Save the page.
2. Current compensator from the previous build is re-used in this build so no additional steps are required for tuning the current loop in the build level.

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3.1.2.4.3.2 Building and Loading Project and Setting up Debug

1. Right click on the project name, and click *Rebuild Project*. The project builds successfully. Click *Run* → *Debug*, which launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU the debug must be performed. In this case, select CPU1. The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.
2. To add the variables in the watch and expressions window click *View* → *Scripting Console* to open the scripting console dialog box. On the upper right corner of this console, click on *Open* to browse to the *setupdebugenv_build2_ac.js* script file, which is located inside the project folder. This file populates the watch window with appropriate variables required to debug the system. Click on *Continuous Refresh* button ( ) on the watch window to enable continuous update of values from the controller. The watch window appears as .

Variables | Expressions | Registers | Breakpoints

Expression	Type	Value	Address
buildInfo	enum enum_BuildLevel	BuildLevel2_CurrentLoop_AC	0x0000A806@Data
pwmSwState	enum enum_pwmSwState	pwmSwState_defaultState	0x0000A824@Data
boardStatus	enum enum_boardStatus	boardStatus_InputUnderVoltageTrip	0x0000A814@Data
clearTrip	int	0	0x0000A809@Data
closeGiLoop	int	0	0x0000A807@Data
ac_cur_ref	float	0.0299999993	0x0000A840@Data
ac_cur_sensed	float	0.010755837	0x0000A8A8@Data
guiVbus	float	0.344914794	0x0000A874@Data
guiVin	float	-0.563325524	0x0000A882@Data
guiVrms	float	0.0	0x0000A872@Data
guiIrms	float	0.0	0x0000A878@Data
guiPrms	float	0.0	0x0000A86E@Data
guiFreqAvg	float	0.0	0x0000A880@Data
guiPowerFactor	float	0.0	0x0000A87C@Data
EPwm1Regs.TZFLG	Register	0x0004	
EPwm2Regs.TZFLG	Register	0x0004	
dutyPU	float	0.00999999978	0x0000A86C@Data
dutyPU_DC	float	0.5	0x0000A862@Data
iL1_sensed	float	-0.00634765625	0x0000A8C4@Data
iL2_sensed	float	-0.00830078125	0x0000A8BE@Data
iL3_sensed	float	-0.0112304688	0x0000A8C0@Data
autoStartSlew	unsigned long	0	0x0000A85E@Data
Add new expression			

图 **32. Build Level 2 AC: Closed Current Loop Expressions View**

3. Enable real-time mode by hovering the mouse on the buttons on the horizontal toolbar, and clicking the button.

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3.1.2.4.3.3 Running Code

1. The project is programmed to wait for input voltage to exceed approximately 70Vrms to drive the in rush relay, and clear the trip.
2. Run the project by clicking  .
3. Now apply an input voltage of approximately 120 V, the board comes out of the undervoltage condition and inrush relay is driven. The trip clears, and a small amount of current of approximately 0.55-A RMS is drawn. The watch window looks similar to 图 33. The bus voltage is close to 180 V.

Variables | Expressions | Registers | Breakpoints

Expression	Type	Value	Address
buildInfo	enum enum_BuildLevel	BuildLevel2_CurrentLoop_AC	0x0000A806@Data
pwmSwState	enum enum_pwmSwState	pwmSwState_positiveHalf	0x0000A824@Data
boardStatus	enum enum_boardStatus	boardStatus_NoFault	0x0000A814@Data
clearTrip	int	1	0x0000A809@Data
closeGiLoop	int	1	0x0000A807@Data
ac_cur_ref	float	0.0299999993	0x0000A840@Data
ac_cur_sensed	float	-0.00663924217	0x0000A8A8@Data
guiVbus	float	180.061981	0x0000A874@Data
guiVin	float	-49.6501122	0x0000A882@Data
guiVrms	float	117.459831	0x0000A872@Data
guiIrms	float	0.551513135	0x0000A878@Data
guiPrms	float	64.2371902	0x0000A86E@Data
guiFreqAvg	float	59.8999023	0x0000A880@Data
guiPowerFactor	float	0.978407621	0x0000A87C@Data
EPwm1Regs.TZFLG	Register	0x0000	
EPwm2Regs.TZFLG	Register	0x0000	
dutyPU	float	-0.880984187	0x0000A86C@Data
dutyPU_DC	float	0.5	0x0000A862@Data
iL1_sensed	float	0.0180664063	0x0000A8C4@Data
iL2_sensed	float	-0.0048828125	0x0000A8BE@Data
iL3_sensed	float	-0.0283203125	0x0000A8C0@Data
autoStartSlew	unsigned long	5	0x0000A85E@Data
Add new expression			

图 **33. Watch Expression, Build Level 2, AC After Closed Current Loop Operation Begins**

4. Now slowly increase ac_cur_ref to 0.14, that is, 2.4-A input, and the bus voltage rises to 380 V. The voltage and current waveform are shown in 图 34.

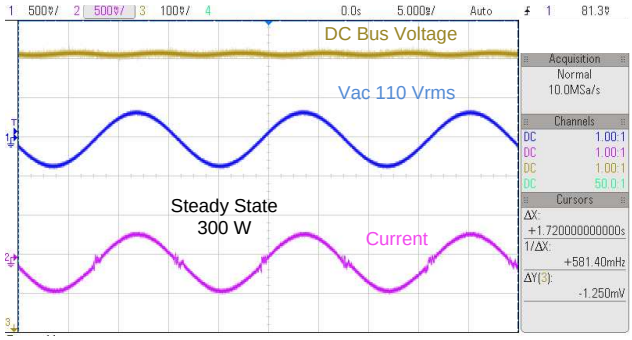

图 **34. Input AC input, Current and Output DC Voltage Waveform**

5. SFRA is integrated in the software of this build to verify the designed compensator provides enough gain and phase margin by measuring on hardware. To run the SFRA keep the project running, and from the cfg page, click on the *SFRA* icon. SFRA GUI appears.
6. Select the options for the device on the SFRA GUI. For example, for F28377D select floating point. Click on *Setup Connection*. On the pop-up window uncheck the boot on connect option, and select an appropriate COM port. Click *OK*. Return to the SFRA GUI, and click *Connect*.

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7. The SFRA GUI connects to the device. A SFRA sweep can now be started by clicking *Start Sweep*. The complete SFRA sweep takes a few minutes to finish. Activity can be monitored by seeing the progress bar on the SFRA GUI and also checking the flashing of blue LED on the back on the control card that indicates UART activity. Once complete, a graph with the open loop plot appears, 图 35. This is similar to the plot seen under DC conditions; however, some additional noise is visible due to AC harmonic frequencies close to the measured frequencies. The BW, PM, and GM numbers are very similar to the DC case. Note the graph shown in 图 35 was taken with direct grid AC input. When using AC source interaction of the AC source output, impedance can be observed, which can affect the control margins.

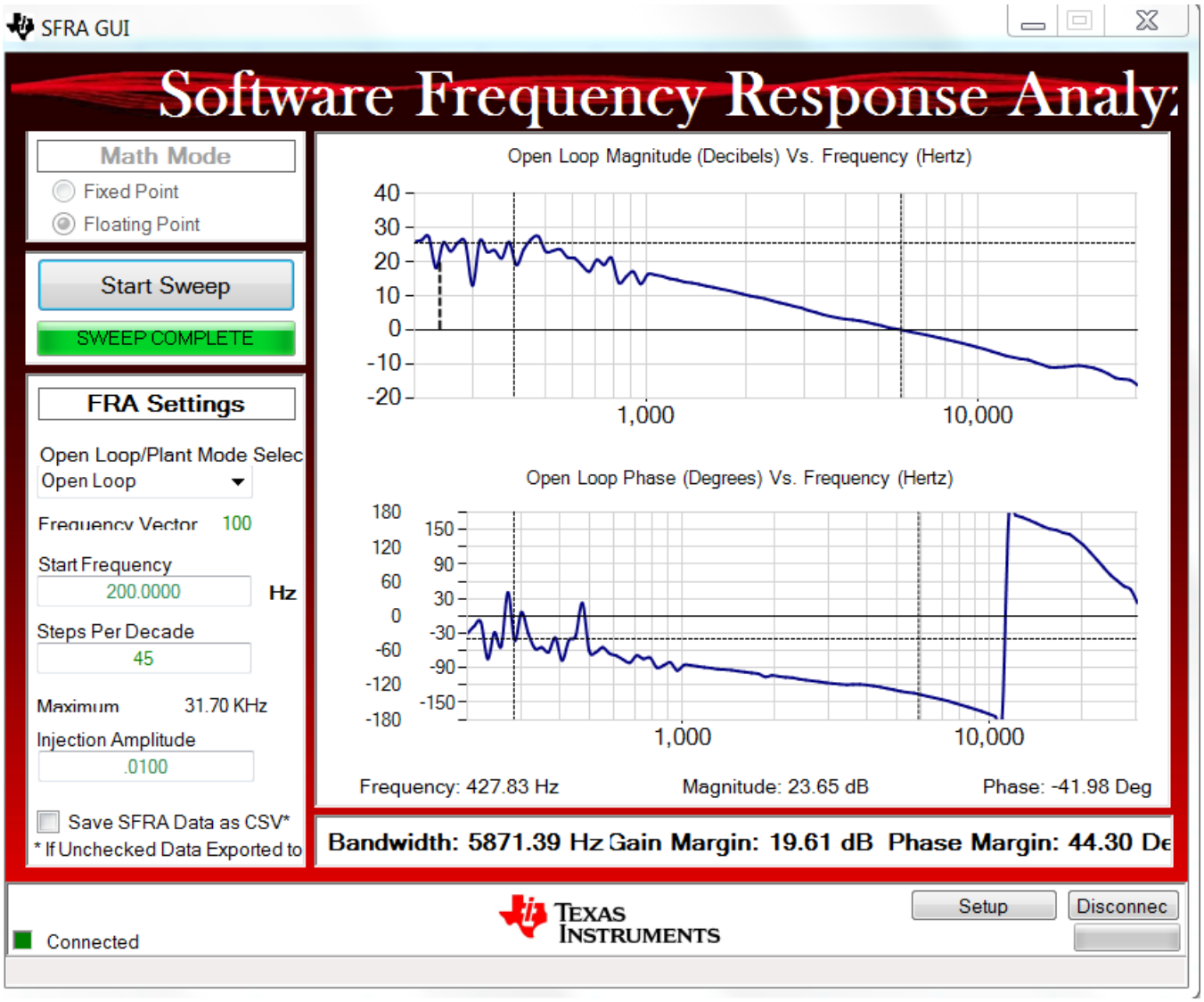

图 35. SFRA Run, Closed Current Loop, Open Loop Gain

8. To bring the system to a safe stop, switch off the output from the AC power supply thus bring the input AC voltage down to zero, observe the guiVbus comes down to zero as well.
9. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the *Halt* button on the toolbar ( ) or by using *Target* → *Halt*. Then take the MCU out of real-time mode by clicking on . Finally, reset the MCU ( ) .
10. Close the CCS debug session by clicking on *Terminate Debug Session* (*Target* → *Terminate all*).

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3.1.2.4.4 INCR_BUILD 3: Closed Voltage and Current Loop

In this build the outer voltage loop is closed with the inner current loop closed. The model of the outer voltage loop was derived in 节 2.4.3. A PI-based compensator is used and tuned through the compensation designer for the outer voltage loop.

图 36 shows the software diagram for this build.

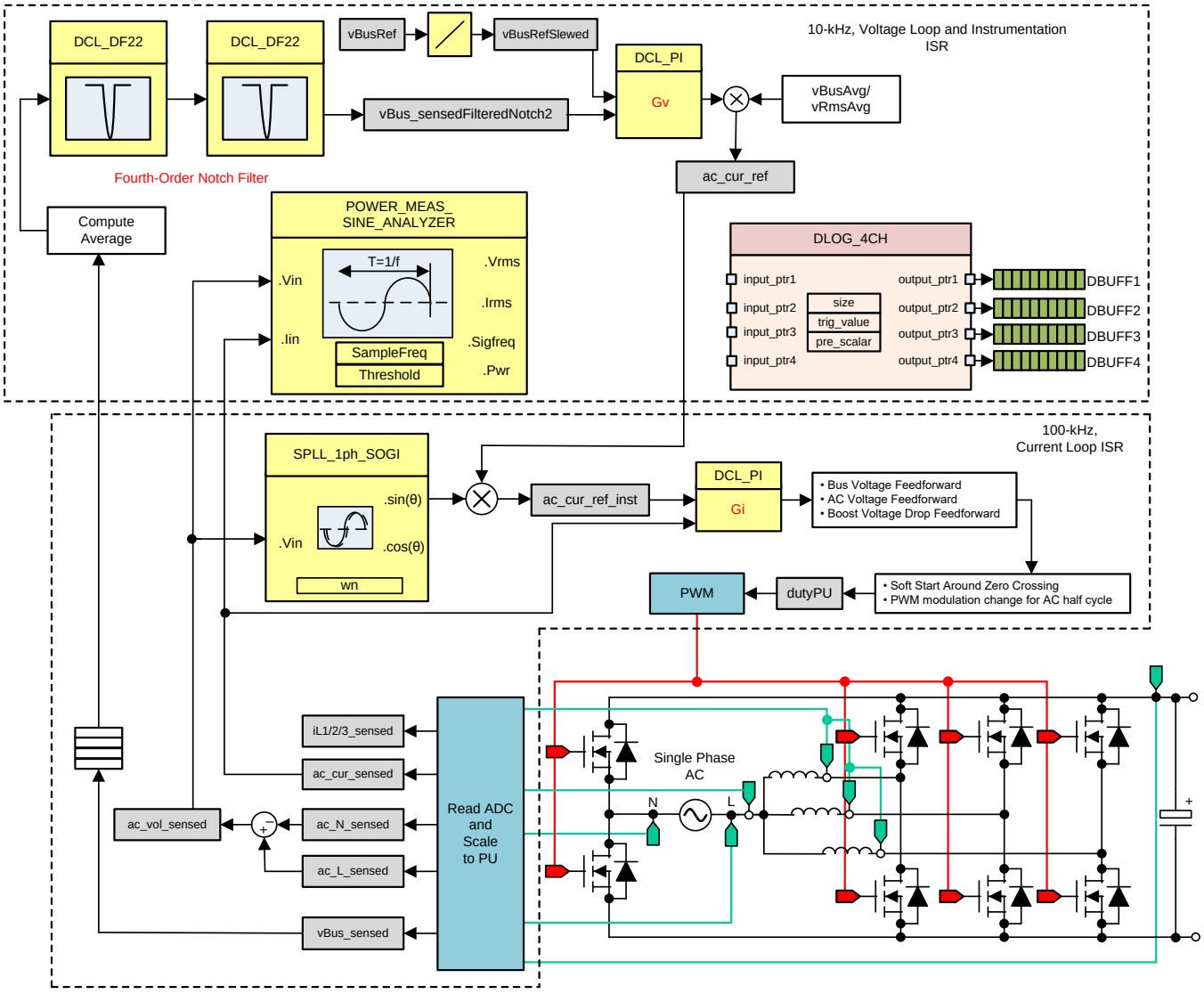

图 36. Build Level 3 Control Diagram: Output Voltage Control With Inner Current Loop

3.1.2.4.4.1 Setting Software Options for BUILD 3

1. Make sure the hardware is setup as outlined in 图 31. Do not supply any HV power yet to the board.
2. powerSUITE Settings : On the powerSUITE page select under *Project Options* section:
   - Select *Closed Voltage & Current Loop* for the build level under INCR_BUILD option.
   - Select input to be AC under INPUT options
   - Also disable the other options such as *Non Linear Voltage Loop, Adaptive Deadtime and Phase shedding*
3. Assuming all other options are same as specified earlier in 节 3.1.2.4.1.1

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4. Under *Control Loop Design*, select *Tuning* as *Voltage Loop*. Style presets to *DCL PI*. Save the page by *Ctrl* + *S*, and click on the Compensation Designer button ( ).
5. Make sure the load connected at the output of the board is correctly entered on the powerSUITE cfg page because this load value is used in the design of the voltage compensator.

3.1.2.4.4.2 Designing Voltage Loop Compensator

1. Compensation designer then launches with the model of the voltage loop plant, as shown in 图 37. The PI compensator can be edited to get the desired gain and phase margin, keeping in mind the bandwidth of the voltage loop has an inverse relationship with the THD achieved. Typically in a PFC application, this bandwidth is kept at approximately 10 Hz.

图 37. Voltage Loop PI Compensation Tuning Using Compensation Designer

2. Once satisfied with the compensator design, click on *Save COMP*. This action saves the compensator values into the project.
   - Note: If the project was not selected from the solution adapter, changes to the compensator are not allowed. To design one's own, select the solution through the solution adapter.
3. Close the Compensation Designer, and return to the powerSUITE page. Save using *Ctrl* + *S*.

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3.1.2.4.4.3 Building and Loading Project and Setting up Debug

1. Right click on the project name, and click *Rebuild Project*. The project builds successfully. Click *Run* → *Debug*, which launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU the debug must be performed. In this case, select CPU1. The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.
2. To add the variables in the watch and expressions window, click *View* → *Scripting Console* to open the scripting console dialog box. On the upper-right corner of this console, click on *Open* to browse to the *setupdebugenv_build3.js* script file located inside the project folder. This file populates the watch window with appropriate variables required to debug the system. Click on the *Continuous Refresh* button ( ) on the watch window to enable continuous update of values from the controller. The watch window appears as shown in 图 38.

Variables | Expressions | Registers

Expression	Type	Value	Address
buildInfo	enum enum_BuildLevel	BuildLevel3_VoltageLoop_AC	0x0000A811@Data
pwmSwState	enum enum_pwmSwState	pwmSwState_defaultState	0x0000A826@Data
boardStatus	enum enum_boardStatus	boardStatus_InputUnderVoltageTrip	0x0000A80F@Data
clearTrip	int	0	0x0000A81A@Data
closeGvLoop	int	0	0x0000A819@Data
vBusRef	float	0.821337461	0x0000A850@Data
vBus_sensed	float	0.000651041686	0x0000A8C0@Data
closeGiLoop	int	0	0x0000A81C@Data
ac_cur_senseOffset	float	0.502499998	0x0000A888@Data
guiVbus	float	0.353723764	0x0000A858@Data
guiVin	float	0.375192761	0x0000A82C@Data
guiVrms	float	0.0	0x0000A842@Data
guiIrms	float	0.0	0x0000A832@Data
guiPrms	float	0.0	0x0000A834@Data
guiPowerFactor	float	0.0	0x0000A82E@Data
guiFreqAvg	float	0.0	0x0000A844@Data
EPwm1Regs.TZFLG	Register	0x0004	
EPwm2Regs.TZFLG	Register	0x0004	
dutyPU	float	0.00999999978	0x0000A86E@Data
dutyPU_DC	float	0.5	0x0000A86C@Data
iL1_sensed	float	-0.00390625	0x0000A884@Data
iL2_sensed	float	-0.00634765625	0x0000A880@Data
iL3_sensed	float	-0.00244140625	0x0000A882@Data
autoStartSlew	unsigned long	0	0x0000A83E@Data
Add new expression			

图 **38. Build Level 3: Expressions View**

3. Enable real-time mode by hovering the mouse on the buttons on the horizontal toolbar and clicking the button.
4. Run the project by clicking on
5. Now Halt the processor by using the *Halt* button on the toolbar ( ).

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3.1.2.4.4.4 Running Code

1. The project is programmed to wait for input voltage to excel at approximately 70 Vrms to drive the in rush relay, and clear the trip.
2. Run the project by clicking  .
3. Now apply an input voltage of approximately 120 V. The board comes out of the undervoltage condition and inrush relay is driven. The trip clears, and the output rises to 380-V DC. A sinusoidal current is drawn from the AC input. 图 39 shows the watch window when the program is running at this stage.

Variables | Expressions | Registers

Expression	Type	Value	Address
buildInfo	enum enum_BuildLevel	BuildLevel3_VoltageLoop_AC	0x0000A811@Data
pwmSwState	enum enum_pwmSwState	pwmSwState_negativeHalf	0x0000A826@Data
boardStatus	enum enum_boardStatus	boardStatus_NoFault	0x0000A80F@Data
clearTrip	int	1	0x0000A81A@Data
closeGvLoop	int	1	0x0000A819@Data
vBusRef	float	0.821337461	0x0000A850@Data
vBus_sensed	float	0.822998047	0x0000A8C0@Data
closeGiLoop	int	1	0x0000A81C@Data
ac_cur_senseOffset	float	0.502499998	0x0000A888@Data
guiVbus	float	380.081421	0x0000A858@Data
guiVin	float	-152.073486	0x0000A82C@Data
guiVrms	float	120.093376	0x0000A842@Data
guiIrms	float	2.40836215	0x0000A832@Data
guiPrms	float	277.007263	0x0000A834@Data
guiPowerFactor	float	0.990778685	0x0000A82E@Data
guiFreqAvg	float	60.0219727	0x0000A844@Data
EPwm1Regs.TZFLG	Register	0x0000	
EPwm2Regs.TZFLG	Register	0x0000	
dutyPU	float	-0.4262546	0x0000A86E@Data
dutyPU_DC	float	0.5	0x0000A86C@Data
iL1_sensed	float	0.0561523438	0x0000A884@Data
iL2_sensed	float	-0.0673828125	0x0000A880@Data
iL3_sensed	float	-0.0434570313	0x0000A882@Data
autoStartSlew	unsigned long	5	0x0000A83E@Data
Add new expression			

图 **39. Build Level 3: Expressions View After AC Voltage is Applied**

4. SFRA is integrated in the software of this build to verify the designed compensator provides enough gain and phase margin by measuring on hardware. To run the SFRA, keep the project running, and from the cfg page, click on the *SFRA* icon. SFRA GUI appears.
5. Select the options for the device on the SFRA GUI. For example, for F28004x, select floating point. Click on *Setup Connection*, and on the pop-up window, uncheck the boot on connect option and select an appropriate COM port. Click *OK*. Return to the SFRA GUI, and click *Connect*.

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6. The SFRA GUI connects to the device. A SFRA sweep can now be started by clicking *Start Sweep*. The complete SFRA sweep takes a few minutes to finish. Activity can be monitored by seeing the progress bar on the SFRA GUI and checking the flashing of blue LED on the back on the control card that indicates UART activity. Once complete, a graph with the open loop plot appears, as seen in 图 40. This action verifies that the designed compensator is indeed stable.

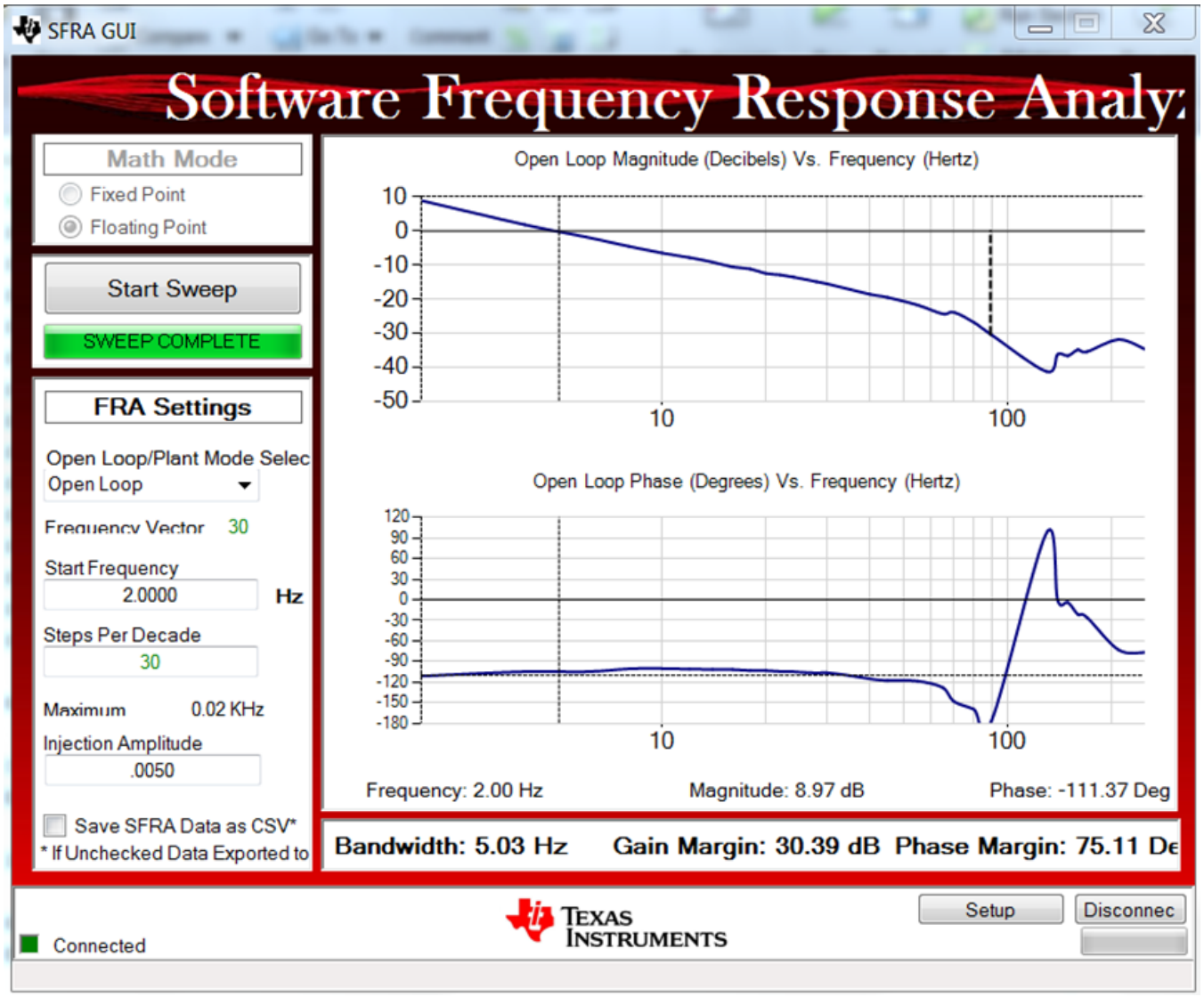

图 **40. SFRA Run on Closed Voltage Loop**

The frequency response data is also saved in the project folder under an SFRA data folder and is time stamped with the time of the SFRA run.

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Note the measured gain and phase margin are close to the modeled values, as shown in 图 12 .

7. Optionally. Click on the Compensation Designer again from the CFG page, and choose *SFRA Data* for plant option on the GUI. This option uses the measured plant information to design the compensator, and can be used to fine tune the compensation. By default the Compensation Designer points to the latest SFRA run. If a previous SFRA run plant information must be used the user can select the *SFRAData.csv* file by browsing to it by clicking on *Browse SFRA Data*. Close the Compensation Designer to return to the cfg page once done.
8. This verifies the voltage compensator design.
9. To bring the system to a safe stop bring the input AC voltage down to zero, observe the guiVBus comes down to zero as well.
10. Fully halting the MCU when in real-time mode is a two-step process. First halt the processor by using the *Halt* button on the toolbar ( ) or by using *Target* → *Halt*. Then take the MCU out of real-time mode by clicking on . Finally, reset the MCU ( ).
11. Close CCS debug session by clicking on *Terminate Debug Session* (*Target* → *Terminate all*).

3.1.2.5 Running Code on CLA

This solution is supported with an option to run the code on the CLA. This option is selected using a drop-down box under project option on the powerSUITE main.cfg page. Running on CLA can be selected for any build level option.

注: SFRA libray does not support CLA, hence the SFRA cannot be run when using CLA.

DLOG is also not used when using CLA, hence the datalogging graphs will not work when using CLA.

Once the option is changed, the CFG file must be saved and the project re-compiled. Once recompiled, follow the steps as outlined in the specific incremental build level documentation.

Depending on the device, for example for F28004x CLA supports CLA tasks and a background task, thus both 100kHz ISR and 10kHz IST can be offloaded to the CLA. By default if the selection from the powerSUITE page is made the faster ISR is moved to the CLA task and the slower ISR is moved to the background task by default. If the user does not want to run the 10kHz ISR on the CLA, the option to do so is available under the "USER SECTION" in the solutions-settings.h file.

```
#if CONTROL_RUNNING_ON == CLA_CORE
#define INSTRUMENTATION_ISR_RUNNING_ON CLA_CORE
#else
#define INSTRUMENTATION_ISR_RUNNING_ON C28x_CORE
#endif
```

3.1.2.6 Advanced Options

In this section some advanced setting that improve the power factor are discussed one by one and their relative impact quantified with test results

3.1.2.6.1 Input Cap Compensation for PF Improvement Under Light Load

Input cap causes PF degradation if the current reference is maintained perfectly in sync with the voltage as shown in 公式 8 and in 图 41(a).

$$i_{ref\_dpllvc} = i^{*}_{ref} \sin(\omega t) - i_{input\_cap\_comp} \cos(\omega t) \quad (8)$$

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The current reference can be adjusted with vectors to offset the PF degradation, 公式 9, 图 41(b) . As the angle from the phase locked loop is used to compute the vector this technique is called the digital phase locked loop vector cancellation (DPLLVC) technique. This improves PF at light load and high line significantly.

$$i_{ref\_DPLLVC} = i^{*}_{ref} \sin(\omega t) - i_{input\_cap\_comp} \cos(\omega t) \quad (9)$$

The amount of correction applied depends on the input capacitor value, for example on this design the input cap is 2.2 µF. Which means at high line a capacitive current equal to $\frac{220}{\frac{1}{2} \times pi \times 60 \times 2.2\,\mu F} = 0.1823$ A is drawn . Under light loads this is significant amount of current and causes power factor loss. The current sensor gain on this design is approximately 24 A, so this translates to an adjustment of approximately 0.01 pu for the high-line condition.

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Furthermore, there is a tracking error under low power conditions. This tracking error can be offset by an adjustment to the current command shown in 图 41(c). The amount of this tracking error is adjusted empirically for the best performance from the system. Thus the total current reference is given by 公式 10.

$$i_{ref\_DPLLVC\_TC} = i^{*}_{ref} \sin(\omega t) - i_{input\_cap\_comp} \cos(\omega t) - i_{tracking\_error}\Big|_{power\_dependent} \cos(\omega t) \quad (10)$$

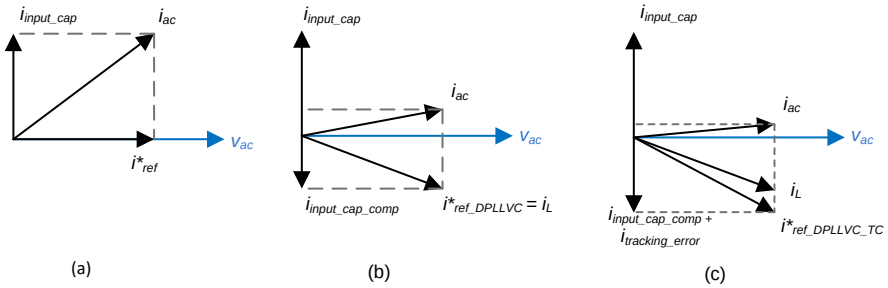

图 41. Power Factor (a) No Adjustment (b) DPLLVC (c) DPLLVC Plus Tracking Error Compensation

The result for PF improvement are graphed in 图 42.

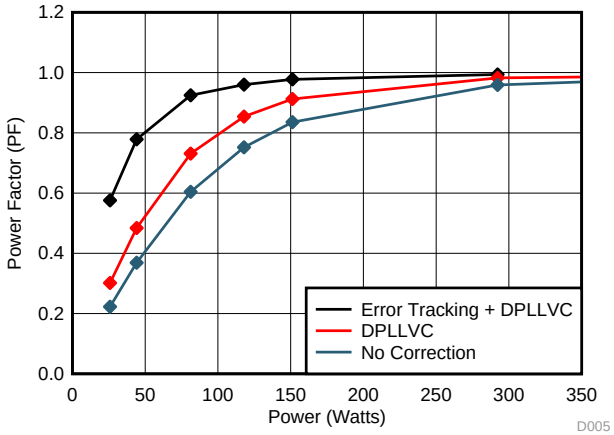

图 42. PF Graph vs Power at 220 Vrms Highlighting Improvement With Input Cap Current Compensation

This feataure can be turned off or on by writing to the INPUT_CAP_COMPENSATION #define variable in the <solution>-settings.h file. This setting is put under the "USER SECTION" area of the header file and can be modified by the user. The value of the adjustment is controlled using the #defines HIGH_LINE_INPUT_CAP_COMP_ADJUST & LOW_LINE_INPUT_CAP_COMP_ADJUST. These are in per-unit format and how this value is determined was explaineed earlier in this section.

```
#define INPUT_CAP_COMPENSATION 1
#define HIGH_LINE_INPUT_CAP_COMP_ADJUST -0.01823
#define LOW_LINE_INPUT_CAP_COMP_ADJUST  -0.00911
```

3.1.2.6.2 *Adaptive Dead Time for Efficiency Improvements*

In continuous conduction mode, the dead-time control for synchronous rectification is critical in terms of short-circuit protection and efficiency. With the optimal dead time, the risk of shoot through can be eliminated and it also prevents an excessive conduction loss from body diode conduction of Sync FET. Therefore, the goal of optimal dead time is not to turn on the Active FET and Sync FET simultaneously while minimize a redundant third quadrant conduction of Sync FET.

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This optimal dead time can be calculated from the measured current and the device output capacitance, this is given by 公式 11.

$$t_{deadtime\_optimal} = \frac{2C_{oss}V_{out}}{i_{L\_peak}} \quad (11)$$

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图 43 shows the block diagram for implementation.

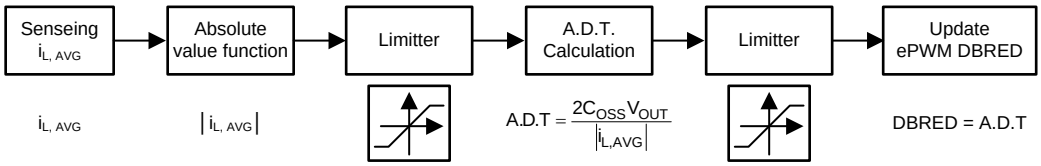

图 43. Adaptive Dead-Time Implementation

The option enables power saving, which is shown for the high line case in 图 44 compared to a fixed dead time from which it can be inferred that avoiding the shoot through at low power levels results in significant power savings. However, once the shoot through is avoided the power savings drop first and then progressively increase as power increases and the diode conduction time is reduced by implementing adaptive dead-time adjustment.

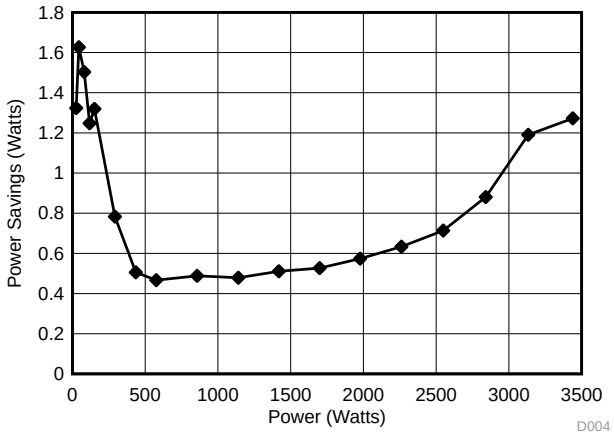

图 44. Power Savings With Adaptive Dead-Time at High Line 230 Vrms

To enable adaptive dead time, select the drop down box under *Project Options* on the *CFG/powerSUITE* page of the solution. For FED the fixed value that is specified on the CFG page is used. When adaptive dead time is enabled the RED is modulated and the minimum and maximum bounds are specified in the *user section* of the *<solution>-settings.h*. The following are the #define that can be adjusted:

- Device output capacitance: #define GAN_COSS 0.000000000145
- Minimum dead time allowed : #define PFC_DEADBAND_RED_MIN_US 0.020
- Maximum dead time allowed: #define PFC_DEADBAND_RED_MAX_US 0.200

Following these adjustments the project must be saved, re-compiled, and loaded on the controller when this option is changed. Hardware setup and software instructions as outlined in 节 3.1.2.4.4 can be followed to see the behavior of the board and measure efficiency.

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3.1.2.6.3 Phase Shedding for Efficiency Improvements

Phase shedding can be an effective technique to improve efficiency in interleaved application by optimizing for the conduction and the switching losses. In this design there are three phases, so three different configurations are possible as shown in 图 45.

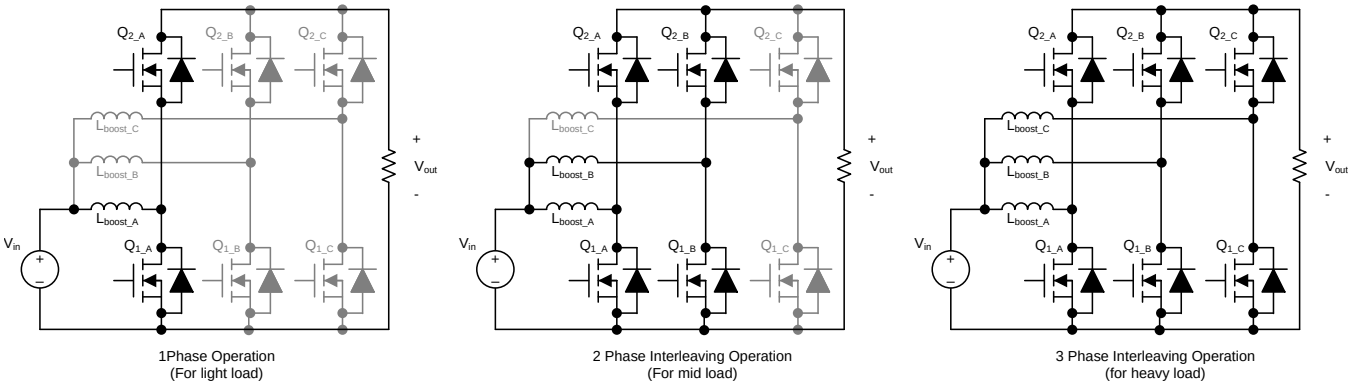

图 45. Phase Shedding Options on TTPL PFC

In each of these modes the phase shift between each of them must be adjusted. When in two-phase mode, a 180° phase shift is desired between the PWMs, and when in three-phase mode, a 120° of phase shift is desired.

The decision to do phase shedding can be made on different parameters, such as the RMS current, power, the peak inductor current, and so on. When using RMS current the change of phases can be significantly delayed. 图 46 shows phase shedding when the decision is based on RMS current. Code takes multiple AC cycles before the phases are added .

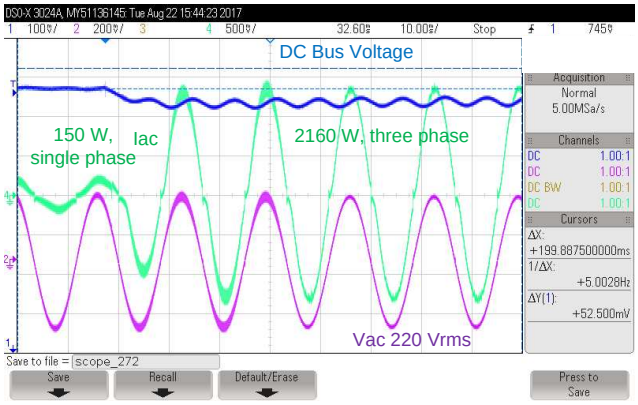

图 46. Waveform When Decision to Add Phases is Based on RMS Calculation

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This delay may not be acceptable for many application. Thus, the voltage controller output is chosen as the decision point to drop or add phases. A state machine is constructed as shown in 图 47, with some hysteresis built around the phase shedding points.

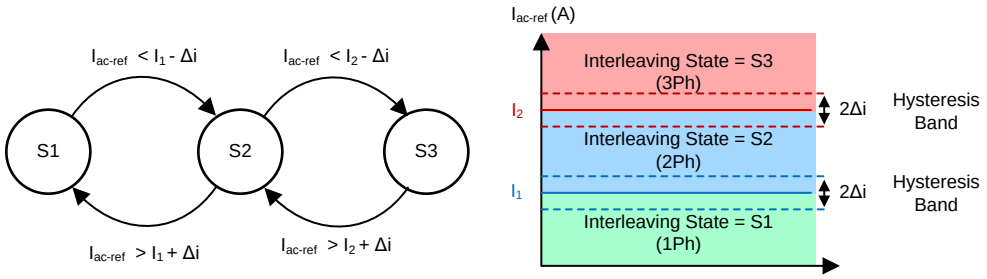

图 47. State Machine for Phase Shedding Control

Bringing a phase in and out can cause in-advertent pulses to be generated. Hence the implementation to drop and add phase is done through the GPIO and PWM peripheral switch using the GPIO pin Mux registers. All PWM capable pins are configured and GPIO outputs and driven low. Now based on how many phases must be applied the GPIO pin mux is changed accordingly. It is safe to enable and disable the phases using the GPIO pin mux switch at any point in the AC cycle as the registers in the PWM are shadowed. 图 48 shows details of the implementation of phase shedding on the C2000 MCU.

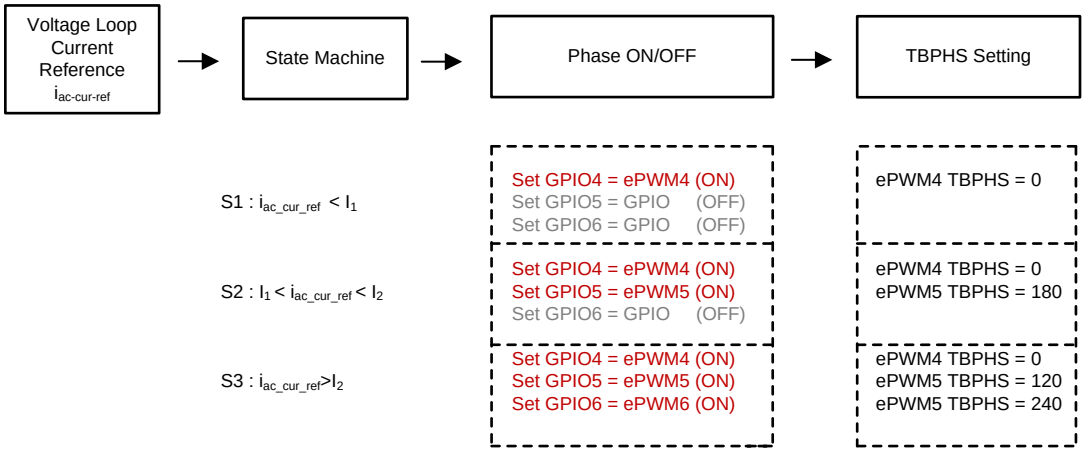

图 48. Implementation of Phase Shedding on TTPL PFC Using C2000™ MCU

To enable phase shedding setting can be set in the user section of the code in *<solution>-settings.h* file and modifying *PHASE_SHEDDING_ENABLED* define. The points at which phases are brought in and out are set by changing the *PHASE_SHEDDING_1PH_2PH_TRANSITION_CURRENT* and *PHASE_SHEDDING_2PH_3PH_TRANSITION_CURRENT* define, which correspond to I1 and I2 as shown in 图 48. Recompile the code, load the code, and repeat the steps as outlined in 节 3.1.2.4.4 to test this feature. With this feature implemented, under transients the phases are dropped and added quickly.

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图 49 and 图 50 show the transient at 110 Vrms of 1.3 KW to 150 W and vice versa. The phases are added back quickly and dropped quickly under transients as the decision is based on the voltage loop generated current reference.

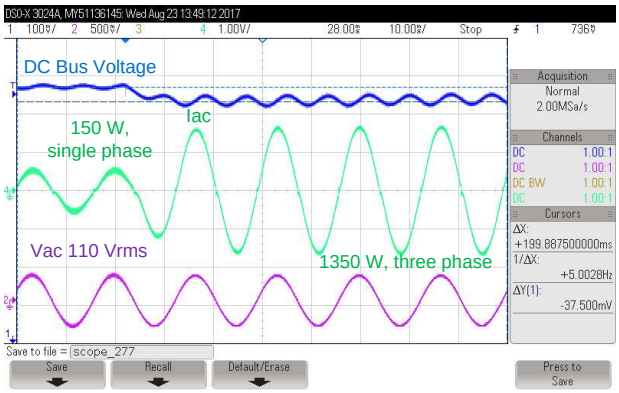

图 49. Phase Added Quickly Under Transient at 120 Vrms, 60 Hz

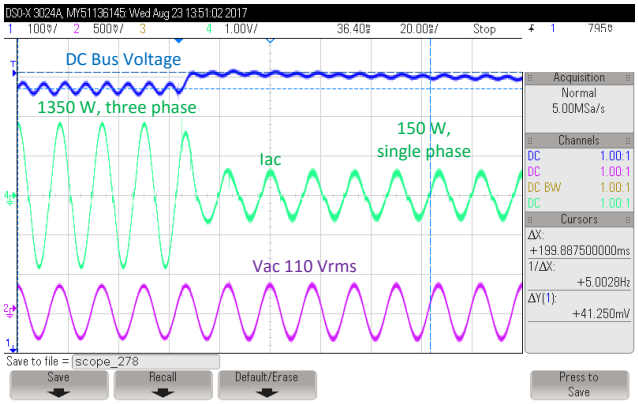

图 50. Phase Shed Quickly Under Transient at 120 Vrms, 60 Hz

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Similarly at high line, a transient greater than 2 KW is applied, and the phase goes from single to three phase almost instantly. 图 51 and 图 51 show the test waveform at high line under transient of 2.16 KW to 150 W and vice versa.

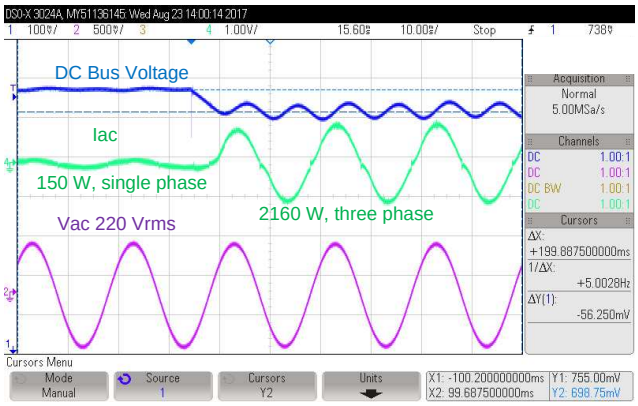

图 51. Phase Added Quickly Under Transient at 230 Vrms, 50 Hz

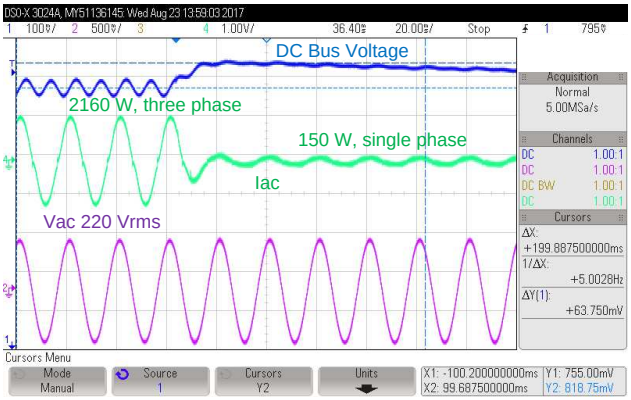

图 52. Phase Shed Quickly Under Transient at 230 Vrms, 50 Hz

图 53 shows the efficiency improvement at 230 Vrms with phase shedding

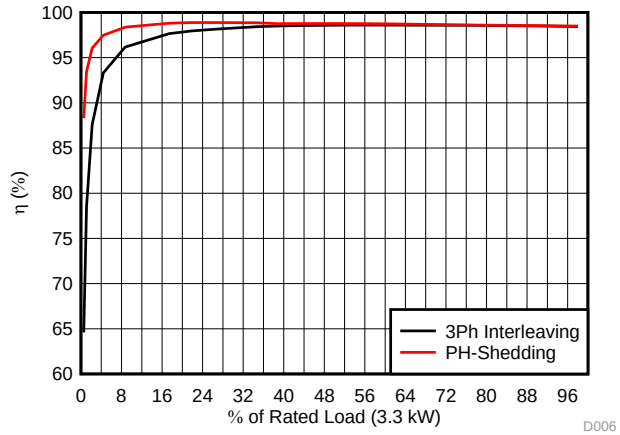

图 53. Efficiency Comparison at 230 Vrms With Phase Shedding and Without

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3.1.2.6.4 Non-Linear Voltage Loop for Transient Reduction

The PFC stage control is composed of an inner current loop, which tries to follow the input voltage and an outer voltage loop that tries to maintain a constant DC bus voltage at the output. The voltage loop is thus in conflict with the current loop and hence must be designed to be very low bandwidth (approximately 10 Hz) in order to achieve good power factor. The slow voltage loop results in significant overshoot and undershoot under transients (see 图 54).

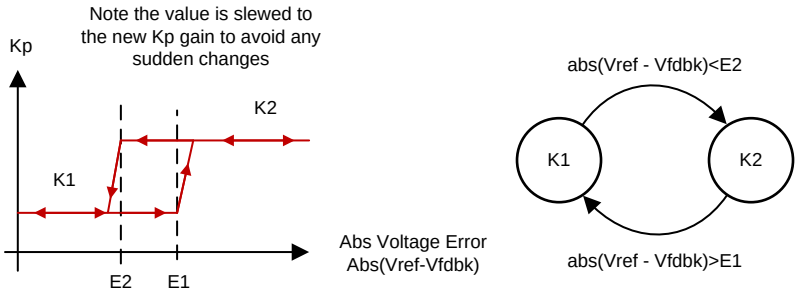

图 **54. Non-Linear Voltage Loop with Hysteresis**

To improve voltage overshoot and undershoot, while maintaining good power factor a non-linear voltage control loop is implemented as shown in 图 55. A hysteresis band is added in the non-linear voltage loop to avoid oscillation between high-gain and low-gain mode. Furthermore the gain change is slewed to avoid any sudden changes. 图 56 shows the result with non-linear voltage loop.

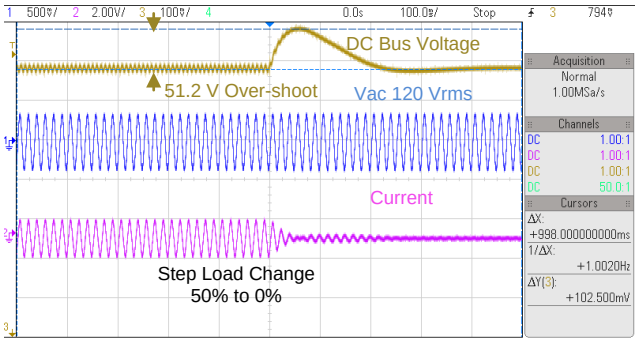

图 **55. Voltage Transient Without Non-Linear Voltage Loop, Vin 120 Vrms, 880 W to 0 W Transient, Overshoot 51.2 V**

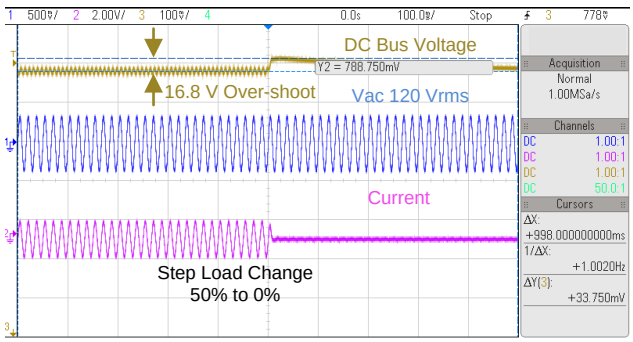

图 **56. Voltage Transient With Non-Linear Voltage Loop, Vin 120 Vrms, 880 W to 0 W Transient, Overshoot 16.8 V**

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To enable non-linear voltage loop, select the drop down box under *Project Options* on the *CFG/powerSUITE* page of the solution. Default value of five times the gain is applied for the proportional term under transient condition. This value can be adjusted under the *user section* of the *<solution>-settings.h* file by modifying the *NON_LINEAR_V_LOOP_KP_MULTIPLIER* define. The project must be saved, re-compiled, and loaded on the controller when this option is changed. Hardware setup and software instructions for the Build Level 3 can be followed to see the behavior of the board under transients.

3.1.2.6.5 Software Phase Locked Loop Methods: SOGI - FLL

To meet industry standards, the design must be tested under frequency transients. This poses a problem when using PLL angle for the drive of the PWM signal if the PLL cannot adapt to the frequency change. Afrequency locked loop scheme, as proposed in *Grid Synchronization of Power Converters Using Multiple Second Order Generalized Integrators* [1], can be used to make the software phase locked loop frequency adaptive.

The module follows the same basic structure as the SOGI PLL module, with implementation discussed in *Software PLL Design Using C2000 MCUs Single Phase Grid Connected Inverter* [2]. A frequency adaptive feature through a frequency locked loop is added as shown in 图 57.

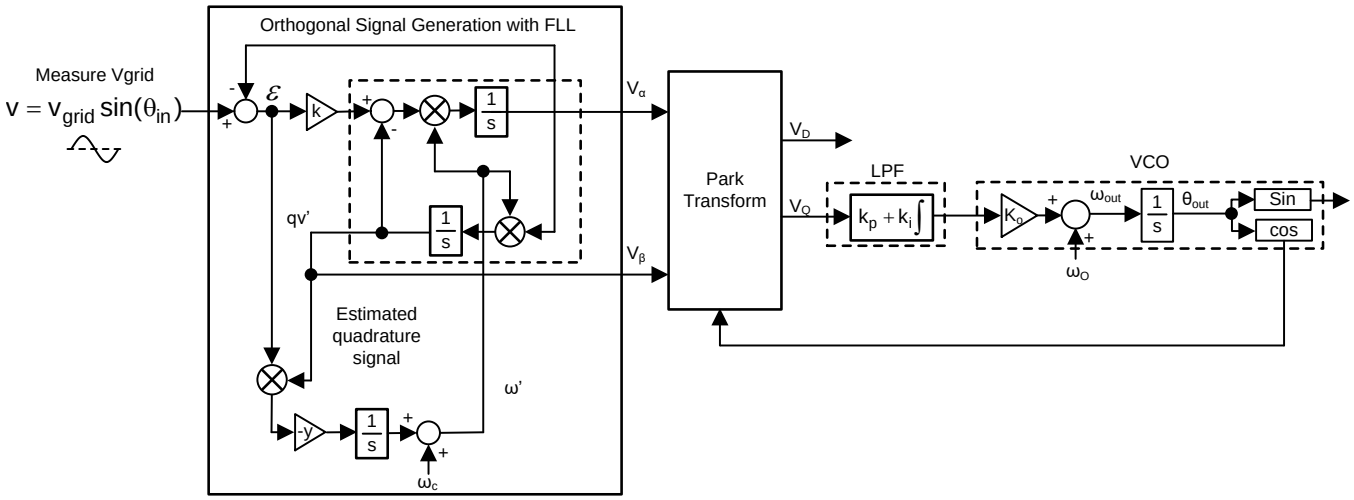

图 57. Software Phase Locked Loop Structure Based on Second Order Generalized Integrator and Frequency Locked Loop

To select a PLL method go to the *user section* of the *<solution>-settings.h*. The following are the #define that can be adjusted:

- #define SPLL_METHOD_SELECT SPLL_1PH_SOGI_FLL_SEL

Following this adjustment the project must be saved, re-compiled, and loaded on the controller. Hardware setup and software instructions for the Build Level 3 can be followed to see the behavior of the board with the new PLL scheme

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3.2 Testing and Results

3.2.1 Test Results at Input 120 Vrms, 60 Hz, Output 380-V DC

3.2.1.1 Startup

The startup sequence of the power stage is shown in 图 58 with input single phase of 120 Vrms VL-N, an output bus regulated at 380 V, and a 1.6-KW load and no load.

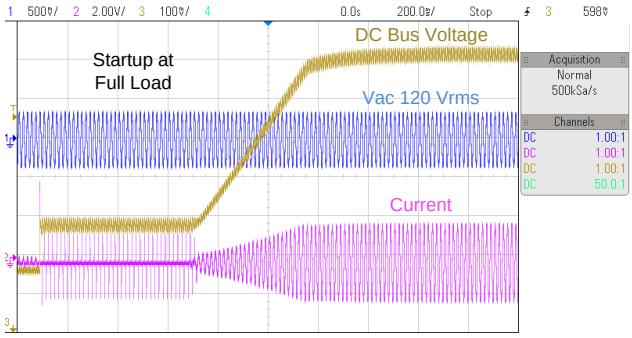

图 **58. Startup of PFC Operation at 120-Vac IN, 380-V DC OUT and 1.6-KW Load**

图 59 shows the startup under no load.

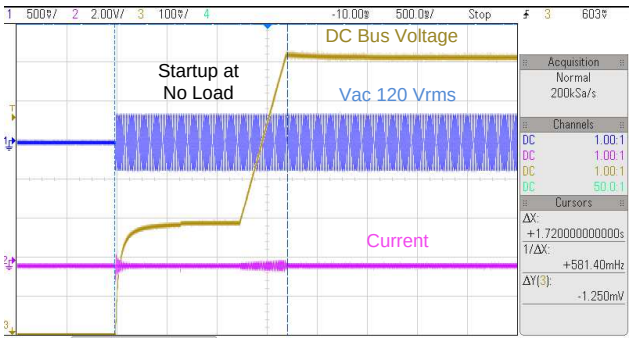

图 **59. Startup of PFC at 120-Vac IN, 380-V DC Output, and 0% Load**

3.2.1.2 Steady State Condition

Steady state current waveforms are shown in 图 60, 图 61, and 图 62 at different load conditions. Phase shedding is disabled for these readings.

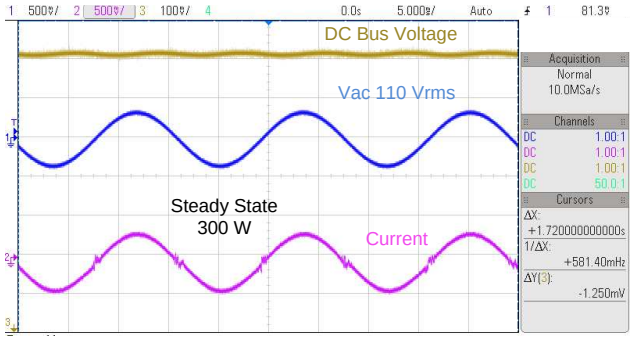

图 **60. Steady State 120-Vac IN, 380-V DC OUT 300W, iTHD 5.5%**

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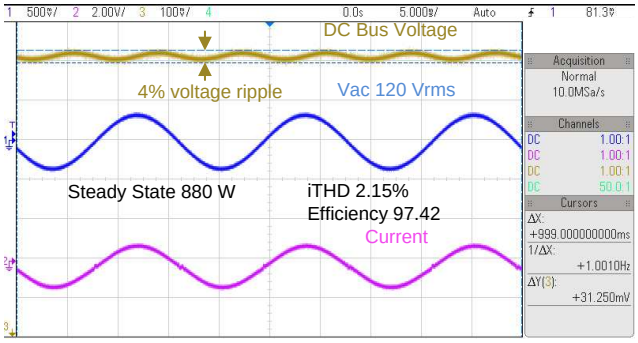

图 **61. Steady State 120-Vac IN, 380-V DC OUT 880W, iTHD 2.15%**

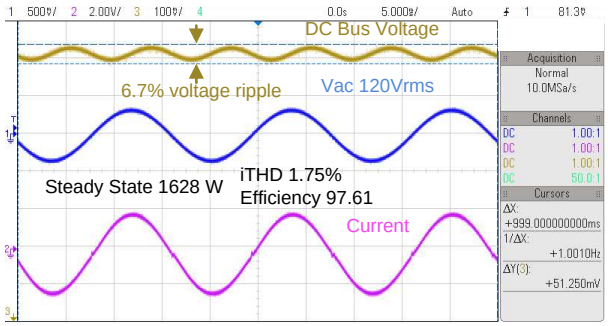

图 **62. Steady State 120-Vac IN, 380-V DC OUT, 1.674-KW, iTHD 1.75%**

表 4 lists the detailed test results of this design under varying load conditions with 120-Vac input and 380-V DC output. For this data, phase shedding is disabled, adaptive dead time is enabled, 100 ns is chosen as the fixed dead time for the hard-switched edge, and the soft switching edge dead time varies between 20 ns and 200 ns.

表 **4. Detailed Test Results with 120-Vac IN, 380-V DC OUT, and Different Power Levels**

Vin (V RMS)	Vout (V)	Pin (W)	Iout (A)	Pout (W)	EFFICIENCY %	iTHD%	PF	% RATED LOAD	THETA OFFSET	GI KP
120.05	382.02	154.27	0.375	143.47	92.98	10.54	0.9927	9.0	-0.014	0.35
119.86	382.01	301.30	0.750	286.36	95.14	5.50	0.9974	17.9	-0.01	0.35
119.49	382.01	444.40	1.120	427.76	96.30	4.16	0.9987	26.7	-0.01	0.35
119.42	382.03	579.10	1.469	561.40	96.94	2.89	0.9950	35.1	-0.01	0.35
119.16	382.02	721.30	1.837	701.80	97.30	2.42	0.9995	43.9	-0.01	0.35
119.02	382.05	863.00	2.202	841.50	97.52	2.15	0.9995	52.6	0	0.35
118.78	381.96	1007.20	2.573	983.30	97.64	1.92	0.9995	61.5	0	0.35
118.63	382.08	1152.00	2.944	1125.30	97.69	1.82	0.9995	70.3	0	0.35
118.40	382.08	1298.40	3.319	1268.20	97.70	1.72	0.9994	79.3	0	0.35
118.25	382.08	1442.00	3.685	1408.30	97.69	1.87	0.9991	88.0	0	0.3
118.03	382.08	1593.80	4.071	1555.50	97.65	1.80	0.9991	97.2	0	0.3
117.98	382.05	1716.40	4.449	1674.80	97.61	1.75	0.9991	104.7	0	0.3

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3.2.1.3 Transient Test With Step Load Change

3.2.1.3.1 0% to 50% Load Step Change

图 63 shows the transient response when input is 120 Vrms and a load step of 50% is applied to the power stage

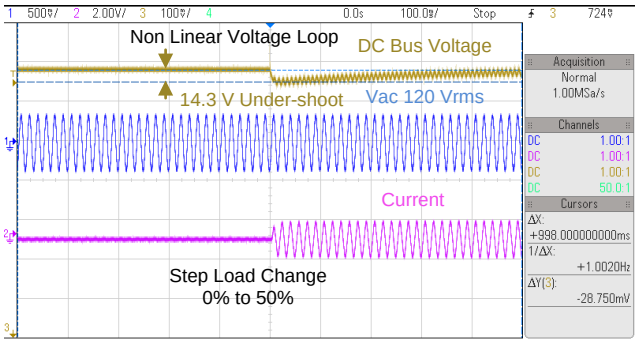

图 **63. Transient Response, 120 Vrms, 60 Hz, 0% to 50% Load Step**

3.2.1.3.2 50% to 100% Load Step Change

图 64 shows the transient response when input is 120 Vrms and load is stepped up from 50% to 100%

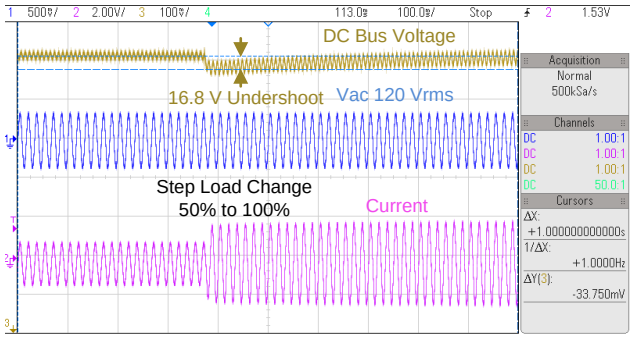

图 **64. Transient Response, 120 Vrms, 60 Hz, 50% to 100% Load Step**

3.2.1.3.3 100% to 50% Load Step Change

图 65 shows the transient response when the input is 120 Vrms and load is stepped down from 100% to 50%.

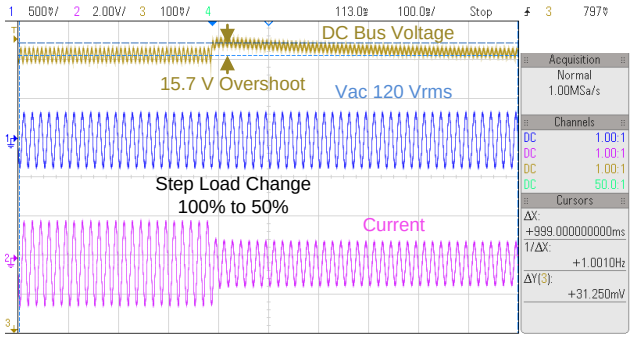

图 **65. Transient Response, 120 Vrms, 60 Hz, 100% to 50% Load Step**

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3.2.1.3.4 50% to 100% Load Step Change

图 66 shows the transient response when input is 120Vrms and load is stepped down from 50% to 0%.

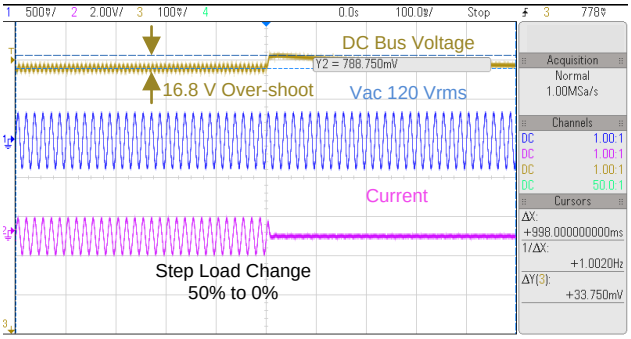

图 66. Transient Response, 120 Vrms, 60 Hz, 50% to 0% Load Step

3.2.2 Test Results at Input 230 Vrms, 50 Hz, Output 380 V DC

3.2.2.1 Startup

图 67 shows the startup sequence of the power stage with input single phase 230-Vrms VL-N and output bus regulated at 380V and a 880-W load.

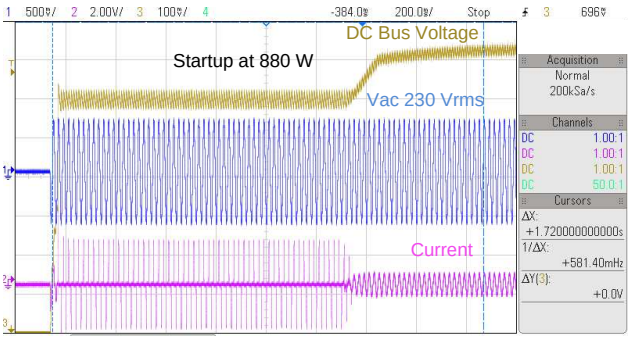

图 67. Startup of PFC Operation at 230-Vac IN, 380-V DC OUT at 880-W Load

图 68 shows the startup of PFC at no load at 230 Vrms.

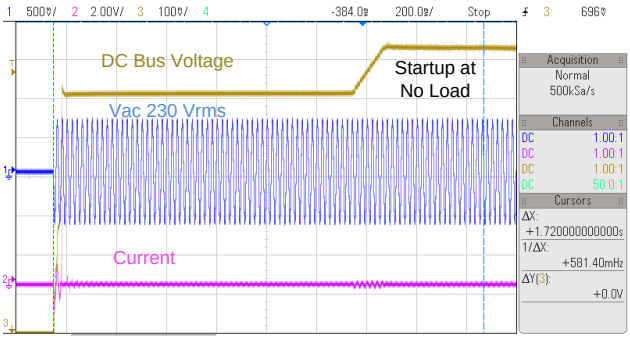

图 68. Startup of PFC Operation at 230-Vac IN, 380-V DC OUT at no Load

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3.2.2.2 Steady State Condition

图 69, 图 70, and 图 71 show the steady state current waveform at different load conditions. Phase shedding is disabled for these readings.

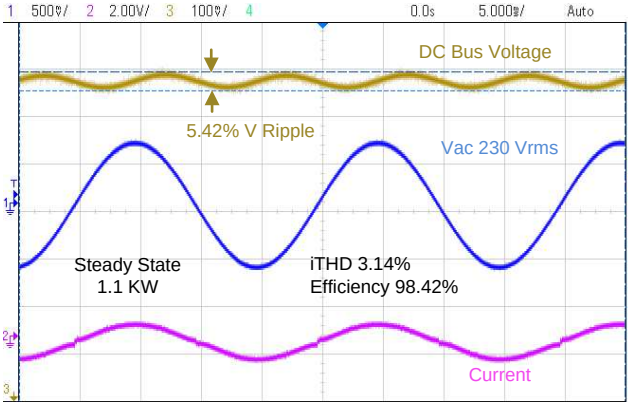

图 69. Steady State 230-Vac IN, 380-V DC OUT, 1.1KW, iTHD 3.14%

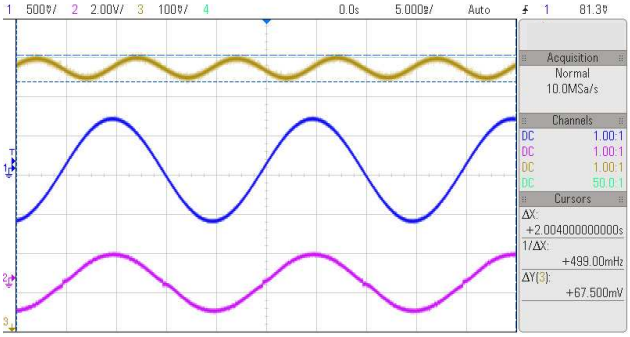

图 70. Steady State 230-Vac IN, 380-V DC OUT, 2.2KW, iTHD 2.62%

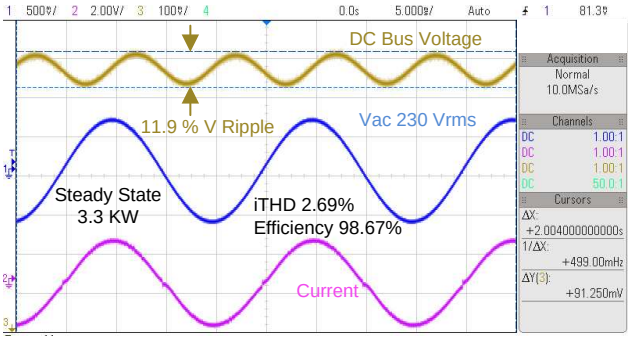

图 71. Steady State 230-Vac IN, 380-V DC OUT, 3.3KW, iTHD 2.69%

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表 5 lists the detailed test results of this design under varying load conditions with 230-Vac input and 380-V DC output. For the following data, phase shedding is disabled, adaptive dead time is enabled, 100 ns is chosen as the fixed dead time for the hard switched edge, and the soft-switching edge dead time varies between 20 ns to 200 ns.

表 5. Detailed Test Results With 230-Vac IN, 380-V DC OUT and Different Power Levels

Vin (V RMS)	Vout (V)	Pin (W)	Iout (A)	Pout (W)	EFFICIENCY %	iTHD%	PF	% RATED LOAD	THETA OFFSET	Gi Kp
230.68	381.98	151.28	0.372	142.16	94.03	18.20	0.9775	4.4	-0.025	0.35
230.43	382.00	292.24	0.736	281.41	96.29	9.15	0.9936	8.8	-0.02	0.35
230.25	382.03	435.90	1.109	423.62	97.18	6.12	0.9938	13.2	-0.01	0.35
230.06	382.06	576.40	1.473	562.86	97.66	4.85	0.9972	17.6	-0.01	0.35
229.80	382.05	856.80	2.201	841.00	98.15	4.16	0.9974	26.3	0	0.35
229.70	382.11	1140.10	2.935	1121.90	98.42	3.14	0.9989	35.1	0	0.35
229.52	382.08	1418.80	3.659	1398.40	98.57	2.42	0.9993	43.7	0	0.3
229.28	382.08	1699.20	4.386	1676.40	98.66	2.74	0.9995	52.4	0	0.3
229.06	382.09	1977.70	5.106	1951.90	98.71	2.56	0.9996	61.0	0	0.3
229.09	382.11	2261.50	5.840	2232.40	98.73	2.62	0.9995	69.8	0	0.25
228.91	382.11	2548.30	6.580	2515.60	98.73	2.50	0.9994	78.6	0	0.25
228.86	382.14	2840.60	7.332	2803.20	98.71	2.89	0.9990	87.6	0	0.2
228.51	382.12	3132.80	8.083	3091.10	98.69	2.80	0.9989	96.6	0	0.2
228.22	382.03	3439.10	8.873	3392.30	98.65	2.69	0.9988	106.0	0	0.2

3.2.2.3 Transient Test With Step Load Change

Following sections show the transient test results with step load change.

3.2.2.3.1 33% to 100% Load Step Change

图 72 shows the transient response when input is 230 Vrms and load is stepped down from 100% to 33%.

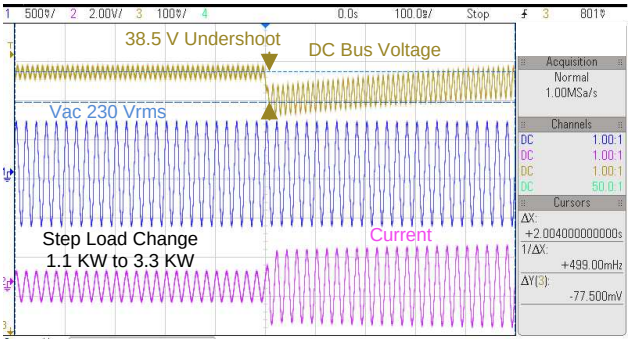

图 72. Transient Response, 230 Vrms 50 Hz, 33% to 100% Load Step

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3.2.2.3.2 100% to 33% Load Step Change

图 73 shows the transient response when input is 230 Vrms and load is stepped down from 100% to 33%.

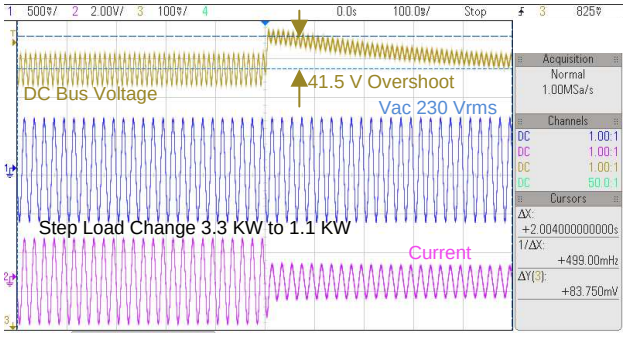

图 73. Transient Response, 230 Vrms 50 Hz, 100% to 33% Load Step

3.2.3 Test Results Graphs

图 74 shows the efficiency data plotted under different test conditions for this design.

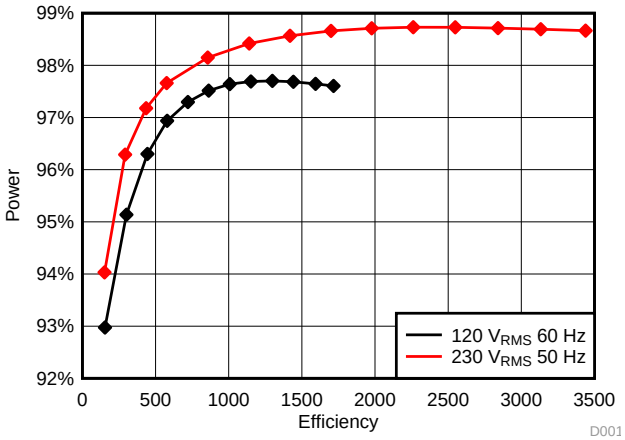

图 74. Efficiency at 230-Vrms Input and 120-Vrms Input

图 75 shows the THD data plotted under these test conditions.

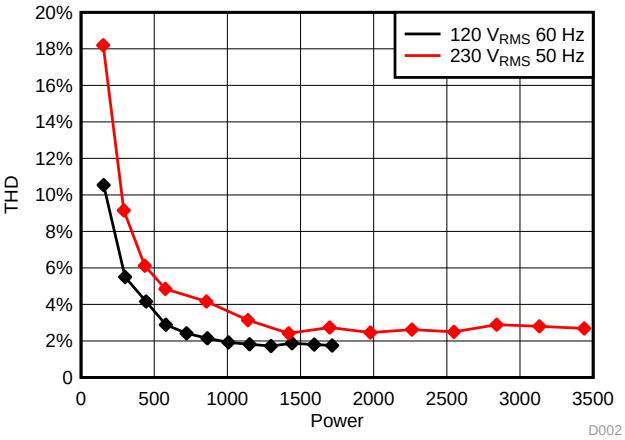

图 75. THD at 230-Vrms Input and 120-Vrms Input

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图 76 shows the PF data plotted under these test conditions.

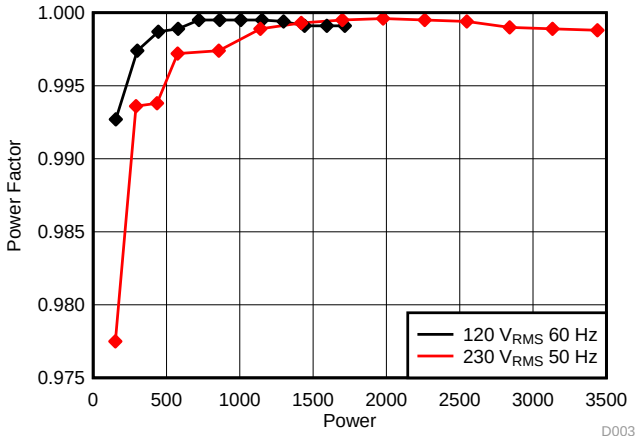

图 76. PF at 230 Vrms and 120Vrms With Varying Load

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4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDM-1007 .

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDM-1007 .

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDM-1007 .

4.4 Altium Project

To download the Altium project files, see the design files at TIDM-1007 .

4.5 Gerber Files

To download the Gerber files, see the design files at TIDM-1007 .

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDM-1007 .

5 Software Files

To download the software files, see the design files at TIDM-1007 .

6 Related Documentation

1. Texas Instruments, *How to reduced current spike at AC zero crossing for totem-pole PFC Technical Brief*
2. Z. Ye, A. Aguilar, Y. Bolurian and B. Daugherty, *GaN FET-Based High CCM Totem-Pole Bridgeless PFC*, Texas Instruments Power Supply Design Seminar, 2014-15.
3. L. Xue, Z. Shen, D. Boroyevich and P. Mattavelli, *GaN-based High Frequency Totem-Pole Bridgeless PFC Design with Digital Implementation*, IEEE 2015 Applied Power Electronics Conference, 2015, pp. 759-766.
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6. "Rodriguez, P.,Luna, A., Candela, I., Teodorescu, R., and Blaabjerg, F. *Grid Synchronization of Power Converters Using Multiple Second Order Generalized Integrators* , In Proceedings of IEEE industrial Electronics Conference (IECON'08), November 2008, pp 755-760"
7. Texas Instruments, *Software PLL Design Using C2000 MCUs Single Phase Grid Connected Inverter Application Report*
8. Texas Instruments, *TMS320F28004x Piccolo™ Microcontrollers Data Manual*
9. Texas Instruments, *LMG3410 600-V 12-A Single Channel GaN Power Stage Data Sheet*

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7 About the Author

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修订版本 B 历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from A Revision (March 2018) to B Revision **Page**

- 已添加 项目添加至特性 1
- 已添加 F28004x to 节 2.3.1 and updated text 7
- 已更改 power supply connection to TP604 from TP612 in 表 3 13
- 已更改 power supply connection to TP606/TP609 from TP609 in 表 3 13
- 已添加 节 3.1.2.3 20
- 已添加 节 3.1.2.5 40

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修订版本 A 历史记录

Changes from Original (November 2017) to A Revision **Page**

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