

# TPD3S716-Q1 可提供可调电流限制、电池短路保护和其他短路保护的汽车类 USB 2.0 接口保护器件

## 1 特性

- 符合 AEC-Q100 标准（1 级）
  - 工作温度范围：-40°C 至 +125°C
- $V_{BUS\_CON}$  引脚上具有电池短路保护（最高可达 18V）和接地短路保护
- $VD+$  和  $VD-$  引脚上具有电池短路保护（最高可达 18V）和  $V_{BUS}$  短路保护
- $V_{BUS\_CON}$ 、 $VD+$  和  $VD-$  引脚上具有 IEC 61000-4-2 静电放电 (ESD) 保护
  - $\pm 8kV$  接触放电
  - $\pm 15kV$  气隙放电
- $V_{BUS\_CON}$ 、 $VD+$  和  $VD-$  引脚上具有 ISO 10605 330pF、330 $\Omega$  ESD 保护
  - $\pm 8kV$  接触放电
  - $\pm 15kV$  气隙放电
- 低  $R_{ON}$  nFET  $V_{BUS}$  开关（典型值为 63m $\Omega$ ）
- 高速数据开关（3dB 带宽为 1GHz）
- 可调节断续电流限制最高达 2.4A）
- 短暂过压响应时间
  - $V_{BUS}$  开关的典型值为 2 $\mu s$
  - 数据开关的典型值为 200ns
- 独立的  $V_{BUS}$  和数据使能引脚（用于配置主机和客户端/OTG 模式）
- 故障输出信号
- 热关断特性
- 16 引脚 SSOP 封装（4.9mm x 3.9mm），直通布线

## 2 应用

- 终端设备
  - 音响主机
  - 后座娱乐系统
  - 远程信息处理
  - USB 集线器
  - 导航模块
  - 媒体接口
- 接口
  - USB 2.0

## 3 说明

TPD3S716-Q1 是一套具有可调节电流限制功能的单芯片解决方案，可为汽车应用中的 USB 连接器的  $V_{BUS}$  和数据线路提供电池短路保护、其他短路保护以及 ESD 保护。集成的数据开关提供了出色的带宽，能够在提供 18V 电池短路保护的同时最大限度地减少信号衰减。该器件具有 1GHz 的高带宽，适用于一些采用 USB2.0 高速数据速率的应用，例如 CarPlay。此外，该器件还具有 720MHz 以上的附加带宽裕量，有助于保持一个干净的 USB 2.0 眼图，并且支持使用较长的不可分离电缆（常见于汽车 USB 环境中）。电池短路保护可将内部系统电路隔离，防止其受到  $V_{BUS\_CON}$ 、 $VD+$  和  $VD-$  引脚上的任何过压情况的影响。在这些引脚上，TPD3S716-Q1 能够处理高达 18V 的过压情况（热插拔和直流事件）。过压保护电路可提供业内一流的电池短路保护，能够极为可靠地关断数据开关以保护上游电路免遭有害电压和电流尖峰的影响。

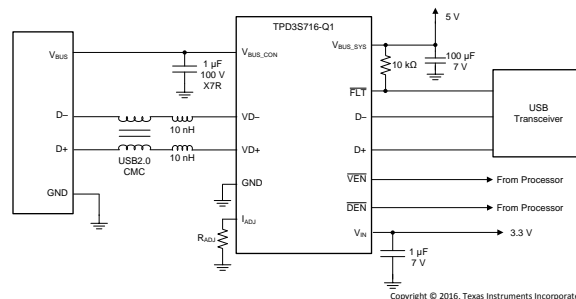
$V_{BUS\_CON}$  引脚还提供可调节的电流限制负载开关以及接地短路保护功能。该器件支持高达 2.4A 的  $V_{BUS}$  电流，支持 USB BC1.2、USB Type-C 5V/1.5A 以及最高达 2.4A 的专用充电方案。独立的数据和  $V_{BUS}$  使能引脚可用于配置主机和客户端-OTG 模式。此外，TPD3S716-Q1 还在  $V_{BUS\_CON}$ 、 $VD+$  和  $VD-$  引脚上集成了系统级 IEC 61000-4-2 和 ISO 10605 ESD 保护，无需使用高电压、低容值的外部二极管。

### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸（标称值）
TPD3S716-Q1	SSOP (16)	4.90mm x 3.90mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

### 典型应用电路原理图



## 目录

<b>1</b>	<b>特性</b> .....	<b>1</b>	8.3	Feature Description .....	<b>13</b>
<b>2</b>	<b>应用</b> .....	<b>1</b>	8.4	Device Functional Modes .....	<b>16</b>
<b>3</b>	<b>说明</b> .....	<b>1</b>	<b>9</b>	<b>Application and Implementation</b> .....	<b>18</b>
<b>4</b>	<b>修订历史记录</b> .....	<b>2</b>	9.1	Application Information .....	<b>18</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	9.2	Typical Application .....	<b>18</b>
<b>6</b>	<b>Specifications</b> .....	<b>4</b>	<b>10</b>	<b>Power Supply Recommendations</b> .....	<b>23</b>
6.1	Absolute Maximum Ratings .....	<b>4</b>	10.1	$V_{BUS}$ Path .....	<b>23</b>
6.2	ESD Ratings—AEC Specification .....	<b>4</b>	10.2	$V_{IN}$ Pin .....	<b>23</b>
6.3	ESD Ratings—IEC Specification .....	<b>4</b>	<b>11</b>	<b>Layout</b> .....	<b>23</b>
6.4	ESD Ratings—ISO Specification .....	<b>4</b>	11.1	Layout Guidelines .....	<b>23</b>
6.5	Recommended Operating Conditions .....	<b>4</b>	11.2	Layout Example .....	<b>23</b>
6.6	Thermal Information .....	<b>5</b>	11.3	Layout Optimized for Thermal Performance .....	<b>24</b>
6.7	Electrical Characteristics .....	<b>5</b>	<b>12</b>	<b>器件和文档支持</b> .....	<b>26</b>
6.8	Timing Characteristics .....	<b>7</b>	12.1	文档支持 .....	<b>26</b>
6.9	Typical Characteristics .....	<b>9</b>	12.2	社区资源 .....	<b>26</b>
<b>7</b>	<b>Parameter Measurement Information</b> .....	<b>12</b>	12.3	商标 .....	<b>26</b>
<b>8</b>	<b>Detailed Description</b> .....	<b>13</b>	12.4	静电放电警告 .....	<b>26</b>
8.1	Overview .....	<b>13</b>	12.5	Glossary .....	<b>26</b>
8.2	Functional Block Diagram .....	<b>13</b>	<b>13</b>	<b>机械、封装和可订购信息</b> .....	<b>26</b>

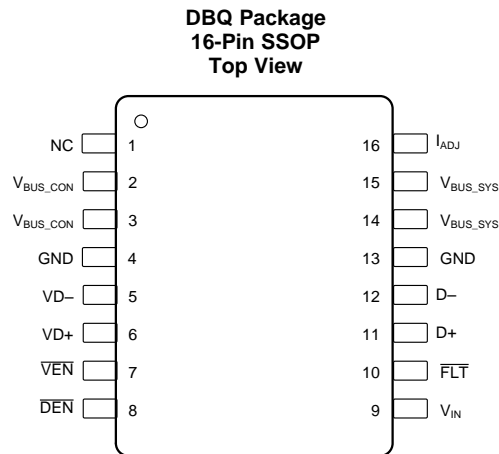
## 4 修订历史记录

<b>Changes from Revision B (April 2016) to Revision C</b>	<b>Page</b>
• 已将可调节断续电流限制从 1.7A 改为 2.4A (特性部分) .....	<b>1</b>
• 已更新说明部分 .....	<b>1</b>
• Changed <i>Current through <math>V_{BUS}</math> switch</i> from 1.7 A to 2.4 A .....	<b>5</b>
• Updated the $R_{ADJ}$ minimum resistance to 57 k $\Omega$ in <i>Recommended Operating Conditions</i> table .....	<b>5</b>
• aDDED new current limit values to <i>Electrical Characteristics</i> table .....	<b>6</b>
• Updated 图 21 .....	<b>14</b>
• Updated <i><math>I_{VBUS}</math> Operating Maximum</i> in 图 28 to go up to 2.4 A .....	<b>21</b>

<b>Changes from Revision A (April 2016) to Revision B</b>	<b>Page</b>
• 已更改 <i>Electrical Characteristics</i> 表 .....	<b>1</b>

<b>Changes from Original (March 2016) to Revision A</b>	<b>Page</b>
• 已将器件状态从产品预览改为量产数据 .....	<b>1</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	NC	NC	No connect, leave floating or connect to ground. Do not connect to $V_{BUS\_CON}$
2	$V_{BUS\_CON}$	O	Connect to USB connector $V_{BUS}$ ; provides IEC 61000-4-2 ESD protection
3	$V_{BUS\_CON}$	O	
4	GND	Ground	Connect to PCB ground plane
5	VD-	I/O	Connect to USB connector D-; provides IEC 61000-4-2 ESD protection
6	VD+	I/O	Connect to USB connector D+; provides IEC 61000-4-2 ESD protection
7	$\overline{VEN}$	I	Enable Active-Low Input. Drive $\overline{VEN}$ low to enable the $V_{BUS}$ path of the device. Drive $\overline{VEN}$ high to disable the $V_{BUS}$ path of the device
8	$\overline{DEN}$	I	Enable Active-Low Input. Drive $\overline{DEN}$ low to enable the data path of the device. Drive $\overline{DEN}$ high to disable the data path of the device
9	$V_{IN}$	I	Connect to 3.3-V I/O. Controls the OVP threshold for VD+/VD-
10	$\overline{FLT}$	O	Open-Drain fault pin. See the <a href="#">Detailed Description</a> section for operation
11	D+	I/O	Connect to the internal transceiver D+ pin
12	D-	I/O	Connect to the internal transceiver D- pin
13	GND	Ground	Connect to PCB ground plane
14	$V_{BUS\_SYS}$	I	Connect to internal $V_{BUS}$ plane
15	$V_{BUS\_SYS}$	I	
16	$I_{ADJ}$	I	Connect to a resistor to GND to adjust the current limit threshold

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

		MIN	MAX	UNIT
V <sub>BUS_CON</sub>	Supply voltage from USB connector	-0.3	18	V
V <sub>BUS_SYS</sub>	Internal Supply DC voltage Rail on the PCB	-0.3	6	V
VD+, VD-	Voltage range from connector-side USB data lines	-0.3	18	V
D+, D-	Voltage range for internal USB data lines	-0.3	V <sub>IN</sub> + 0.3	V
V <sub>IN</sub>	Voltage range for V <sub>IN</sub> supply input	-0.3	4	V
$\overline{\text{DEN}}$	Voltage on enable pins		7	V
$\overline{\text{VEN}}$			7	V
I <sub>BUS</sub>	Maximum DC output current on V <sub>BUS_CON</sub> pin <sup>(3)</sup>		2.4	A
V <sub>IADJ</sub>	Voltage range for I <sub>ADJ</sub> pin	-0.3	V <sub>BUS_SYS</sub> + 0.3	V
V <sub>FLT</sub>	Voltage range for the $\overline{\text{FLT}}$ pin	-0.3	7	V
T <sub>A</sub>	Operating free air temperature <sup>(3)</sup>	-40	125	°C
T <sub>STG</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) Thermal limits and power dissipation limits must be observed.

### 6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2, V <sub>BUS_CON</sub> , VD+, VD- pins	Contact discharge <sup>(1)</sup>	V
			Air-gap discharge <sup>(1)</sup>	

- (1) See [Figure 20](#) for details on system level ESD testing setup.

### 6.4 ESD Ratings—ISO Specification

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	ISO 10605 (330 pF, 330 Ω), V <sub>BUS_CON</sub> , VD+, VD- pins	Contact discharge <sup>(1)</sup>	V
			Air-gap discharge <sup>(1)</sup>	

- (1) See [Figure 20](#) for details on system level ESD testing setup.

### 6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>BUS_CON</sub>	Supply voltage from USB connector			5.9	V
V <sub>BUS_SYS</sub>	Internal supply DC voltage Rail on the PCB	4.75		5.9	V
VD+, VD-	Voltage range from connector-side USB data lines	0		V <sub>IN</sub> + 0.3	V
D+, D-	Voltage range for internal USB data lines	0		V <sub>IN</sub> + 0.3	V
V <sub>IN</sub>	Voltage range for V <sub>IN</sub> supply	3		3.6	V

## Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$I_{BUS}$	Current through $V_{BUS}$ switch <sup>(1)</sup>			2.4	A
$\overline{VEN}$ , $\overline{DEN}$	Voltage range for enable	0		5.9	V
$C_{SYS}$	Input capacitance <sup>(2)</sup>		100		$\mu$ F
$C_{LOAD}$	Output load capacitance <sup>(2)</sup>				$\mu$ F
$C_{VIN}$	$V_{IN}$ capacitance <sup>(2)</sup>				$\mu$ F
$R_{ADJ}$	Resistance of $R_{ADJ}$ resistor <sup>(2)</sup>			57	k $\Omega$

(1) Depending on your  $I_{BUS}$  current level, maximum operating junction temperature derating may be required. For  $I_{BUS} > 1.5A$ , care should be taken in the PCB design to improve the board's thermal coefficient. Please see both the [Power Dissipation and Junction Temperature](#) and [Layout Optimized for Thermal Performance](#) sections for more details.

(2) See the [Figure 22](#) for configuration details.

## 6.6 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPD3S716-Q1	UNIT
		DBQ (SSOP)	
		16 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	98.8	$^{\circ}C/W$
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance	48.0	$^{\circ}C/W$
$\theta_{JB}$	Junction-to-board thermal resistance	41.6	$^{\circ}C/W$
$\Psi_{JT}$	Junction-to-top characterization parameter	8.5	$^{\circ}C/W$
$\Psi_{JB}$	Junction-to-board characterization parameter	41.2	$^{\circ}C/W$
$\theta_{JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	$^{\circ}C/W$
$\theta_{JA(Custom)}$	See the <a href="#">Layout Optimized for Thermal Performance</a> section	57.0	$^{\circ}C/W$

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.7 Electrical Characteristics

over operating free-air temperature range,  $\overline{VEN} = 0V$ ,  $\overline{DEN} = 0V$ ,  $V_{BUS\_SYS} = 5V$ ,  $V_{IN} = 3.3V$ ,  $VD+/VD-/D+/D-/V_{BUS\_CON} =$  float (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT CONSUMPTION</b>							
$I_{VBUS\_SLEEP}$	$V_{BUS}$ Sleep current consumption	Measured at $V_{BUS\_SYS}$ pin, $\overline{VEN} = 5V$ , $\overline{DEN} = 5V$		45	150		$\mu$ A
$I_{VBUS}$	$V_{BUS}$ Operating current consumption	Measured at $V_{BUS\_SYS}$ pin		285	380		$\mu$ A
$I_{VIN}$	Leakage current for $V_{IN}$	Measured at $V_{IN}$ pin, $V_{IN} = 3.6V$		12	20		$\mu$ A
$I_{ON(LEAK)}$	Leakage into $V_{BUS\_SYS}$ while shorted to battery and powered on	Measured flowing into $V_{BUS\_SYS}$ pin, $V_{BUS\_SYS} = 5V$ , $V_{BUS\_CON} = 18V$		225	300		$\mu$ A
$I_{OFF(LEAK)}$	Leakage through $V_{BUS}$ path while shorted to battery and unpowered	Measured flowing out of $V_{BUS\_SYS}$ pin, $V_{BUS\_SYS} = 0V$ , $V_{BUS\_CON} = 18V$			50		$\mu$ A
$I_{D(OFF\_LEAK)}$	Leakage out of data path while shorted to battery and unpowered	Measured flowing out of D+ or D- pins, $V_{BUS\_SYS} = 0V$ , $VD+$ or $VD- = 18V$ , $V_{IN} = 0V$ , $D+/D- = 0V$		-1		1	$\mu$ A
$I_{D(ON\_LEAK)}$	Leakage out of data path while shorted to battery and powered on	Measured flowing out of D+ or D- pins, $V_{BUS\_SYS} = 5V$ , $VD+$ or $VD- = 18V$ , $V_{IN} = 3.3V$ , $D+/D- = 0V$		-1		1	$\mu$ A
$I_{VD(OFF\_LEAK)}$	Leakage into data path while shorted to battery and unpowered	Measured flowing in to $VD+$ or $VD-$ pins, $V_{BUS\_SYS} = 0V$ , $VD+$ or $VD- = 18V$ , $V_{IN} = 0V$ , $D+/D- = 0V$				85	$\mu$ A
$I_{VD(ON\_LEAK)}$	Leakage into data path while shorted to battery and powered on	Measured flowing in to $VD+$ or $VD-$ pins, $V_{BUS\_SYS} = 5V$ , $VD+$ or $VD- = 18V$ , $V_{IN} = 3.3V$ , $D+/D- = 0V$				85	$\mu$ A
<b><math>V_{IN}</math> PIN</b>							
$V_{UVLO(RISING)}$	Undervoltage lockout rising for $V_{IN}$	$V_{IN}$	Ramp $V_{IN}$ up until $V_{BUS}$ and Data FETs turn on, $\overline{VEN} = 0V$ , $\overline{DEN} = 0V$	2.6	2.7	2.9	V
$V_{UVLO(FALLING)}$	Undervoltage lockout falling for $V_{IN}$		Ramp $V_{IN}$ down until $V_{BUS}$ and Data FETs turn off, $\overline{VEN} = 0V$ , $\overline{DEN} = 0V$	2.5	2.6	2.8	
<b><math>\overline{VEN}</math>, <math>\overline{DEN}</math>, FLT PINS</b>							

**Electrical Characteristics (continued)**

over operating free-air temperature range,  $\overline{VEN} = 0\text{ V}$ ,  $\overline{DEN} = 0\text{ V}$ ,  $V_{BUS\_SYS} = 5\text{ V}$ ,  $V_{IN} = 3.3\text{ V}$ ,  $VD+/VD-/D+/D-/V_{BUS\_CON} = \text{float}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IH}$	High-level input voltage	$\overline{VEN}$ , $\overline{DEN}$	Set $\overline{VEN}$ ( $\overline{DEN}$ ) = 0 V; Sweep $\overline{VEN}$ ( $\overline{DEN}$ ) to 1.4 V; Measure when $V_{BUS}$ (Data) FET turns off	1.2			V
$V_{IL}$	Low-level input voltage	$\overline{VEN}$ , $\overline{DEN}$	Set $\overline{VEN}$ ( $\overline{DEN}$ ) = 3.3 V; Sweep $\overline{VEN}$ ( $\overline{DEN}$ ) from 3.3 V to 0.5 V; Measure when $V_{BUS}$ (Data) FET turns on			0.8	V
$I_{IL}$	Input Leakage Current	$\overline{VEN}$ , $\overline{DEN}$	$V_{(\overline{VEN})}$ ( $V_{(\overline{DEN})}$ ) = 3.3 V; Measure Current into $\overline{VEN}$ ( $\overline{DEN}$ ) pin			1	$\mu\text{A}$
$V_{OL}$	Low-level output voltage	$\overline{FLT}$	$I_{OL} = 3\text{ mA}$			0.4	V
<b>OCP CIRCUIT—<math>V_{BUS}</math></b>							
$I_{LIM}$	Overcurrent limit, $R_{ADJ} = 280\text{ k}\Omega \pm 1\%$	$V_{BUS}$	Progressively load $V_{BUS\_CON}$ until device asserts $\overline{FLT}$	505		620	mA
$I_{LIM}$	Overcurrent limit, $R_{ADJ} = 158\text{ k}\Omega \pm 1\%$	$V_{BUS}$	Progressively load $V_{BUS\_CON}$ until device asserts $\overline{FLT}$	0.905		1.1	A
$I_{LIM}$	Overcurrent limit, $R_{ADJ} = 143\text{ k}\Omega \pm 1\%$	$V_{BUS}$	Progressively load $V_{BUS\_CON}$ until device asserts $\overline{FLT}$	1.005		1.2	A
$I_{LIM}$	Overcurrent limit, $R_{ADJ} = 93.1\text{ k}\Omega \pm 1\%$	$V_{BUS}$	Progressively load $V_{BUS\_CON}$ until device asserts $\overline{FLT}$	1.505		1.8	A
$I_{LIM}$	Overcurrent limit, $R_{ADJ} = 76.8\text{ k}\Omega \pm 1\%$	$V_{BUS}$	Progressively load $V_{BUS\_CON}$ until device asserts $\overline{FLT}$	1.8		2.16	A
$I_{LIM}$	Overcurrent limit, $R_{ADJ} = 66.5\text{ k}\Omega \pm 1\%$	$V_{BUS}$	Progressively load $V_{BUS\_CON}$ until device asserts $\overline{FLT}$	2.105		2.57	A
$I_{LIM}$	Overcurrent limit, $R_{ADJ} = 57.6\text{ k}\Omega \pm 1\%$	$V_{BUS}$	Progressively load $V_{BUS\_CON}$ until device asserts $\overline{FLT}$	2.405		2.93	A
$I_{LIM}$	Overcurrent limit, $I_{ADJ} = \text{GND}$	$V_{BUS}$	Progressively load $V_{BUS\_CON}$ until device asserts $\overline{FLT}$	550	700	850	mA
$I_{LIM}$	Overcurrent limit, $I_{ADJ} = V_{BUS\_SYS}$	$V_{BUS}$	Progressively load $V_{BUS\_CON}$ until device asserts $\overline{FLT}$	1.1	1.4	1.7	A
<b>OVER TEMPERATURE PROTECTION</b>							
$T_{SD(\text{RISING})}$	The rising over-temperature protection shutdown threshold	$V_{BUS\_SYS} = 5\text{ V}$ , $\overline{VEN} = 0\text{ V}$ , $\overline{DEN} = 0\text{ V}$ , No Load on $V_{BUS\_CON}$ , $T_A$ stepped up until $\overline{FLT}$ is asserted		150	165	180	$^{\circ}\text{C}$
$T_{SD(\text{FALLING})}$	The falling over-temperature protection shutdown threshold	$V_{BUS\_SYS} = 5\text{ V}$ , $\overline{VEN} = 0\text{ V}$ , $\overline{DEN} = 0\text{ V}$ , No Load on $V_{BUS\_CON}$ , $T_A$ stepped down from $T_{SD(\text{RISING})}$ until $\overline{FLT}$ is deasserted		125	130	142	$^{\circ}\text{C}$
$T_{SD(\text{HYST})}$	The over-temperature protection shutdown threshold hysteresis	$T_{SD(\text{RISING})} - T_{SD(\text{FALLING})}$		10	35	55	$^{\circ}\text{C}$
<b>OVP CIRCUIT—<math>V_{BUS}</math></b>							
$V_{OVP(\text{RISING})}$	Input overvoltage protection threshold	$V_{BUS\_CON}$	Increase $V_{BUS\_CON}$ from 5 V to 7 V. Measure when $\overline{FLT}$ is asserted	5.6	5.8	6	V
$V_{HYS(\text{OVP})}$	Hysteresis on OVP	$V_{BUS\_CON}$	Difference between rising and falling OVP thresholds on $V_{BUS\_CON}$		50		mV
$V_{OVP(\text{FALLING})}$	Input overvoltage protection threshold	$V_{BUS\_CON}$	Decrease $V_{BUS\_CON}$ from 7 V to 5 V. Measure when $\overline{FLT}$ is deasserted	5.52	5.75	5.98	V
$V_{REV\_SUPPLY(\text{RISING})}$	Reverse supply detection threshold	$V_{BUS\_CON} - V_{BUS\_SYS}$	Set $V_{BUS\_SYS}$ to 5 V. Increase $V_{BUS\_CON}$ from $V_{BUS\_SYS}$ to $V_{BUS\_SYS} + 300\text{ mV}$ . Measure the value of $V_{BUS\_CON} - V_{BUS\_SYS}$ when $\overline{FLT}$ asserts. $25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$	140	200	260	mV
$V_{REV\_SUPPLY(\text{FALLING})}$	Reverse supply detection threshold	$V_{BUS\_CON} - V_{BUS\_SYS}$	Set $V_{BUS\_SYS}$ to 5 V. Decrease $V_{BUS\_CON}$ from $V_{BUS\_SYS} + 300\text{ mV}$ to $V_{BUS\_SYS}$ . Measure the value of $V_{BUS\_CON} - V_{BUS\_SYS}$ when $\overline{FLT}$ deasserts. $25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$	70	120	165	mV
$V_{REV\_SUPPLY(\text{HYST})}$	Hysteresis on reverse supply detection	$V_{BUS\_CON} - V_{BUS\_SYS}$	Difference between rising and falling reverse supply detection thresholds		80		mV
$V_{UVLO(\text{SYS\_RISING})}$	Undervoltage lockout rising for $V_{BUS\_SYS}$	$V_{BUS\_SYS}$	$V_{BUS\_SYS}$ voltage rising from 0 V to 5 V	3.1	3.3	3.6	V
$V_{HYS(\text{UVLO\_SYS})}$	$V_{BUS\_SYS}$ UVLO Hysteresis	$V_{BUS\_SYS}$	Difference between rising and falling UVLO thresholds on $V_{BUS\_SYS}$	50	75	100	mV
$V_{UVLO(\text{SYS\_FALLING})}$	Undervoltage lockout falling for $V_{BUS\_SYS}$	$V_{BUS\_SYS}$	$V_{BUS\_SYS}$ voltage falling from 5 V to 2.9 V	3	3.2	3.5	V

## Electrical Characteristics (continued)

over operating free-air temperature range,  $\overline{VEN} = 0\text{ V}$ ,  $\overline{DEN} = 0\text{ V}$ ,  $V_{BUS\_SYS} = 5\text{ V}$ ,  $V_{IN} = 3.3\text{ V}$ ,  $VD+/VD-/D+/D-/V_{BUS\_CON} = \text{float}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{SHRT(RISING)}$	Short-to-ground comparator rising threshold	$V_{BUS\_CON}$	Increase $V_{BUS\_CON}$ voltage from 0 V until the device transitions from the short-circuit to over-current mode of operation	2.5	2.6	2.7	V
$V_{SHRT(FALLING)}$	Short-to-ground comparator falling threshold	$V_{BUS\_CON}$	Set $V_{BUS\_SYS} = 5\text{ V}$ ; $V_{IN} = 3.3\text{ V}$ ; $\overline{VEN} = 0\text{ V}$ , $\overline{DEN} = 0\text{ V}$ ; Decrease $V_{BUS\_CON}$ voltage from 5 V until the device transitions from the over-current to short-circuit mode of operation	2.4	2.5	2.6	V
$V_{SHRT(HYST)}$	Short-to-ground comparator hysteresis	$V_{BUS\_CON}$	Difference between $V_{SHRT(RISING)}$ and $V_{SHRT(FALLING)}$		125		mV
$I_{SHRT}$	Short-to-ground current source	$V_{BUS\_CON}$	Current sourced from $V_{BUS\_SYS}$ when device is in short-circuit mode	150		350	mA
<b>OVP CIRCUIT—VD+/VD–</b>							
$V_{OVP(RISING)}$	Input overvoltage protection threshold	VD+/VD–	Increase VD+ or VD– (with D+ and D–) from 3.3 V to 4.5 V. Measure the value at which FLT is asserted	$V_{IN} + 0.6$	$V_{IN} + 0.8$	$V_{IN} + 1$	V
$V_{HYS(OVP)}$	Hysteresis on OVP	VD+/VD–	Difference between rising and falling OVP thresholds on VD+/VD–		50		mV
$V_{OVP(FALLING)}$	Input overvoltage protection threshold	VD+/VD–	Decrease VD+ or VD– (with D+ or D–) from 4.5 V to 2 V. Measure the value at FLT is deasserted	$V_{IN} + 0.525$	$V_{IN} + 0.75$	$V_{IN} + 0.975$	V
<b>SHORT TO BATTERY</b>							
$V_{(VBUS\_STB)}$	$V_{BUS}$ hotplug short-to-battery tolerance	$V_{BUS\_CON}$	Charge battery-equivalent capacitor to test voltage then discharge to pin under test through a 1 meter, 18 gauge wire. (See <a href="#">Figure 19</a> for more details)			18	V
$V_{(DATA\_STB)}$	Data line hotplug short-to-battery tolerance	VD+/VD–				18	V
<b>DATA LINE SWITCHES—VD+ to D+ or VD– to D–</b>							
$C_{ON}$	Equivalent On Capacitance		Capacitance of D+/D– switches when enabled – measure on connector side at $VDx = 0.4\text{ V}$		6.9		pF
$R_{ON}$	On Resistance		Measure resistance between D+ and VD+ or D– and VD–, voltage between 0 V and 0.4 V		4	6.5	$\Omega$
$R_{ON(Flat)}$	On Resistance flatness		Measure resistance between D+ and VD+ or D– and VD–, sweep voltage between 0 V and 0.4 V		0.2	1	$\Omega$
$BW_{ON}$	On Bandwidth (–3dB)		Measure $S_{D21}$ bandwidth from D+ to VD+ or D– to VD– with voltage swing = 400 mVpp, $V_{CM} = 0.2\text{ V}$		910		MHz
$BW_{ON\_DIFF}$	On Bandwidth (–3dB)		Measure $S_{D21}$ bandwidth from D+ to VD+ and D– to VD– with voltage swing = 800 mVpp differential, $V_{CM} = 0.2\text{ V}$		1050		MHz
$X_{talk}$	Crosstalk		Measure $S_{21}$ bandwidth from D+ to VD– or D– to VD+ with voltage swing = 400 mVpp. Make sure to terminate open sides to 50 ohms. $f = 480\text{ MHz}$		–28		dB
<b>nFET SWITCH—<math>V_{BUS}</math></b>							
$R_{(DISCHARGE)}$	Output discharge resistance		$\overline{VEN} = 5\text{ V}$ , $\overline{DEN} = 5\text{ V}$ , Set $V_{BUS\_CON} = 5\text{ V}$ and measure current flow to ground		18	30	k $\Omega$
$R_{ON}$	$V_{BUS}$ path ON resistance		$V_{BUS\_CON} = 5\text{ V}$ , $I_{OUT} = 1.5\text{ A}$ . See <a href="#">Figure 29</a> for a plot of the maximum $V_{BUS}$ $R_{ON}$ possible at a given junction temperature		63	135	m $\Omega$

## 6.8 Timing Characteristics

over operating free-air temperature range,  $\overline{VEN} = 0\text{ V}$ ,  $\overline{DEN} = 0\text{ V}$ ,  $V_{BUS\_SYS} = 5\text{ V}$ ,  $V_{IN} = 3.3\text{ V}$ ,  $D+/D- = 45\ \Omega$  to GND,  $VD+/VD-/V_{BUS\_CON} = \text{float}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>ENABLE PIN</b>							
$t_{ON\_HOST}$	Host mode enable on time		Time between $\overline{VEN}$ and $\overline{DEN}$ asserted low and $V_{BUS}$ and Data FETs turn on, $C_{VBUS\_CON} = 0\ \mu\text{F}$		5.7		ms
$t_{ON\_CLIENT}$	Client mode enable on time		Time between $\overline{DEN}$ asserted low and Data FETs turn on. $\overline{VEN}$ remains high		2.4		ms
$t_{OFF\_HOST}$	Host mode disable time		Time between $\overline{VEN}$ and $\overline{DEN}$ deasserted high and $V_{BUS}$ and Data FETs turn off, $C_{VBUS\_CON} = 0\ \mu\text{F}$		30		$\mu\text{s}$



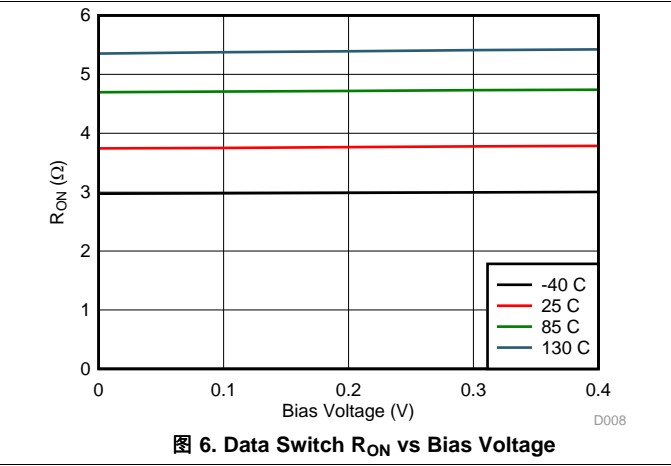
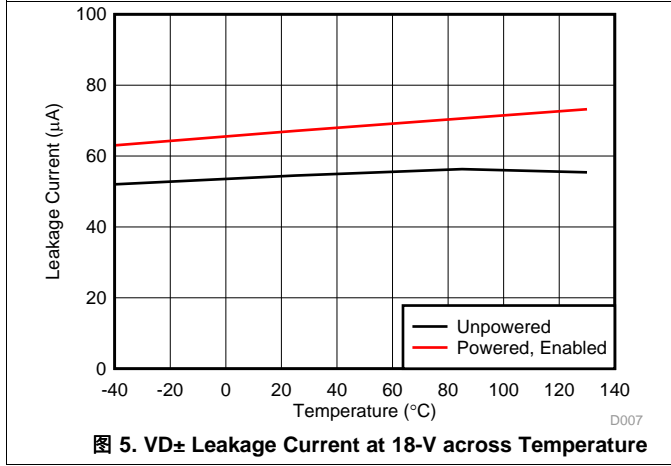
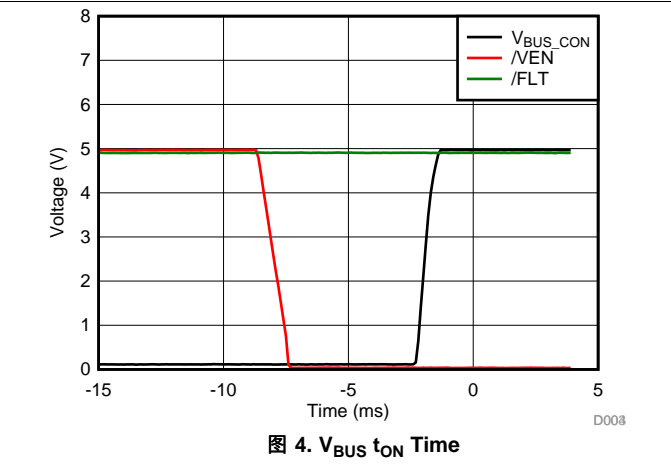
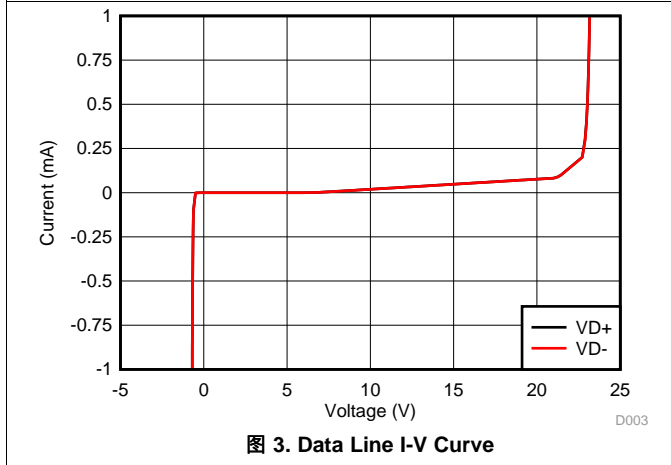
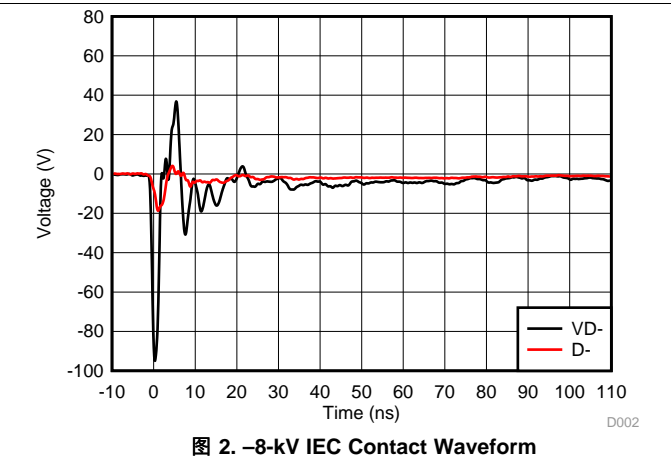
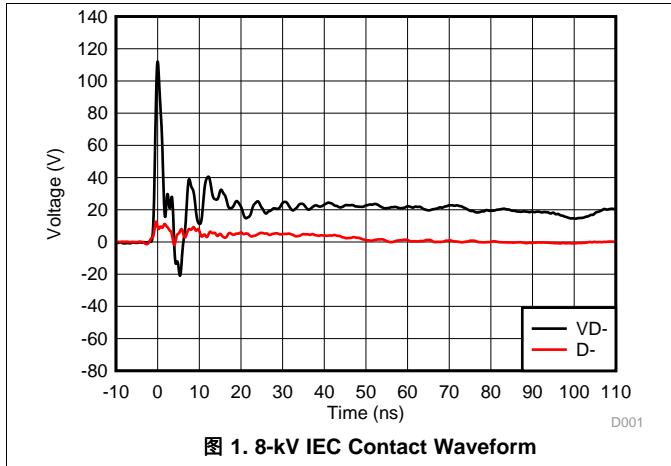
**Timing Characteristics (continued)**

over operating free-air temperature range,  $\overline{VEN} = 0\text{ V}$ ,  $\overline{DEN} = 0\text{ V}$ ,  $V_{BUS\_SYS} = 5\text{ V}$ ,  $V_{IN} = 3.3\text{ V}$ ,  $D+/D- = 45\ \Omega$  to GND,  $VD+/VD-/V_{BUS\_CON} = \text{float}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{OFF\_CLIENT}$	Client mode disable time	Time between $\overline{DEN}$ deasserted high and Data FETs turn off. $\overline{VEN}$ remains high		5		$\mu\text{s}$
$t_{HOST\_TO\_CLIENT}$	Host to Client mode transition time	Time between $\overline{VEN}$ deasserted high and $V_{BUS}$ FET turns off. $\overline{DEN}$ remains low, $C_{VBUS\_CON} = 0\ \mu\text{F}$		70		$\mu\text{s}$
$t_{CLIENT\_TO\_HOST}$	Client to Host mode transition time	Time between $\overline{VEN}$ asserted low and $V_{BUS}$ FET turns on. $\overline{DEN}$ remains low, $C_{VBUS\_CON} = 0\ \mu\text{F}$		3.4		ms
<b>OVER CURRENT PROTECTION</b>						
$t_{BLANK}$	Overcurrent blanking time	Time from overcurrent condition until $\overline{FLT}$ assertion and $V_{BUS}$ FET turn off			2	ms
$t_{RETRY}$	Overcurrent retry time	Time from overcurrent FET shut off until FET turns back on		100		ms
$t_{RECV}$	Overcurrent recovery time	Time from end of $t_{RETRY}$ until $\overline{FLT}$ deassertion if overcurrent condition is removed		8		ms
<b>OVER VOLTAGE PROTECTION</b>						
$t_{OVP\_response}$	OVP Response time – $V_{BUS}$	Measured from OVP Condition to FET turnoff		2	4	$\mu\text{s}$
$t_{OVP\_response}$	OVP Response time – data switches	Measured from OVP Condition to FET turnoff		200		ns
$t_{OVP\_FLT\_ASSET}$	OVP $\overline{FLT}$ assertion time	Measured from an OVP Condition to $\overline{FLT}$ assertion		14		$\mu\text{s}$
<b>SHORT TO GROUND PROTECTION</b>						
$t_{SHRT}$	Short to ground response time	Time from short condition until current falls below 120% of $I_{SHRT}$ , $C_{VBUS\_CON} = 0\ \mu\text{F}$		2	4	$\mu\text{s}$
$t_{SHRT\_FLTZ}$	Short to ground $\overline{FLT}$ assertion time	Time from short condition until $\overline{FLT}$ is asserted, $C_{VBUS\_CON} = 0\ \mu\text{F}$		20		$\mu\text{s}$
<b>REVERSE SUPPLY DETECTION</b>						
$t_{REV\_SUPPLY\_BLANK}$	Reverse supply blanking time	Time from reverse current condition until $\overline{FLT}$ assertion			2	ms



### 6.9 Typical Characteristics



Typical Characteristics (接下页)

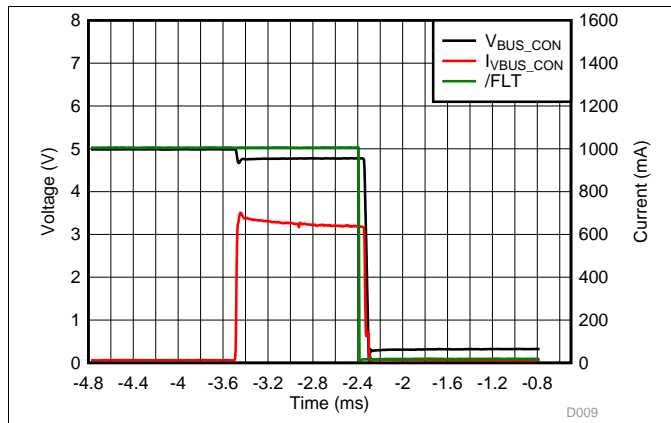


图 7. Overcurrent  $t_{BLANK}$  Response Waveform

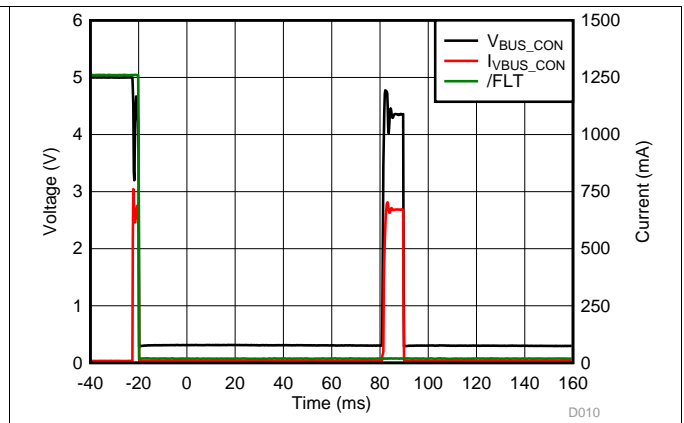


图 8. Overcurrent  $t_{BLANK\_RETRY}$  Response Waveform

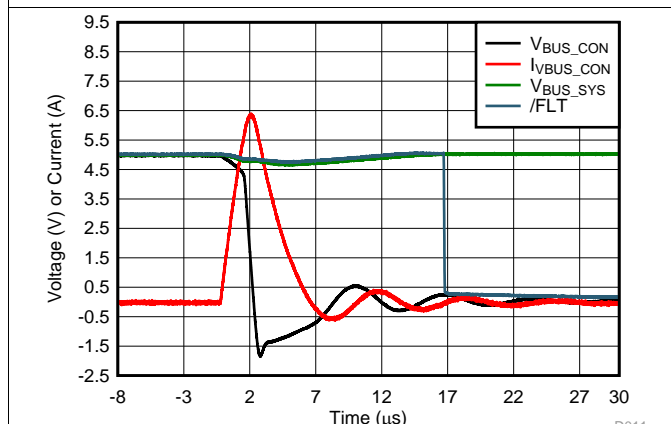


图 9.  $V_{BUS}$  Short-to-Ground Response Waveform

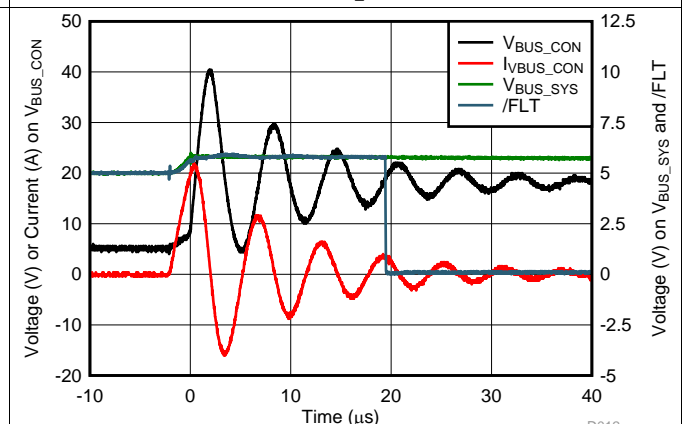


图 10.  $V_{BUS}$  Short-to-18 V Response Waveform

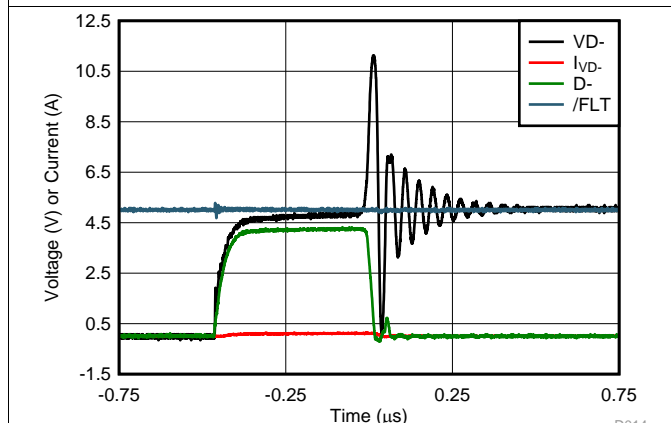


图 11. Data Switch Short-to-5 V Response Waveform

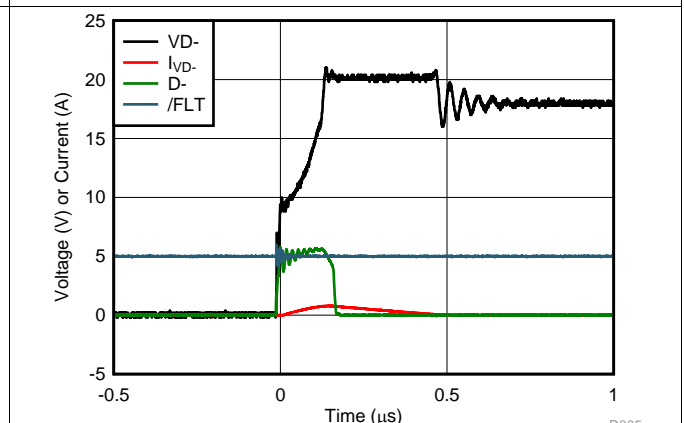


图 12. Data Switch Short-to-18 V Response Waveform

Typical Characteristics (接下页)

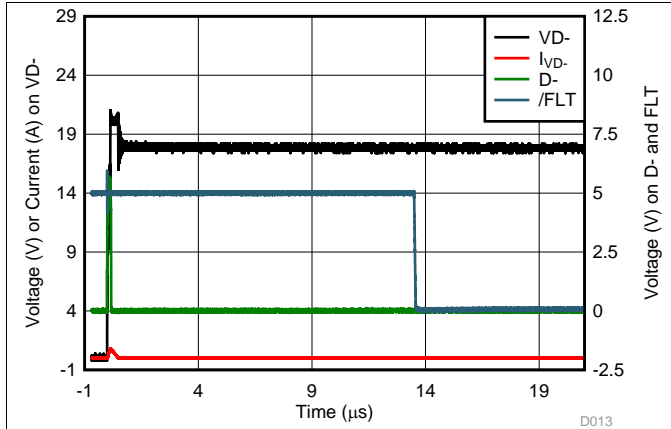


图 13. Data Switch Short-to-18 V Response Waveform (Long)

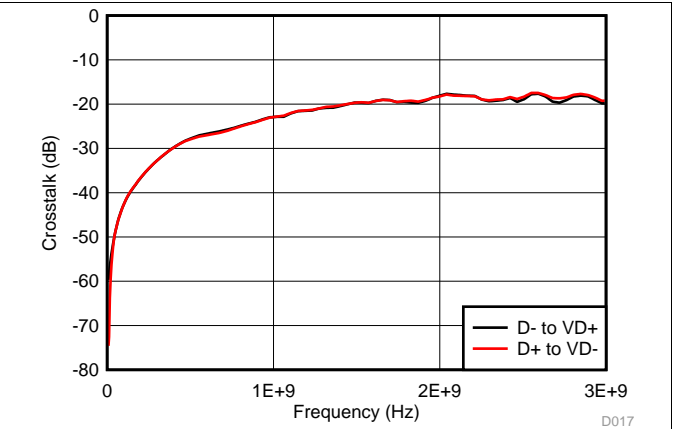


图 14. Data Switch Crosstalk

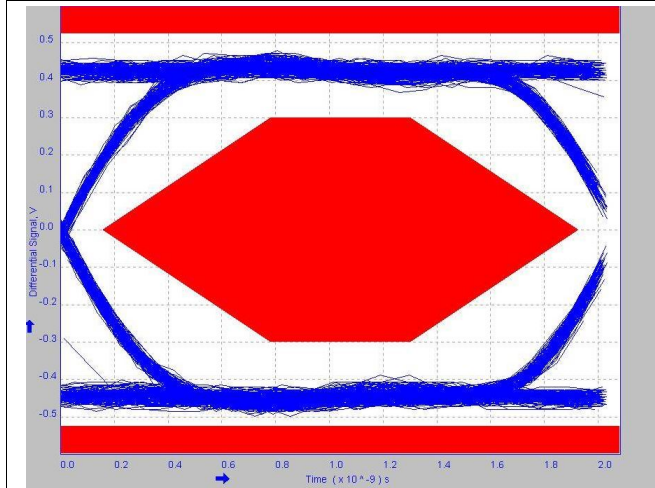


图 15. USB2.0 Eye Diagram (no TPD3S716-Q1)

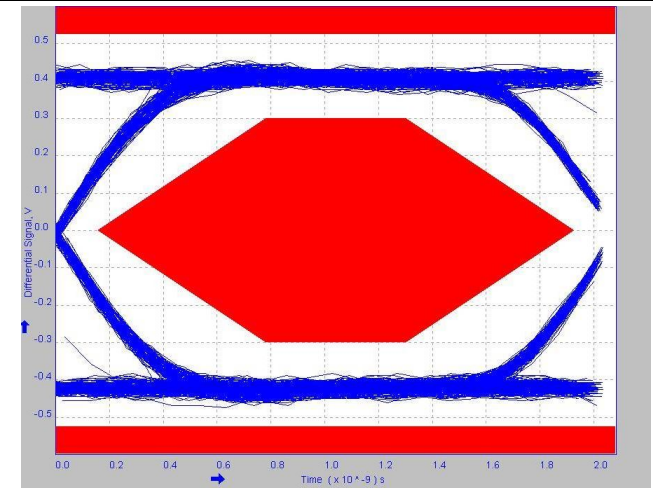


图 16. USB2.0 Eye Diagram (with TPD3S716-Q1)

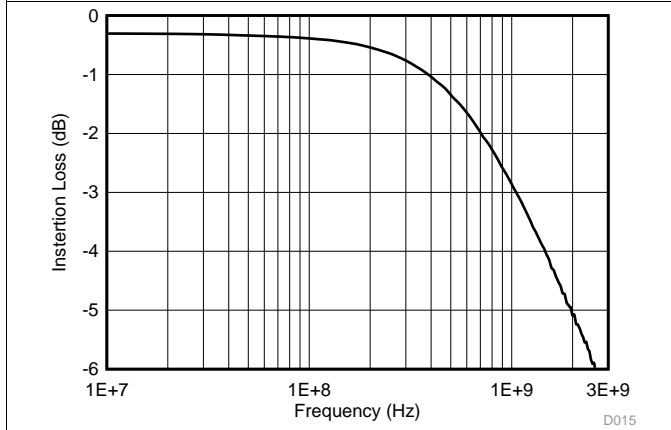


图 17. Data Switch Differential Bandwidth

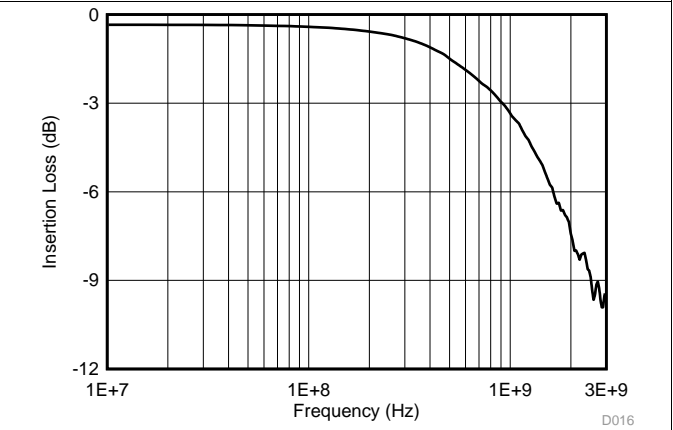
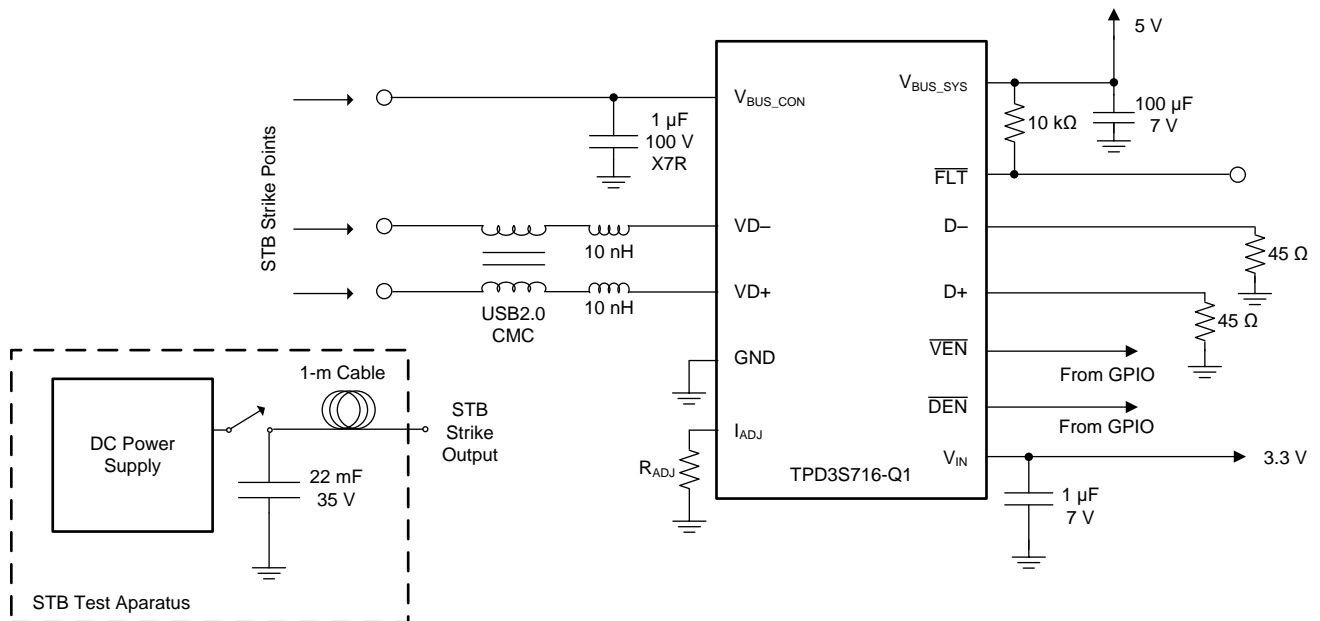


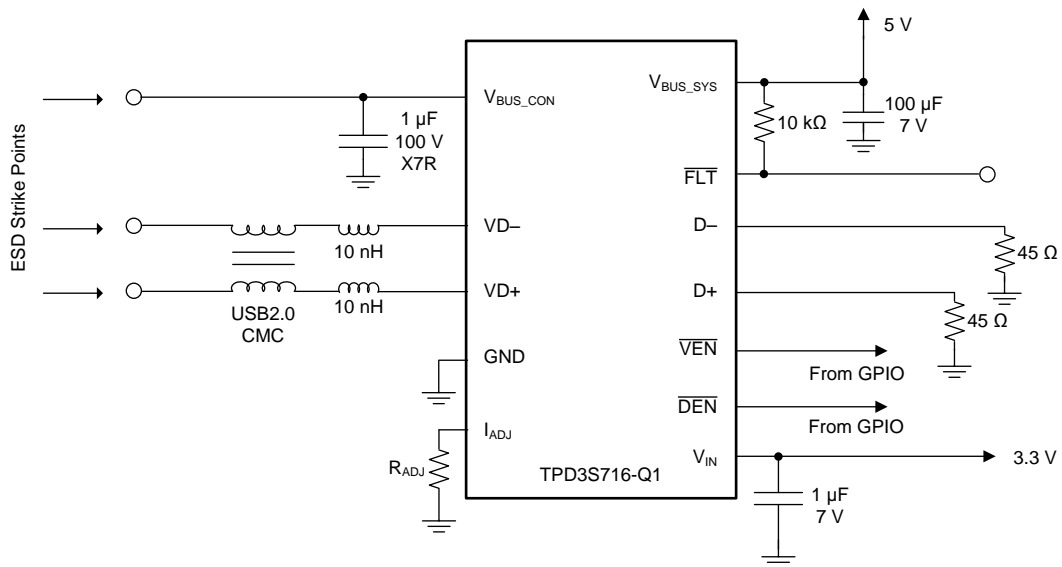
图 18. Data Switch Single-Ended Bandwidth

## 7 Parameter Measurement Information



Copyright © 2016, Texas Instruments Incorporated

图 19. Short-to-Battery System Test Setup



Copyright © 2016, Texas Instruments Incorporated

图 20. ESD System Test Setup

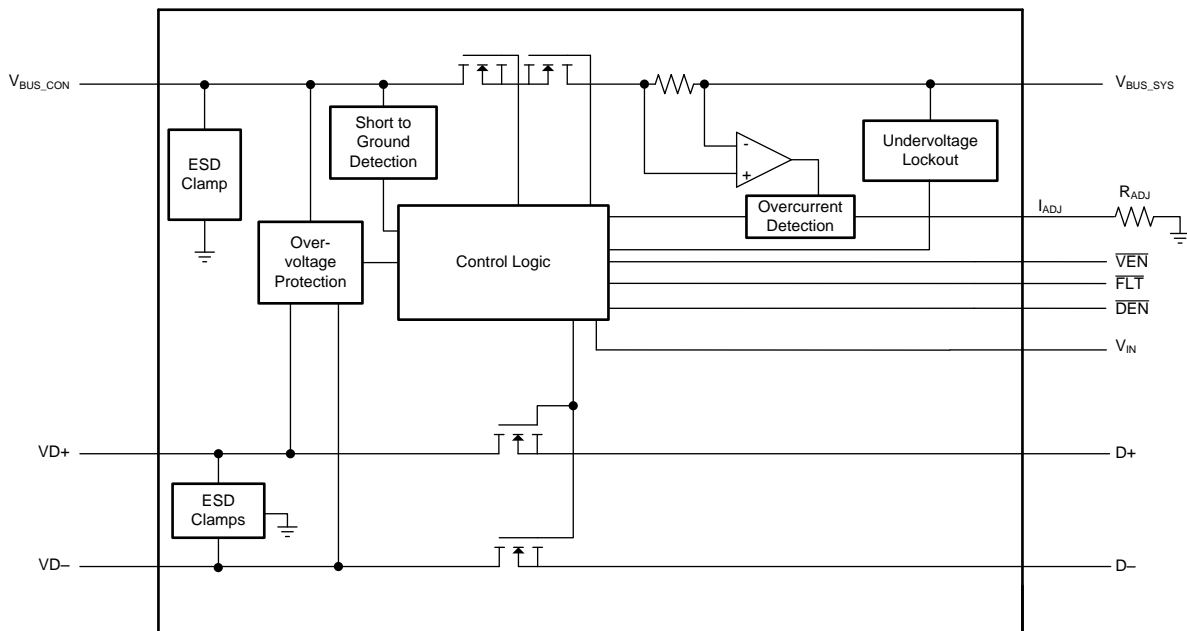
## 8 Detailed Description

### 8.1 Overview

The TPD3S716-Q1 provides a single-chip ESD protection and over voltage protection solution for automotive USB interfaces. It offers short to battery protection up to 18 V and short to ground protection on  $V_{BUS\_CON}$ . The TPD3S716-Q1 also provides a  $\overline{FLT}$  pin that indicates to the system if a fault condition has occurred. The TPD3S716-Q1 offers ESD clamps on the  $V_{BUS\_CON}$ ,  $VD+$ , and  $VD-$  pins, therefore eliminating the need for external TVS clamp circuits in the application.

The TPD3S716-Q1 has internal circuitry that controls the turnon of the internal nFET switches. An internal oscillator controls the timers that enable the switches and resets the open-drain  $\overline{FLT}$  output. If  $V_{BUS\_CON}$  and  $VD+/VD-$  are less than  $V_{OVP}$ , the switches are enabled. After an internal delay the charge-pump starts-up and turns on the internal nFET switches through a soft start. At any time, if any of the external USB pins rise above their respective  $V_{OVP}$  thresholds, the nFET switches are turned OFF and the  $\overline{FLT}$  pin is pulled LOW.

### 8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

### 8.3 Feature Description

#### 8.3.1 AEC-Q100 Qualified

The TPD3S716-Q1 is an automotive qualified device according to the AEC-Q100 standards. The TPD3S716-Q1 is qualified to operate from  $-40$  to  $+125^{\circ}\text{C}$  ambient temperature.

#### 8.3.2 Short-to-Battery and Short-to-Ground Protection on $V_{BUS\_CON}$

The  $V_{BUS\_CON}$  pin is protected against shorts to battery and shorts to ground.

If a voltage on  $V_{BUS\_CON}$  is detected as too low (below the  $V_{SHRT}$  threshold) after the device is enabled, the device enters short-circuit protection mode and asserts  $\overline{FLT}$ . It sources the  $I_{SHRT}$  current until it detects the voltage rising above the  $V_{SHRT}$  threshold, where it resumes standard operating mode and deasserts  $\overline{FLT}$ .

If a voltage above the  $V_{OVP}$  threshold is detected by the device, it shuts off all FETs and asserts a fault on the  $\overline{FLT}$  pin. When the excessive voltage is removed, the device automatically re-enables and  $\overline{FLT}$  deasserts.

## Feature Description (接下页)

### 8.3.3 Short-to-Battery and Short-to- $V_{BUS}$ Protection on $VD+$ , $VD-$

The  $VD+$  and  $VD-$  pins are protected against shorts to battery and shorts to bus. The OVP threshold on the  $VD+$  and  $VD-$  pins is low enough that it protects against shorts to  $V_{BUS}$ .

When a voltage above the  $V_{OVP}$  threshold is detected by the device, it shuts off all FETs and asserts a fault on the  $FLT$  pin. When the excessive voltage is removed, the device automatically re-enables and  $FLT$  deasserts.

### 8.3.4 ESD Protection on $V_{BUS\_CON}$ , $VD+$ , $VD-$

The protected pins ( $V_{BUS\_CON}$ ,  $VD+$ ,  $VD-$ ) are tested to pass the IEC 61000-4-2 ESD standard up to Level 4 ESD protection. Additionally, these pins are tested against ISO 10605 with the 330-pF, 330- $\Omega$  equivalent network. This guarantees passing of at least  $\pm 8$ -kV contact discharge and  $\pm 15$ -kV air gap discharge according to both standards. See [图 20](#) for the test set-up used for testing IEC 61000-4-2 and ISO 10605.

### 8.3.5 Low $R_{ON}$ nFET $V_{BUS}$ Switch

The  $V_{BUS}$  switch has a low  $R_{ON}$  that provides minimal voltage droop from system to connector. Typical resistance is 63 m $\Omega$  and is specified for 135 m $\Omega$  at 150°C junction temperature.

### 8.3.6 High Speed Data Switches

The  $D+$  and  $D-$  switches have a very low capacitance and a high bandwidth (1-GHz typical), allowing for a clean USB 2.0 eye diagram.

### 8.3.7 Adjustable Hiccup Current Limit up to 2.4-A

The  $V_{BUS}$  path of this device has an integrated overcurrent protection circuit. The current limit threshold for the overcurrent protection is adjustable via an external resistor  $R_{ADJ}$  to GND on the  $I_{ADJ}$  pin. [公式 1](#) 到 [公式 3](#) approximate the minimum, nominal, and maximum current limit values for TPD3S716-Q1 assuming a 1% tolerant resistor:

$$I_{LIM(TYP)} = 143 \times R_{ADJ}^{(-0.983)} \tag{1}$$

$$I_{LIM(MIN)} = 129 \times R_{ADJ}^{(-0.981)} - 0.02 \tag{2}$$

$$I_{LIM(MAX)} = 141.5 \times R_{ADJ}^{(-0.962)} + 0.015 \tag{3}$$

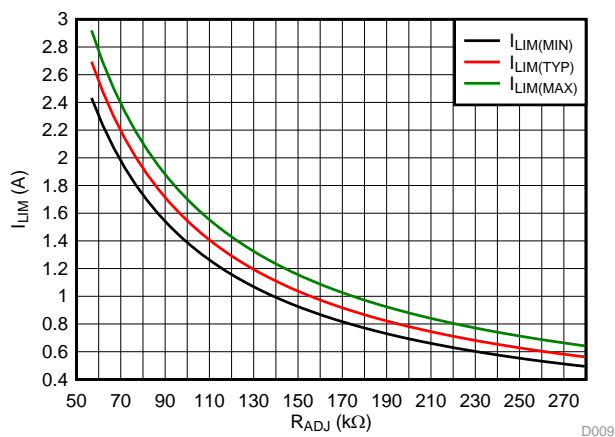


图 21. TPD3S716-Q1 Current Limit Thresholds vs.  $R_{ADJ}$

[公式 1](#), [公式 2](#) 和 [公式 3](#) are useful for approximating the current limit threshold of TPD3S716-Q1; however, they do not constitute as part of TI's published device specifications for purposes of TI's product warranty. For the officially tested current limit threshold values, see the [Electrical Characteristics](#) table.

When the  $V_{BUS}$  current exceeds the overcurrent threshold, the device goes into a fault state where it limits the current to the overcurrent threshold value and asserts the  $FLT$  pin. After a short blanking time, the device cycles on and off to try to check if the connected device is still in overcurrent.

## Feature Description (接下页)

### 8.3.8 Fast Over-Voltage Response Time

The over-voltage FETs are designed to have a fast turnoff time to protect the upstream SoC as quickly as possible. Typical response time for complete turnoff is 2  $\mu$ s for the  $V_{BUS}$  path and 200 ns for the data path.

### 8.3.9 Independent $V_{BUS}$ and Data Enable Pins for Configuring both Host and Client/OTG Mode

The TPD3S716-Q1 has two enable inputs to turn on and off the device's internal FETs. The  $\overline{VEN}$  pin disables and enables the  $V_{BUS}$  path. The  $\overline{DEN}$  pin disables and enables the data path. Independent control of the  $V_{BUS}$  and data paths enables the TPD3S716-Q1 to be configured for both USB Host and Client/OTG mode. See [表 1](#).

### 8.3.10 Fault Output Signal

The TPD3S716-Q1 has a fault pin,  $\overline{FLT}$  that indicates when there is any sort of fault condition because of an OVP, OCP, short-circuit, reverse-current, or thermal shutdown event occurring.

### 8.3.11 Thermal Shutdown Feature

In the event that the device exceeds the maximum allowable junction temperature, the thermal shutdown circuit disables the  $V_{BUS}$  and data switches and assert the fault pin low.

### 8.3.12 16-Pin SSOP Package

The TPD3S716-Q1 is packaged in a standard 16-pin SSOP leaded package.

### 8.3.13 Reverse Current Detection

If  $V_{BUS\_CON}$  exceeds  $V_{BUS\_SYS}$  by a voltage greater than  $V_{REV\_SUPPLY(RISING)}$  for  $t_{REV\_SUPPLY\_BLANK}$ , then TPD3S716-Q1 detects this reverse current condition and asserts the fault pin. When  $V_{BUS\_CON} - V_{BUS\_SYS}$  falls below  $V_{REV\_SUPPLY(FALLING)}$ , the fault pin is deasserted and TPD3S716-Q1 enters back into its normal operating mode.



## 8.4 Device Functional Modes

### 8.4.1 Normal Operation

The TPD3S716-Q1 operates in normal operation modes when enabled, both  $V_{BUS\_SYS}$  and  $V_{IN}$  are above their UVLO thresholds, and the device is not in any fault conditions. 表 1 shows the normal operating modes of the TPD3S716-Q1.

表 1. Device Normal Operating Mode Table

MODE	$\overline{VEN}$	$\overline{DEN}$	$V_{BUS}$ PATH	DATA PATH
USB Host	0	0	ON	ON
Power Only	0	1	ON	OFF
USB Client/OTG	1	0	OFF	ON
Disabled	1	1	OFF	OFF

### 8.4.2 Overvoltage Condition

When the  $VD+$ ,  $VD-$ , or  $V_{BUS\_CON}$  pins exceed their OVP threshold, the device enters the overvoltage state. All FETs are disabled and the  $\overline{FLT}$  pin is asserted. When the protected pins drop below their OVP threshold, the device automatically turns back on and deasserts the  $\overline{FLT}$  pin. An overvoltage condition is only detected on an enabled path. For example, if the data path is enabled and the  $V_{BUS}$  path is disabled (USB Client/OTG mode), if an overvoltage condition occurs on  $V_{BUS\_CON}$ , the fault pin is not be asserted. However, because the FETs of disabled paths are already turned off, proper protection from overvoltage conditions are still guaranteed by the device on disabled paths.

### 8.4.3 Overcurrent Condition

When the current through the  $V_{BUS}$  path exceeds the  $I_{LIM}$  current threshold, the device enters into the overcurrent state. The TPD3S716-Q1 limits current to the  $I_{LIM}$  threshold by dropping voltage across the  $V_{BUS}$  FET to maintain constant current. When it continues to sense an overcurrent condition for the blanking time ( $t_{BLANK}$ ), the device disables itself for the retry time ( $t_{RETRY}$ ) and then retry automatically for the retry time ( $t_{BLANK\_RETRY}$ ). In the event that the current is below the overcurrent threshold, the device deasserts fault and resumes normal operation.

### 8.4.4 Short-Circuit Condition

If the voltage on the  $V_{BUS\_CON}$  side is pulled below the  $V_{SHRT}$  threshold while the device is enabled, the TPD3S716-Q1 enters the short-circuit mode. It sources a constant current of  $I_{SHRT}$  until it rises above the  $V_{SHRT}$  threshold. When that occurs, the device automatically re-enters normal operation and deasserts the fault pin.

### 8.4.5 Device Logic Table

表 2 shows the TPD3S716-Q1 logic table.

表 2. TPD3S716-Q1 Logic Table

Mode	$\overline{\text{VEN}}$	$\overline{\text{DEN}}$	$V_{\text{BUS\_CON}}$	$\text{VDx}$	$I_{\text{VBUS}}$	$V_{\text{BUS\_SYS}}, V_{\text{IN}}$	$T_{\text{J}}$	$\overline{\text{FLT}}$	$V_{\text{BUS PATH}}$	DATA PATH
Unpowered	X	X	X	X	None	< UVLO	X	H	OFF	OFF
Disabled	H	H	X	X	None	> UVLO	< TSD	H	OFF	OFF
Host	L	L	< OVP & < $V_{\text{BUS\_SYS}} + 200 \text{ mV (typical)}$ & > $V_{\text{SHRT}}$	< OVP	< OCP	> UVLO	< TSD	H	ON	ON
Client/OTG	H	L	X	< OVP	None	> UVLO	< TSD	H	OFF	ON
Power Only	L	H	< OVP & < $V_{\text{BUS\_SYS}} + 200 \text{ mV (typical)}$ & > $V_{\text{SHRT}}$	X	< OCP	> UVLO	< TSD	H	ON	OFF
Thermal Shutdown	X	X	X	X	None	> UVLO	> TSD	L	OFF	OFF
Host: $V_{\text{BUS}}$ OVP Fault	L	L	> OVP	X	None	> UVLO	< TSD	L	OFF	OFF
Host: Data OVP Fault	L	L	X	> OVP	None	> UVLO	< TSD	L	OFF	OFF
Host: OCP Fault	L	L	< OVP & < $V_{\text{BUS\_SYS}} + 200 \text{ mV (typical)}$ & > $V_{\text{SHRT}}$	X	> OCP	> UVLO	< TSD	L	CURRENT LIMITED, AUTO-RETRY	AUTO-RETRY
Host: Short-Circuit Fault	L	L	< $V_{\text{SHRT}}$	X	X	> UVLO	< TSD	L	CURRENT LIMITED 250 mA (typical)	OFF
Host: RCP Fault	L	L	< OVP & > $V_{\text{BUS\_SYS}} + 200 \text{ mV (typical)}$	X	X	> UVLO	< TSD	L	ON	ON
OTG: Data OVP Fault	H	L	X	> OVP	None	> UVLO	< TSD	L	OFF	OFF
Power Only: $V_{\text{BUS}}$ OVP Fault	L	H	> OVP	X	None	> UVLO	< TSD	L	OFF	OFF
Power Only: OCP Fault	L	H	X	X	> OCP	> UVLO	< TSD	L	CURRENT LIMITED, AUTO-RETRY	OFF
Power Only: Short-Circuit Fault	L	H	< $V_{\text{SHRT}}$	X	X	> UVLO	< TSD	L	CURRENT LIMITED 250 mA (typical)	OFF
Power Only: RCP Fault	L	H	< OVP & > $V_{\text{BUS\_SYS}} + 200 \text{ mV (typical)}$	X	X	> UVLO	< TSD	L	ON	OFF

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPD3S716-Q1 offers fully featured automotive USB2.0 protection including short-to-battery, overcurrent, and ESD protection. Care must be taken during the implementation to make sure the device provides adequate protection to the system.

### 9.2 Typical Application

图 22 shows a fully featured USB2.0 high speed port, with an 18-V short-to-battery requirement on the connector side.

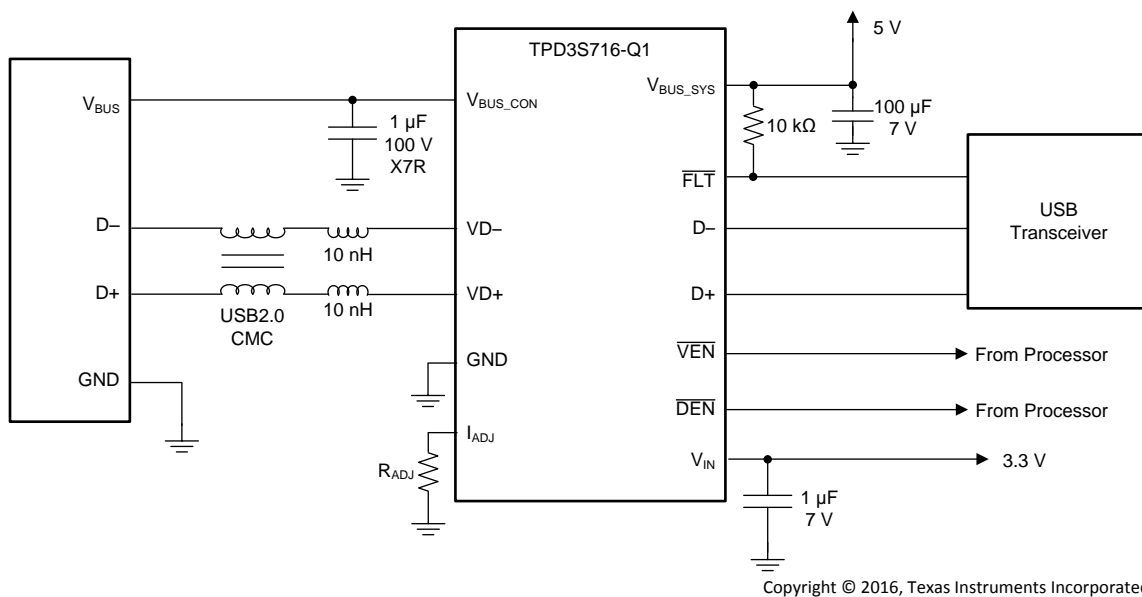


图 22. Typical Application Configuration for TPD3S716-Q1

#### 9.2.1 Design Requirements

表 3 shows the TPD3S716-Q1 input parameters for this application example.

表 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Short-to-battery tolerance on VD+, VD-, V <sub>BUS_CON</sub>	18 V
Max current in normal operation on V <sub>BUS</sub>	1.5 A
Current Limit Setting on V <sub>BUS</sub>	1.505 A (minimum)
Maximum Ambient Temperature Requirement	105°C
USB Data Rate	480 Mbps

## 9.2.2 Detailed Design Procedure

The following parameters must be known to the designer to begin the design process:

- Short-to-battery tolerance on connector pins
- Maximum current in normal operation on  $V_{BUS}$
- Maximum operating ambient temperature
- USB Data Rate

### 9.2.2.1 Short-to-Battery Tolerance

The TPD3S716-Q1 is capable of handling up to 18 V DC on the VD+, VD–, and  $V_{BUS\_CON}$  pins. In the event of a short-to-battery on  $V_{BUS\_CON}$ , significant ringing would be expected because of the hot plug-like nature of the short-to-battery event. In typical ceramic capacitor configurations, a standard RLC response is expected which results in a ringing of nearly two times the applied DC voltage. The TPD3S716-Q1 is capable of withstanding the transient ringing from hot plug-like events, assuming some precautions are taken.

Careful capacitor selection on the  $V_{BUS\_CON}$  pin must be observed. A capacitor with a low derating percentage under the applied voltages must be used to prevent excess ringing. In the example, a 1- $\mu$ F, 100-V tolerant ceramic X7R capacitor is used. It is best practice to carefully select the capacitors used in this circuit to prevent derating-based voltage spikes under hot plug events. See [图 25](#) and [图 26](#) to compare ringing of a 50-V capacitor to a 100-V capacitor. [图 27](#) shows the 100-V capacitor with the TPD3S716-Q1 installed.

Another alternative to a high rated ceramic capacitor is to implement either a standard R-C snubber circuit, or a small external TVS diode. Depending on the short-to-battery tolerance needed, no special precautions may be needed.

### 9.2.2.2 Maximum Current on $V_{BUS}$

The TPD3S716-Q1 is capable of operating up to 2.4 A maximum DC current. In this example, the maximum current for USB2.0 BC1.2 of 1.5 A has been chosen.

### 9.2.2.3 Power Dissipation and Junction Temperature

This section demonstrates how to analyze the power dissipation and junction temperature of the TPD3S716-Q1 to validate that the application requirements of an  $I_{VBUS}$  operating current level of 1.5 A and a maximum operating ambient temperature of 105 °C can be met.

It is good design practice to estimate power dissipation and maximum expected junction temperature of TPD3S716-Q1. This is important to insure the device does not go into thermal shutdown in normal operation and that the long term reliability of the device is maintained. Using [公式 4](#) to [公式 6](#), the system designer can control choices of the device's proximity to other power dissipating devices and the design of the printed circuit board (PCB). These have a direct influence on maximum junction temperature. Other factors, such as airflow and maximum ambient temperature, are often determined by system considerations. It is important to remember that these calculations do not include the effects of adjacent heat sources, and enhanced or restricted air flow. Addition of extra PCB copper area around these devices is recommended to reduce the thermal impedance and maintain the junction temperature as low as practical.

For TPD3S716-Q1, the operating junction temperature must be kept below 150°C in order to prevent the device from going into thermal shutdown. [公式 4](#) is used to calculate the junction temperature of the device:

$$T_J = T_A + [(I_{OUT}^2 \times R_{ON}) \times R_{\theta JA}]$$

where

- $I_{OUT}$  = Rated OUT pin current (A)
  - $R_{ON}$  = Power path on-resistance at an assumed  $T_J$  ( $\Omega$ )
  - $T_A$  = Maximum ambient temperature (°C)
  - $T_J$  = Maximum junction temperature (°C)
  - $R_{\theta JA}$  = Thermal resistance (°C/W)
- (4)

This application example requires an  $I_{VBUS}$  operating current level of 1.5 A. TPD3S716-Q1 has maximum junction temperature derating requirements depending on the maximum operating current of the device according to [公式 5](#):

$$T_{J(MAX)} = -15.6 \times (I_{VBUS(MAX \text{ OPERATING})}) + 161.5 \text{ (}^\circ\text{C)}$$

where

- $T_{J(MAX)}$  = Maximum allowed junction temperature ( $^{\circ}\text{C}$ )
  - $I_{VBUS(MAX OPERATING)}$  = Maximum  $I_{VBUS}$  operating current (A)
- (5)

See [图 28](#) for a plot of the reliability curve equation. Using this equation,  $138.1^{\circ}\text{C}$  is the maximum allowed junction temperature in this application.

This example requires a maximum operating ambient temperature of  $105^{\circ}\text{C}$ . To determine if this can be supported using [公式 4](#), the maximum  $V_{BUS}$  path  $R_{ON}$  must be determined. [公式 6](#) calculates the maximum  $V_{BUS}$  path  $R_{ON}$  possible for TPD3S716-Q1 for a given junction temperature:

$$R_{ON(MAX)} = (T_J + 183.15) / 2726.7 \ (\Omega)$$

where

- $R_{ON(MAX)}$  = Maximum  $V_{BUS}$   $R_{ON}$  at a given junction temperature ( $\Omega$ )
  - $T_J$  = Device junction temperature ( $^{\circ}\text{C}$ )
- (6)

See [图 29](#) for a plot of the maximum  $V_{BUS}$  path  $R_{ON}$  vs. Junction Temperature curve. Using the above equation, the maximum  $V_{BUS}$   $R_{ON}$  possible for TPD3S716-Q1 at  $138.1^{\circ}\text{C}$  is  $R_{ON(MAX)} = 0.118 \ \Omega$ .

Using the calculated parameters for this example and the standard datasheet  $R_{\theta JA}$  for TPD3S716-Q1, the maximum operating ambient temperature possible in this example is  $T_A = 111^{\circ}\text{C}$ . Because this is greater than the application requirement of  $105^{\circ}\text{C}$ , TPD3S716-Q1 can safely be operated at 1.5 A with  $R_{\theta JA} = 98.8 \ (^{\circ}\text{C}/\text{W})$ . If the resulting ambient temperature in the above calculations resulted in a  $T_A < 105 \ ^{\circ}\text{C}$ , methods for improving  $R_{\theta JA}$  would need to be taken. See the [Layout Optimized for Thermal Performance](#) section for guidelines on improving  $R_{\theta JA}$  for TPD3S716-Q1. The example given in the [Layout Optimized for Thermal Performance](#) yields an  $R_{\theta JA} = 57 \ (^{\circ}\text{C}/\text{W})$ . Excellent thermal performance of TPD3S716-Q1 can be achieved with the proper PCB layout.

#### 9.2.2.4 USB Data Rate

The TPD3S716-Q1 is capable of operating at the maximum USB2.0 High Speed data rate of 480-Mbps because of the high data switch bandwidth of 1-GHz (typical). In this design example the maximum data rate of 480-Mbps has been chosen.

9.2.3 Application Curves

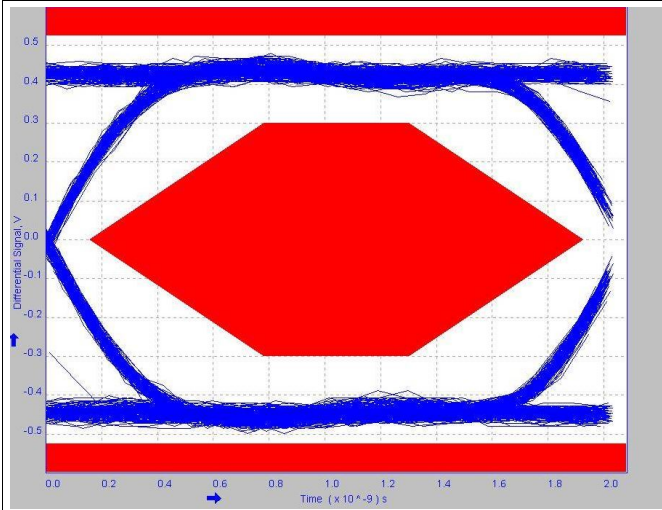


图 23. USB2.0 Eye Diagram (Board only, Through Path)

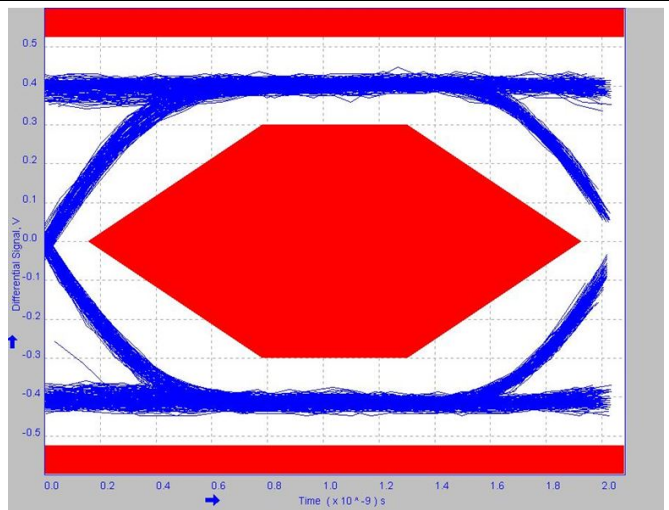


图 24. USB2.0 Eye Diagram (System from Typical Application Schematic)

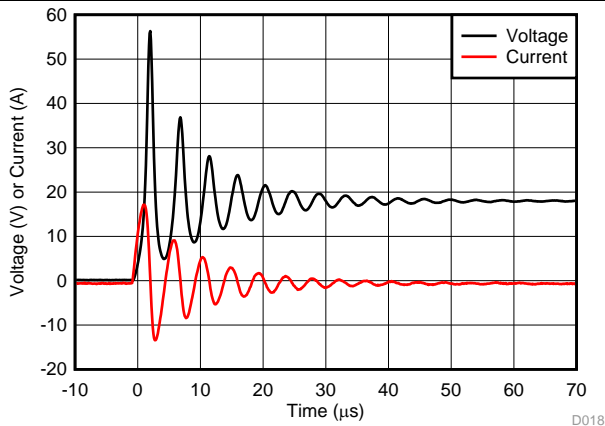


图 25. 50-V, 1-µF X7R Ceramic Shorted to 18-V (Not Recommended)

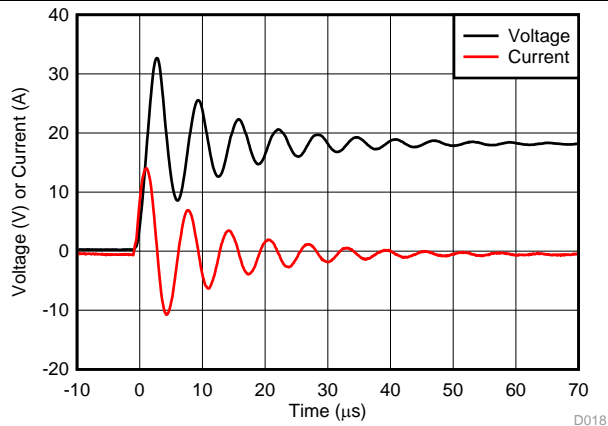


图 26. 100-V, 1-µF X7R Ceramic Shorted to 18 V

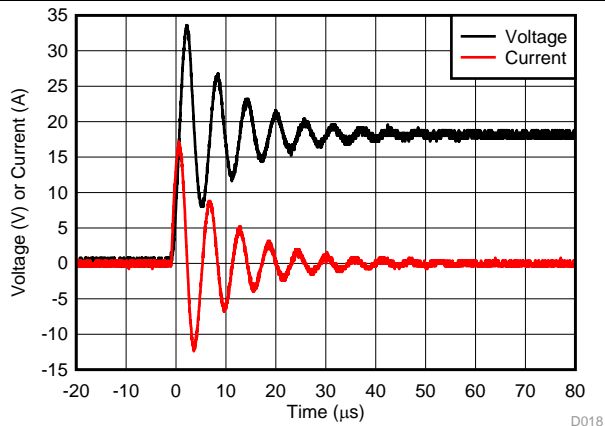


图 27. TPD3S716-Q1 and 100-V, 1-µF X7R Shorted to 18 V (Powered Off)

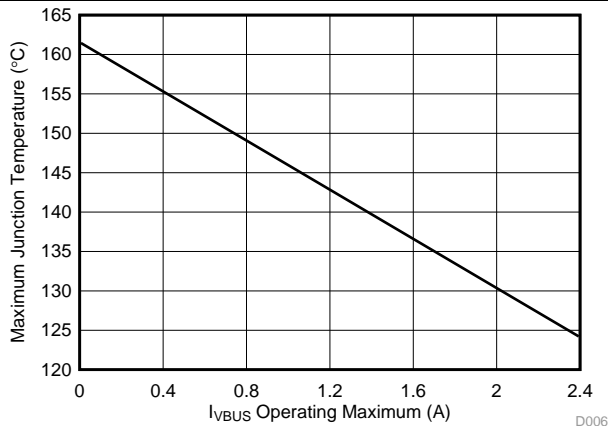


图 28. TPD3S716-Q1 I\_VBUS Temperature Derating Curve

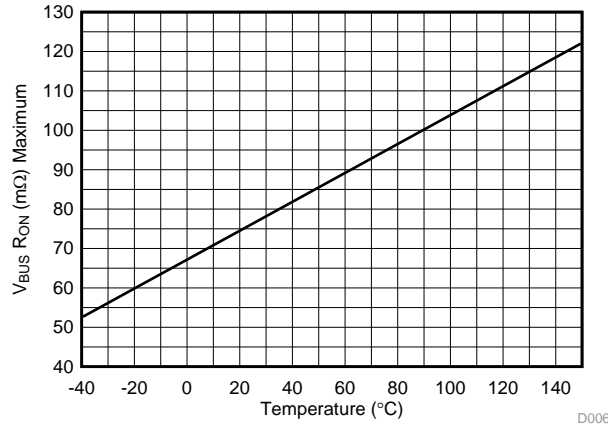


图 29. TPD3S716-Q1 Maximum  $V_{BUS} R_{ON}$  vs. Junction Temperature D006



## 10 Power Supply Recommendations

### 10.1 $V_{BUS}$ Path

The  $V_{BUS\_SYS}$  pins provide power to the chip and supply current through the load switch to  $V_{BUS\_CON}$ . A 100- $\mu$ F bulk capacitor is recommended on  $V_{BUS\_SYS}$  to supply the USB port and maintain compliance. A 1- $\mu$ F capacitor is recommended on the  $V_{BUS\_CON}$  pin with adequate voltage rating to tolerate short-to-battery conditions. A supply voltage above the UVLO threshold for  $V_{BUS\_SYS}$  must be supplied for the device to power on.

### 10.2 $V_{IN}$ Pin

The  $V_{IN}$  pin provides a voltage reference for the data switch OVP level as well as a bypass for ESD clamping. A 1- $\mu$ F capacitor must be placed as close to the pin as possible and the supply must be set to be above the UVLO threshold for  $V_{IN}$ .

## 11 Layout

### 11.1 Layout Guidelines

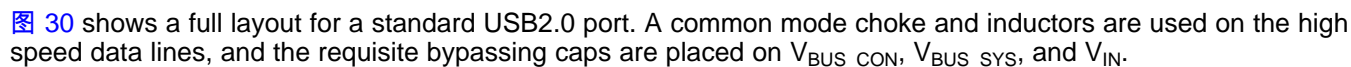
Proper routing and placement maintains signal integrity for high-speed signals. The following guidelines apply to the TPD3S716-Q1:

- Place the bypass capacitors as close as possible to the  $V_{IN}$ ,  $V_{BUS\_SYS}$ , and  $V_{BUS\_CON}$  pins. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during transient events such as short-to-battery, ESD, or overcurrent conditions.
- High speed traces (data switch path) must be routed as straight as possible and any sharp bends must be minimized.

Standard ESD recommendations apply to the  $VD+$ ,  $VD-$ , and  $V_{BUS\_CON}$  pins as well:

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

### 11.2 Layout Example

 30 shows a full layout for a standard USB2.0 port. A common mode choke and inductors are used on the high speed data lines, and the requisite bypassing caps are placed on  $V_{BUS\_CON}$ ,  $V_{BUS\_SYS}$ , and  $V_{IN}$ .

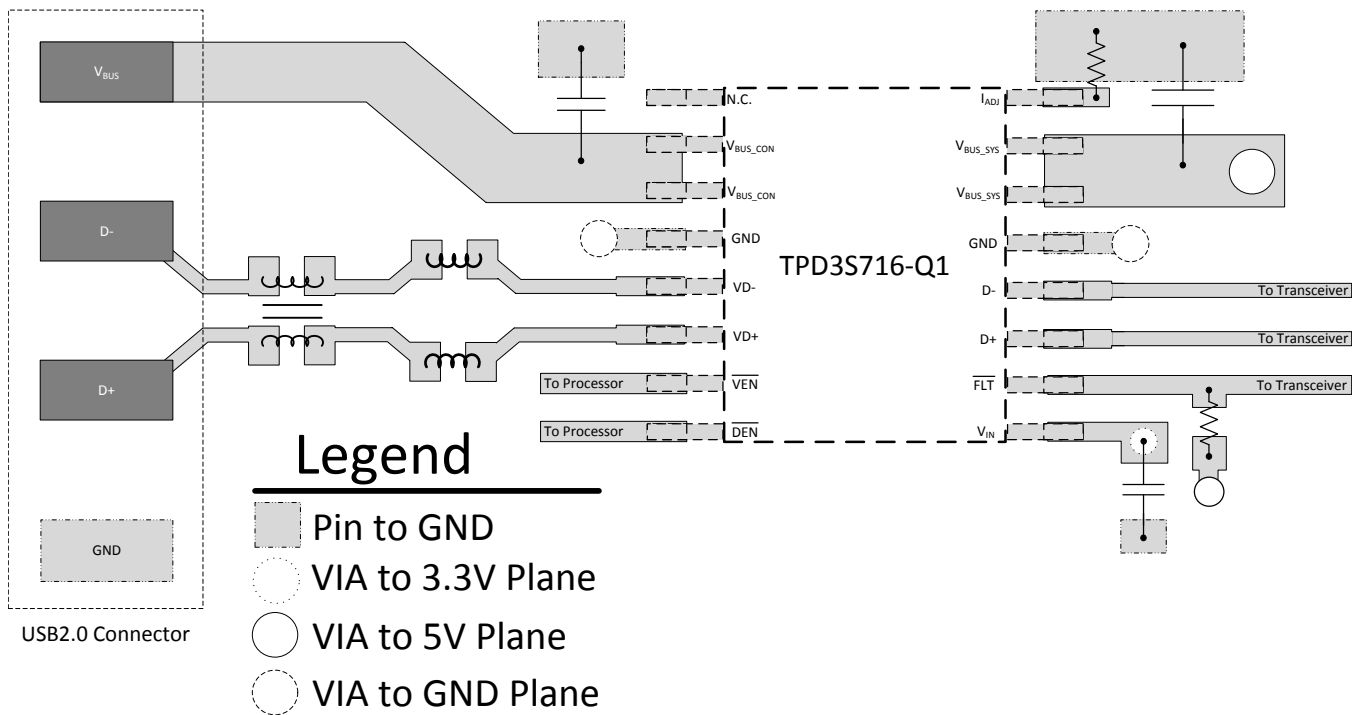
**Layout Example (接下页)**

**图 30. Typical Layout Example for TPD3S716-Q1**
**11.3 Layout Optimized for Thermal Performance**

图 31 和 图 32 显示来自实际 PCB 设计优化的最佳热性能 TPD3S716-Q1 的图像。此 PCB 布局具有 6 层（2 信号和 4 平面层）。2 信号层是 PCB 的外层，由 2-oz 铜制成，4 个内部平面层由 1-oz 铜制成。使用此 PCB 布局产生了  $R_{\theta JA(CUSTOM)} = 57$  (°C/W)。图像包含铜迹和铜倒角的大致尺寸，用于围绕器件路由器件电源、GND 和信号引脚。优化器件热性能的一个关键策略是尽可能最大化铜迹和铜倒角的面积，用于路由器件电源、GND 和信号引脚。另一个关键策略是最大化 PCB 金属层的铜重量。这个例子证明，通过 TPD3S716-Q1 可以实现卓越的热性能，只要 PCB 布局正确。

Layout Optimized for Thermal Performance (接下页)

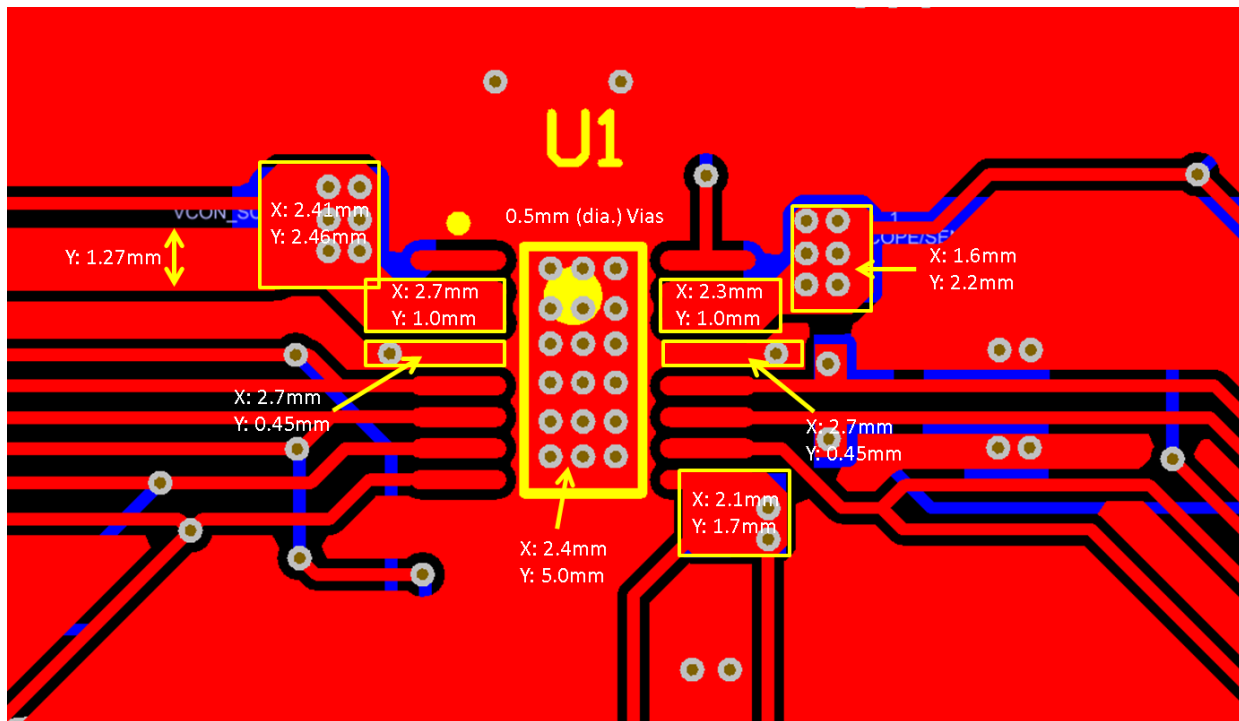


图 31. Thermally Optimized PCB Layout Top Layer

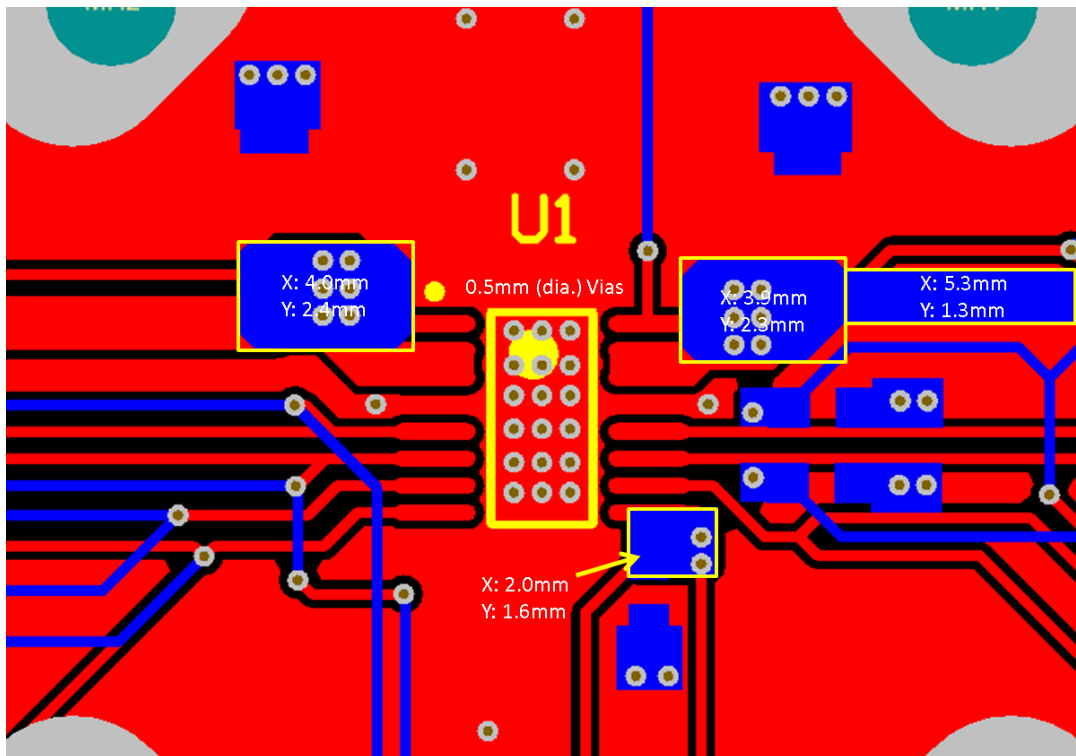


图 32. Thermally Optimized PCB Layout Bottom Layer

## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

相关文档如下：

《TPD3S716-Q1 评估模块》，[SLVUAL9](#)

### 12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## 重要声明

德州仪器(TI)及其下属子公司有权根据 JESD46 最新标准,对所提供的产品和服务进行更正、修改、增强、改进或其它更改,并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息,并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内,且 TI 认为有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定,否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险,客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息,不能构成从 TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可,或是 TI 的专利权或其它知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分,仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时,如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分,则会失去相关 TI 组件或服务的所有明示或暗示授权,且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意,尽管任何应用相关信息或支持仍可能由 TI 提供,但他们将独立负责满足与其产品及其在应用中使用的 TI 产品相关的所有法律、法规和安全相关要求。客户声明并同意,他们具备制定与实施安全措施所需的全部专业技术和知识,可预见故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中,为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此,此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备)的授权许可,除非各方授权官员已经达成了专门管控此类使用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同意,对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用,其风险由客户单独承担,并且由客户独立负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品,这些产品主要用于汽车。在任何情况下,因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	<a href="http://www.ti.com.cn/audio">www.ti.com.cn/audio</a>	通信与电信	<a href="http://www.ti.com.cn/telecom">www.ti.com.cn/telecom</a>
放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
电源管理	<a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>	视频和影像	<a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>
微控制器 (MCU)	<a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>		
RFID 系统	<a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>		
OMAP应用处理器	<a href="http://www.ti.com/omap">www.ti.com/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122  
Copyright © 2016, 德州仪器半导体技术(上海)有限公司

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD3S716QDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RJ716Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD3S716QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

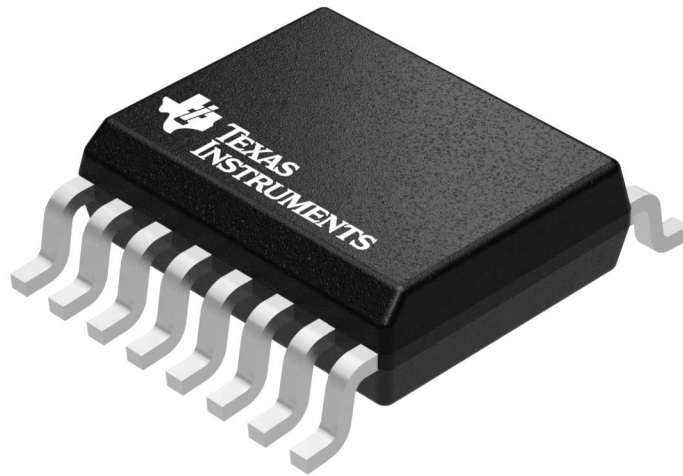
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD3S716QDBQRQ1	SSOP	DBQ	16	2500	367.0	367.0	35.0

**GENERIC PACKAGE VIEW**

**DBQ 16**

**SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4073301-2/1



# DBQ0016A

# PACKAGE OUTLINE

## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

# EXAMPLE BOARD LAYOUT

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

TI 均以“原样”提供技术性及其可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

Copyright © 2020 德州仪器半导体技术（上海）有限公司