符合 Qi (WPC v1.2) 标准的 bq51003 高度集成无线接收器电源

1 特性

- 集成型无线电源接收器解决方案（针对 2.5W 应用进行了优化）
  - 93% 的整体峰值交流/直流转换效率
  - 完全同步整流器
  - 符合 WPC v1.2 标准的通信控制
  - 输出电压调节
  - 在 RX 线圈与输出之间只需要集成电路 (IC)
- 符合无线电源联盟 (WPC) v1.2 标准（启用 FOD）的高精度电流传感
- 动态整流器控制，可改进负载瞬态响应
- 可在宽泛的输出电源范围内优化性能的动态效率调节
- 针对稳健通信的自适应通信限制
- 支持 20V 最高输入电压
- 低功率耗散整流器过压钳位 ($V_{RECT-OVP}$ = 15V)
- 热关断
- 用于温度监控、充电完成和故障主机控制的多功能负温度系数热敏电阻 (NTC) 和控制引脚

2 应用

- 符合 WPC 标准的接收器
- 手机和智能电话
- 耳机
- 数码摄像机
- 便携式媒体播放器
- 手持式设备

3 说明

bq51003 是一款用于在便携式应用中进行无线电源传输的高级集成型 接收器 IC， 针对功率为 2.5W 及其以下的应用 进行了优化。该器件可提供交流/直流电源转换，同时集成了使用 Qi v1.2 通信协议所需的数字控制功能。配合使用 bq500212A 发送器控制器，bq51003 可为无线电源解决方案提供完整的非接触式电力传输系统。通过使用近场感应式电力传输，嵌入在便携式设备中的接收器线圈可通过相互耦合的电感器接受发送器线圈发出的电能。然后，来自接收器线圈的交流信号经过整流和调节可用作系统关闭电子产品的电源。为了稳定电力传输过程，建立了从次级侧到发送器的全局反馈机制（通过反向散射调制）。此反馈是通过使用支持高达 2.5W 应用的 Qi v1.2 通信协议 建立的。

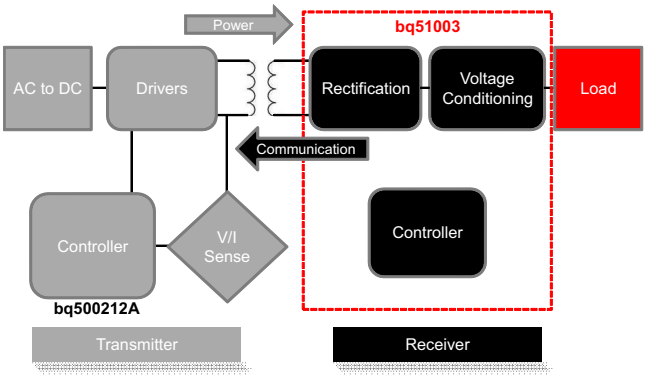
该器件集成了低阻抗完全同步整流器、低压降稳压器、数字控制以及精确电压和电流环路。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
bq51003	DSBGA (28)	1.90mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

无线电源联盟（WPC 或者 Qi）感应式充电系统



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (March 2017) to Revision C — **Page**

- 将“配合使用 bq500210...” 更改成了“配合使用 bq500212A...”（位于*说明部分*） ... 1
- 将 *无线电源联盟（WPC 或 Qi）感应式充电系统* 图像中的 bq500210 更改成了 bq500212A ... 1
- Changed the *Device Comparison Table* ... 3
- Changed bq500210 To: bq500212A in the Figure 17 ... 12
- Changed "No Response" To: "EPT 0x00, Unknown" in the EPT column of Table 4 ... 17
- Changed "Termination" To: " EPT 0x01, Charge Complete" in the EPT column of Table 4 ... 17
- Added row "Unknown" to Table 5 ... 18
- Changed the condition of row "Charge Complete" in Table 5 ... 18
- Changed bq500210 To: bq500212A in the Figure 22 ... 20
- Changed the *3-State Driver Recommendations for the TS-CTRL Pin* section ... 25

Changes from Revision A (June 2016) to Revision B — **Page**

- 将文档中的 WPC v1.1 更改为 WPC v1.2 ... 1

Changes from Original (December 2013) to Revision A — **Page**

- 添加了 *ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 ... 1
- 删除了*订购信息*表和*封装摘要*部分，请参阅数据表末尾的 POA ... 1

5 Device Comparison Table

DEVICE	FUNCTION	V_{OUT} ($V_{BAT-REG}$)	MAXIMUM P_{OUT}	I^2C
bq51003	Wireless Receiver	5 V	2.5 W	No
bq51013B	Wireless Receiver	5 V	5 W	No
bq51010B	Wireless Receiver	7 V	5 W	No
bq51020	Wireless Receiver	4.5 to 8 V	5 W	No
bq51021	Wireless Receiver	4.5 to 8 V	5 W	Yes
bq51221, bq51222	Dual Mode Wireless Receiver	4.5 to 8 V	5 W	Yes
bq51050B	Wiress Receiver and Direct Charger	4.2 V	5 W	No
bq51051B	Wiress Receiver and Direct Charger	4.35 V	5 W	No
bq51052B	Wiress Receiver and Direct Charger	4.4 V	5 W	No

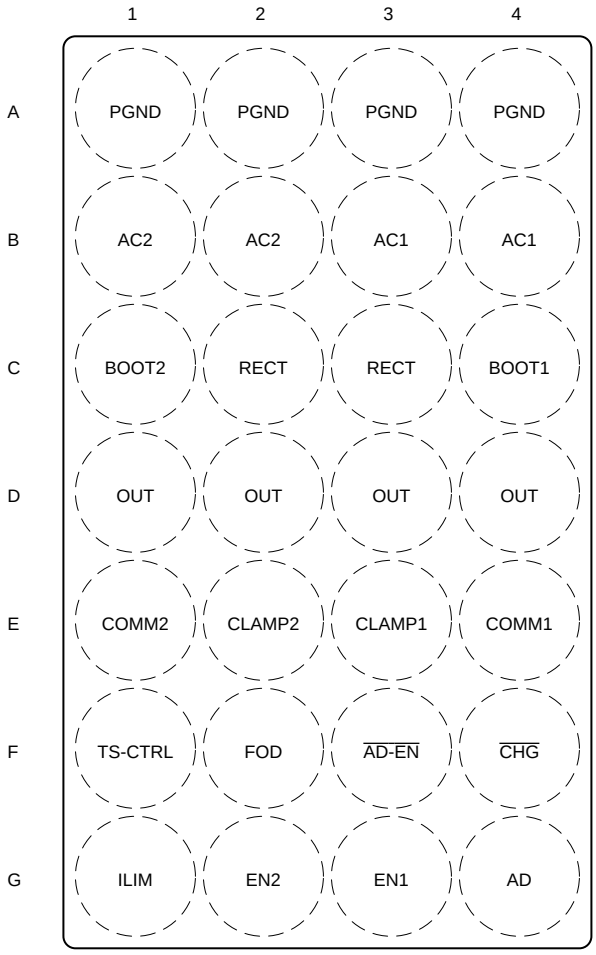
Table 1. Available Options

DEVICE	FUNCTION	WPC VERSION	$V_{RECT-OVP}$	$V_{OUT-(REG)}$	OVER CURRENT SHUTDOWN	AD-OVP	TERMINATION	COMMUNICATION CURRENT LIMIT(1)(2)
bq51003	5-V Power Supply	v1.2	15 V	5 V	Disabled	Disabled	Disabled	Adaptive + 1 s Hold-Off

(1) Enabled if EN2 is low and disabled if EN2 is high
(2) Communication current limit is disabled for 1 second at start-up

6 Pin Configuration and Functions

YFP Package
28-Pin DSBGA
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
B3, B4	AC1	I	AC input from receiver coil antenna.
B1, B2	AC2	I	
G4	AD	I	Connect this pin to the wired adapter input. When a voltage is applied to this pin wireless charging is disabled and $\overline{\text{AD\_EN}}$ is driven low. Connect to GND through a 1 µF capacitor. If unused, capacitor is not required and should be grounded directly.
F3	$\overline{\text{AD-EN}}$	O	Push-pull driver for external PFET connecting AD and OUT. This node is pulled to the higher of OUT and AD when turning off the external FET. This voltage tracks approximately 4 V below AD when voltage is present at AD and provides a regulated V_{GS} bias for the external FET. Float this pin if unused.
C4	BOOT1	O	Bootstrap capacitors for driving the high-side FETs of the synchronous rectifier. Connect a 10 nF ceramic capacitor from BOOT1 to AC1 and from BOOT2 to AC2.
C1	BOOT2	O	
F4	$\overline{\text{CHG}}$	O	Open-drain output – Active when the output of the wireless power supply is enabled.
E3	CLAMP1	O	
E2	CLAMP2	O	Open drain FETs which are utilized for a non-power dissipative over-voltage AC clamp protection. When the RECT voltage goes above 15 V, both switches will be turned on and the capacitors will act as a low impedance to protect the IC from damage. If used, CLAMP1 is required to be connected to AC1, and CLAMP2 is required to be connected to AC2 through 0.47-µF capacitors.
E4	COMM1	O	Open-drain output used to communicate with primary by varying reflected impedance. Connect COMM1 through a capacitor to either AC1 or AC2 for capacitive load modulation (COMM2 must be connected to the alternate AC1 or AC2 pin). For resistive modulation connect COMM1 and COMM2 to RECT through a single resistor; connect through separate capacitors for capacitive load modulation.
E1	COMM2	O	
G3	EN1	I	Inputs that allow user to enable/disable wireless and wired charging <EN1 EN2>: <00> Wireless charging is enabled <01> Dynamic communication current limit disabled <10> Wireless charging disabled <11> Wireless charging disabled.
G2	EN2	I	
F2	FOD	I	Input for the recieved power measurement. Connect to GND with a R_{FOD} resistor.
G1	ILIM	I/O	Programming pin for the over current limit. Connect external resistor to VSS. Size R_{ILIM} with the following equation: $R_{ILIM} = 262 / I_{MAX}$ where I_{MAX} is the expected maximum output current of the wireless power supply. The hardware current limit (I_{ILIM}) will be 20% greater than I_{MAX} or 1.2 x I_{MAX}. If the supply is meant to operate in current limit use $R_{ILIM} = 314 / I_{ILIM}$ $R_{ILIM} = R1 + R_{FOD}$
D1, D2, D3, D4	OUT	O	Output pin, delivers power to the load.
A1, A2, A3, A4	PGND		Power ground
C2, C3	RECT	O	Filter capacitor for the internal synchronous rectifier. Connect a ceramic capacitor to PGND. Depending on the power levels, the value may be 4.7 µF to 22 µF.
F1	TS-CTRL	I	Must be connected to ground through a resistor. If an NTC function is not desired connect to GND with a 10-kΩ resistor. As a CTRL pin pull to ground to send end power transfer (EPT) fault to the transmitter or pullup to an internal rail (i.e. 1.8 V) to send EPT termination to the transmitter. Note that a 3-state driver should be used to interface this pin (see *3-State Driver Recommendations for the TS-CTRL Pin* for further description).

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Input voltage	AC1, AC2	–0.8	20	V
	RECT, COMM1, COMM2, OUT, $\overline{CHG}$, CLAMP1, CLAMP2	–0.3	20	
	AD, $\overline{AD\text{-}EN}$	–0.3	30	
	BOOT1, BOOT2	-0.3	26	
	EN1, EN2, FOD, TS-CTRL, ILIM	–0.3	7	
Input current	AC1, AC2		1	A(RMS)
Output current	OUT		525	mA
Output sink current	$\overline{CHG}$		15	mA
	COMM1, COMM2		1	A
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the VSS terminal, unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±500	

(1) 100 pF, 1.5 kΩ
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage	RECT	4	10	V
I_{IN}	Input current	RECT		500	mA
I_{OUT}	Output current	OUT		500	mA
$I_{AD\text{-}EN}$	Sink current	$\overline{AD\text{-}EN}$		1	mA
I_{COMM}	COMM sink current	COMM		500	mA
T_J	Junction temperature		0	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		bq51003 YFP (DSBGA) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range, 0°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO	Undervoltage lockout	V_{RECT}: 0 V → 3 V	2.6	2.7	2.8	V
V_{HYS}	Hysteresis on UVLO	V_{RECT}: 3 V → 2 V		250		mV
	Hysteresis on OVP	V_{RECT}: 16 V → 5 V		150		mV
$V_{RECT-OVP}$	Input overvoltage threshold	V_{RECT}: 5 V → 16 V	14.5	15	15.5	V
$V_{RECT-REG}$	Dynamic V_{RECT} threshold 1	I_{LOAD} < 0.1 x I_{IMAX} (I_{LOAD} rising)		7.08		V
	Dynamic V_{RECT} threshold 2	0.1 x I_{IMAX} < I_{LOAD} < 0.2 x I_{IMAX} (I_{LOAD} rising)		6.28		
	Dynamic V_{RECT} threshold 3	0.2 x I_{IMAX} < I_{LOAD} < 0.4 x I_{IMAX} (I_{LOAD} rising)		5.53		
	Dynamic V_{RECT} threshold 4	I_{LOAD} > 0.4 x I_{IMAX} (I_{LOAD} rising)		5.11		
	V_{RECT} TRACKING	In current limit voltage above V_{OUT}		V_O+0.25		
I_{LOAD}	I_{LOAD} hysteresis for dynamic V_{RECT} thresholds as a % of I_{ILIM}	I_{LOAD} falling		4%		
$V_{RECT-DPM}$	Rectifier undervoltage protection, restricts I_{OUT} at $V_{RECT-DPM}$		3	3.1	3.2	V
$V_{RECT-REV}$	Rectifier reverse voltage protection at the output	$V_{RECT-REV}$ = V_{OUT} – V_{RECT}, V_{OUT} = 10 V		8	9	V
QUIESCENT CURRENT						
I_{RECT}	Active chip quiescent current consumption from RECT	I_{LOAD} = 0 mA, 0°C ≤ T_J ≤ 85°C		8	10	mA
		I_{LOAD} = 300 mA, 0°C ≤ T_J ≤ 85°C		2	3	mA
I_{OUT}	Quiescent current at the output when wireless power is disabled (Standby)	V_{OUT} = 5 V, 0°C ≤ T_J ≤ 85°C		20	35	µA
I_{LIM} SHORT CIRCUIT						
R_{ILIM}	Highest value of I_{LIM} resistor considered a fault (short). Monitored for I_{OUT} > 100 mA	R_{ILIM}: 200 Ω → 50 Ω. I_{OUT} latches off, cycle power to reset			120	Ω
t_{DGL}	Deglitch time transition from I_{LIM} short to I_{OUT} disable			1		ms
I_{LIM_SC}	$I_{LIM-SHORT,OK}$ enables the I_{LIM} short comparator when I_{OUT} is greater than this value	I_{LOAD}: 0 mA → 200 mA	120	145	165	mA
	Hysteresis for $I_{LIM-SHORT,OK}$ comparator	I_{LOAD}: 0 mA → 200 mA		30		mA
I_{OUT}	Maximum output current limit, C_L	Maximum I_{LOAD} that will be delivered for 1 ms when I_{LIM} is shorted			2.45	A

Electrical Characteristics (continued)

over operating free-air temperature range, 0°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
$V_{OUT-REG}$	Regulated output voltage	I_{LOAD} = 500 mA	4.96	5	5.04	V
		I_{LOAD} = 10 mA	4.97	5.01	5.05	
K_{ILIM}	Current programming factor for hardware protection	$R_{LIM} = K_{ILIM} / I_{ILIM}$, where I_{ILIM} is the hardware current limit. I_{OUT} = 500 mA	303	314	321	AΩ
K_{IMAX}	Current programming factor for the nominal operating current	$I_{IMAX} = K_{IMAX} / R_{LIM}$ where I_{MAX} is the maximum normal operating current. I_{OUT} = 500 mA		262		AΩ
I_{OUT}	Current limit programming range				750	mA
I_{COMM}	Current limit during WPC communication	I_{OUT} > 300 mA		I_{OUT} + 50		mA
		I_{OUT} < 300 mA	343	378	425	mA
t_{HOLD}	Holdoff time for the communication current limit during start-up			1		s
TS / CTRL						
V_{TS}	Internal TS bias voltage	$I_{TS-Bias}$ < 100 µA (periodically driven see $t_{TS-CTRL}$)	2	2.2	2.4	V
V_{COLD}	Rising threshold	V_{TS}: 50% → 60%	56.5	58.7	60.8	%$V_{TS-Bias}$
	Falling hysteresis	V_{TS}: 60% → 50%		2		
V_{HOT}	Falling threshold	V_{TS}: 20% → 15%	18.5	19.6	20.7	
	Rising hysteresis	V_{TS}: 15% → 20%		3		
V_{CTRL}	CTRL pin threshold for a high	$V_{TS-CTRL}$: 50 → 150 mV	80	100	130	mV
	CTRL pin threshold for a low	$V_{TS-CTRL}$: 150 → 50 mV	50	80	100	
$t_{TS-CTRL}$	Time V_{TS}-Bias is active when TS measurements occur	Synchronous to the communication period		24		ms
t_{TS}	Deglitch time for all TS comparators			10		ms
R_{TS}	Pullup resistor for the NTC network. Pulled up to the voltage bias.		18	20	22	kΩ
THERMAL PROTECTION						
T_J	Thermal shutdown temperature			155		°C
	Thermal shutdown hysteresis			20		
OUTPUT LOGIC LEVELS ON $\overline{CHG}$						
V_{OL}	Open-drain $\overline{CHG}$ pin	I_{SINK} = 5 mA			500	mV
I_{OFF}	$\overline{CHG}$ leakage current when disabled	$V_{\overline{CHG}}$ = 20 V			1	µA
COMM PIN						
$R_{DS(ON)}$	COMM1 and COMM2	V_{RECT} = 2.6 V		1.5		Ω
f_{COMM}	Signaling frequency on COMM pin			2		Kbps
I_{OFF}	Comm pin leakage current	V_{COMM1} = 20 V, V_{COMM2} = 20 V			1	µA
CLAMP PIN						
$R_{DS(ON)}$	CLAMP1 and CLAMP2			0.8		Ω
ADAPTER ENABLE						
$V_{\overline{AD-EN}}$	V_{AD} rising threshold voltage. EN-UVLO	V_{AD} 0 V → 5 V	3.5	3.6	3.8	V
	$V_{\overline{AD-EN}}$ hysteresis, EN-HYS	V_{AD} 5 V → 0 V		400		mV
I_{AD}	Input leakage current	V_{RECT} = 0 V, V_{AD} = 5 V			60	µA
R_{AD}	Pullup resistance from $\overline{AD-EN}$ to OUT when adapter mode is disabled and $V_{OUT} > V_{AD}$, EN-OUT	V_{AD} = 0 V, V_{OUT} = 5 V		200	350	Ω
V_{AD}	Voltage difference between V_{AD} and $V_{\overline{AD-EN}}$ when adapter mode is enabled, EN-ON	V_{AD} = 5 V, 0°C ≤ T_J ≤ 85°C	3	4.5	5	V

Electrical Characteristics (continued)

over operating free-air temperature range, 0°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNCHRONOUS RECTIFIER						
I_{OUT}	I_{OUT} at which the synchronous rectifier enters half synchronous mode, SYNC_EN	I_{LOAD} : 200 mA → 0 mA	80	100	130	mA
	Hysteresis for $I_{OUT,RECT-EN}$ (full-synchronous mode enabled)	I_{LOAD} : 0 mA → 200 mA		25		mA
$V_{HS-DIODE}$	High-side diode drop when the rectifier is in half synchronous mode	$I_{AC-VRECT}$ = 250 mA and T_J = 25°C		0.7		V
EN1 AND EN2						
V_{IL}	Input low threshold for EN1 and EN2				0.4	V
V_{IH}	Input high threshold for EN1 and EN2		1.3			V
R_{PD}	EN1 and EN2 pull down resistance			200		kΩ
ADC (WPC Related Measurements and Coefficients)						
IOUT SENSE	Accuracy of the current sense over the load range	I_{OUT} = 300 mA - 500 mA	–1.5%	0%	0.9%	

7.6 Typical Characteristics

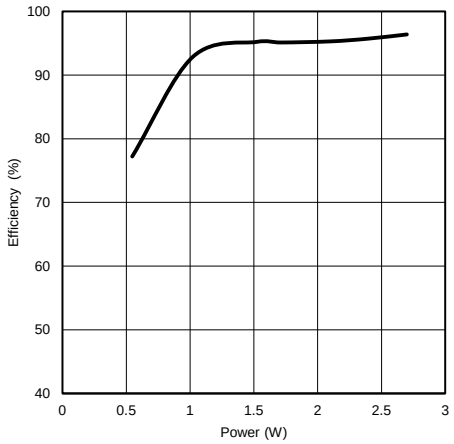


Figure 1. Rectifier Efficiency

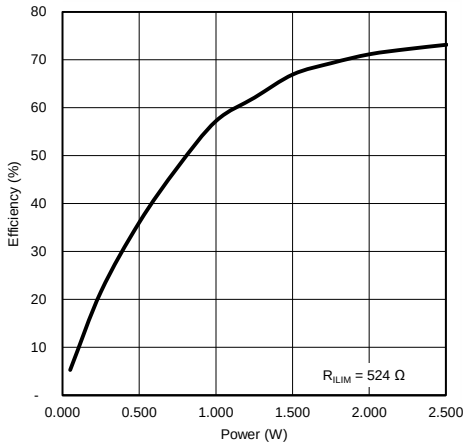


Figure 2. System Efficiency from DC Input to DC Output

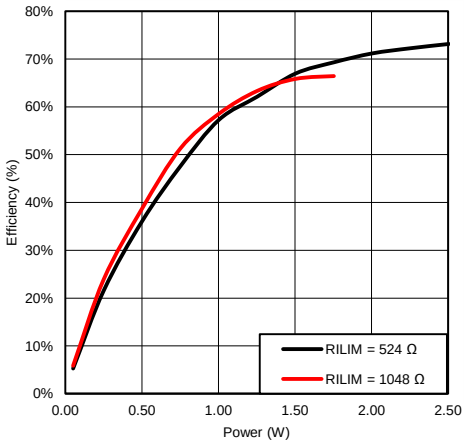


Figure 3. Light Load System Efficiency Improvement Due to Dynamic Efficiency Scaling Feature

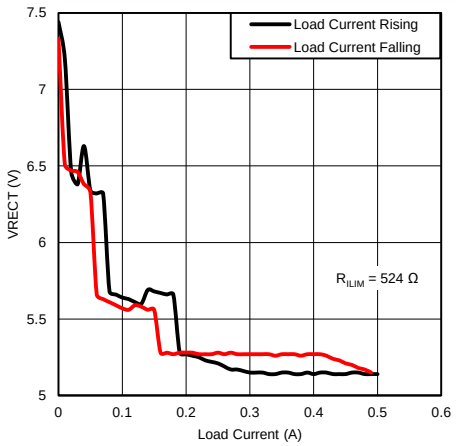


Figure 4. V_{RECT} vs I_{LOAD} at R_{ILIM} = 524 Ω

Typical Characteristics (continued)

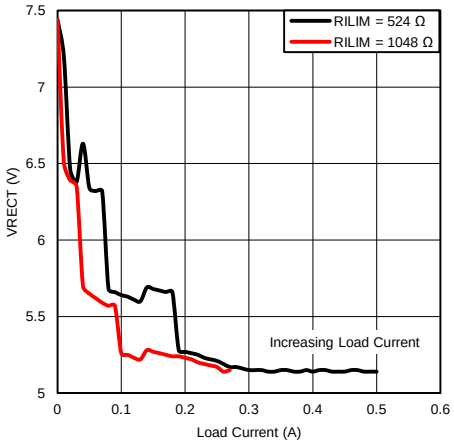


Figure 5. V_{RECT} vs I_{LOAD} at R_{ILIM} = 524 Ω and 1048 Ω

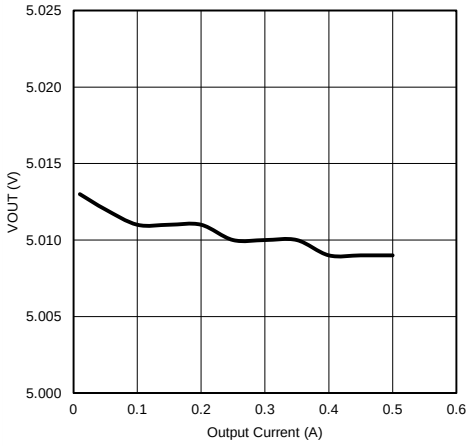


Figure 6. I_{LOAD} Sweep (I-V Curve)

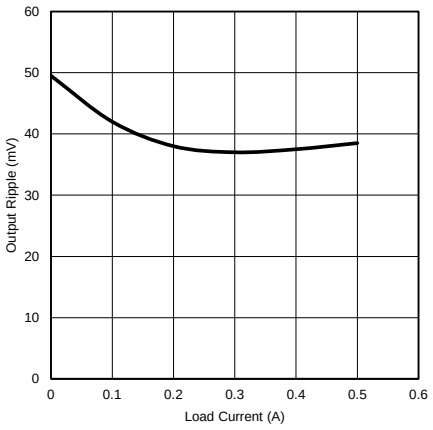


Figure 7. Output Ripple vs I_{LOAD} (C_{OUT} = 1 µF) Without Communication

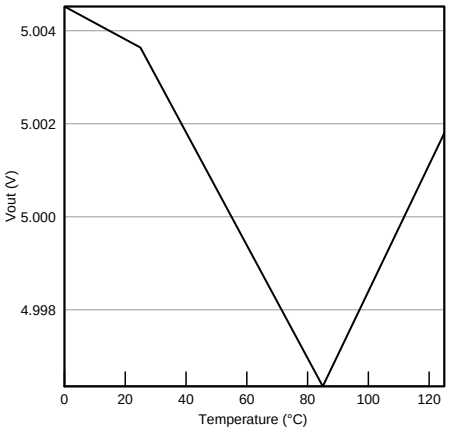


Figure 8. V_{OUT} vs Temperature

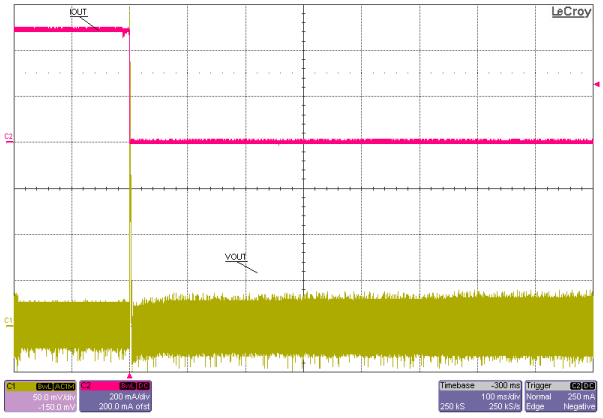


Figure 9. 0.5-A Instantaneous Load Dump

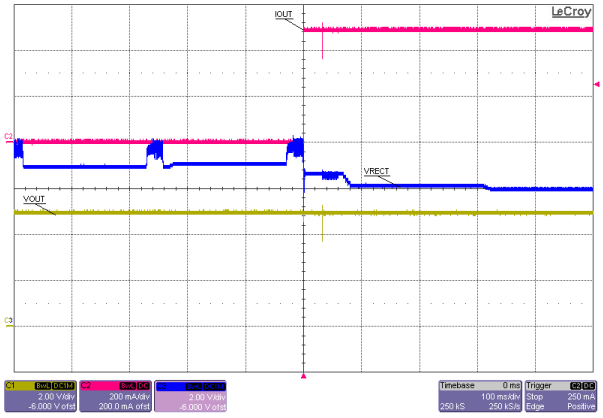


Figure 10. 0.5-A Load Step Full System Response

Typical Characteristics (continued)

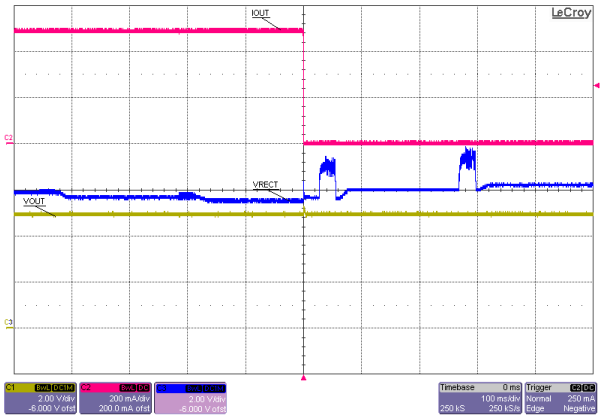


Figure 11. 0.5-A Load Dump Full System Response

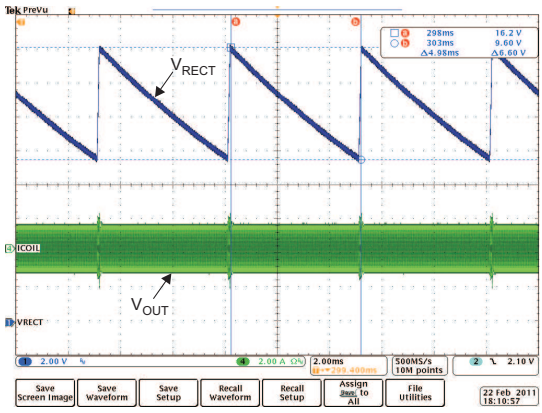


Figure 12. Rectifier Overvoltage Clamp (f_{op} = 110 kHz)

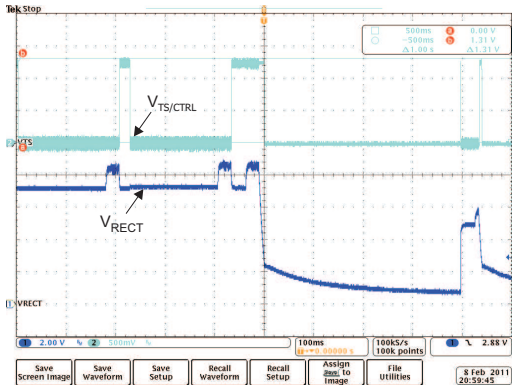


Figure 13. TS Fault

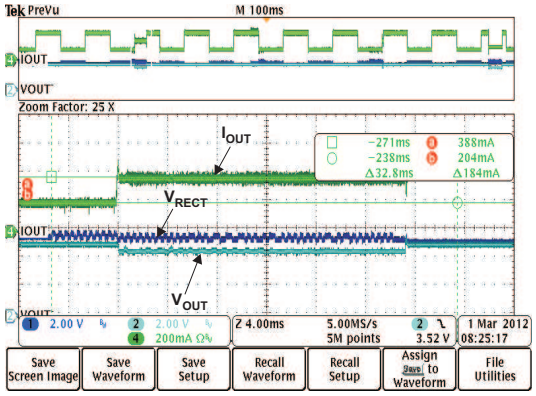


Figure 14. Adaptive Communication Limit Event Where the 400-mA Current Limit is Enabled (I_{OUT-DC} < 300 mA)

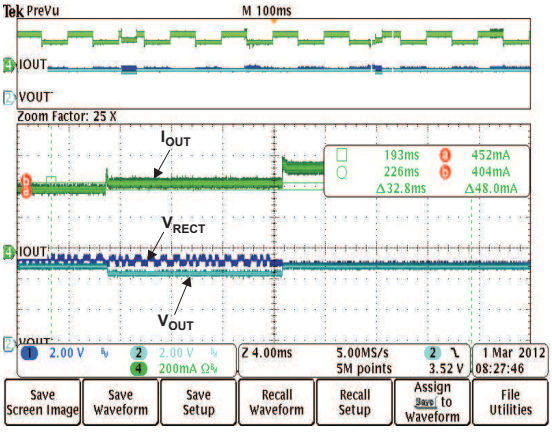


Figure 15. Adaptive Communication Limit Event Where the Current Limit is I_{OUT} + 50 mA (I_{OUT-DC} > 300 mA)

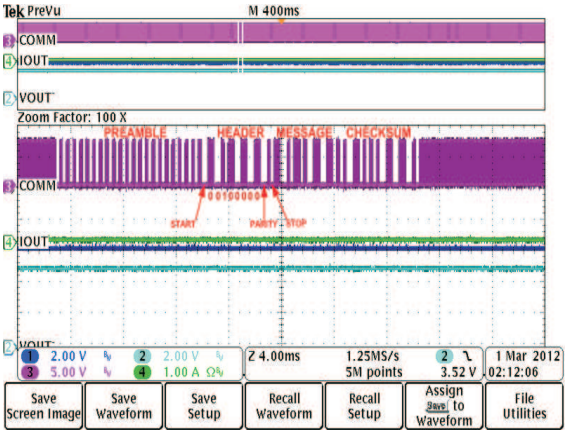


Figure 16. Rx Communication Packet Structure

8 Detailed Description

8.1 Overview

The principle of wireless power transfer is simply an open-cored transformer consisting of transmitter and receiver coils. The transmitter coil and electronics are typically built into a charger pad, and the receiver coil and electronics are typically built into a portable device such as a cell phone. When the receiver coil is positioned on the transmitter coil, magnetic coupling occurs when the transmitter coil is driven. The flux is coupled into the secondary coil, which induces a voltage and current flows. The secondary voltage is rectified, and power can be transferred effectively to a load wirelessly. Power transfer can be managed through any of the various closed-loop control schemes.

8.1.1 A Brief Description of the Wireless System

A wireless system consists of a charging pad (transmitter or primary) and the secondary-side equipment (receiver or secondary). There is a coil in the charging pad and in the secondary equipment which are magnetically coupled to each other when the secondary is placed on the primary. Power is then transferred from the transmitter to the receiver through coupled inductors (for example, an air-core transformer). Controlling the amount of power transferred is achieved by sending feedback (error signal) communication to the primary (that is, to increase or decrease power).

The receiver communicates with the transmitter by changing the load seen by the transmitter. This load variation results in a change in the transmitter coil current, which is measured and interpreted by a processor in the charging pad. Communication is done through digital-packets which are transferred from the receiver to the transmitter. Differential Biphase encoding is used for the packets. The bit rate is 2-kbps.

Various types of communication packets have been defined. These include identification and authentication packets, error packets, control packets, end power packets, and power usage packets.

The transmitter coil stays powered off most of the time. It occasionally wakes up to see if a receiver is present. When a receiver authenticates itself to the transmitter, the transmiter will remain powered on. The receiver maintains full control over the power transfer using communication packets.

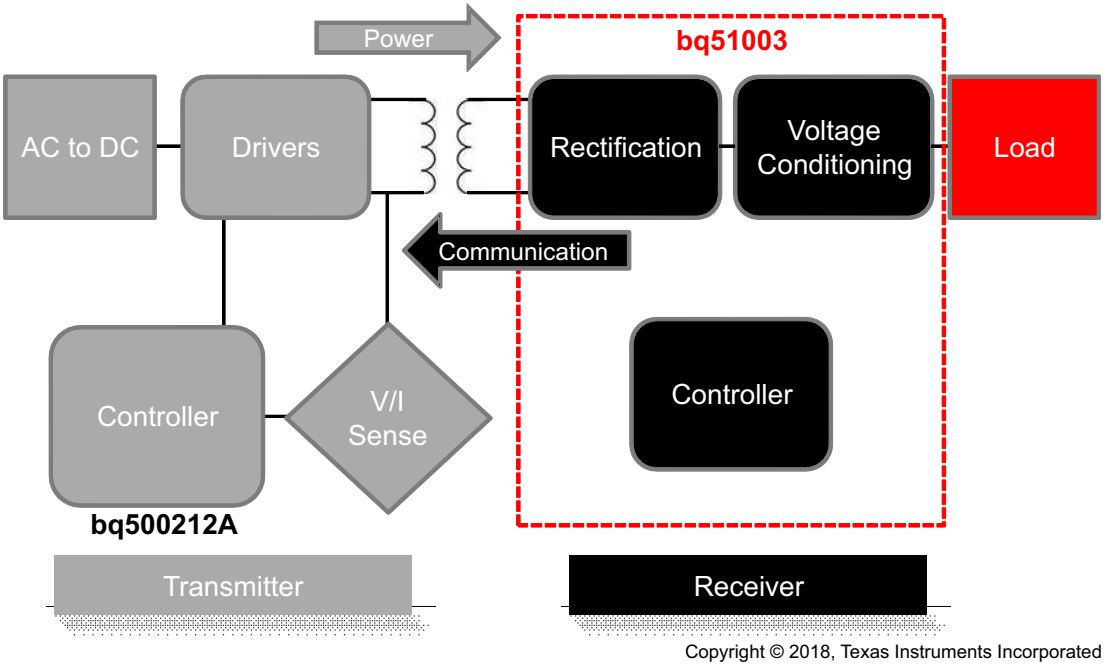
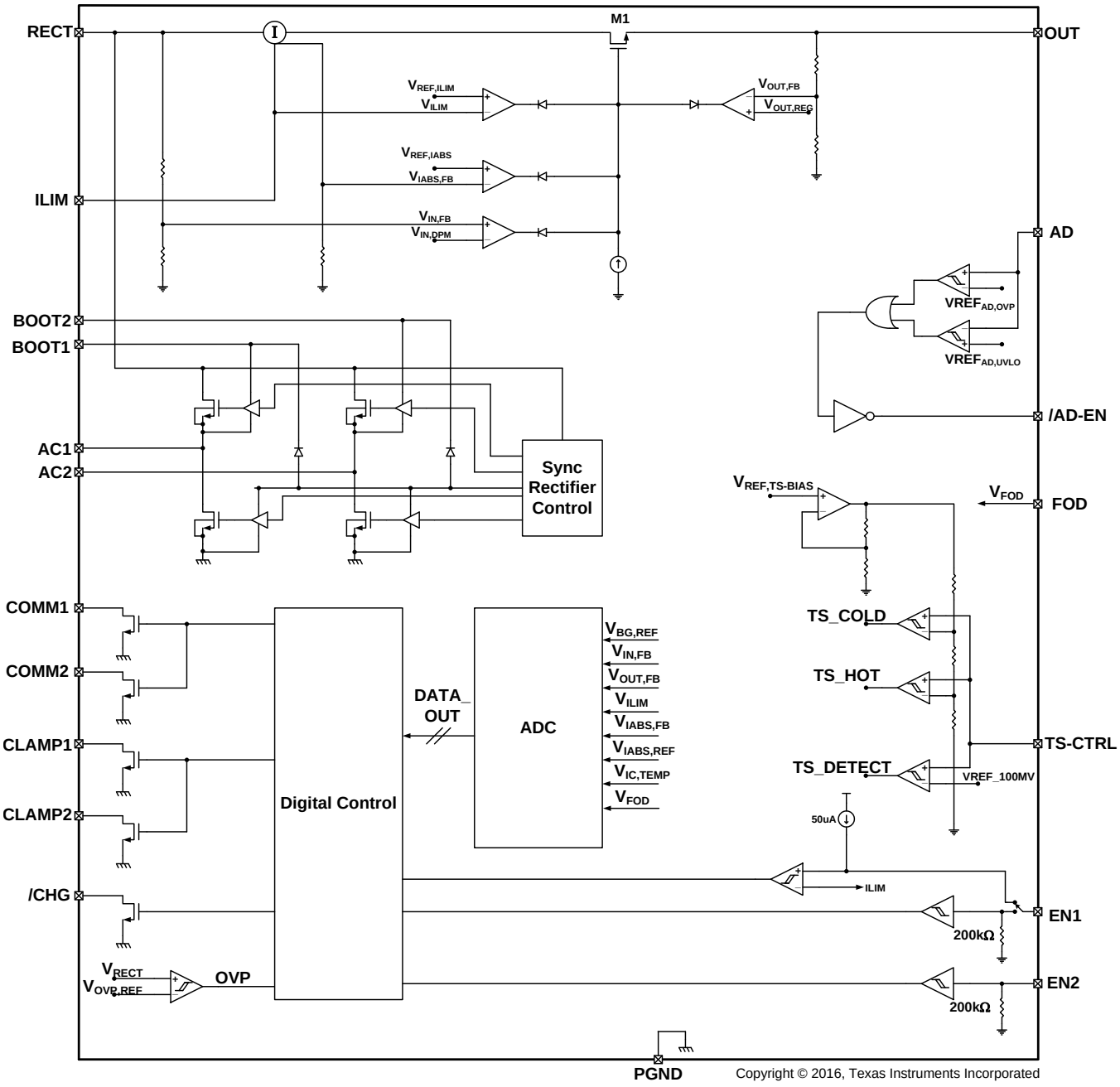


Figure 17. WPC Wireless Power System Indicating the Functional Integration of the bq51003

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Details of a Qi Wireless Power System and bq51003 Power Transfer Flow Diagrams

The bq51003 integrates a fully compliant WPC v1.2 communication algorithm to streamline receiver designs (no extra software development required). Other unique algorithms such as Dynamic Rectifier Control are also integrated to provide best-in-class system performance. This section provides a high-level overview of these features by illustrating the wireless power transfer flow diagram from start-up to active operation.

Feature Description (continued)

During start-up operation, the wireless power receiver must comply with proper handshaking to be granted a power contract from the Tx. The Tx initiates the hand shake by providing an extended digital ping. If an Rx is present on the Tx surface, the Rx then provides the signal strength, configuration, and identification packets to the Tx (see volume 1 of the WPC specification for details on each packet). These are the first three packets sent to the Tx. The only exception is if there is a true shutdown condition on the EN1/EN2, AD, or TS-CTRL pins where the Rx will shut down the Tx immediately. See Table 5 for details. Once the Tx has successfully received the signal strength, configuration, and identification packets, the Rx will be granted a power contract and is then allowed to control the operating point of the power transfer. With the use of the bq51003 Dynamic Rectifier Control algorithm, the Rx will inform the Tx to adjust the rectifier voltage above 7 V prior to enabling the output supply. This method enhances the transient performance during system start-up. See Figure 18 for the start-up flow diagram details.

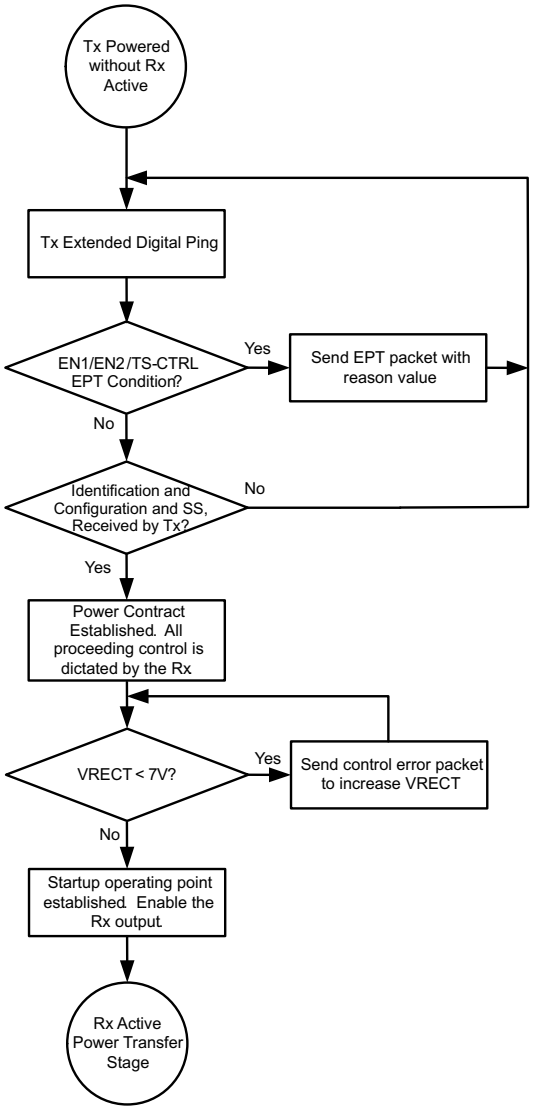


Figure 18. Wireless Power Start-Up Flow Diagram

Feature Description (continued)

Once the start-up procedure has been established, the Rx will enter the active power transfer stage. This is considered the *main loop* of operation. The Dynamic Rectifier Control algorithm will determine the rectifier voltage target based on a percentage of the maximum output current level setting (set by K_{IMAX} and the ILIM resistance to GND). The Rx will send control error packets to converge on these targets. As the output current changes, the rectifier voltage target will dynamically change. As a note, the feedback loop of the WPC system is relatively slow where it can take up to 90 ms to converge on a new rectifier voltage target. It should be understood that the instantaneous transient response of the system is open loop and dependent on the Rx coil output impedance at that operating point. The *main loop* will also determine if any conditions in Table 5 are true to discontinue power transfer. See Figure 19 which illustrates the active power transfer loop.

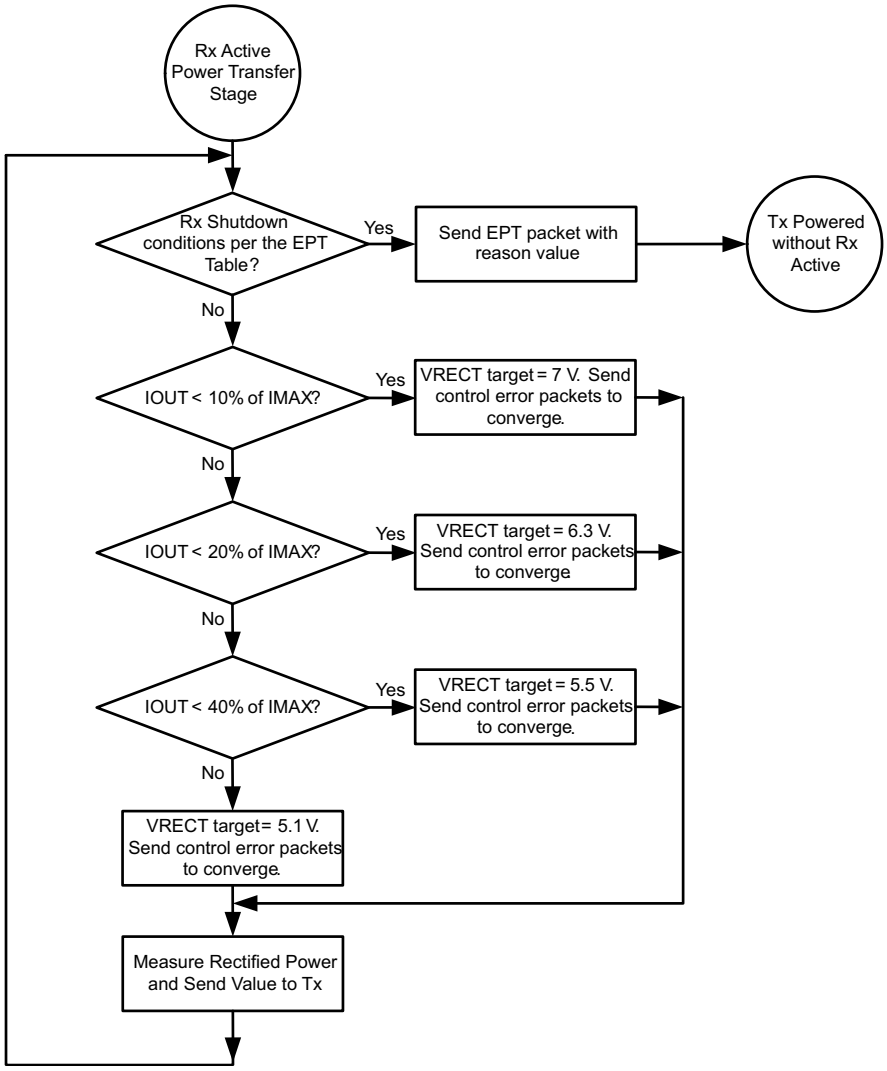


Figure 19. Active Power Transfer Flow Diagram

Another requirement of the WPC v1.2 specification is to send the measured received power. This task is enabled on the IC by measuring the voltage on the FOD pin which is proportional to the output current and can be scaled based on the choice of the resitor to ground on the FOD pin.

Feature Description (continued)

8.3.2 Dynamic Rectifier Control

The Dynamic Rectifier Control algorithm offers the end system designer optimal transient response for a given max output current setting. This is achieved by providing enough voltage headroom across the internal regulator at light loads to maintain regulation during a load transient. The WPC system has a relatively slow global feedback loop where it can take more than 90 ms to converge on a new rectifier voltage target. Therefore, the transient response is dependent on the loosely coupled transformers output impedance profile. The Dynamic Rectifier Control allows for a 2-V change in rectified voltage before the transient response will be observed at the output of the internal regulator (output of the bq51003).

8.3.3 Dynamic Efficiency Scaling

The Dynamic Efficiency Scaling feature allows for the loss characteristics of the bq51003 to be scaled based on the maximum expected output power in the end application. This effectively optimizes the efficiency for each application. This feature is achieved by scaling the loss of the internal LDO based on a percentage of the maximum output current. Note that the maximum output current is set by the K_{IMAX} term and the R_{ILIM} resistance (where R_{ILIM} = K_{IMAX} / I_{MAX}). The flow diagram show in Figure 19 illustrates how the rectifier is dynamically controlled (*Dynamic Rectifier Control*) based on a fixed percentage of the I_{MAX} setting. Table 2 summarizes how the rectifier behavior is dynamically adjusted based on two different R_{ILIM} settings.

Table 2. Dynamic Efficiency Scaling

OUTPUT CURRENT PERCENTAGE	R_{ILIM} = 1116 Ω I_{MAX} = 250 mA	R_{ILIM} = 488 Ω I_{MAX} = 500 mA	V_{RECT}
0 to 10%	0 A to 0.025 A	0 A to 0.05 A	7.08 V
10 to 20%	0.025 A to 0.050 A	0.050 A to 0.100 A	6.28 V
20 to 40%	0.050 A to 0.100 A	0.100 A to 0.200 A	5.53 V
>40%	> 0.100 A	> 0.200 A	5.11 V

Figure 5 illustrates the shift in the *Dynamic Rectifier Control* behavior based on the two different R_{ILIM} settings. With the rectifier voltage (V_{RECT}) being the input to the internal LDO, this adjustment in the *Dynamic Rectifier Control* thresholds will dynamically adjust the power dissipation across the LDO where:

$$P_{DIS} = \left(V_{RECT} - V_{OUT}\right) \times I_{OUT} \quad (1)$$

Figure 3 illustrates how the system efficiency is improved due to the *Dynamic Efficiency Scaling* feature. Note that this feature balances efficiency with optimal system transient response.

8.3.4 R_{ILIM} Calculations

The bq51003 includes a means of providing hardware overcurrent protection by means of an analog current regulation loop. The hardware current limit provides an extra level of safety by clamping the maximum allowable output current (that is, a current compliance). The R_{ILIM} resistor size also sets the thresholds for the dynamic rectifier levels and thus providing efficiency tuning per each application's maximum system current. The calculation for the total R_{ILIM} resistance is as follows:

$$R_{ILIM} = \frac{262}{I_{MAX}}$$

$$I_{ILIM} = 1.2 \times I_{MAX} = \frac{314}{R_{ILIM}}$$

$$R_{ILIM} = R_1 + R_{FOD} \quad (2)$$

where

- I_{MAX} is the expected maximum output current during normal operation
- I_{ILIM} is the hardware over current limit

When referring to the application diagram shown in Figure 32, R_{ILIM} is the sum of R_{FOD} and the R_1 resistance (that is, the total resistance from the ILIM pin to GND).

8.3.5 Input Overvoltage

If the input voltage suddenly increases in potential (that is, due to a change in position of the equipment on the charging pad), the voltage-control loop inside the bq51003 becomes active, and prevents the output from going beyond $V_{OUT-REG}$. The receiver then starts sending back error packets to the transmitter every 30 ms until the input voltage comes back to the $V_{RECT-REG}$ target, and then maintains the error communication every 250 ms.

If the input voltage increases in potential beyond $V_{RECT-OVP}$, the IC switches off the LDO and communicates to the primary to bring the voltage back to $V_{RECT-REG}$. In addition, a proprietary voltage protection circuit is activated by means of C_{CLAMP1} and C_{CLAMP2} that protects the IC from voltages beyond the maximum rating of the IC (that is, 20 V).

8.3.6 Adapter Enable Functionality and EN1/EN2 Control

Figure 38 is an example application that shows the bq51003 used as a wireless power receiver that can power mutliplex between wired or wireless power for the down-system electronics. In the default operating mode pins EN1 and EN2 are low, which activates the adapter enable functionality. In this mode, if an adapter is not present the AD pin will be low, and $\overline{\text{AD-EN}}$ pin will be pulled to the higher of the OUT and AD pins so that the PMOS between OUT and AD will be turned off. If an adapter is plugged in and the voltage at the AD pin goes above 3.6 V then wireless charging is disabled and the $\overline{\text{AD-EN}}$ pin will be pulled approximately 4 V below the AD pin to connect AD to the secondary charger. The difference between AD and $\overline{\text{AD-EN}}$ is regulated to a maximum of 7 V to ensure the V_{GS} of the external PMOS is protected.

The EN1 and EN2 pins include internal 200-kΩ pulldown resistors, so that if these pins are not connected bq51003 defaults to $\overline{\text{AD-EN}}$ control mode. However, these pins can be pulled high to enable other operating modes as described in Table 3:

Table 3. Adapter Enable Functionality

EN1	EN2	RESULT
0	0	Adapter control enabled. If adapter is present then secondary charger is powered by adapter, otherwise wireless charging is enabled when wireless power is available. Communication current limit is enabled.
0	1	Disables communication current limit.
1	0	$\overline{\text{AD-EN}}$ is pulled low, whether or not adapter voltage is present. This feature can be used, for example, for USB OTG applications.
1	1	Adapter and wireless charging are disabled, that is, power will never be delivered by the OUT pin in this mode.

Table 4. EN1/EN2 Control

EN1	EN2	WIRELESS POWER	WIRED POWER	OTG MODE	ADAPTIVE COMMUNICATION LIMIT	EPT
0	0	Enabled	Priority(1)	Disabled	Enabled	Not Sent to Tx
0	1	Priority(1)	Enabled	Disabled	Disabled	Not Sent to Tx
1	0	Disabled	Enabled	Enabled(2)	N/A	EPT 0x00, Unknown
1	1	Disabled	Disabled	Disabled	N/A	EPT 0x01, Charge Complete

(1) If both wired and wireless power are present, wired power is given priority.
(2) Allows for a boost-back supply to be driven from the output terminal of the Rx to the adapter port through the external back-to-back PMOS FET.

As described in Table 4, pulling EN2 high disables the adapter mode and only allows wireless charging. In this mode the adapter voltage will always be blocked from the OUT pin. An application example where this mode is useful is when USB power is present at AD, but the USB is in suspend mode so that no power can be taken from the USB supply. Pulling EN1 high enables the off-chip PMOS regardless of the presence of a voltage. This function can be used in USB OTG mode to allow a charger connected to the OUT pin to power the AD pin. Finally, pulling both EN1 and EN2 high disables both wired and wireless charging.

NOTE

It is required to connect a back-to-back PMOS between AD and OUT so that voltage is blocked in both directions. Also, when AD mode is enabled no load can be pulled from the RECT pin as this could cause an internal device overvoltage in bq51003.

8.3.7 End Power Transfer Packet (WPC Header 0x02)

The WPC allows for a special command for the receiver to terminate power transfer from the transmitter termed End Power Transfer (EPT) packet. Table 5 specifies the v1.2 reasons column and their corresponding data field value. The condition column corresponds to the methodology used by bq51003 to send equivalent message.

Table 5. End Power Transfer Packet

MESSAGE	VALUE	CONDITION
Unknown	0x00	TS-CTRL = 1, or ,EN1 EN2> = <10> or AD > V_{AD_EN}
Charge Complete	0x01	<EN1 EN2> = <11>
Internal Fault	0x02	T_J > 150°C or R_{ILIM} < 100 Ω
Over Temperature	0x03	TS < V_{HOT}, TS > V_{COLD}, or TS-CTRL < 100 mV
Over Voltage	0x04	Not Sent
Over Current	0x05	NOT USED
Battery Failure	0x06	Not Sent
Reconfigure	0x07	Not Sent
No Response	0x08	V_{RECT} target does not converge

8.3.8 Status Outputs

The bq51003 has one status output, $\overline{CHG}$. This output is an open-drain NMOS device that is rated to 20 V. The open-drain FET connected to the $\overline{CHG}$ pin will be turned on whenever the output of the power supply is enabled. Note that the output of the power supply will not be enabled if the $V_{RECT-REG}$ does not converge at the no-load target voltage.

8.3.9 WPC Communication Scheme

The WPC communication uses a modulation technique termed *backscatter modulation* where the receiver coil is dynamically loaded to provide amplitude modulation of the transmitter's coil voltage and current. This scheme is possible due to the fundamental behavior between two loosely coupled inductors (that is, between the Tx and Rx coil). This type of modulation can be accomplished by switching in and out a resistor at the output of the rectifier, or by switching in and out a capacitor across the AC1/AC2 net. Figure 20 shows how to implement resistive modulation.

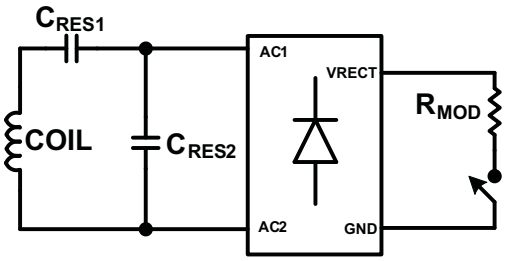


Figure 20. Resistive Modulation

Figure 21 shows how to implement capacitive modulation.

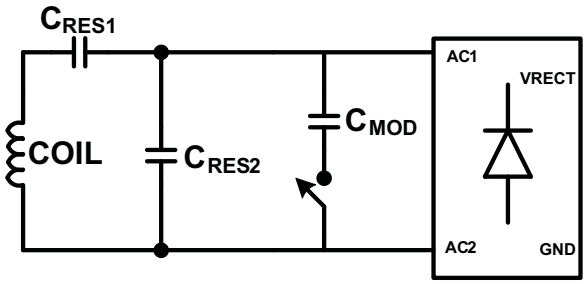


Figure 21. Capacitive Modulation

The amplitude change in Tx coil voltage or current can be detected by the transmitters decoder. Figure 22 shows the resulting signal observed by the Tx.

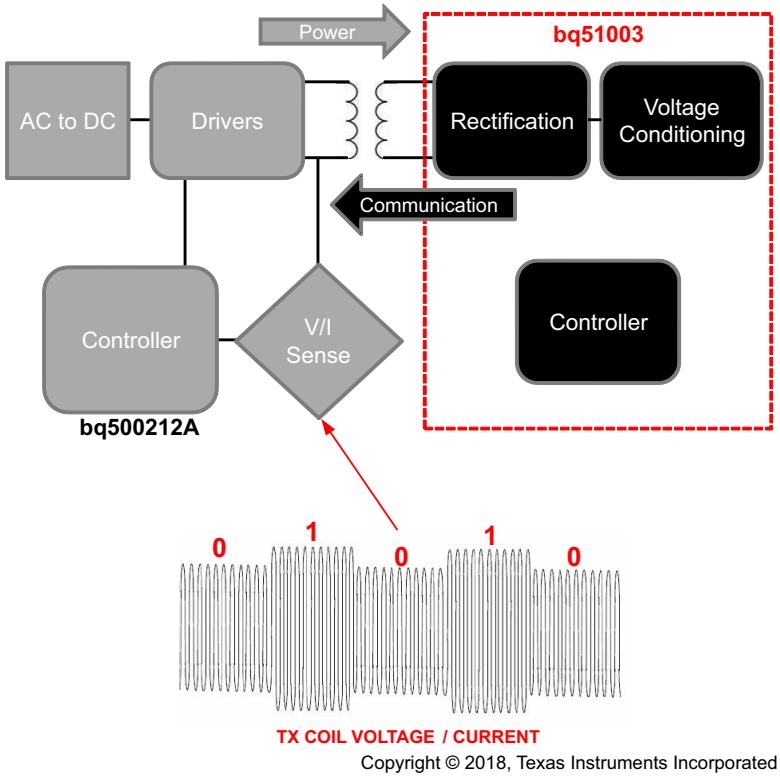


Figure 22. TX Coil Voltage and Current

The WPC protocol uses a differential biphase encoding scheme to modulate the data bits onto the Tx coil voltage and current. Each data bit is aligned at a full period of 0.5 ms (t_{CLK}) or 2 kHz. An encoded ONE results in two transitions during the bit period and an encoded ZERO results in a single transition. See Figure 23 for an example of the differential biphase encoding.

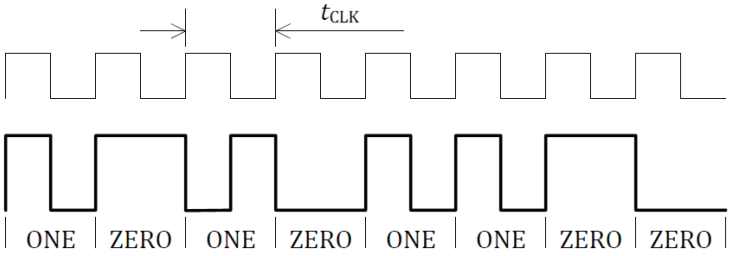


Figure 23. Differential Biphase Encoding Scheme (WPC Volume 1: Low Power, Part 1 Interface Definition)

The bits are sent LSB first and use an 11-bit asynchronous serial format for each portion of the packet. This includes one start bit, n-data bytes, a parity bit, and a single stop bit. The start bit is always ZERO and the parity bit is odd. The stop bit is always ONE. Figure 24 shows the details of the asynchronous serial format.

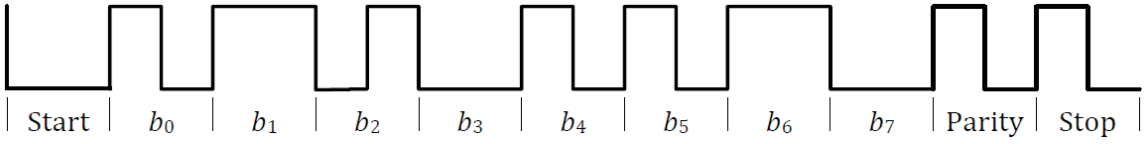


Figure 24. Asynchronous Serial Formatting (WPC volume 1: Low Power, Part 1 Interface Definition)

Each packet format is organized as shown in Figure 25.

Figure 25. Packet Format (WPC Volume 1: Low Power, Part 1 Interface Definition)

Figure 16 shows an example waveform of the receiver sending a rectified power packet (header 0x04).

8.3.10 Communication Modulator

The bq51003 provides two identical, integrated communication FETs which are connected to the pins COMM1 and COMM2. These FETs are used for modulating the secondary load current which allows bq51003 to communicate error control and configuration information to the transmitter. Figure 26 shows how the COMM pins can be used for resistive load modulation. Each COMM pin can handle at most a 24-Ω communication resistor. Therefore, if a COMM resistor between 12 Ω and 24 Ω is required COMM1 and COMM2 pins must be connected in parallel. The bq51003 does not support a COMM resistor less than 12 Ω.

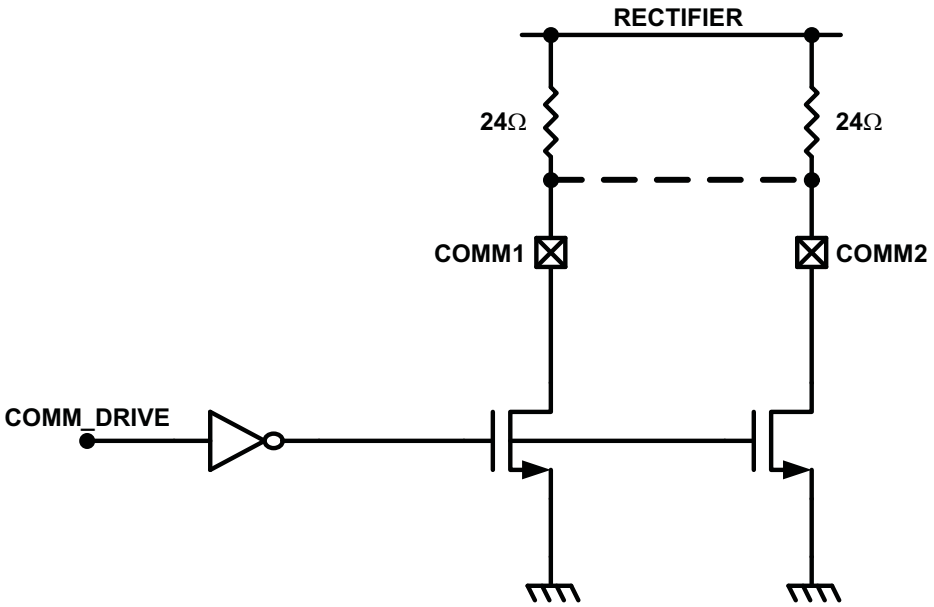


Figure 26. Resistive Load Modulation

In addition to resistive load modulation, the bq51003 is also capable of capacitive load modulation as shown in Figure 27. In this case, a capacitor is connected from COMM1 to AC1 and from COMM2 to AC2. When the COMM switches are closed there is effectively a 22-nF capacitor connected between AC1 and AC2. Connecting a capacitor in between AC1 and AC2 modulates the impedance seen by the coil, which will be reflected in the primary as a change in current.

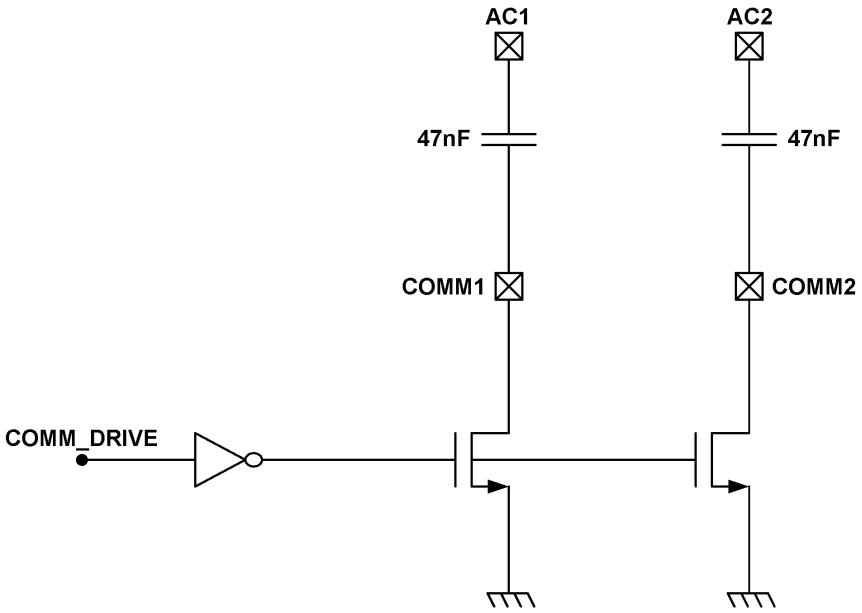


Figure 27. Capacitive Load Modulation

8.3.11 Adaptive Communication Limit

The Qi communication channel is established through backscatter modulation as described in the previous sections. This type of modulation takes advantage of the loosely coupled inductor relationship between the Rx and Tx coil. Essentially the switching in-and-out of the communication capacitor or resistor adds a transient load to the Rx coil to modulate the Tx coil voltage and current waveform (amplitude modulation). The consequence of this technique is that a load transient (load current noise) from the mobile device has the same signature. To provide noise immunity to the communication channel, the output load transients must be isolated from the Rx coil. The proprietary feature *Adaptive Communication Limit* achieves this by dynamically adjusting the current limit of the regulator. When the regulator is put in current limit, any load transients will be offloaded to the battery in the system.

Note that this requires the battery charger IC to have input voltage regulation (weak adapter mode). The output of the Rx appears as a weak supply if a transient occurs above the current limit of the regulator.

The Adaptive Communication Limit feature has two current limit modes and is detailed in Table 6:

Table 6. Adaptive Communication Limit

I_{OUT}	COMMUNICATION CURRENT LIMIT
< 300 mA	Fixed 400 mA
> 300 mA	I_{OUT} + 50 mA

8.3.12 Synchronous Rectification

The bq51003 provides an integrated, self-driven synchronous rectifier that enables high-efficiency AC to DC power conversion. The rectifier consists of an all NMOS H-Bridge driver where the backgates of the diodes are configured to be the rectifier when the synchronous rectifier is disabled. During the initial start-up of the WPC system the synchronous rectifier is not enabled. At this operating point, the DC rectifier voltage is provided by the diode rectifier. Once V_{RECT} is greater than UVLO, half-synchronous mode will be enabled until the load current surpasses 120 mA. Above 120 mA the full synchronous rectifier stays enabled until the load current drops back below 100 mA where half-synchronous mode is enabled instead.

8.3.13 Temperature Sense Resistor Network (TS)

bq51003 includes a ratiometric external temperature sense function. The temperature sense function has two ratiometric thresholds which represent a hot and cold condition. TI recommends an external temperature sensor to provide safe operating conditions for the receiver product. This pin is best used for monitoring the surface that can be exposed to the end user (that is, place the NTC resistor closest to the user).

Figure 28 allows for any NTC resistor to be used with the given V_{HOT} and V_{COLD} thresholds.

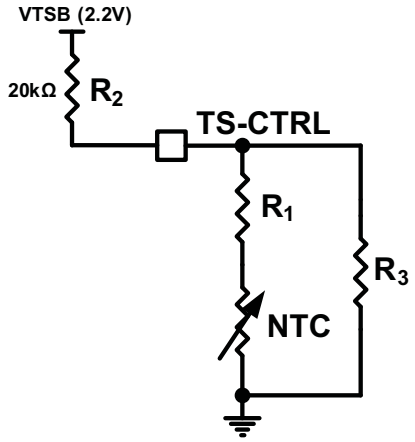


Figure 28. NTC Circuit Used for Safe Operation of the Wireless Receiver Power Supply

The resistors R_1 and R_3 can be solved by resolving the system of equations at the desired temperature thresholds (see Equation 3 and Equation 4).

$$\%V_{COLD} = \frac{\left(\frac{R_3\left(R_{NTC}\big|_{TCOLD} + R_1\right)}{R_3 + \left(R_{NTC}\big|_{TCOLD} + R_1\right)}\right)}{\left(\frac{R_3\left(R_{NTC}\big|_{TCOLD} + R_1\right)}{R_3 + \left(R_{NTC}\big|_{TCOLD} + R_1\right)}\right) + R2} \times 100$$

$$\%V_{HOT} = \frac{\left(\frac{R_3\left(R_{NTC}\big|_{THOT} + R_1\right)}{R_3 + \left(R_{NTC}\big|_{THOT} + R_1\right)}\right)}{\left(\frac{R_3\left(R_{NTC}\big|_{THOT} + R_1\right)}{R_3 + \left(R_{NTC}\big|_{THOT} + R_1\right)}\right) + R2} \times 100 \quad (3)$$

$$R_{NTC}\big|_{TCOLD} = R_O e^{\beta\left(1/T_{COLD} - 1/T_O\right)}$$

$$R_{NTC}\big|_{THOT} = R_O e^{\beta\left(1/T_{HOT} - 1/T_O\right)}$$

where

- T_{COLD} and T_{HOT} are the desired temperature thresholds in degrees Kelvin
- R_O is the nominal resistance
- and β is the temperature coefficient of the NTC resistor
- R_O is fixed at 20 kΩ (4)

An example solution is provided:

- R1 = 4.23 kΩ
- R3 = 66.8 kΩ

where the chosen parameters are:

- $\%V_{HOT}$ = 19.6%

- $\%V_{COLD}$ = 58.7%
- T_{COLD} = –10°C
- T_{HOT} = 100°C
- β = 3380
- R_O = 10 kΩ

Figure 29 shows the plot of the percent V_{TSB} vs temperature.

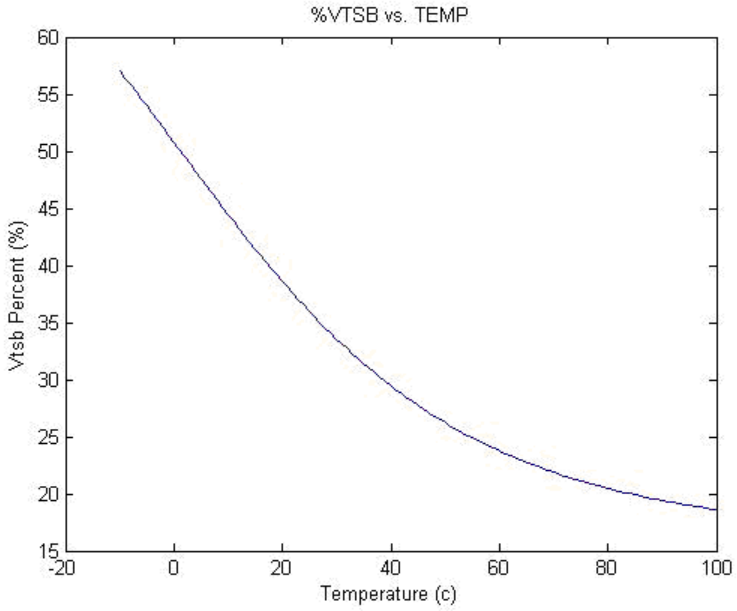


Figure 29. Example Solution for an NTC resistor with R_O = 10 kΩ and β = 4500

Figure 30 illustrates the periodic biasing scheme used for measuring the TS state. The TS_READ signal enables the TS bias voltage for 24 ms. During this period the TS comparators are read (each comparator has a 10-ms deglitch) and appropriate action is taken based on the temperature measurement. After this 24-ms period has elapsed, the TS_READ signal goes low, which causes the TS-Bias pin to become high impedance. During the next 35 ms (priority packet period) or 235 ms (standard packet period), the TS voltage is monitored and compared to 100 mV. If the TS voltage is greater than 100 mV then a secondary device is driving the TS-CTRL pin and a CTRL = '1' is detected.

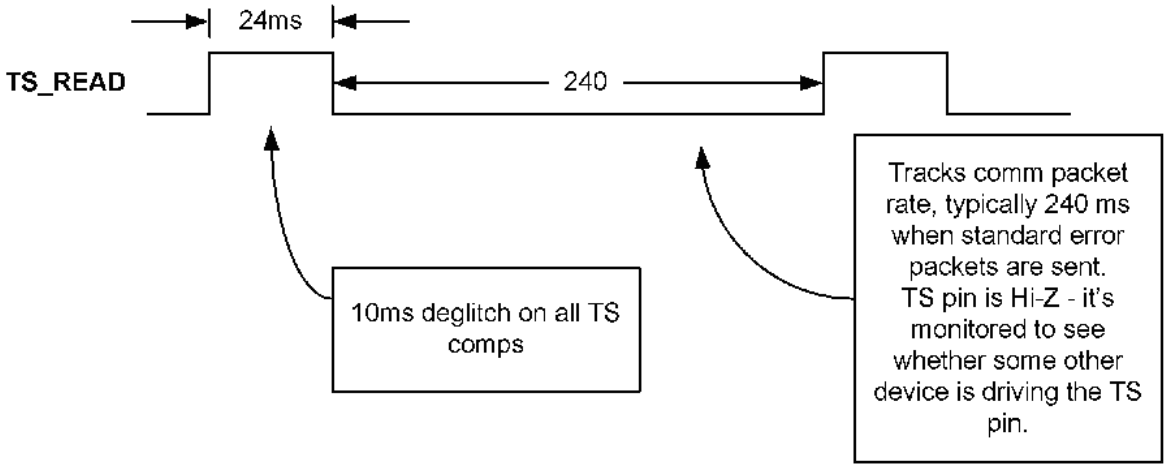


Figure 30. Timing Diagram for TS Detection Circuit

8.3.14 3-State Driver Recommendations for the TS-CTRL Pin

The TS-CTRL pin offers three functions with one 3-state driver interface

1. NTC temperature monitoring,
2. Fault indication,
3. End Power Transfer Unknown

A 3-state driver can be implemented with the circuit in Figure 31 and the use of two GPIO connections.

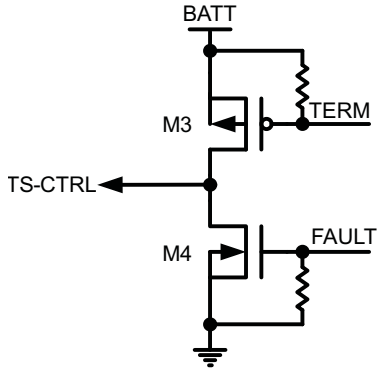


Figure 31. 3-State Driver for TS-CTRL

Note that the signals TERM and FAULT are given by two GPIOs. The truth table for this circuit is found in Table 7:

Table 7. Truth Table

TERM	FAULT	F (Result)
1	0	Z (Normal Mode)
0	0	End Power Transfer 0X00
1	1	End Power Transfer 0X03

The default setting is TERM / FAULT = 1 / 0. In this condition, the TS-CTRL net is high impedance (high-z) and the NTC function is allowed to operate, normal operation. When TERM / FAULT = 1 /1 the TS-CTRL pin is pulled to GND and the RX is shutdown with End Power Transfer Over Temperature sent to TX. When TERM / FAULT = 0 / 0, the TS-CTRL pin is pulled to the battery and the RX is shutdown with End Power Transfer Unknown sent to the TX.

8.3.15 Thermal Protection

The bq51003 includes a thermal shutdown protection. If the die temperature reaches T_J(OFF), the LDO is shut off to prevent any further power dissipation. In this event, bq51003 sends an EPT message of internal fault (0x02).

8.3.16 WPC v1.2 Compliance – Foreign Object Detection

The bq51003 is a WPC v1.2 compatible device. To enable a Power Transmitter to monitor the power loss across the interface as one of the possible methods to limit the temperature rise of Foreign Objects, the bq51003 reports its Received Power to the Power Transmitter. The Received Power equals the power that is available from the output of the Power Receiver plus any power that is lost in producing that output power (the power loss in the Secondary Coil and series resonant capacitor, the power loss in the Shielding of the Power Receiver, the power loss in the rectifier). In WPC v1.2 specification, foreign object detection (FOD) is enforced. This means the bq51003 will send received power information with known accuracy to the transmitter.

WPC v1.2 defines Received Power as “the average amount of power that the Power Receiver receives through its Interface Surface, in the time window indicated in the Configuration Packet”.

To receive certification as a WPC v1.2 receiver, the Device Under Test (DUT) is tested on a Reference Transmitter whose transmitted power is calibrated, the receiver must send a received power determined by Equation 5:

$$0 \text{ mW} < (\text{Tx PWR})_{REF} - (\text{Rx PWR out})_{DUT} < -250 \text{ mW} \quad (5)$$

This 250-mW bias ensures that system will remain interoperable.

WPC v1.2 Transmitter will be tested to see if they can detect reference Foreign Objects with a Reference receiver.

WPC v1.2 Specification will allow much more accurate sensing of Foreign Objects.

8.4 Device Functional Modes

The operational modes of the bq51003 are described in the *Feature Description*. The bq51003 has several functional modes. Start-up refers to the initial power transfer and communication between the receiver (bq51003 circuit) and the transmitter. Power transfer refers to any time that the TX and RX are communicating and power is being delivered from the TX to the RX. Power transfer termination occurs when the RX is removed from the TX, power is removed from the TX, or the RX requests power transfer termination.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq51003 is a fully integrated wireless power receiver in a single device. The device complies with the WPC v1.2 specifications for a wireless power receiver. When paired with a WPC v1.2 compliant transmitter, it can provide up to 2.5 W of power. There are several tools available for the design of the system. These tools may be obtained by checking the product page at www.ti.com/product/bq51003.

9.2 Typical Applications

9.2.1 bq51003 Wireless Power Receiver Used as a Power Supply

The following application discussion covers the requirements for setting up the bq51003 in a Qi-compliant system for use as a power supply.

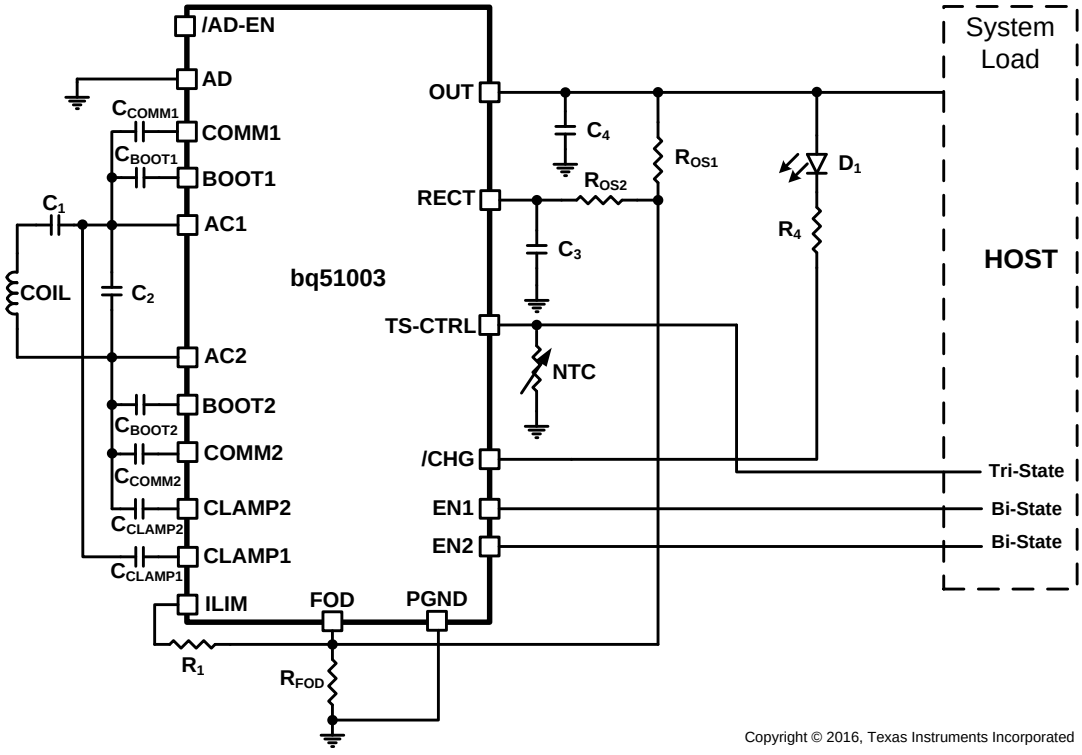


Figure 32. bq51003 Used as a Wireless Power Receiver and Power Supply for System Loads Only One of R_{OS1} or R_{OS2} Needed

9.2.1.1 Design Requirements

This application is for a system that has varying loads up to 500 mA (2.5 W). It must work with any Qi-certified transmitter. There is no requirement for any external thermal measurements. An LED indication is required to indicate an active power supply. Each of the components from the application drawing will be examined.

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Using the bq51003 as a Wireless Power Supply

Figure 32 is the schematic of a system which uses the bq51003 as a power supply.

When the system shown in Figure 32 is placed on the charging pad, the receiver coil is inductively coupled to the magnetic flux generated by the coil in the charging pad which consequently induces a voltage in the receiver coil. The internal synchronous rectifier feeds this voltage to the RECT pin which has the filter capacitor C3.

The bq51003 identifies and authenticates itself to the primary using the COMM pins by switching on and off the COMM FETs and hence switching in and out C_{COMM}. If the authentication is successful, the transmitter will remain powered on. The bq51003 measures the voltage at the RECT pin, calculates the difference between the actual voltage and the desired voltage $V_{RECT-REG}$, (threshold 1 at no load) and sends back error packets to the primary. This process goes on until the input voltage settles at $V_{RECT-REG}$. During a load transient, the dynamic rectifier algorithm will set the targets specified by $V_{RECT-REG}$ thresholds 1, 2, 3, and 4. This algorithm is termed Dynamic Rectifier Control and is used to enhance the transient response of the power supply.

During power up, the LDO is held off until the $V_{RECT-REG}$ threshold 1 converges. The voltage control loop ensures that the output voltage is maintained at $V_{OUT-REG}$ to power the system. The bq51003 meanwhile continues to monitor the input voltage, and maintains sending error packets to the primary every 250 ms. If a large overshoot occurs, the feedback to the primary speeds up to every 32 ms to converge on an operating point in less time.

9.2.1.2.2 Series and Parallel Resonant Capacitor Selection

Shown in Figure 32, the capacitors C1 (series) and C2 (parallel) make up the dual resonant circuit with the receiver coil. These two capacitors must be sized correctly per the WPC v1.2 specification. Figure 33 illustrates the equivalent circuit of the dual resonant circuit:

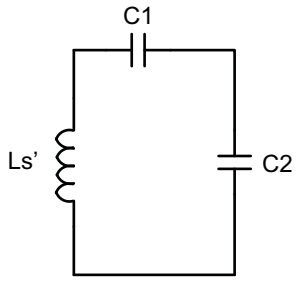


Figure 33. Dual Resonant Circuit With the Receiver Coil

Section 4.2 (Power Receiver Design Requirements) in Part 1 of the WPC v1.2 specification highlights in detail the sizing requirements. To summarize, the receiver designer will be required take inductance measurements with a fixed test fixture. Figure 34 shows the test fixture.

Typical Applications (continued)

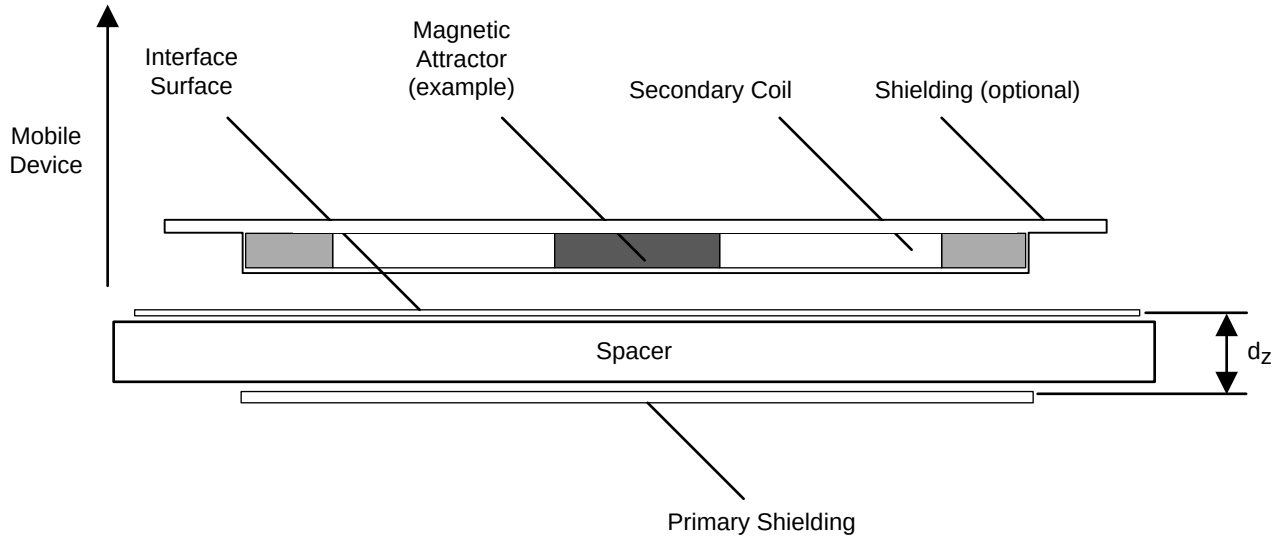


Figure 34. WPC v1.2 Receiver Coil Test Fixture for the Inductance Measurement Ls' (Copied from System Description Wireless Power Transfer, Volume 1: Low Power, Part 1 Interface Definition, Version 1.2)

The primary shield is to be 50 mm x 50 mm x 1 mm of Ferrite material PC44 from TDK Corp. The gap d_Z is to be 3.4 mm. The receiver coil, as it will be placed in the final system (that is, the back cover and battery must be included if the system calls for this), is to be placed on top of this surface and the inductance is to be measured at 1-V RMS and a frequency of 100 kHz. This measurement is termed Ls'. The same measurement is to be repeated without the test fixture shown in Figure 34. This measurement is termed Ls or the free-space inductance. Each capacitor can then be calculated using Equation 6:

$$C_1 = \left[\left(f_S \times 2\pi \right)^2 \times L_S' \right]^{-1}$$

$$C_2 = \left[\left(f_D \times 2\pi \right)^2 \times L_S - \frac{1}{C_1} \right]^{-1}$$

where

- f_S is 100 kHz +5/-10%
- f_D is 1 MHz ±10%. (6)

C1 must be chosen first prior to calculating C2.

The quality factor must be greater than 77 and can be determined by Equation 7:

$$Q = \frac{2\pi \cdot f_D \cdot L_S}{R}$$

where

- R is the DC resistance of the receiver coil. All other constants are defined above. (7)

9.2.1.2.3 COMM, CLAMP, and BOOT Capacitors

For most applications, the COMM, CLAMP, and BOOT capacitance values will be chosen to match the bq51003EVM-764.

The BOOT capacitors are used to allow the internal rectifier FETs to turn on and off properly. These capacitors are from AC1 to BOOT1 and from AC2 to BOOT2 and must have a minimum 25-V rating. A 10-nF capacitor with a 25-V rating is chosen.

Typical Applications (continued)

The CLAMP capacitors are used to aid in the clamping process to protect against overvoltage. These capacitors are from AC1 to CLAMP1 and from AC2 to CLAMP2 and must have a minimum 25-V rating. A 0.47-µF capacitor with a 25-V rating is chosen.

The COMM capacitors are used to facilitate the communication from the RX to the TX. This selection can vary a bit more than the BOOT and CLAMP capacitors. In general, TI recommends an 22-nF capacitor. Based on the results of testing of the communication robustness in the final solution, a change to a 47-nF capacitor may be in order. The larger the capacitor the larger the deviation will be on the coil which sends a stronger signal to the TX. This also decreases the efficiency somewhat. In this case, a 22-nF capacitor with a 25-V rating is chosen.

9.2.1.2.4 Control Pins and $\overline{\text{CHG}}$

This section discusses the pins that control the functions of the bq51003 (AD, $\overline{\text{AD\_EN}}$, EN1, EN2, and TS or CTRL).

This solution uses wireless power exclusively. The AD pin is tied low to disable wired power interaction. The output pin $\overline{\text{AD\_EN}}$ is left floating.

EN1 and EN2 are tied to the system controller GPIO pins. This allows the system to control the wireless power transfer. Normal operation leaves EN1 and EN2 low or floating (GPIO low or high impedance). EN1 and EN2 have internal pulldown resistors. With both EN1 and EN2 low, wireless power is enabled and power can be transferred whenever the RX is on a suitable TX. The RX system controller can terminate power transfer and send an EPT 0x01 (Charge Complete) by setting EN1=EN2=1. The TX will terminate power when the EPT 0x01 is received. The TX will continue to test for power transfer, but will not engage until the RX requests power. For example, if the TX is the bq500212A, the TX will send digital pings approximately once per 5 seconds. During each ping, the bq51003 will resend the EPT 0x01. Between the pings, the bq500212A goes into low power Sleep mode reducing power consumption. When the RX system controller determines it is time to resume power transfer (for example, the battery voltage is below its recharge threshold) the controller simply returns EN1 and EN2 to low (or float) states. The next ping of the bq500212A will power the bq51003 which will now communicate that it is time to transfer power. The TX and RX communication resumes and power transfer is reinitiated.

The TS or CTRL pin will be used as a temperature sensor (with the NTC) and maintain the ability to terminate power transfer through the system controller. In this case, the GPIO will be in high impedance for normal NTC (Temperature Sense) control.

The $\overline{\text{CHG}}$ pin is used to indicate power transfer. A 2.1-V forward bias LED is used for D_1 with a current limiting 1.5-kΩ series resistor. The LED and resistor are tied from OUT to PGND and D_1 will light during power transfer.

9.2.1.2.5 Current Limit and FOD

The current limit and foreign object detection functions are related. The current limit is set by $R_1 + R_{FOD}$. R_{FOD} and Ros are determined by FOD calibration. Default values of 20 kΩ for Ros1 (RECT to FOD). Ros2 (OUT to FOD) remains open. 196 Ω for R_{FOD} is used. The final values need to be determined based on the FOD calibration. The tool for FOD calibration can be found on the bq51003 web folder under *Tools & software*. Good practice is to set the layout with 2 resistors for Ros and 2 for R_{FOD} to allow for precise values once the calibration is complete.

After setting R_{FOD}, R_1 can be calculated based on the desired current limit. The maximum current for this solution under normal operating conditions (I_{MAX}) is 500 mA. Using Equation 2 to calculate the maximum current yields a value of 524 Ω for R_{ILIM}. With R_{FOD} set to 196 Ω the remaining resistance for R_1 is 328 Ω. This also sets the hardware current limit to 600 mA to allow for temporary current surges without system performance concerns.

9.2.1.2.6 RECT and OUT Capacitance

RECT capacitance is used to smooth the AC to DC conversion and to prevent minor current transients from passing to OUT. For this 500-mA I_{MAX}, select two 10-µF capacitors and one 0.1-µF capacitor. These should be rated to 16 V.

OUT capacitance is used to reduce any ripple from minor load transients. For this solution, a single 10-µF capacitor and a single 0.1-µF capacitor are used.

Typical Applications (continued)

9.2.1.3 Application Curves

The following figures show the bq51003EVM-764 under 3 conditions. The RECT pin signal shows the bq51003 rectifier response due to the changing conditions. The OUT pin signal shows the impact to the OUT pin during the changed conditions. IOUT shows the current being sourced by the OUT pin.

Figure 35 shows the bq51003EVM-764 being placed on a transmitter with no load at the OUT pin. This shows the RECT pin receiving the Ping from the transmitter and responding with identification and other packets to establish power transfer. Once the RECT pin has reached its required voltage, the OUT pin is enabled and produces 5 V. The communication packet after 5 V is produced indicates the steady state condition being sent to the transmitter.

Figure 36 shows the same conditions, but the OUT pin has a resistive load which produces 400 mA at 5 V. The OUT pin current, IOUT, increases with the OUT pin voltage. The communication packets that occur after IOUT increases are sent to adjust the RECT voltge to the appropriate level.

Figure 37 shows the bq51003 under a no load condition until a 400-mA resistive load is added. Communication packets are sent until the RECT has come to the appropriate steady state value.

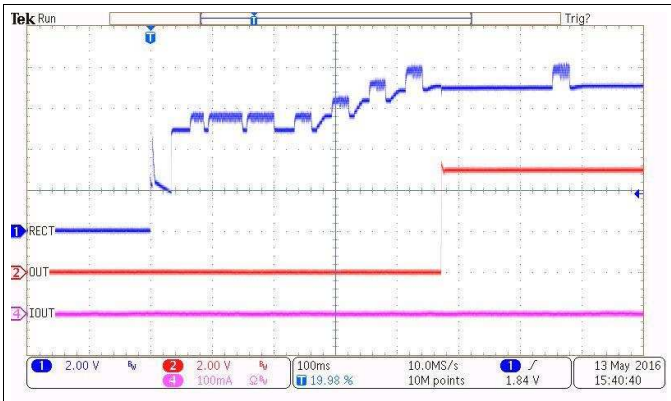


Figure 35. bq51003 Added to TX With No Load

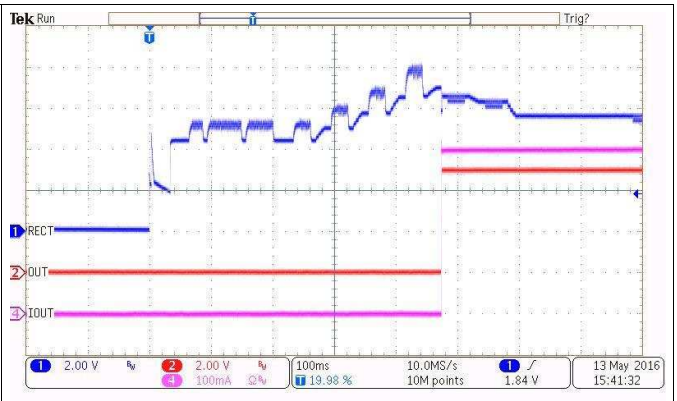


Figure 36. bq51003 Added to TX With 400-mA Resistive Load

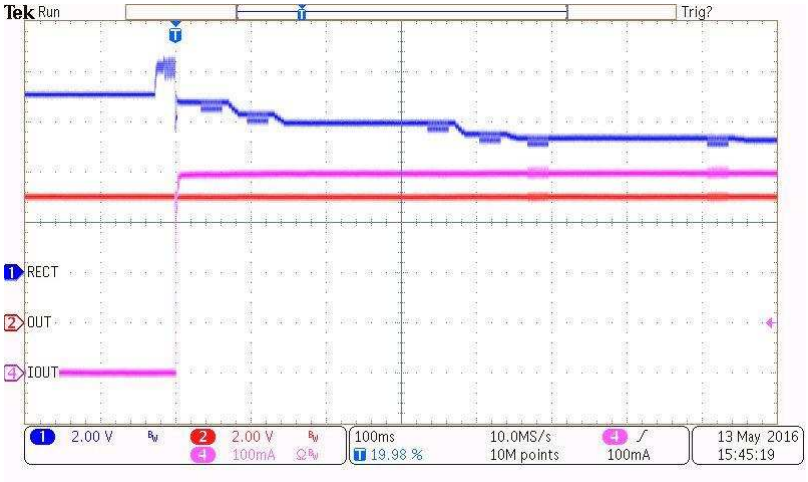


Figure 37. bq51003 – No Load to 400-mA Resistive Load

Typical Applications (continued)

9.2.2 Dual Power Path: Wireless Power and DC Input

This application discussion expands the bq51003 in a Qi-compliant system from the previous solution and adds a secondary DC input. The bq51003 reacts to the added power and disables wireless power transfer then passes the DC voltage. When the DC voltage is removed, the bq51003 reinitiates wireless power transfer then enables its OUT pin.

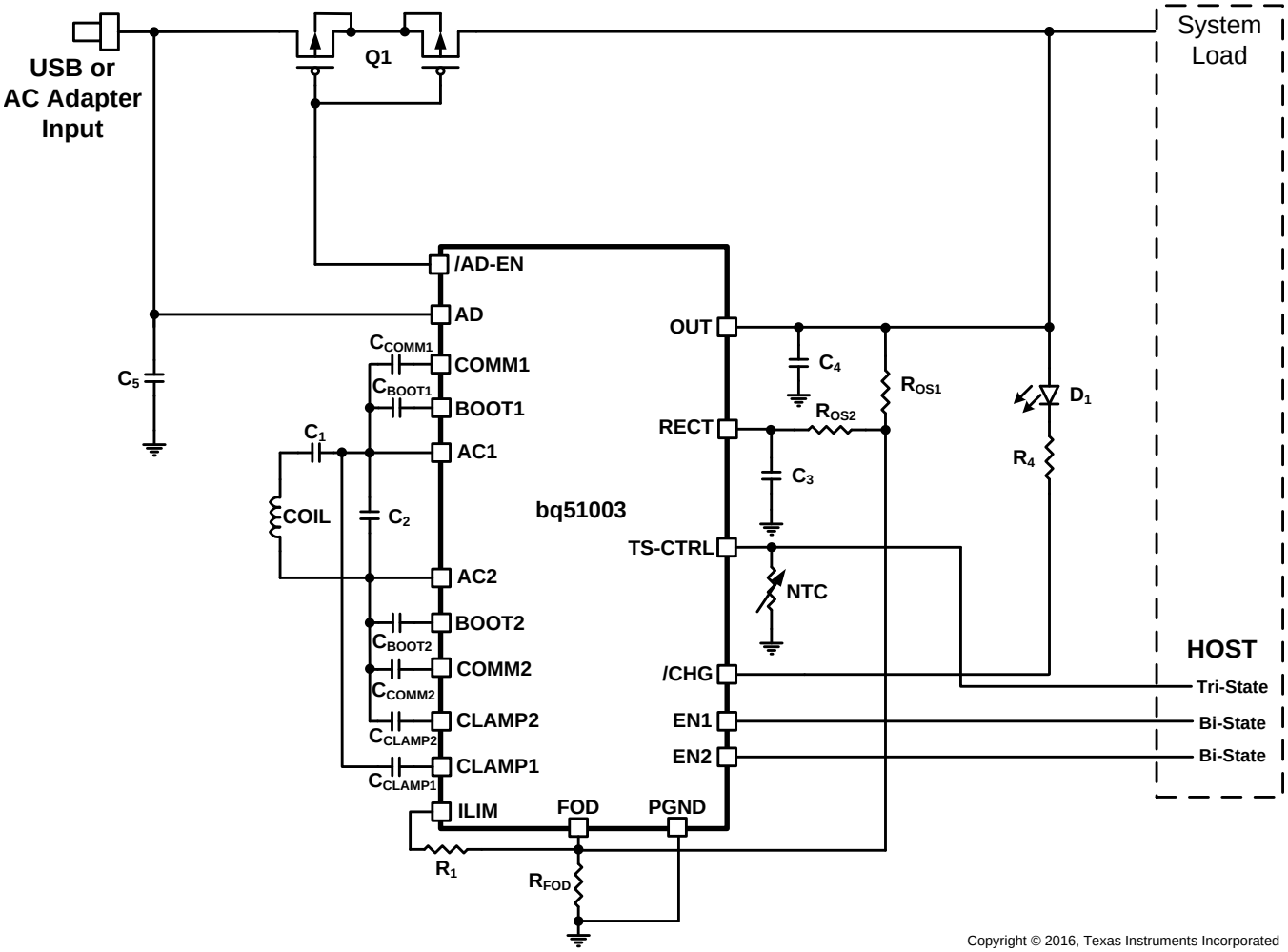


Figure 38. bq51003 Used as a Wireless Power Receiver and Power Supply for System Loads with Adapter Power-Path Multiplexing Only One of R_{OS1} or R_{OS2} Needed

9.2.2.1 Design Requirements

This solution adds the ability to disable wireless charging with the AD and $\overline{\text{AD\_EN}}$ pins. A DC supply (USB or AC adapter with DC output) can also be used to power the subsystem. This can occur during wireless power transfer or without wireless power transfer. The system must allow power transfer without any backflow or damage to the circuitry.

Typical Applications (continued)

9.2.2.2 Detailed Design Procedure

The basic components used in Figure 32 are reused here in Figure 38. The additional circuitry needed for source control will be discussed. Adding a blocking FET while using the bq51003 for control is the only addition to the circuitry. The AD pin will be tied to the DC input as a threshold detector. The AD_EN pin will be used to enable or disable the blocking FET. The blocking FET must be chosen to handle the appropriate current level and the DC voltage level supplied from the input. In this example, the expectation is that the DC input will be 5 V with a maximum current of 500 mA (same configuration as the wireless power supply). The CSD75207W15 is a good fit because it is a P-Channel, –20-V, 3.9-A FET pair in a 1.5-mm^2 WCSP.

9.2.2.3 Application Curves

The following figures show the bq51003EVM-764 when DC voltage is applied to the AD pin and when it is removed. The AD pin signal shows when the DC power is applied or removed. The AD_EN signal shows the response of to the added or removed power on the AD pin. The OUT pin signal shows the impact to the OUT pin during the AD addition or removal. IOUT shows the current being sourced by the OUT pin. The resistive load is set to produce 400 mA at 5 V. On both of the following plots, note the communication packets are not present when AD_EN is low.

Figure 39 shows the bq51003EVM-764 when a power source is added to the AD pin. The bq51003 disables the OUT pin then sets AD_EN to low which enables the CSD75207W15, passing the DC voltage to the load.

Figure 40 shows the response when the DC voltage is removed. Note the time after the removal before OUT is enabled which allows the bq51003 to communicate with the transmitter to get RECT back to the correct level.

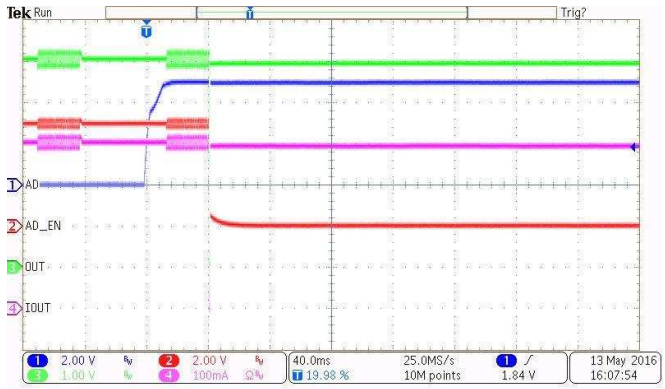


Figure 39. DC Voltage is Added at AD

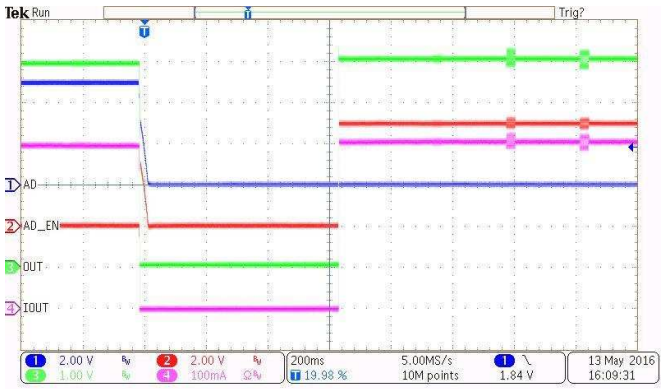


Figure 40. DC Voltage is Removed from AD

10 Power Supply Recommendations

The bq51003 requires a Qi-compatible transmitter as its power source.

11 Layout

11.1 Layout Guidelines

- Keep the trace resistance as low as possible on AC1, AC2, and BAT.
- Detection and resonant capacitors must be placed as close to the device as possible.
- COMM, CLAMP, and BOOT capacitors must be placed as close to the device as possible.
- Via interconnect on PGND net is critical for appropriate signal integrity and proper thermal performance.
- High-frequency bypass capacitors must be placed close to RECT and OUT pins.
- ILIM and FOD resistors are important signal paths and the loops in those paths to PGND must be minimized.

  Signal and sensing traces are the most sensitive to noise; the sensing signal amplitudes are usually measured in mV, which is comparable to the noise amplitude. Make sure that these traces are not being interfered by the noisy and power traces. AC1, AC2, BOOT1, BOOT2, COMM1, and COMM2 are the main source of noise in the board. These traces should be shielded from other components in the board. It is usually preferred to have a ground copper area placed underneath these traces to provide additional shielding. Also, make sure they do not interfere with the signal and sensing traces. The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components).

  For a 1-A fast charge current application, the current rating for each net is as follows:
  - AC1 = AC2 = 1.2 A
  - OUT = 500 mA
  - RECT = 100 mA (RMS)
  - COMMx = 300 mA
  - CLAMPx = 500 mA
  - All others can be rated for 10 mA or less

11.2 Layout Example

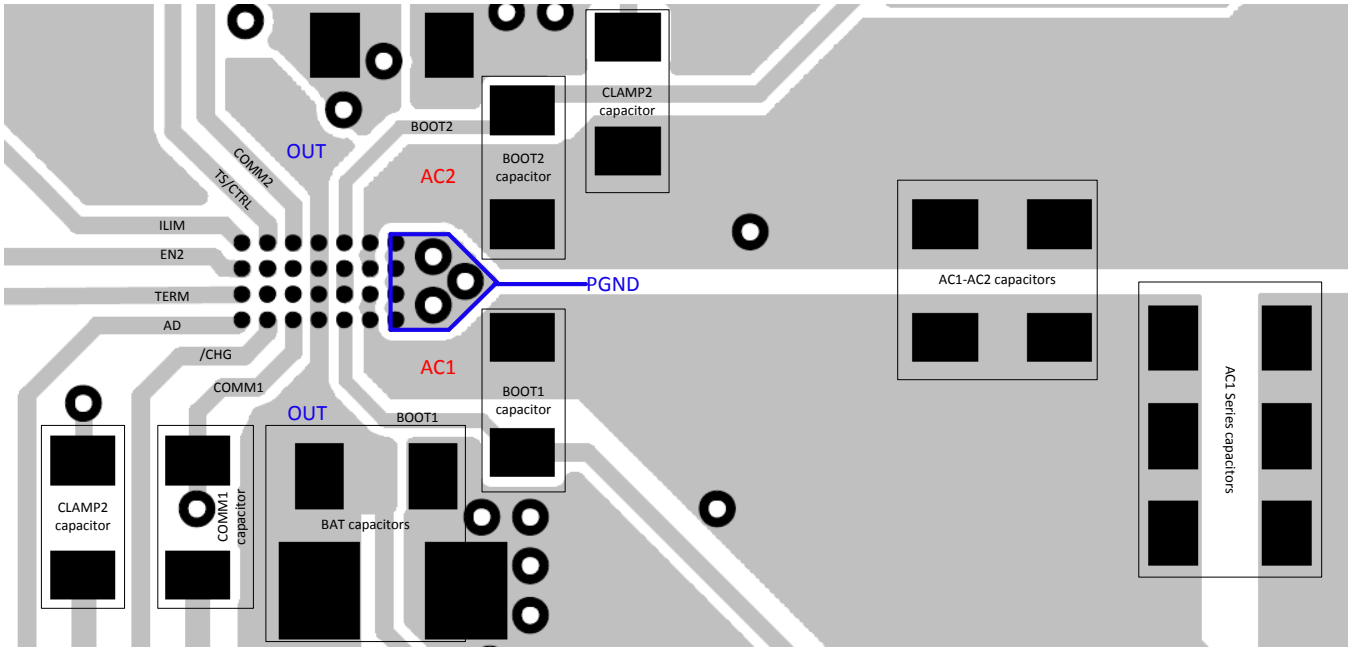


Figure 41. bq51003 Layout Schematic

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

相关开发支持，请参见以下文档：

- *适用于低功耗可穿戴应用且符合 Qi (WPC) 标准的 TIDA-00318 无线 充电器*
- *适用于低功耗可穿戴应用的 TIDA-00329 微型无线 接收器 参考设计*
- *TIDA-00712 智能手表电池管理解决方案参考设计*
- *TIDA-00668 50mA 无线充电器 Booster Pack 参考设计*
- *TIDA-00881 50mA 无线充电器 BoosterPack 参考设计（带有 19mm 线圈）*
- *适用于通过 bq51003 和 bq25120 进行无线充电的可穿戴设备的 PMP11311 电源参考设计*

12.2 接收文档更新通知

如需接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ51003YFPR	ACTIVE	DSBGA	YFP	28	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ51003	Samples
BQ51003YFPT	ACTIVE	DSBGA	YFP	28	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ51003	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

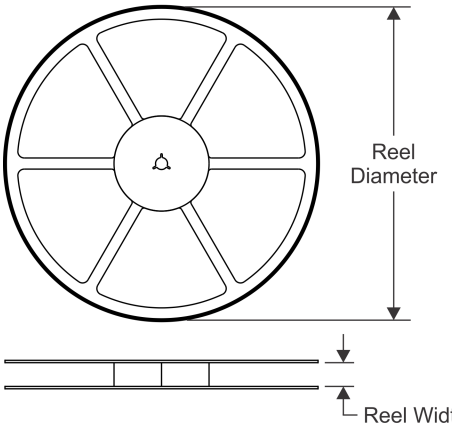
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

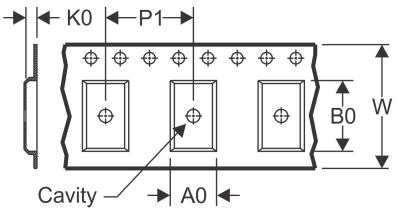
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

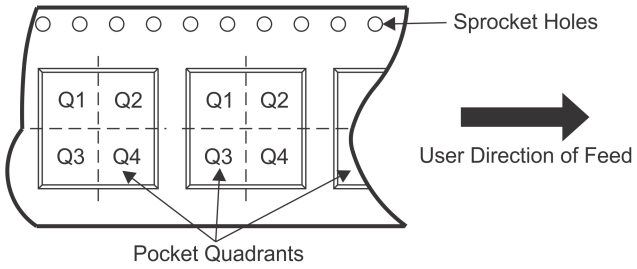


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

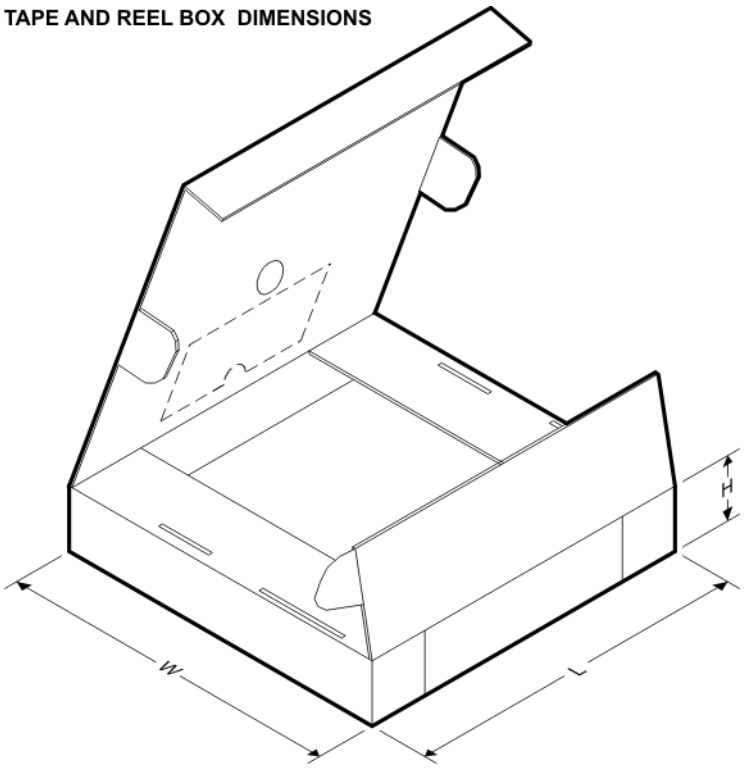
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ51003YFPR	DSBGA	YFP	28	3000	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1
BQ51003YFPT	DSBGA	YFP	28	250	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1

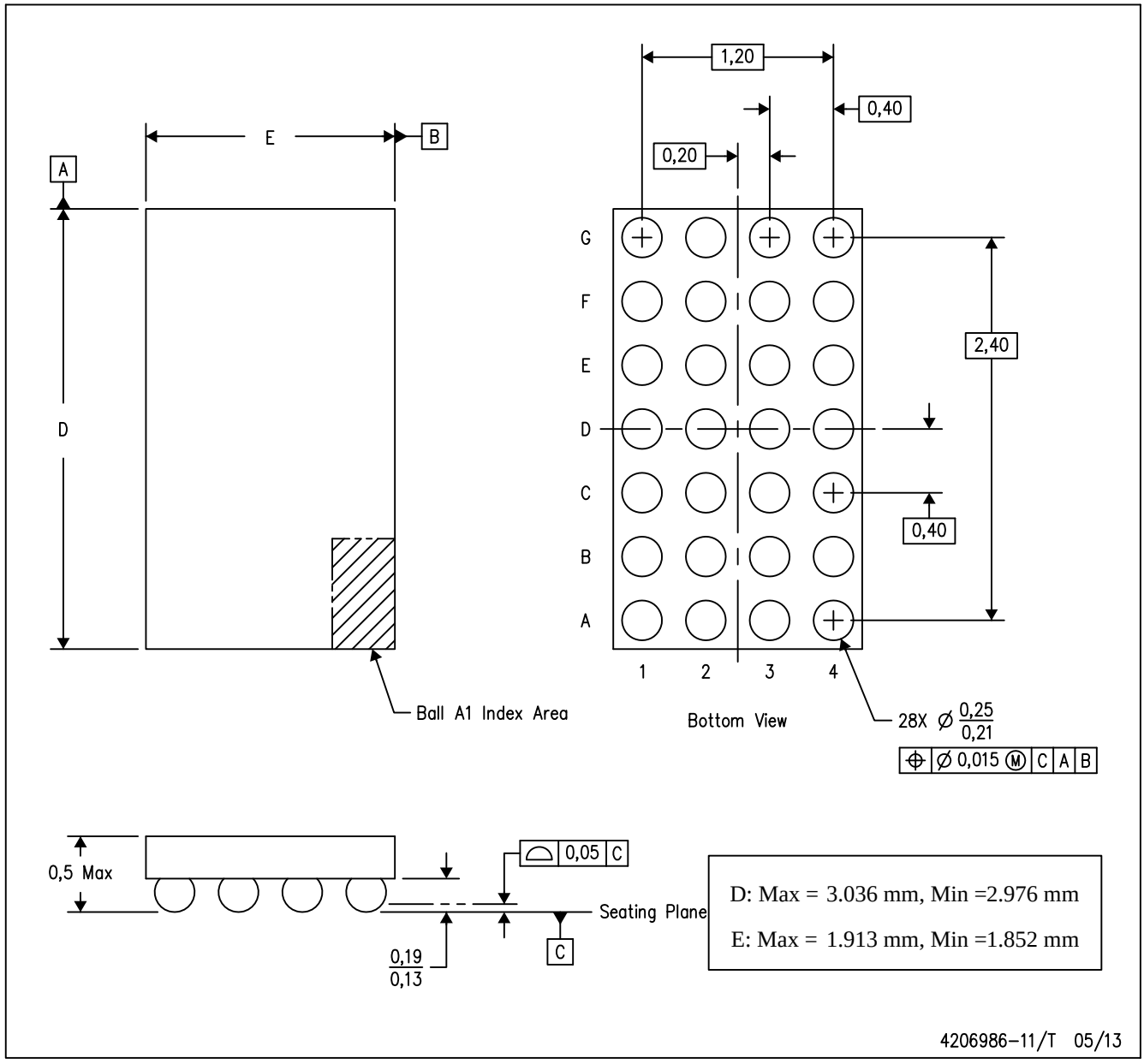
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ51003YFPR	DSBGA	YFP	28	3000	182.0	182.0	20.0
BQ51003YFPT	DSBGA	YFP	28	250	182.0	182.0	20.0

YFP (R–XBGA–N28) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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