Application Report
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Understanding Smart Gate Drive

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ABSTRACT

The gate driver in a motor system design is an integrated circuit (IC) that primarily deals with enhancing external power MOSFETs to drive current to a electric motor. The gate driver acts as an intermediate stage between the logic-level control inputs and the power MOSFETs. The gate driver must be robust and flexible enough to accommodate a wide variety of external MOSFET selections and external system conditions.

Texas Instrument's Smart Gate Drive provides an intelligent solution for driving and protecting the external power MOSFETs. This feature lets system designers adjust the MOSFET slew rate, optimize switching and EMI performance, decrease bill of materials (BOM) count, automatically generate dead-time, and provide additional protection for the external power MOSFETs and motor system.

This application report describes the theory and methods behind enhancing a power MOSFET, how the IDRIVE and TDRIVE features are implemented in TI Smart Gate Drivers, and details many of the system-level benefits.

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1 Power MOSFET Theory and Operation

1.1 Basics

The metal-oxide-semiconductor field-effect transistor, or MOSFET, is the most common transistor used in present-day electronic-circuit design. The MOSFET has many properties that make it useful in a variety of applications. These properties include scalability, low turnon current, high switching speeds, and high OFF-state impedance. The MOSFET has been used in IC design (analog and digital), switching power applications, motor control, load switches, and numerous other designs.

The MOSFET consists of four terminals which include the drain (D), source (S), gate (G), and body (B) as show in Figure 1. Often, the body terminal is short-circuited to the source terminal making it a three terminal device.

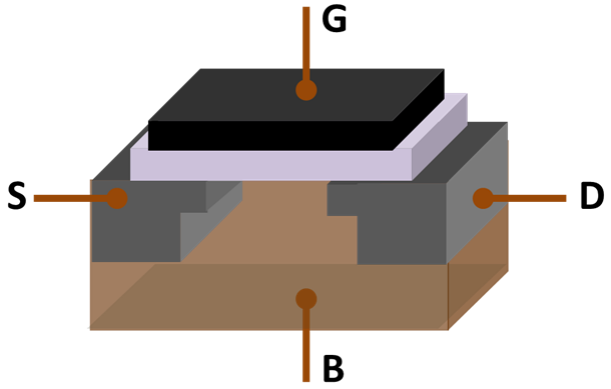

Figure 1. MOSFET Model

The MOSFET has three basic regions of operation that can be defined with a few simple equations. These regions and their corresponding equations are listed as follows:

- Cutoff

  $V_{GS} \leq V_{th}$

  where

  - V_{GS} = Voltage between the gate and source terminals of the MOSFET
  - V_{th} = MOSFET threshold voltage (1)

- Linear

  $V_{GS} > V_{th}$, $V_{DS} \leq V_{GS} - V_{th}$

  where

  - V_{DS} = Voltage between the drain and source terminals of the MOSFET (2)

- Saturation

  $V_{GS} > V_{th}$, $V_{DS} > V_{GS} - V_{th}$ (3)

In the cutoff region, the MOSFET is OFF and no conduction occurs between the drain and the source. In the linear region, the MOSFET is ON and the MOSFET behaves similar to a resistor controlled by the gate voltage with respect to both the source and drain voltages. In the saturation region, the MOSFET is ON and behaves similar to a current source controlled by the drain and gate-to-source voltages.

1.2 Parameters

Figure 2 shows a common MOSFET model highlighting the terminal-to-terminal capacitances and gate resistance.

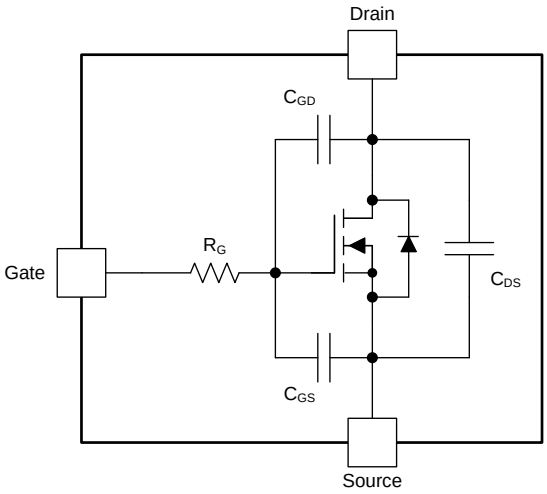

Figure 2. MOSFET Circuit Model

While the C_{GS} capacitance is fairly constant, the C_{GD} and C_{DS} capacitances vary heavily with the gate-to-drain voltage, drain-to-source voltage, and applied frequency. Table 1 lists some typical data sheet parameters of a power-MOSFET. Review these values to understand how they affect the switching performance of the MOSFET.

Table 1. MOSFET Data Sheet Parameters (CSD18532Q5B)

Parameter		Test Conditions	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		3900	5070	pF
C_{oss}	Output capacitance			470	611	pF
C_{rss}	Reverse transfer capacitance			13	17	pF
R_G	Series gate resistance			1.2	2.4	Ω
Q_g	Gate charge total (10 V)	V_{DS} = 30 V, I_D = 25 A		44	58	nC
Q_{gd}	Gate charge gate-to-drain			6.9		nC
Q_{gs}	Gate charge gate-to-source			10		nC
$Q_{g(th)}$	Gate charge at V_{th}			6.3		nC
Q_{oss}	Output charge	V_{DS} = 30 V, V_{GS} = 0 V		52		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 25 A, R_G = 0 Ω		5.8		ns
t_r	Rise time			7.2		ns
$t_{d(off)}$	Turnoff delay time			22		ns
t_f	Fall time			3.1		ns

The capacitors and resistor are defined as follows:

C_{ISS} — A measure of the input capacitance between the gate and source terminals with the drain and source shorted ($C_{ISS} = C_{GS} + C_{GD}$).

C_{OSS} — A measure of the output capacitance between the drain and source terminals with the gate and source shorted ($C_{OSS} = C_{DS} + C_{GD}$).

C_{RSS} — The reverse transfer capacitance measured between the drain and gate terminals with the source connected to ground ($C_{RSS} = C_{GD}$).

R_G — The series resistance in line with the gate terminal.

To account for variation in the capacitance value with respect to voltage, a gate charge curve is typically used to provide more meaningful information. Gate charge values relate to the charge stored within the inter-terminal capacitances. Gate charge is more useful for system designers because it takes into account the changes in capacitance with respect to voltage during a switching transient.

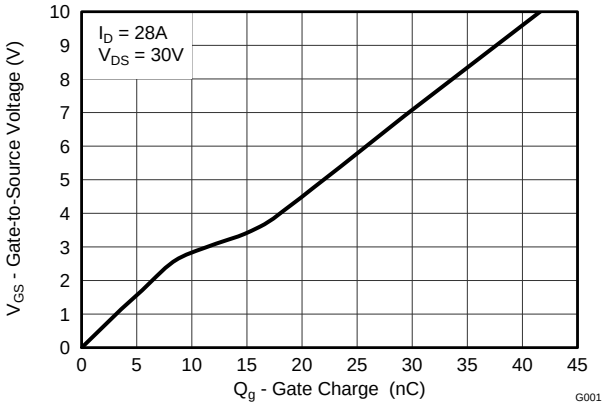

Figure 3. MOSFET Gate-Charge Curve

The gate charge parameters are defined as follows:

Q_G — The total gate charge required to raise the gate-to-source voltage to the specified value (4.5 V and 10 V are commonly used voltages).

$Q_{G(th)}$ — The charge required from 0 V to the threshold voltage of the MOSFET. Current will start to flow from the drain to the source at the threshold voltage.

Q_{GS} — The charge required from 0 V to the Miller plateau voltage. At the plateau voltage the drain to source voltage will start to slew.

Q_{GD} — The charge required to move through the Miller region. The Miller region derives its name from the fact that the gate-to-source voltage stays relatively constant during this period as the reverse transfer capacitance is charged. The MOSFET V_{DS} slew occurs during this period as the MOSFET becomes enhanced.

1.3 Turnon Behavior

Based on the information provided in Section 1.2, a specific amount of charge is required to bias the gate to a certain voltage. Using these parameters, how the MOSFET behaves when certain voltages and currents are applied to it becomes clearer. Figure 4 shows the typical turnon response of a MOSFET.

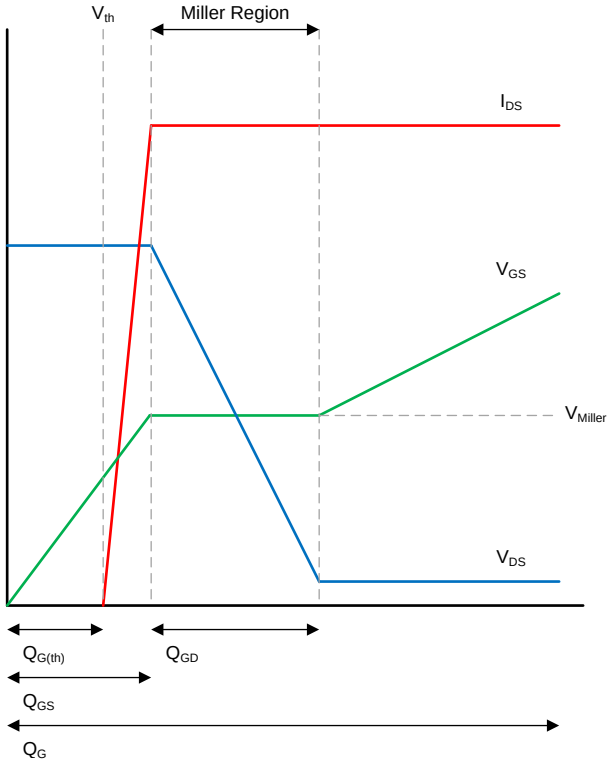

Figure 4. MOSFET Turnon Response

The curve starts with the gate-to-source voltage increasing as a charge is supplied to the gate. When the gate-to-source voltage reaches the MOSFET threshold voltage, current starts to flow from the drain to the source. The gate-to-source voltage then stays fairly steady as the MOSFET moves through the Miller region. During the Miller region, the drain-to-source voltage drops. After the Miller region, the gate continues to charge until it reaches the final drive voltage.

1.4 Simple Slew-Rate Calculation

Unfortunately, calculating precise MOSFET V_{DS} slew rates from parameters and equations requires specific knowledge of the MOSFET, the board and package parasitics, and detailed information on the gate drive circuit. These calculations go beyond the scope of this document. This document just focuses on simple first order approximations that are compared to lab data.

Because the MOSFET V_{DS} slew occurs during the Miller region, the Miller charge (Q_{GD}) and gate drive strength can be used to approximate the slew rate. The first assumption that should be made is that an ideal, or close to ideal, constant-current source is being used for the MOSFET gate drive.

1.4.1 Example

Figure 5 shows a DRV8701 Smart Gate Driver driving a CSD18532Q5B at 24 V. The DRV8701 device is configured for the 25-mA source-current setting. The waveform shows an approximately 312-ns slew rate which matches closely with the first order approximation calculated using Equation 4.

$$t_{SLEW} = \frac{Q_{GD}}{I_{SOURCE}}$$

$$t_{SLEW} = \frac{6.9\ nC}{25\ mA} = 276\ ns$$

where

- Q_{GD} = 6.9 nC
- I_{SOURCE} = 25 mA (4)

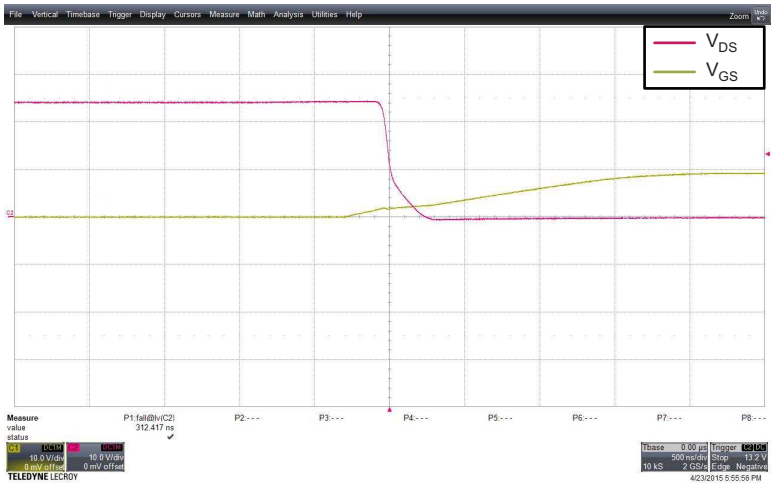

Figure 5. Measured MOSFET Slew Rate

1.5 Gate Drive Current

Two key current parameters should be examined when designing a switching power-MOSFET system such as a motor driver. These parameters are the peak gate drive current and average gate drive current.

1.5.1 Peak Gate Drive Current

The peak gate drive current is the peak current that the gate driver can source or sink to the power MOSFET gate during the turnon and turnoff periods. This value is primarily responsible for how fast the MOSFET can slew.

1.5.1.1 Example

The DRV8701 supports a peak source current of 150 mA and a peak sink current of 300 mA. Using the example from Section 1.4.1, a rise and fall time can be calculated using Equation 5 and Equation 6 (respectively).

$$t_{RISE} = \frac{Q_{GD}}{I_{SOURCE}}$$

$$t_{RISE} = \frac{6.9\ nC}{150\ mA} = 46\ ns$$

where

- Q_{GD} = 6.9 nC
- I_{SOURCE} = 150 mA (5)

$$t_{FALL} = \frac{Q_{GD}}{I_{Sink}}$$

$$t_{FALL} = \frac{6.9\ nC}{300\ mA} = 23\ ns$$

where

- Q_{GD} = 6.9 nC
- I_{SINK} = 300 mA (6)

1.5.2 Average Gate Drive Current

The average gate drive current is the average current required from the gate driver when switching the power MOSFETs constantly. As previously described, the amount of charge to switch a power MOSFET is small (44 nC), but when switching the MOSFET in the kHz range, this charge will average into a constant current draw from the gate driver supply.

Use Equation 7 to calculate the average gate drive current.

$$I_{AVG} = Q_G \times \#\ MOSFETs\ Switching \times Switching\ Frequency \quad (7)$$

1.5.2.1 Example

$$I_{AVG} = 44\ nC \times 6 \times 45\ kHz = 11.88\ mA \quad (8)$$

2 Smart Gate Driver Parameters: IDRIVE and TDRIVE

2.1 IDRIVE Implementation

As described in the previous section, precisely controlling the current applied to the MOSFET gate lets the user make a reasonable calculation for and adjust the MOSFET V_{DS} slew rate. This feature is valuable for power-stage design and several system-level benefits are expanded upon in Section 3.

Texas Instruments Smart Gate Drivers incorporate an adjustable gate drive current scheme in many of the motor gate drivers to easily control the MOSFET slew rate. The adjustable gate drive current parameter is called IDRIVE. This section describes how IDRIVE is commonly setup and implemented.

The most commonly implemented method is shown in Figure 6. In this method, a MOSFET predriver switch is enabled between the gate and the voltage supply to manage the current directed to the external power MOSFET gate.

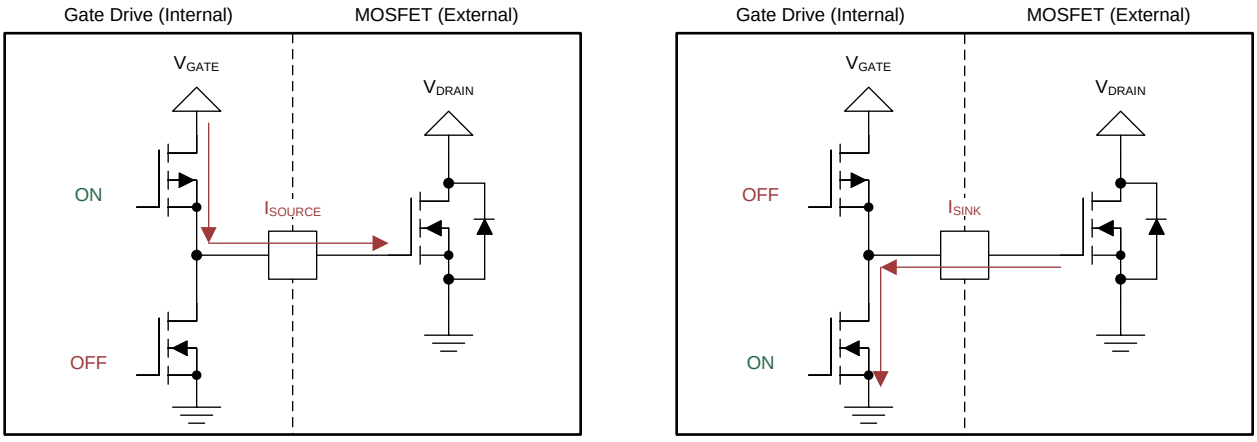

Figure 6. Switch IDRIVE Method

To control the current to the gate of the external MOSFET during the V_{DS} slew, the Smart Gate Driver takes advantage of several MOSFET properties. If the switch (predriver MOSFET) can be operated in the saturation region (Section 1.1), the current to the external MOSFET is limited to a fixed value. As the external MOSFET moves through the Miller region, the gate-to-source voltage plateaus and stays relatively constant (Section 1.3).

Using these two properties, the Smart Gate Driver can make sure the correct voltage bias is applied to the gate of the predriver switch and the switch is in the saturation region for the duration of the Miller charging period. Because the gate of the external MOSFET appears as a short (AC voltage applied to a capacitance) the source or sink current is limited to the saturation current of the switch.

By using multiple switches (shown in Figure 7), the Smart Gate Driver can alternate between different current levels during normal operation.

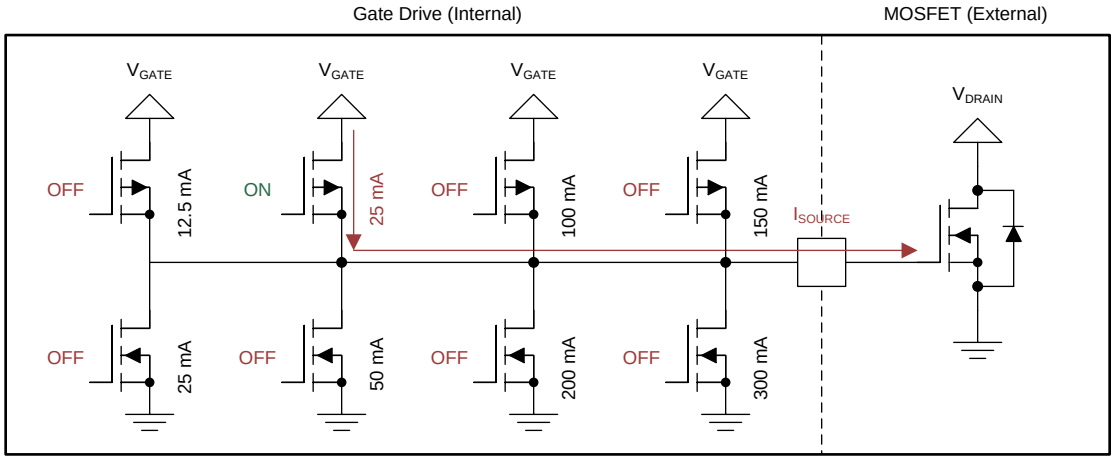

Figure 7. Multiple IDRIVE Settings

The second method to implement the IDRIVE feature uses current sources instead of switches. This implementation occurs in applications that require very precise and consistent control of the external MOSFET V_{DS} slew rate across device, voltage, and temperature. While a switch in saturation can be sized appropriately to act as a simple current source, a variation still exists across the previously described factors. To remove this variation, a current source is used in place of the switch (see Figure 8). This architecture is especially important in applications that are EMI sensitive and depend on characterizing the system at a specific slew rate.

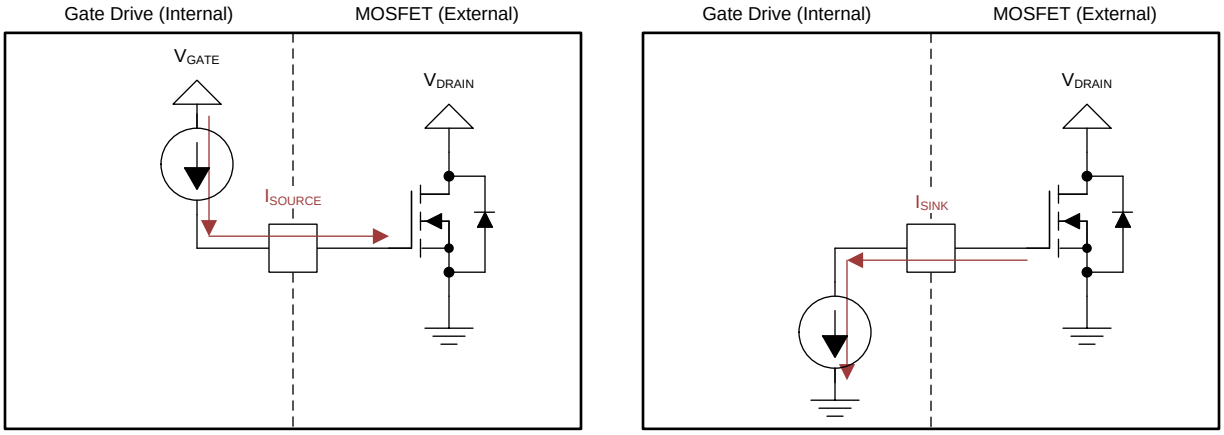

Figure 8. Current Source IDRIVE Method

Similar to the switch method (Figure 7), multiple current sources can be used to provide adjustable gate drive levels.

2.2 TDRIVE Implementation

In addition to the IDRIVE slew-rate control, TI Smart Gate Drivers also implement the TDRIVE feature. TDRIVE consists of an internal gate drive state machine that optimizes the dead time between high-side and low-side switching, protects against dV/dt turnon, and monitors for excessive current to the MOSFET gate. The state machine allows for the design of a robust, protected, and efficient motor drive system with minimal external overhead.

This section describes the various components of the TDRIVE state machine and how they are implemented.

2.2.1 MOSFET Handshaking

The IDRIVE state machine incorporates internal handshaking when switching from the low-side to high-side (or high-side to low-side) external MOSFET. The handshaking is designed to prevent the external MOSFETs from going to a period of cross conduction, also known as shoot-through.

Cross conduction (shown in Figure 9) occurs when both the high-side and low-side MOSFET are enabled at the same time. A low impedance path is introduced between the power supply and ground. The path lets large current flow, potentially damaging the external MOSFETs or power supply.

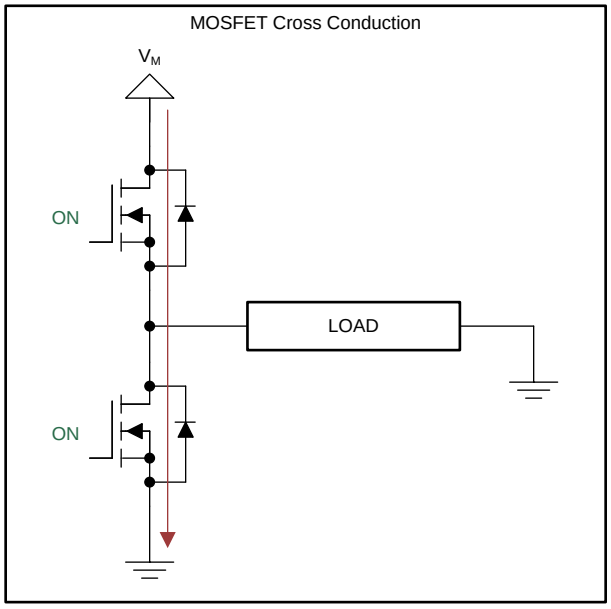

Figure 9. Cross Conduction Example

Cross conduction, or shoot-through, most commonly occurs when switching from the low-side to high-side (or high-side to low-side). A delay occurs from when the input signal is received to when the external MOSFET is off related to the internal propagation delay and slew rate of the MOSFET. If the opposite MOSFET is enabled before this delay period expires, cross conduction can occur. A simple method to prevent this issue is to add a period of timing before enabling the opposite MOSFET (shown in Figure 10). This period of time is called dead time. Increased dead time decreases the efficiency of the motor driver because of diode conduction losses.

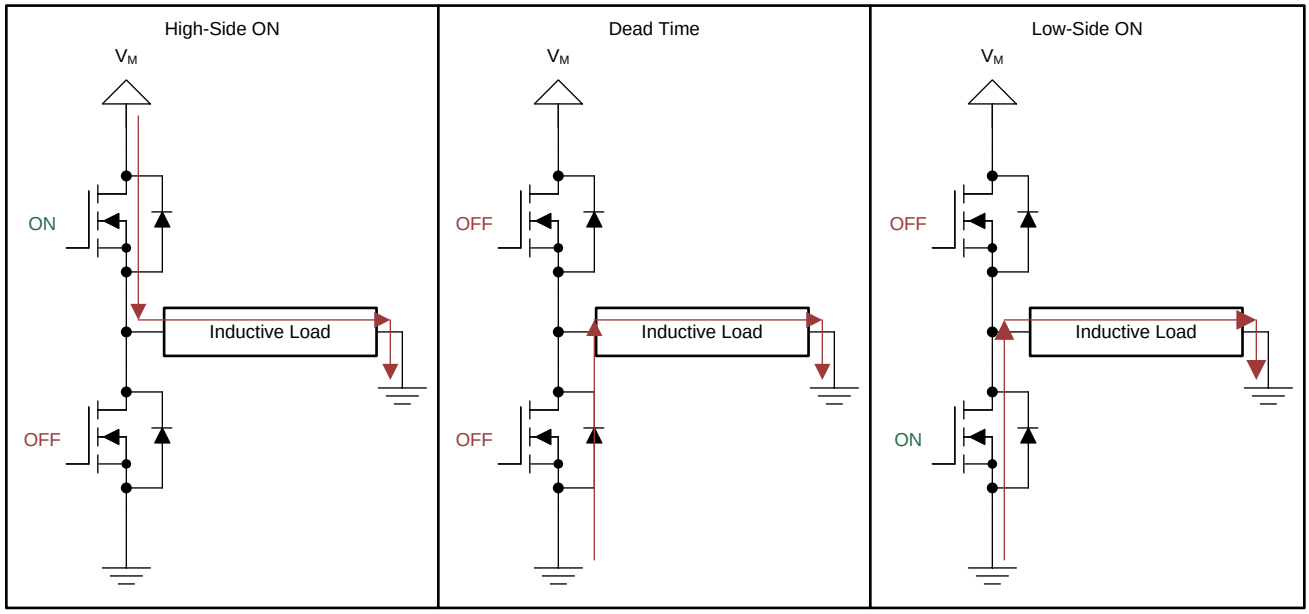

Figure 10. Dead Time Example

The internal handshaking uses V_{GS} monitors of the external MOSFETs (Figure 11) to determine when one MOSFET has been disabled and the other can be enabled. This handshaking lets the system insert an optimized dead time into the system without the risk of cross conduction.

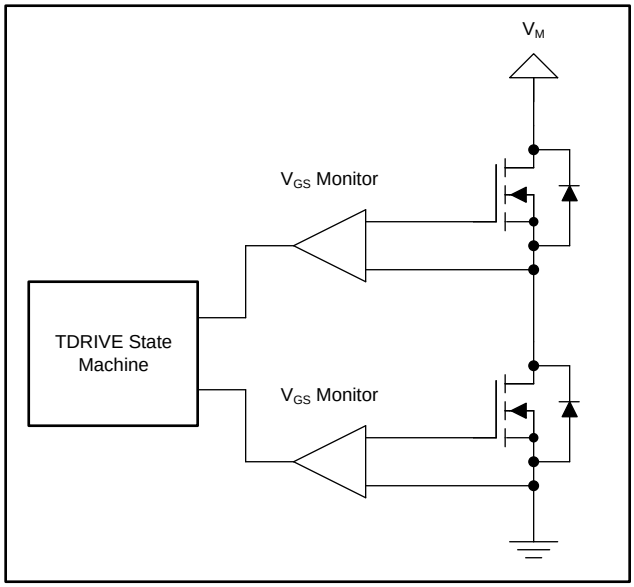

Figure 11. V_{GS} Monitor Example

2.2.2 Gate Drive Timer

The TDRIVE gate drive timer makes sure that under abnormal circumstances, such as a short on the MOSFET gate or the inadvertent turning on of a MOSFET V_{GS} clamp, the high peak current through the Smart Gate Driver and MOSFET gate is limited to a fixed duration. Figure 12 shows this concept which is outlined as follows:

1. The Smart Gate Driver receives a command to enable the MOSFET gate.
2. A strong current source is then applied to the external MOSFET gate and the gate voltage starts to rise.
3. If the gate voltage has not increased after the t_{DRIVE} period (indicating a short circuit or overcurrent condition on the MOSFET gate), the Smart Gate Driver signals a gate drive fault and the gate drive is disabled to protect the external MOSFET and gate driver.
4. If a gate drive fault does not occur, the Smart Gate Driver enables a small current source after the T_{DRIVE} period to keep the correct gate voltage and decrease internal current consumption.

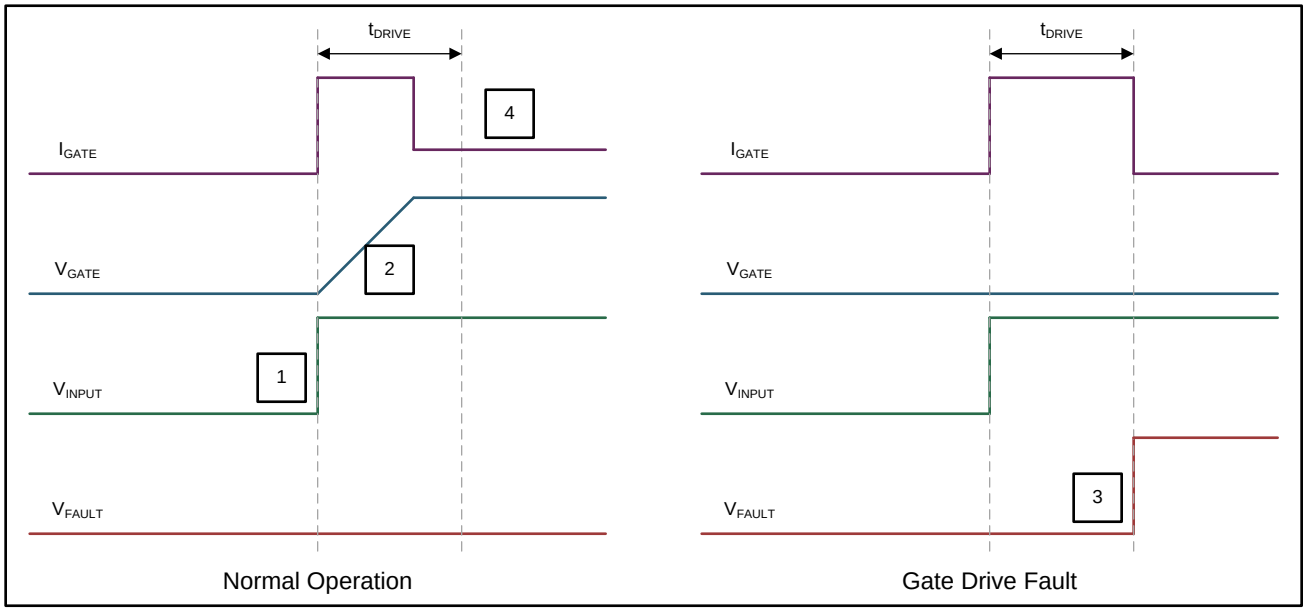

Figure 12. TDRIVE Example

2.2.3 Strong Gate Pulldown

In addition to the cross conduction and gate overcurrent protection features, the internal TDRIVE state machine also provides a mechanism for preventing dV/dt turnon.

A dV/dt turnon is a system issue that can occur when rapidly slewing the high-side MOSFET. When the switch node rapidly slews from low to high (Figure 13), it can couple into the gate of the low-side MOSFET through the parasitic gate-to-drain capacitance (C_{GD}). The coupling can raise the gate-to-source voltage of the low-side MOSFET and enable the MOSFET if the voltage crosses the MOSFET threshold voltage (V_{th}). If the low-side MOSFET enables while the high-side MOSFET is on, cross conduction occurs.

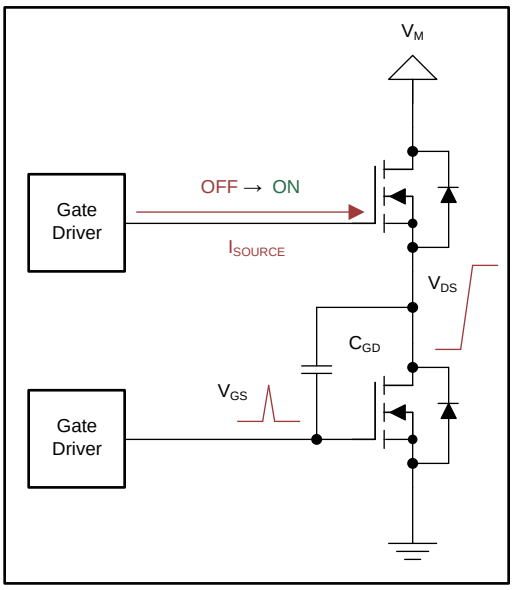

Figure 13. dV/dt Example

To protect against this scenario, the TDRIVE state machine of the Smart Gate Driver enables a strong gate pulldown on the low-side MOSFET while the high-side MOSFET is slewing (Figure 14). The pulldown provides a path for the charge that couples into the MOSFET gate.

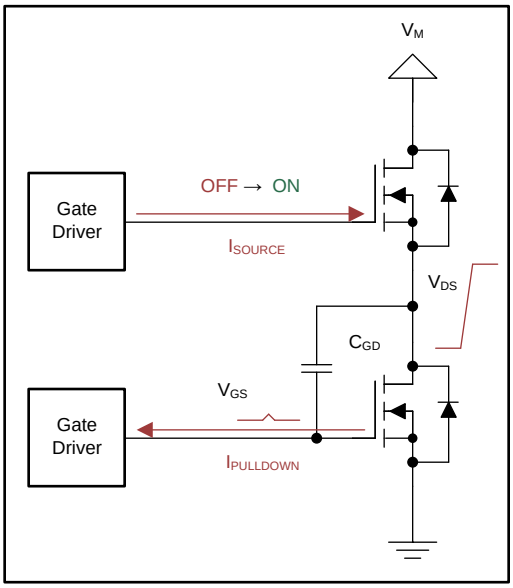

Figure 14. TDRIVE Pulldown

3 System Benefits

The IDRIVE and TDRIVE features of the Smart Gate Driver provide a more efficient, flexible, and robust motor gate driver solution. This section focuses specifically on key system benefits that these features deliver.

3.1 Slew Rate Control

The IDRIVE feature lets the V_{DS} slew rate to be adjusted at any time without adding or removing external components to the system. This capability lets a system designer fine tune the switching performance of the MOSFET with regards to efficiency, radiated emissions performance, diode recovery inductive spikes, and dV/dt turnon.

The persistence plot (Figure 15) shows the effect on the V_{DS} slew rate from adjusting the IDRIVE setting on a TI Smart Gate Driver. The MOSFET V_{DS} is slewing from 24 V to 0 V and the slew rate decreases as IDRIVE is adjusted across seven levels (10 mA, 20 mA, 30 mA, 40 mA, 50 mA, 60 mA, and 70 mA) of gate source current.

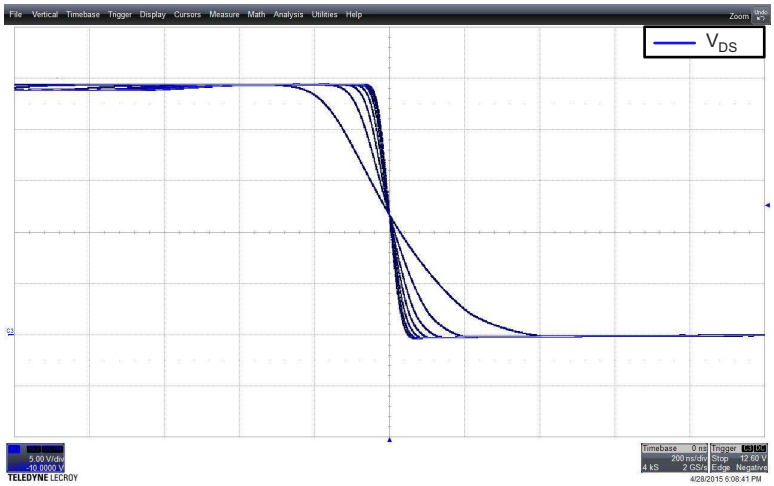

Figure 15. V_{DS} Persistence Plot Across IDRIVE Settings

The following figures show additional signals of the MOSFET while it is being enhanced. The current from the Smart Gate Driver and the Miller region of the external MOSFET is clearly shown when the V_{DS} slews.

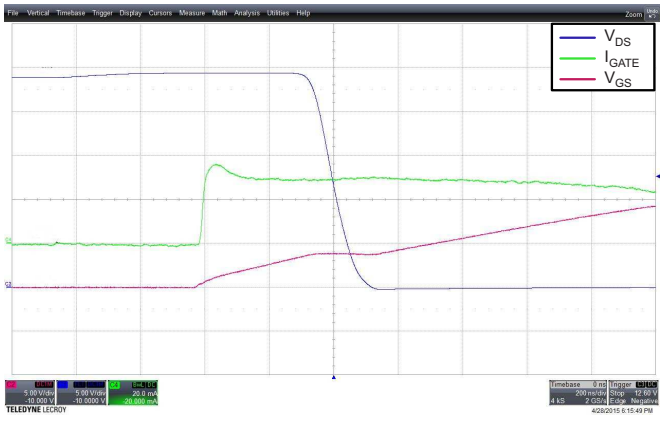

Figure 16. IDRIVE 30-mA Setting

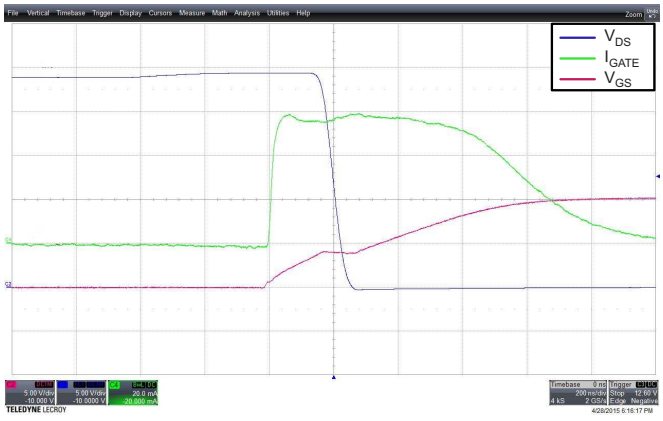

Figure 17. IDRIVE 60-mA Setting

As mentioned in Section 1.4, if a close-to-ideal current source and an accurate MOSFET Q_{GD} parameter are available, an approximate calculation for the V_{DS} slew rate can be made. In Equation 9, the calculated V_{DS} slew rate is compared to the measured V_{DS} slew rate for several IDRIVE settings. In these calculations, assume that the effects of the series gate resistance and additional non-idealities are minimal.

$$t_{SLEW} = Q_{GD} / I_{SOURCE} \quad (9)$$

Table 2. IDRIVE Slew-Rate Correlation

MOSFET Q_{GD} Typical (nC)	IDRIVE Setting (mA)	Calculated Slew Rate (ns)	Measured Slew Rate (ns)	Approximate Error (%)
8	10	800	617	23
8	20	400	305	24
8	30	267	206	23
8	40	200	158	21
8	50	160	128	20
8	60	133	109	18
8	70	114	97	15

Although some error exists from the ideal calculation, these values let a system designer design for an approximate slew rate and then finely tune the system during prototyping. The accuracy of the MOSFET Q_{GD} plays a large part in the accuracy of the calculation.

The following scope plots are for the measurements listed in Table 2.

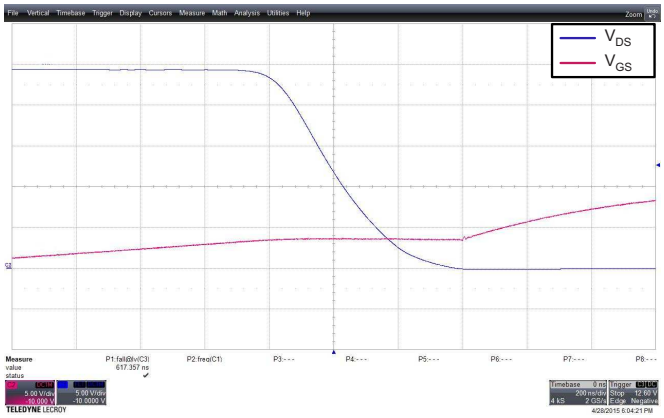

Figure 18. 10-mA IDRIVE

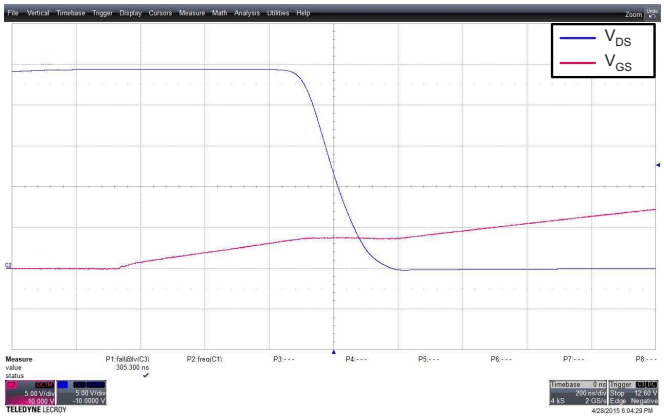

Figure 19. 20-mA IDRIVE

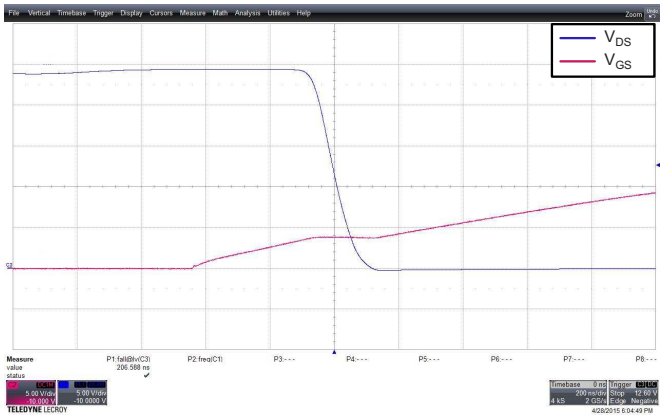

Figure 20. 30-mA IDRIVE

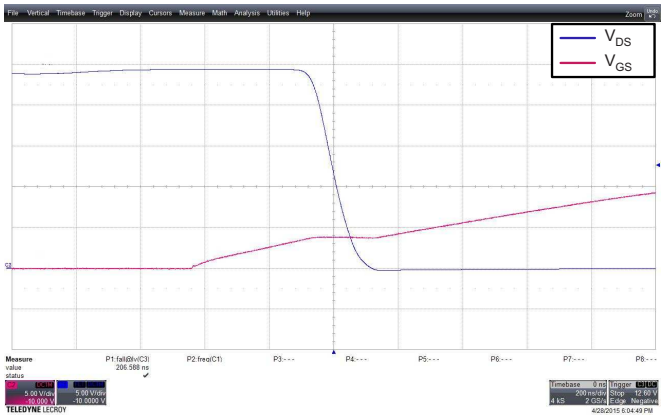

Figure 21. 40-mA IDRIVE

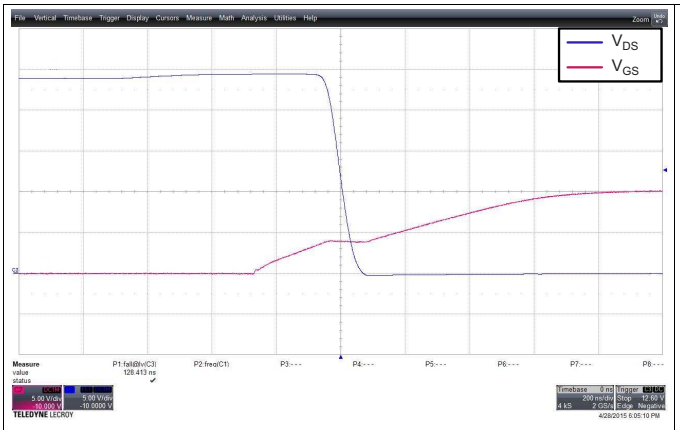

Figure 22. 50-mA IDRIVE

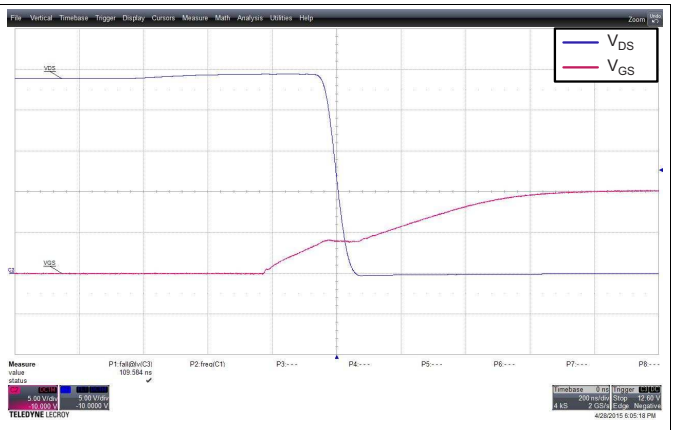

Figure 23. 60-mA IDRIVE

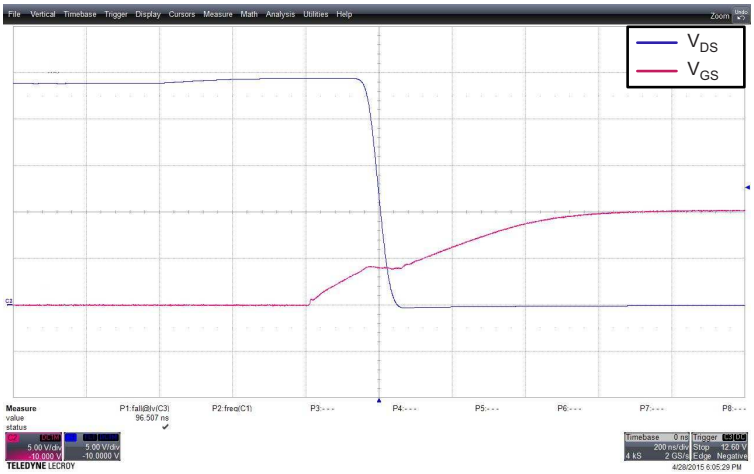

Figure 24. 70-mA IDRIVE

3.2 BOM Reduction

In addition to system flexibility, a Smart Gate Driver provides the ability to decrease the system BOM and required board area. Figure 25 shows a typical configuration for driving a power MOSFET.

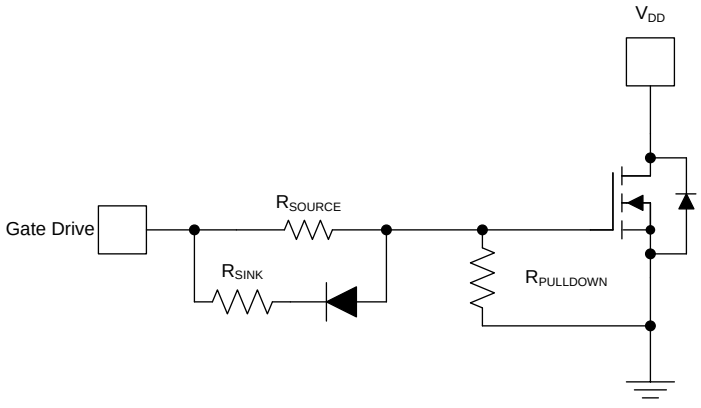

Figure 25. Typical Gate Driver Configuration

The R_{SOURCE} and R_{SINK} resistors manually adjust the impedance between the gate driver and MOSFET gate. The diode lets the rise and fall V_{DS} slew rates to be individually adjusted. The $R_{PULLDOWN}$ resistor makes sure that the MOSFET stays disabled even when the gate driver is inactive.

The IDRIVE and TDRIVE features of the Smart Gate Driver remove the requirement for up to 24 passive components for controlling slew rate and gate pulldown in a triple half-bridge design.

3.3 System Protection

Lastly, the TDRIVE state machine provides additional system protection through intelligently driving the external power MOSFETs.

3.3.1 Switching Protection and Dead-Time Optimization

As described in Section 2.2, by monitoring the MOSFET V_{GS} voltage, the Smart Gate Driver can provide an optimized amount of dead time for the switching MOSFET system. The V_{GS} monitors make sure the opposite MOSFET in the half-bridge is disabled before enabling the commanded MOSFET.

In addition to cross conduction protection (shoot-through), this method can provide system performance benefits by reducing the period of diode conduction. Conduction losses of the MOSFET internal body diode are typically worse than standard MOSFET conduction losses and decrease the overall system efficiency.

3.3.2 dV/dt Turnon Prevention

The TDRIVE state machine works to prevent dV/dt turnon which can lead to cross conduction in the external half-bridge. By enabling a strong pulldown on the low-side MOSFET during high-side V_{DS} slew, the Smart Gate Driver can provide a low-impedance path for parasitic charge that couples through the parasitic capacitance of the low-side MOSFET gate to drain capacitance (C_{GD}). This impedance path prevents a rise in the gate-to-source voltage of the low-side MOSFET, which could potentially enable the MOSFET while it is supposed to be off.

The TDRIVE state machine disables the strong pulldown after the switching period and moves to a weak pulldown to decrease the chance of damage to the Smart Gate Driver or system in the scenario of a gate-to-drain short of the external low-side MOSFET. By limiting the period of high current, the Smart Gate Driver can prevent damage to itself and limit further damage to the system.

3.3.3 MOSFET Gate-Fault Detection

In addition to the slew rate flexibility provided with IDRIVE, the TDRIVE state machine lets the Smart Gate Driver detect fault conditions on the gate of the external MOSFET.

By monitoring the voltage and managing the current to the external power MOSFET, the Smart Gate Driver can detect and report when an abnormal event (partial short, short circuit) has occurred on the MOSFET gate. Additional information is provided in Section 2.2.

3.4 EMI Optimization

One of the leading contributors to electromagnetic interference, also known as EMI, is high frequency noise from the switching of the power MOSFETs. Ideally the square-voltage waveforms generated by the power stage are clean ground-to-supply signals, but this is seldom the case. Parasitics in the MOSFET package and PCB layout can cause undershoot and overshoot voltages that can ring on the switching output. This parasitic ringing can occur at frequencies much greater than 1 MHz, often directly in sensitive spectrum bands. Additionally, the fundamental edge rate of the MOSFET switching can translate into noise in the high frequency spectrum.

While these parasitics can be tackled with layout improvements, snubbers, and design enhancements, often the key knob to tune is the switching speed of the power MOSFETs. IDRIVE provides an ideal way to tune the motor gate drive system by providing simple control of the MOSFET slew rate through either a register write or one resistor setting which lets system designers select the optimal setting that minimizes efficiency losses while keeping an acceptable EMI level.

The data listed in Table 3 is an example from an actual application of the Smart Gate Driver IDRIVE feature. Table 3 shows the peak readings from a CISP 25 EMI engineering scan from 30 to 200 MHz with a Smart Gate Driver at different IDRIVE settings. As the IDRIVE current setting is decreased, the peak scan readings are also decreased.

Table 3. EMI Scan Results

IDRIVE Setting (mA)	35-MHz Peak (dBµV/m)	65-MHz Peak (dBµV/m)	160-MHz Peak (dBµV/m)
10/20	5	<0	<0
20/40	12	<0	<0
50/100	12	<0	<0
200/400	28	12	2
250/500	30	15	5

Analyzing the output waveforms on an oscilloscope, it can be seen that at the higher IDRIVE settings, a high-frequency oscillation is induced on the switch-node. Figure 26 shows the high-level oscilloscope capture where the oscillation is not obvious, but by zooming into the end of the rising edge (Figure 27) the 35-MHz signal that is in the EMI scans is shown. By reducing the IDRIVE, the oscillation is almost completely removed (Figure 28) which gives an example of how the IDRIVE architecture would be used in a real-world application. Figure 29 through Figure 33 show the source EMI scans with the entire 30- to 200-MHz spectrum.

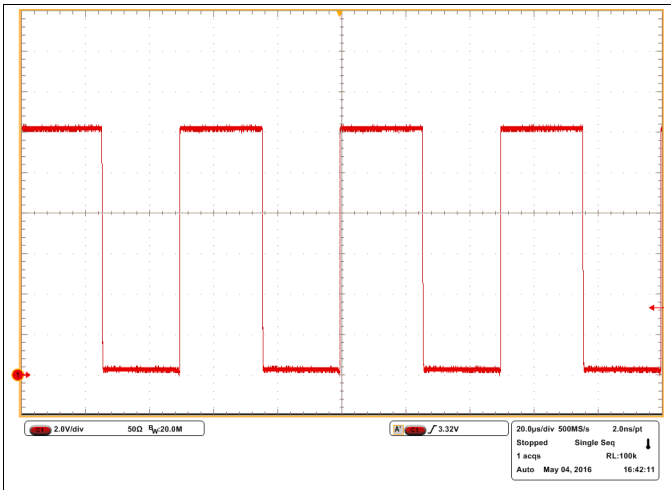

Figure 26. 250/500-mA Switch-Node Waveform

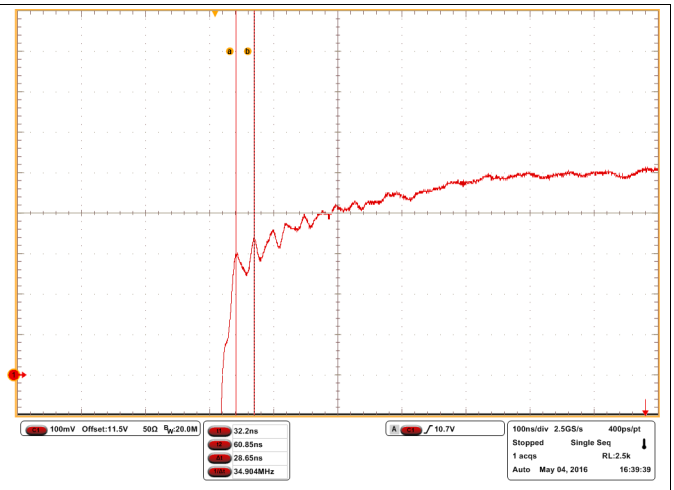

Figure 27. 250/500-mA Switch-Node Waveform Zoom

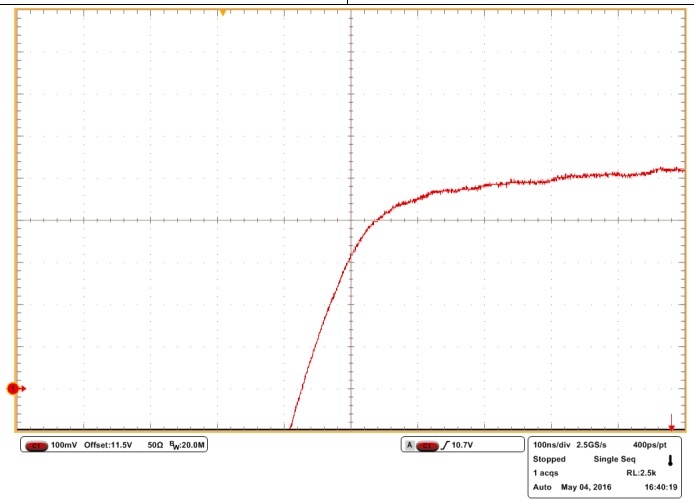

Figure 28. 10/20-mA Switch-Node Waveform Zoom

Figure 29 through Figure 33 show the results from the radiated emissions engineering scans for each of the IDRIVE settings.

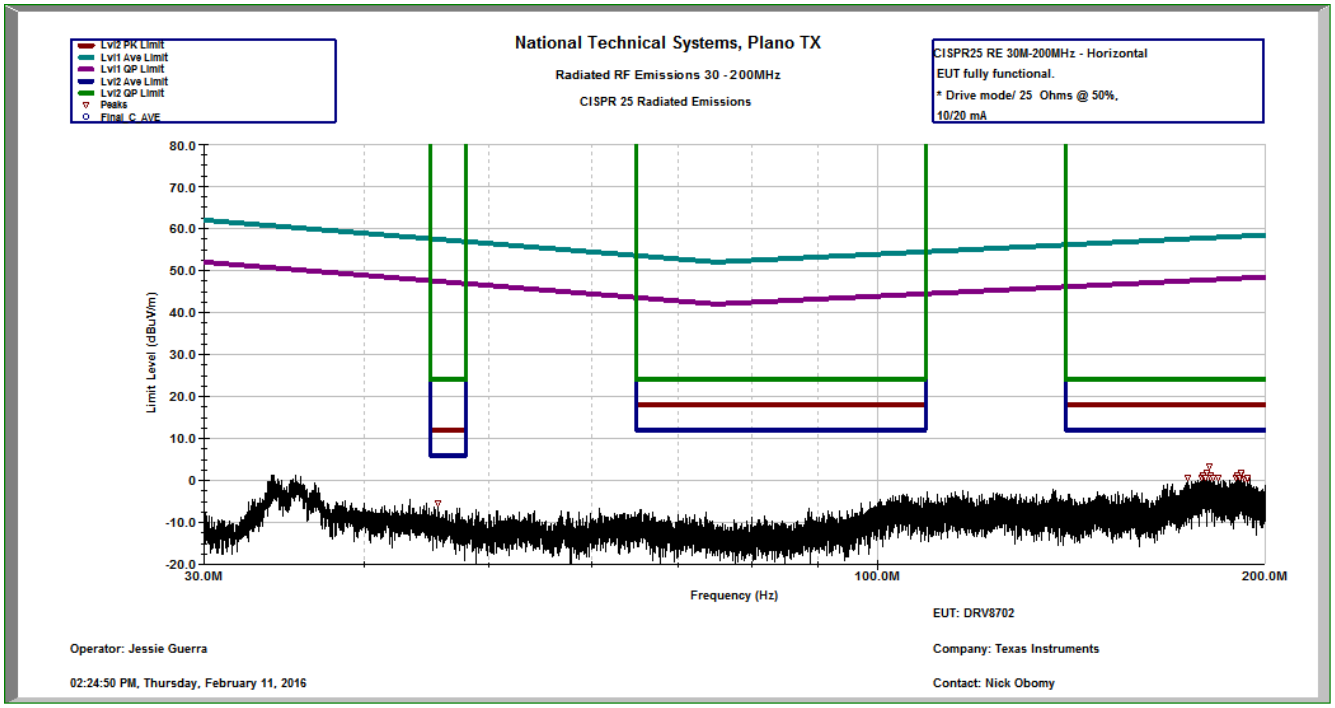

Figure 29. 10/20-mA EMI Scan

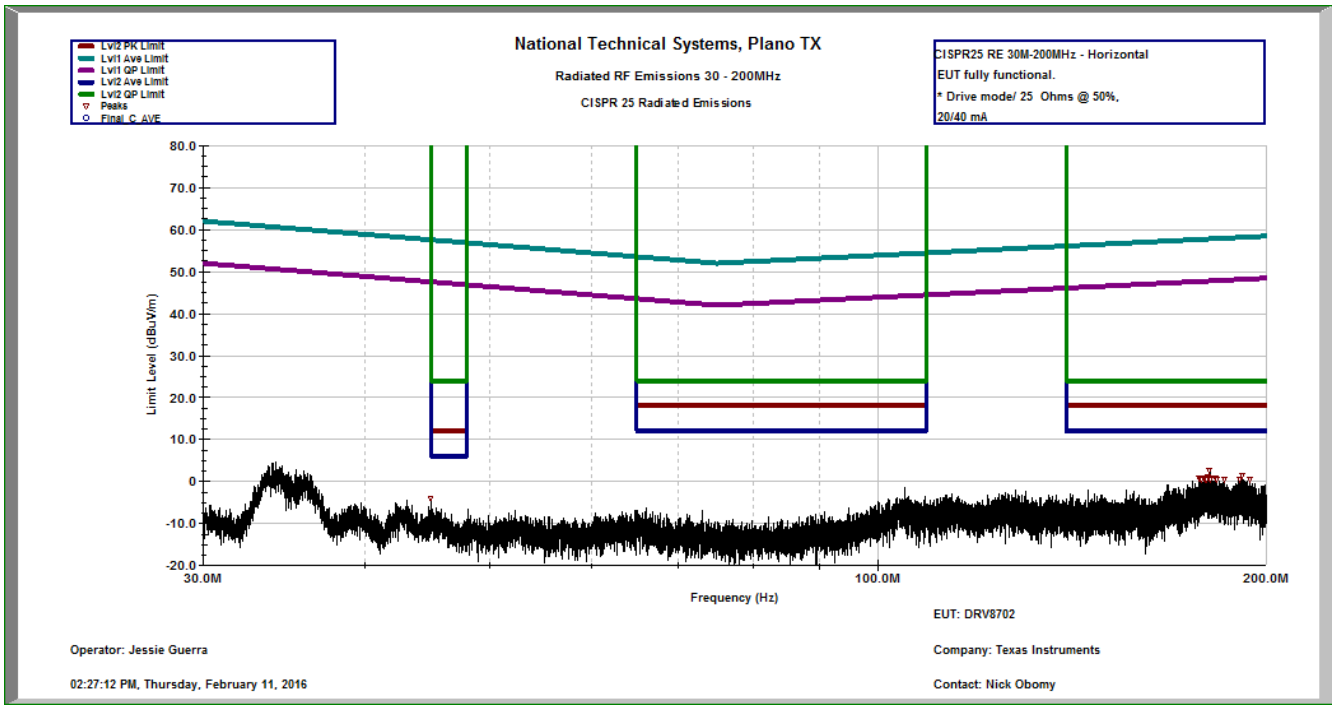

Figure 30. 20/40-mA EMI Scan

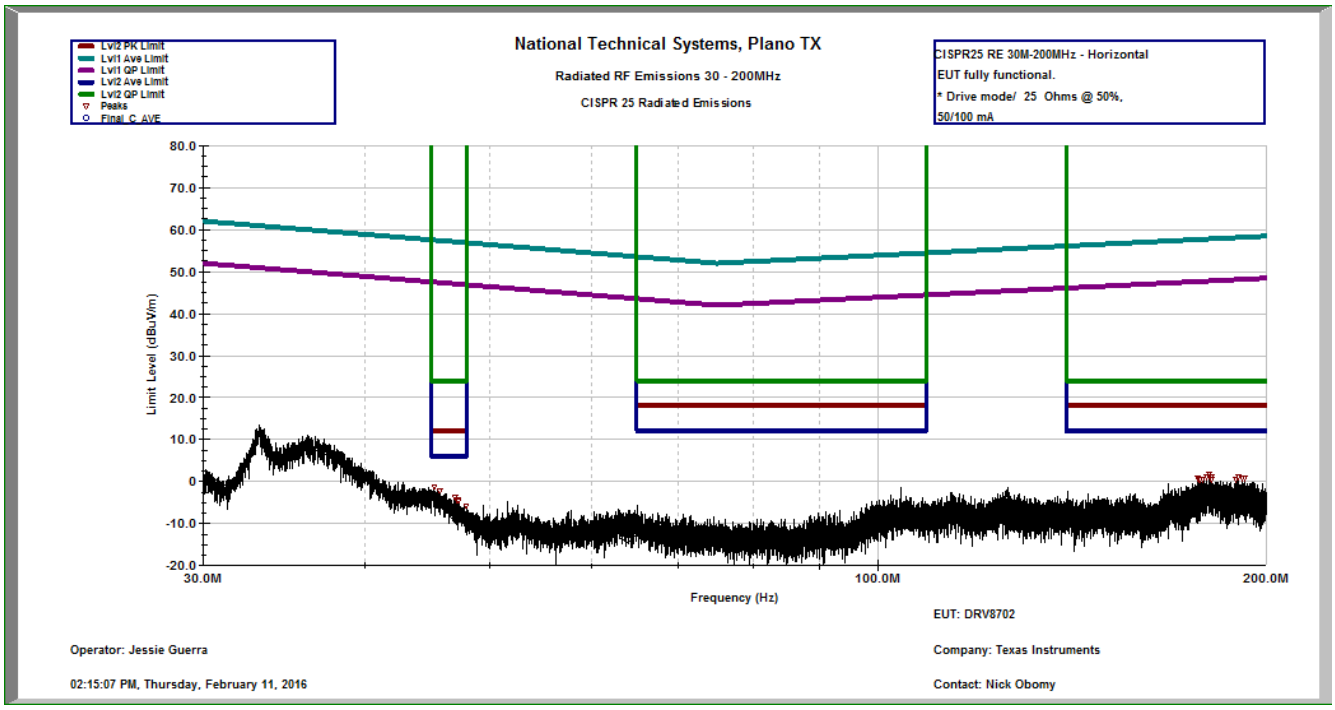

Figure 31. 50/100-mA EMI Scan

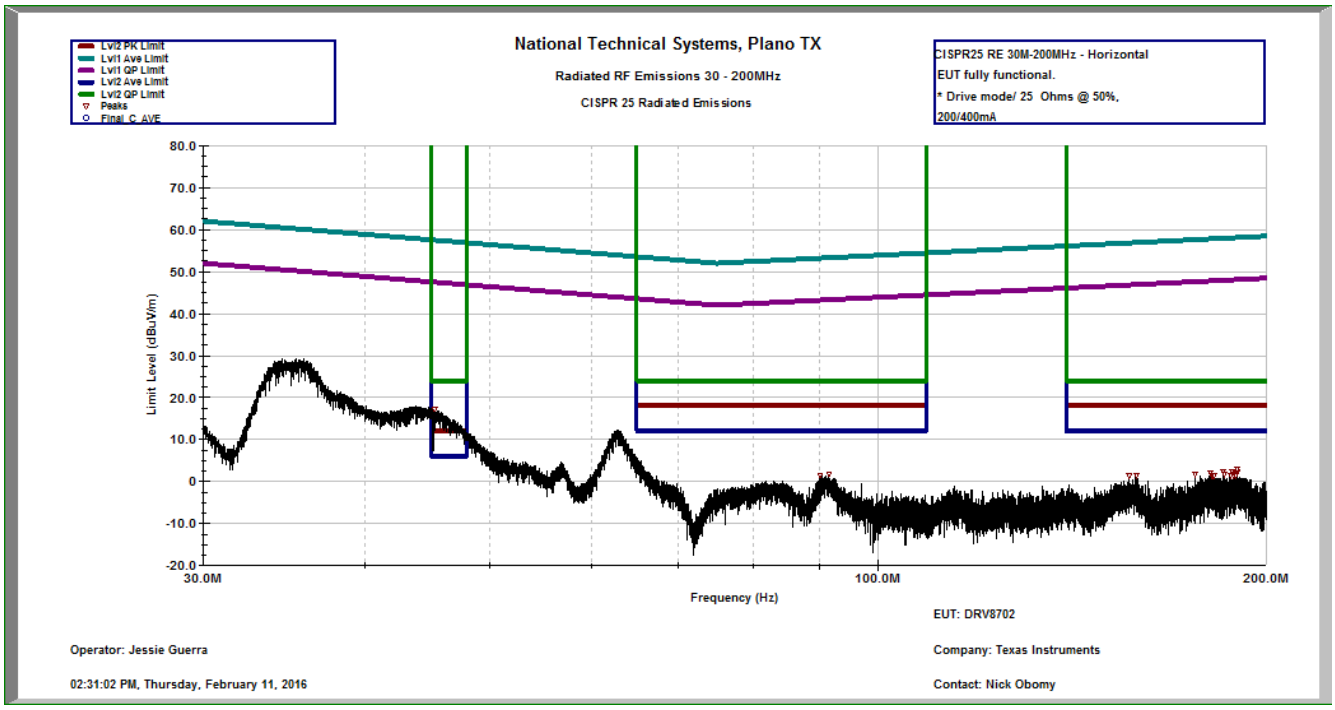

Figure 32. 200/400-mA EMI Scan

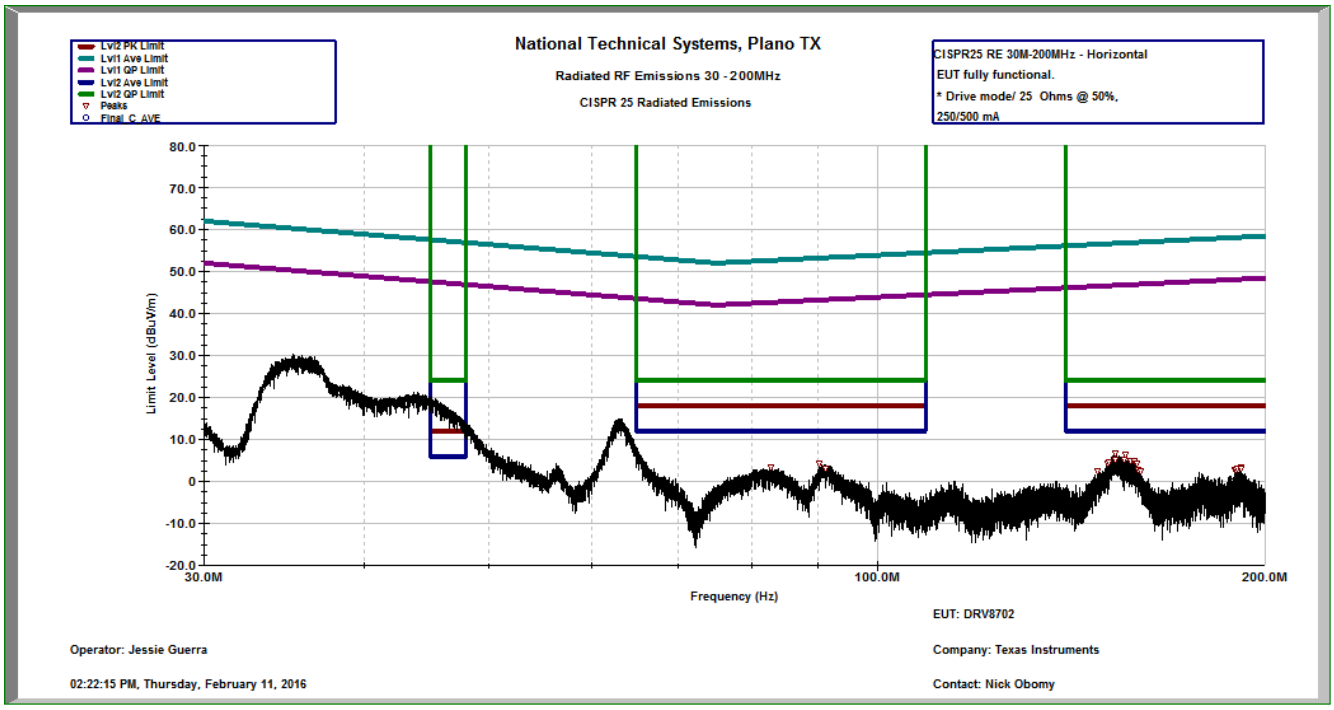

Figure 33. 250/500-mA EMI Scan

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (January 2018) to C Revision **Page**

- Changed spec values in Table 1 4
- Changed "6.9 nC" to "44 nC" in *Section 1.5.2* 8

Changes from A Revision (May 2016) to B Revision **Page**

- Updated terminology to Smart Gate Driver 1

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