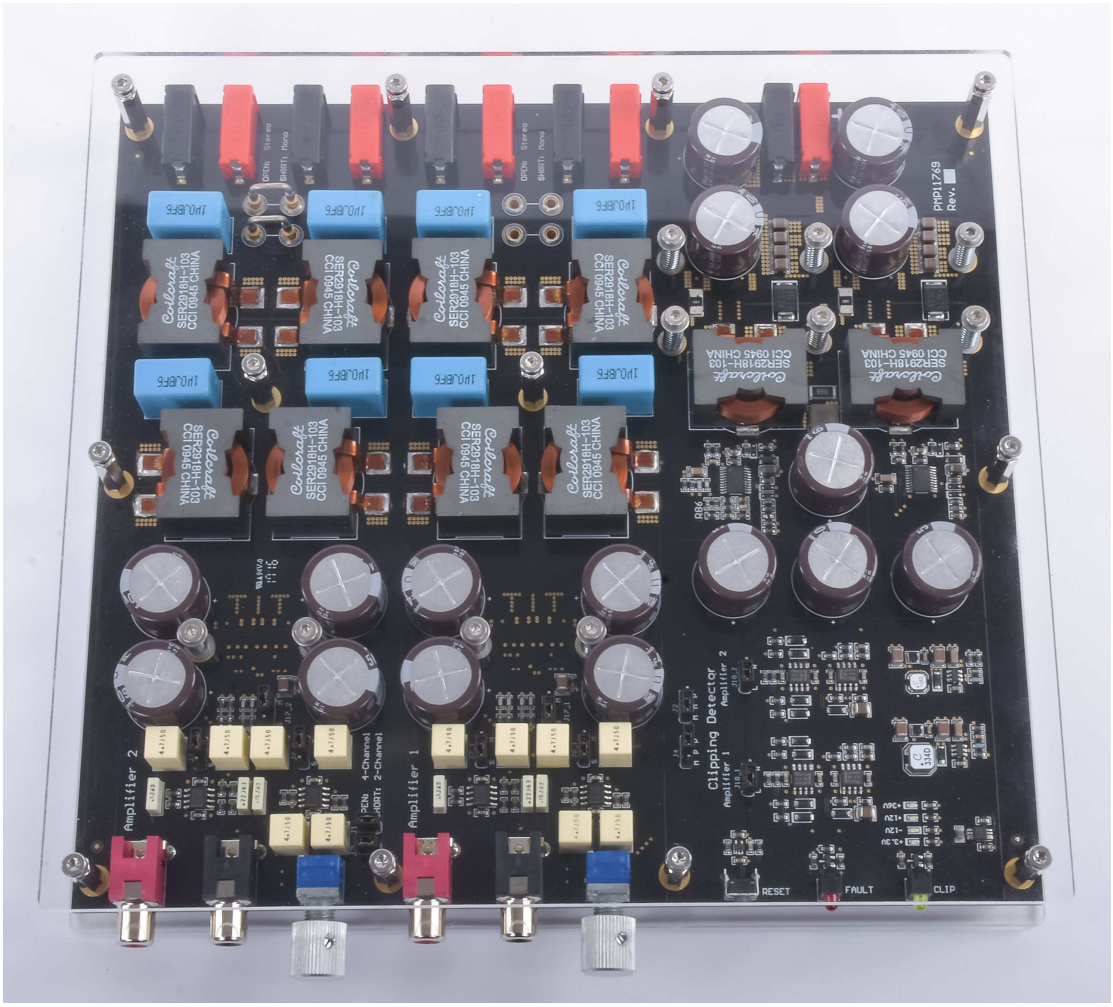
Automotive Interleaved Synchronous Boost + Audio Amplifier

- Input 9.0 .. 16.0V (full load) / 6.0 .. 16.0V (functional)
- Output 36.0V @ 10.0A (continuous) / 20.0A (peak)
- Controller 2x LM25112-Q1 in master-slave configuration
- Free-Running switching frequency of 250 kHz
- Working in continuous conduction mode
- Amplifier 2x TPA3251D2
  Amplifier 1 in stereo mode for left & right channel (175W)
  Amplifier 2 in parallel mode for subwoofer (350W)
- Buck converter (+12.0V @ 200mA) with LM2841X-Q1
- Inverting buck-boost converter (-12.0V @ 50mA) with LM2841X-Q1
- Linear regulator (+3.3V @ 50mA) with TPS7A6633-Q1



1 Interleaved Boost with LM25122

1.1 Startup

The startup waveform is shown in Figure 1. The input voltage is set at 13.8V with no load on the 36.0V output.

Channel C1: **13.8V Input voltage**
5V/div, 50ms/div

Channel C2: **36.0V Output voltage**
10V/div, 50ms/div

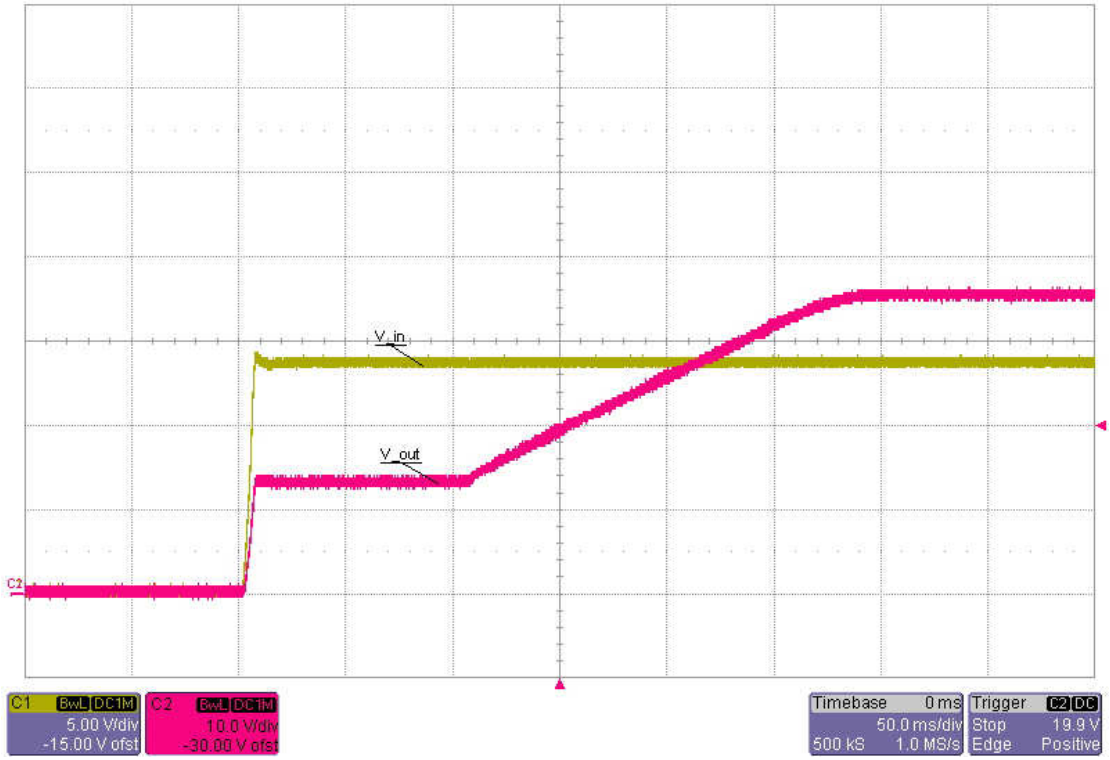


Figure 1

1.2 Shutdown

The shutdown waveform is shown in Figure 2. The input voltage is set at 13.8V with a 10.0A load on the 36.0V output.

Channel C1: **13.8V Input voltage**
5V/div, 10ms/div
Channel C2: **5.0V Output voltage**
10V/div, 10ms/div

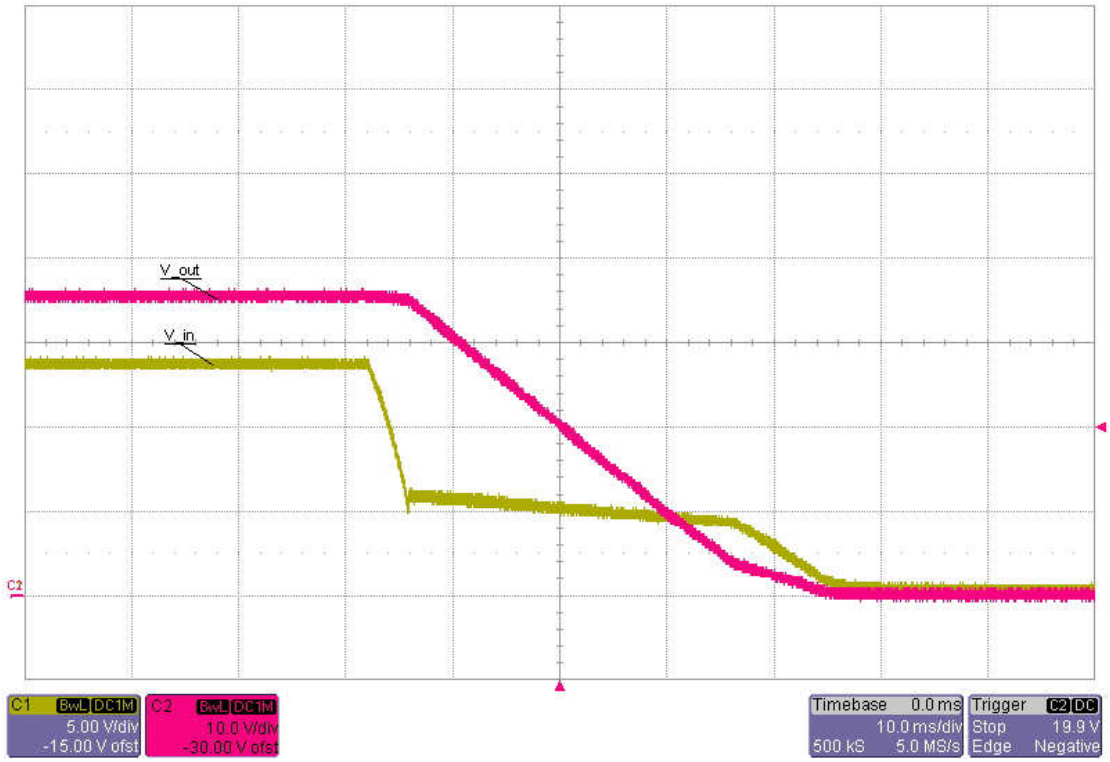


Figure 2

1.3 Efficiency, Losses & Load Regulation

The efficiency and losses are shown in Figure 3 and Figure 4.

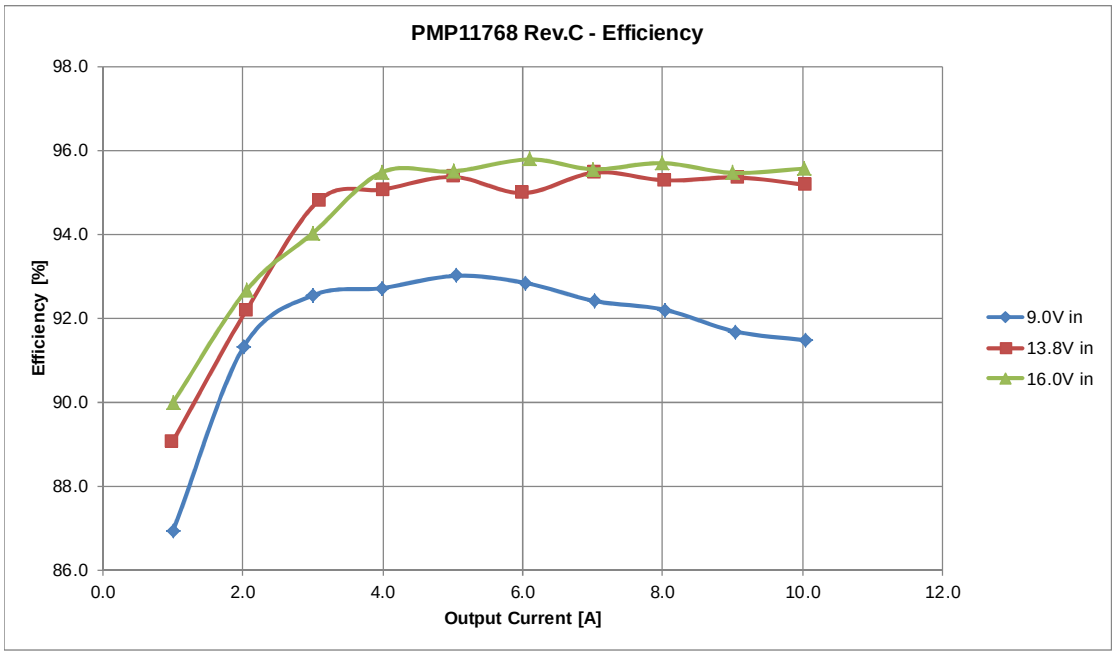


Figure 3

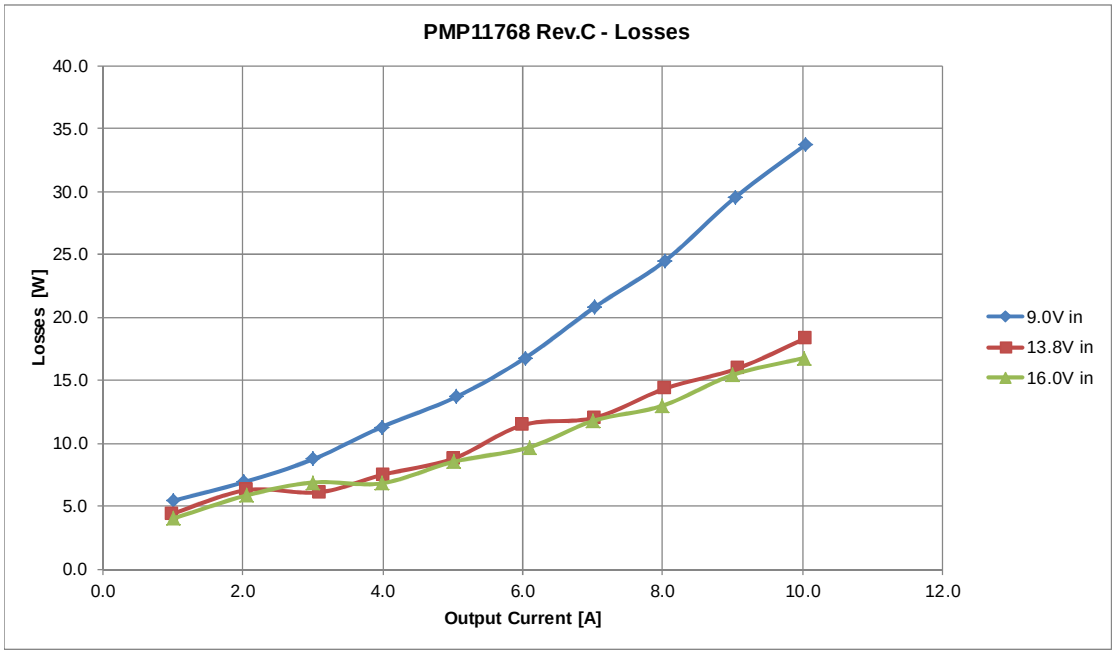


Figure 4

The load regulation is shown in Figure 5.

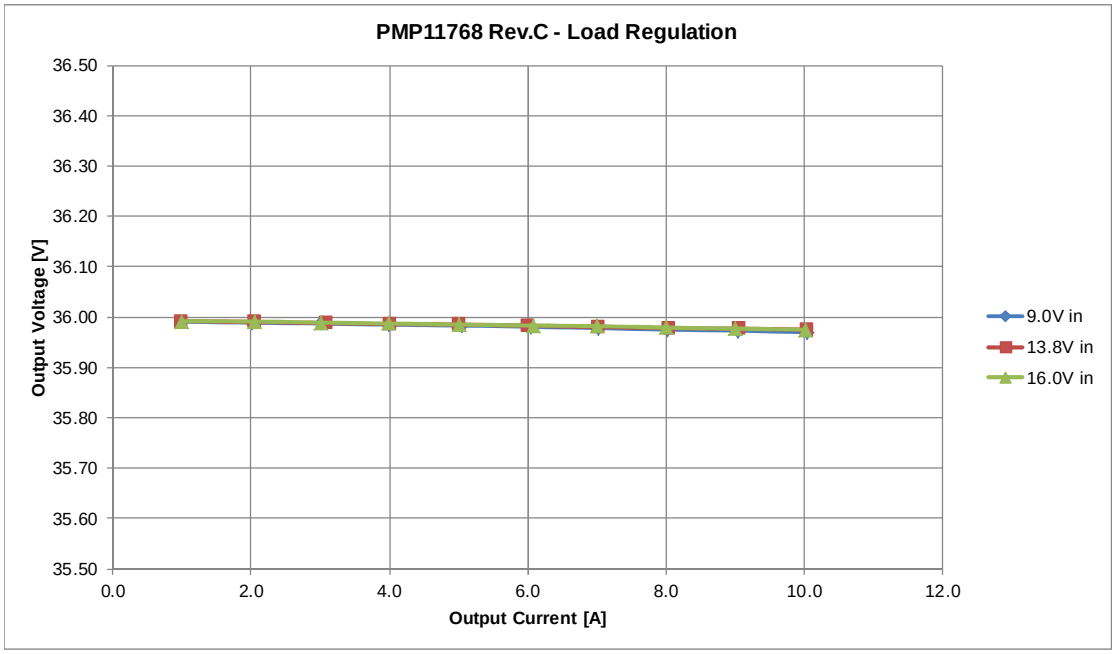


Figure 5

1.4 Load Step – High Profile Capacitors

The response to a load step and a load dump for the 36.0V output at an input voltage of 13.8V is shown in Figure 6.
The board was populated with 12x 820uF electrolytic capacitors Nichicon UPW1H821MHD6 (18x20mm) on the output and 4x 1800uF electrolytic capacitors Nichicon UPW1V182MHD6 (18x20mm) on the input.

Channel C2: **Output voltage**, -204mV undershoot (0.6%), 199mV overshoot (0.6%)
200mV/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 10A to 20A and vice versa
10A/div, 1ms/div

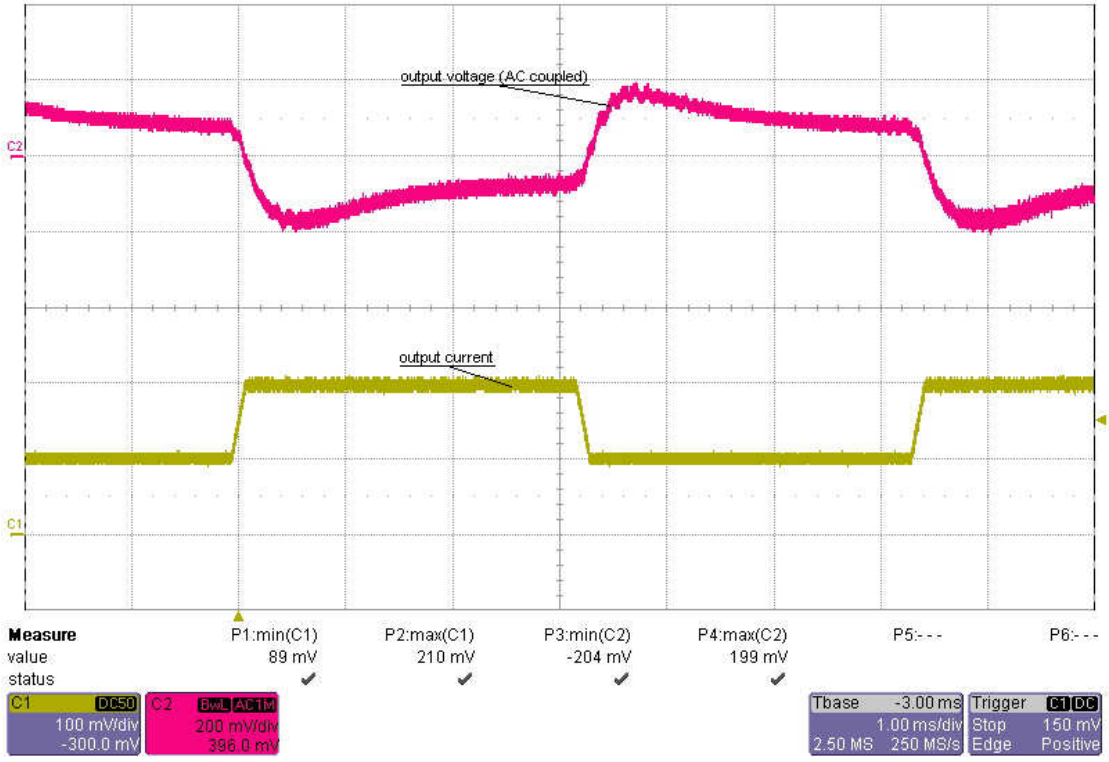


Figure 6

1.5 Frequency Response – High Profile Capacitors

Figure 7 shows the loop response at 10A load.
The board was populated with 12x 820uF electrolytic capacitors Nichicon UPW1H821MHD6 (18x20mm) on the output and 4x 1800uF electrolytic capacitors Nichicon UPW1V182MHD6 (18x20mm) on the input.
Compensation network: R74 = 100kOhm, C85 = 47nF, C90 = 1nF

- 9.0V input 67 deg phase margin, 410 Hz bandwidth, -22 dB gain margin
- 13.8V input 71 deg phase margin, 740 Hz bandwidth, -24 dB gain margin
- 16.0V input 70 deg phase margin, 910 Hz bandwidth, -25 dB gain margin

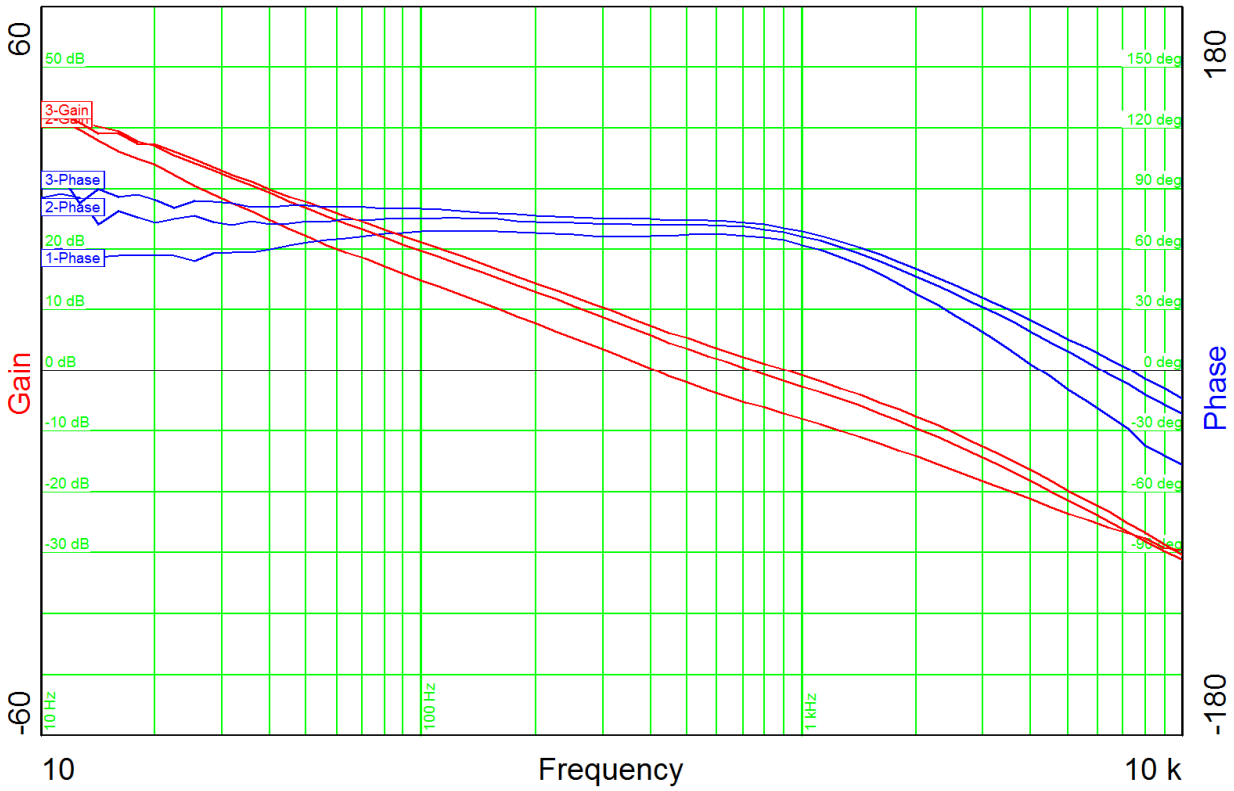


Figure 7

1.6 Load Step – Low Profile Capacitors

The response to a load step and a load dump for the 36.0V output at an input voltage of 13.8V is shown in Figure 8.
The board was populated with 12x 560uF electrolytic capacitors Nichicon UPW1G561MHDANE (18x15mm) on the output and 4x 1200uF electrolytic capacitors Nichicon UPA1E122MHDANE (18x15mm) on the input.

Channel C2: **Output voltage**, -249mV undershoot (0.7%), 212mV overshoot (0.6%)
200mV/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 10A to 20A and vice versa
10A/div, 1ms/div

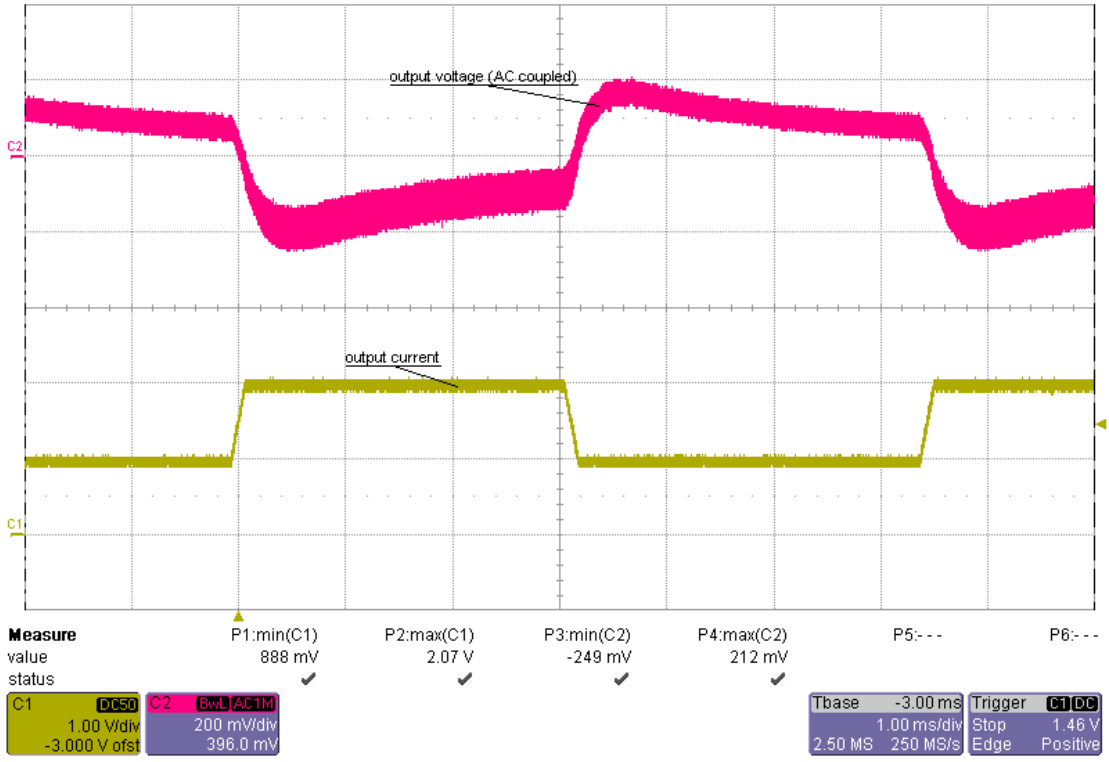


Figure 8

1.7 Frequency Response – Low Profile Capacitors

Figure 9 shows the loop response at 10A load.
The board was populated with 12x 560uF electrolytic capacitors Nichicon UPW1G561MHDANE (18x15mm) on the output and 4x 1200uF electrolytic capacitors Nichicon UPA1E122MHDANE (18x15mm) on the input.
Compensation network: R74 = 68.1kOhm, C85 = 68nF, C90 = 270pF

- 9.0V input 75 deg phase margin, 490 Hz bandwidth, -18 dB gain margin
- 13.8V input 81 deg phase margin, 830 Hz bandwidth, -21 dB gain margin
- 16.0V input 81 deg phase margin, 1.0 kHz bandwidth, -23 dB gain margin

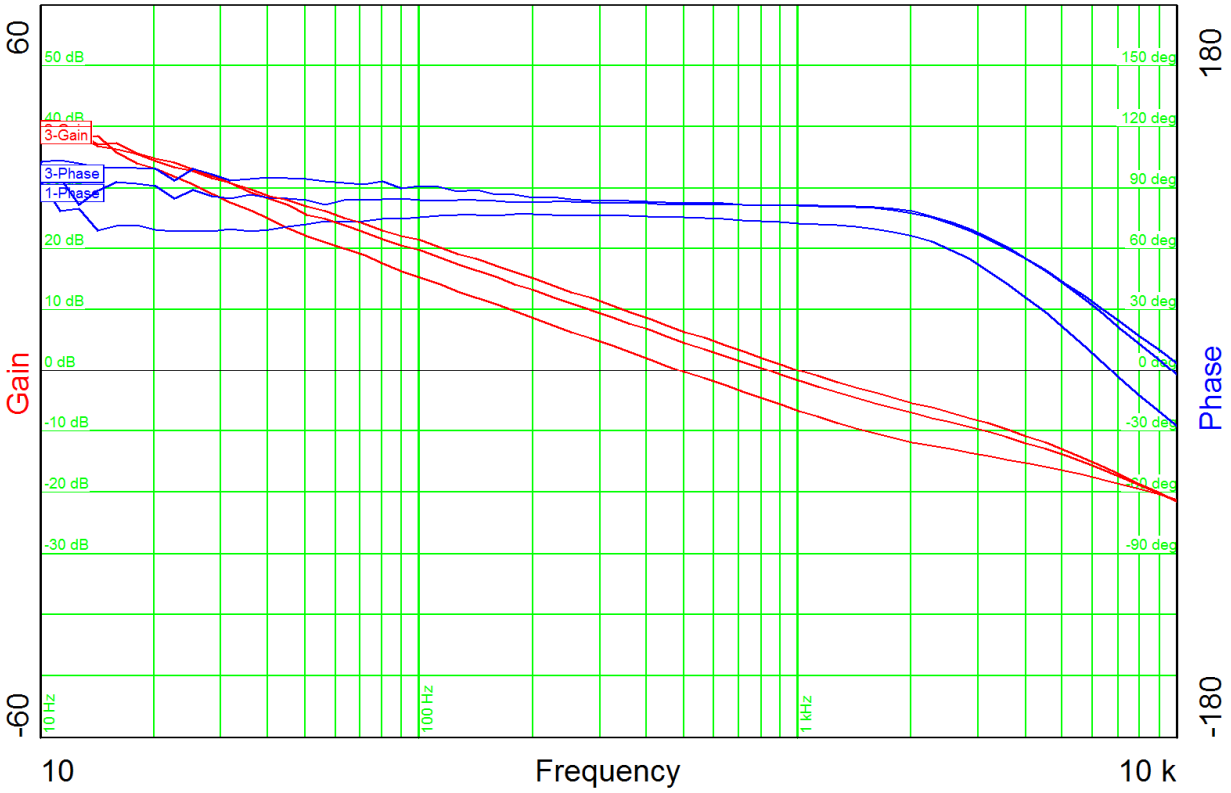


Figure 9

1.8 Low Side FET

The gate-source voltage of the low side FET is shown in Figure 10. The image was captured with 13.8V input voltage and 10.0A load.

Channel C2: **Gate-source voltage**, -0.5V minimum voltage, 7.9V maximum voltage
2V/div, 500ns/div

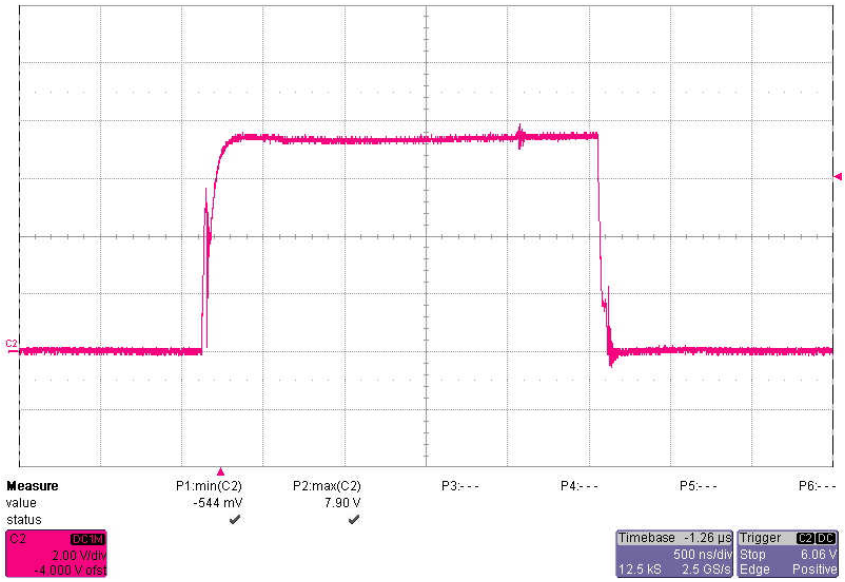


Figure 10

The drain-source voltage of the low side FET is shown in Figure 11. The image was captured with 13.8V input voltage and 10.0A load.

Channel C2: **Drain-source voltage**, -1.4V minimum voltage, 47.6V maximum voltage
10V/div, 1us/div

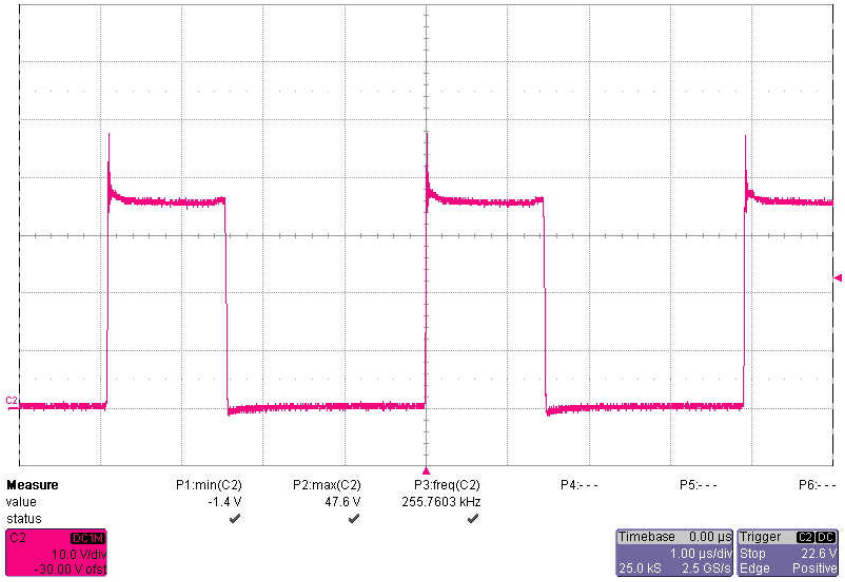


Figure 11

1.9 High Side FET

The gate-source voltage of the high side FET is shown in Figure 12. The image was captured with 13.8V input voltage and 10.0A load.

Channel C2: **Gate-source voltage**, -6.0V minimum voltage, 7.2V maximum voltage
2V/div, 500ns/div

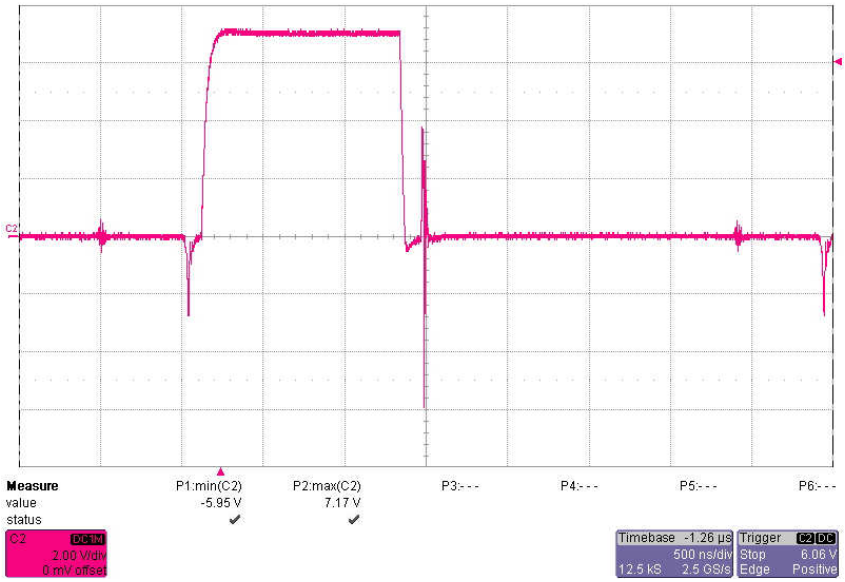


Figure 12

The drain-source voltage of the low side FET is shown in Figure 13. The image was captured with 13.8V input voltage and 10.0A load.

Channel C2: **Drain-source voltage**, -3.6V minimum voltage, 47.8V maximum voltage
10V/div, 1us/div

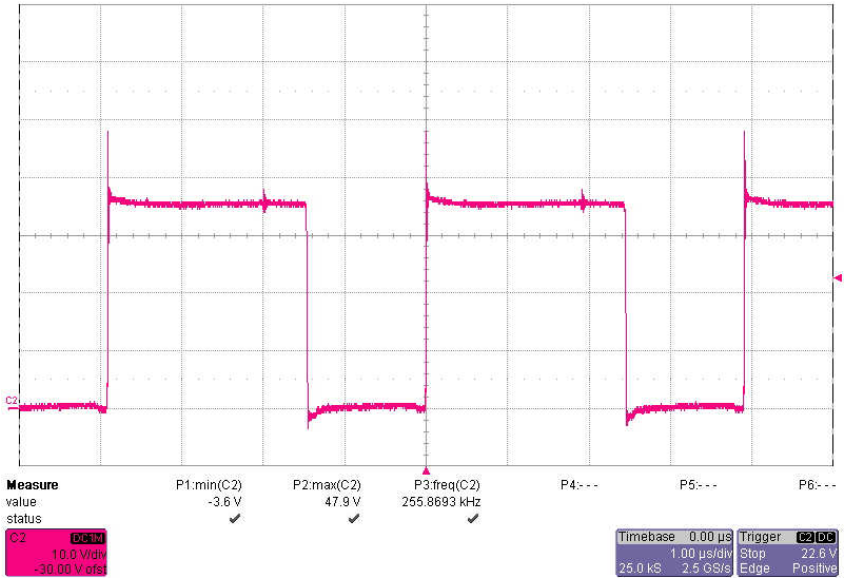


Figure 13

1.10 Output Ripple Voltage – Before Post-Filter

The output ripple voltage at 10.0A load and 9.0V, 13.8V and 16.0V V input voltage is shown in Figure 14.
The board was populated with the high profile capacitors.

Channel M1: **Output voltage @ 9.0V input**, 966mV peak-peak (2.7%)
500mV/div, 2us/div, AC coupled

Channel M2: **Output voltage @ 13.8V input**, 570mV peak-peak (1.6%)
500mV/div, 2us/div, AC coupled

Channel M3: **Output voltage @ 16.0V input**, 474mV peak-peak (1.3%)
500mV/div, 2us/div, AC coupled

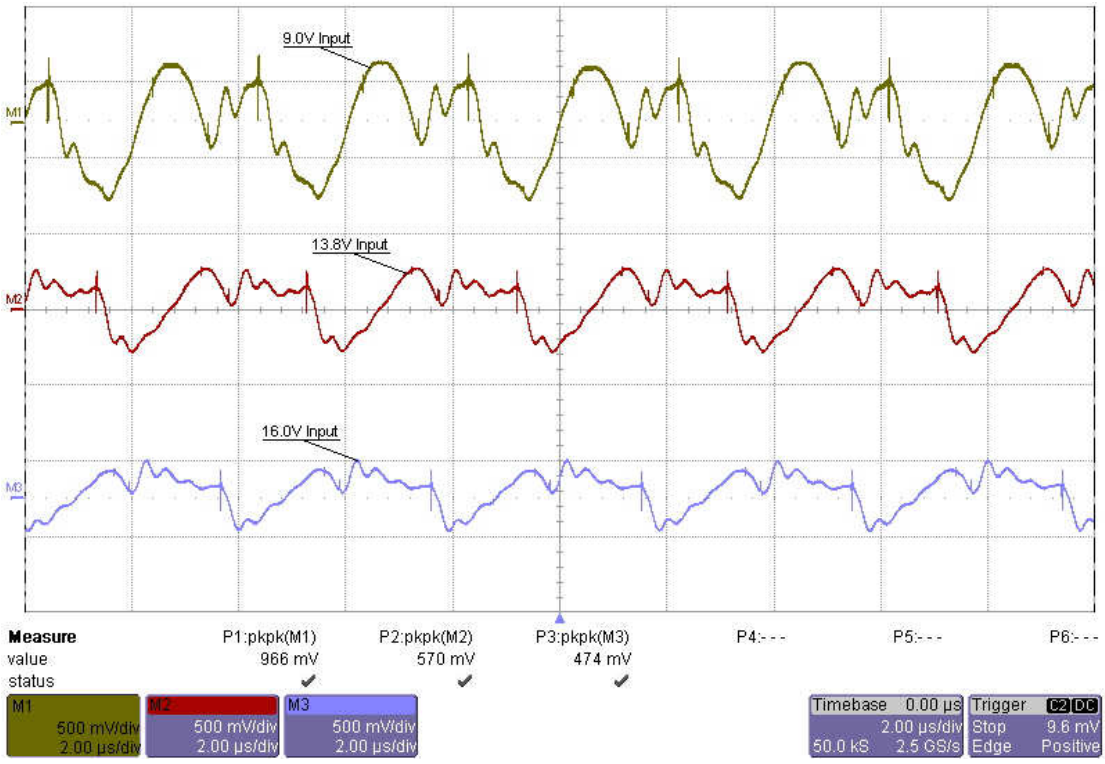


Figure 14

1.11 Output Ripple Voltage – After Post-Filter

The output ripple voltage at 10.0A load and 9.0V, 13.8V and 16.0V V input voltage is shown in Figure 15.
The board was populated with the high profile capacitors.

Channel M1: **Output voltage @ 9.0V input**, 15mV peak-peak / 60mV spikes
50mV/div, 2us/div, AC coupled

Channel M2: **Output voltage @ 13.8V input**, 15mV peak-peak / 58mV spikes
50mV/div, 2us/div, AC coupled

Channel M3: **Output voltage @ 16.0V input**, 10mV peak-peak / 83mV spikes
50mV/div, 2us/div, AC coupled

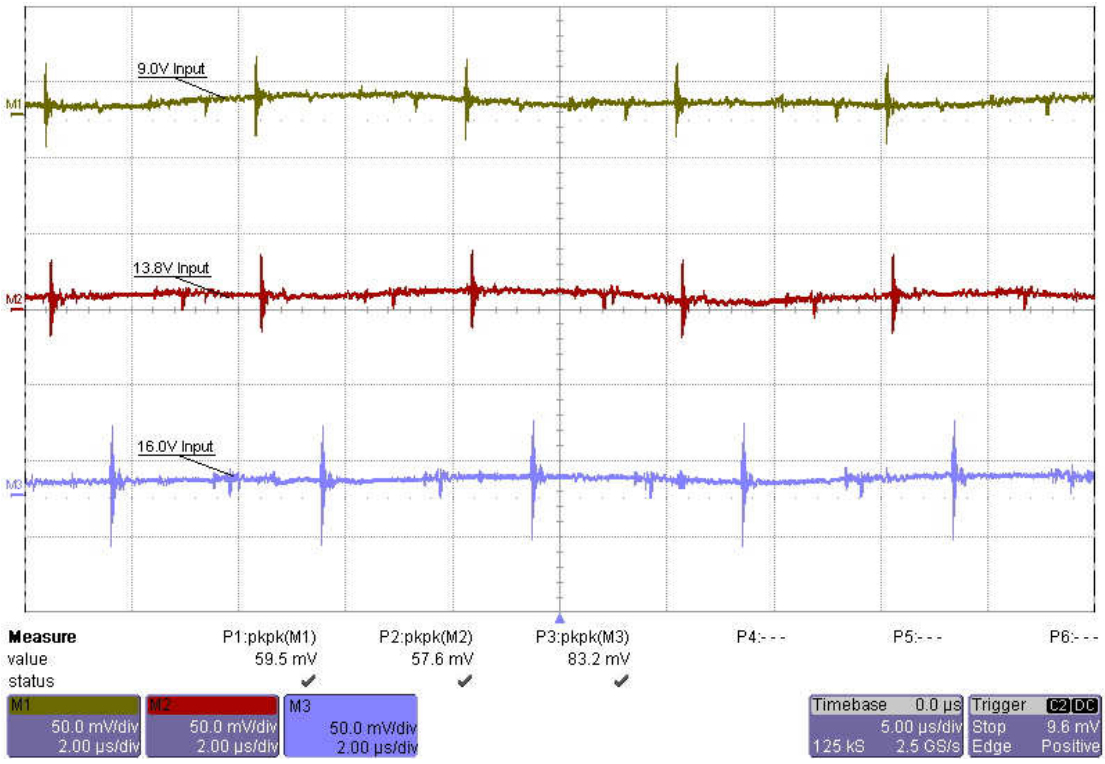


Figure 15

1.12 Input Ripple Voltage

The input ripple voltage at 10.0A load and 9.0V, 13.8V and 16.0V V input voltage is shown in Figure 16.
The board was populated with the high profile capacitors.

Channel M1: **Input voltage @ 9.0V input**, 38mV peak-peak
50mV/div, 2us/div, AC coupled

Channel M2: **Input voltage @ 13.8V input**, 79mV peak-peak
50mV/div, 2us/div, AC coupled

Channel M3: **Input voltage @ 16.0V input**, 67mV peak-peak
50mV/div, 2us/div, AC coupled

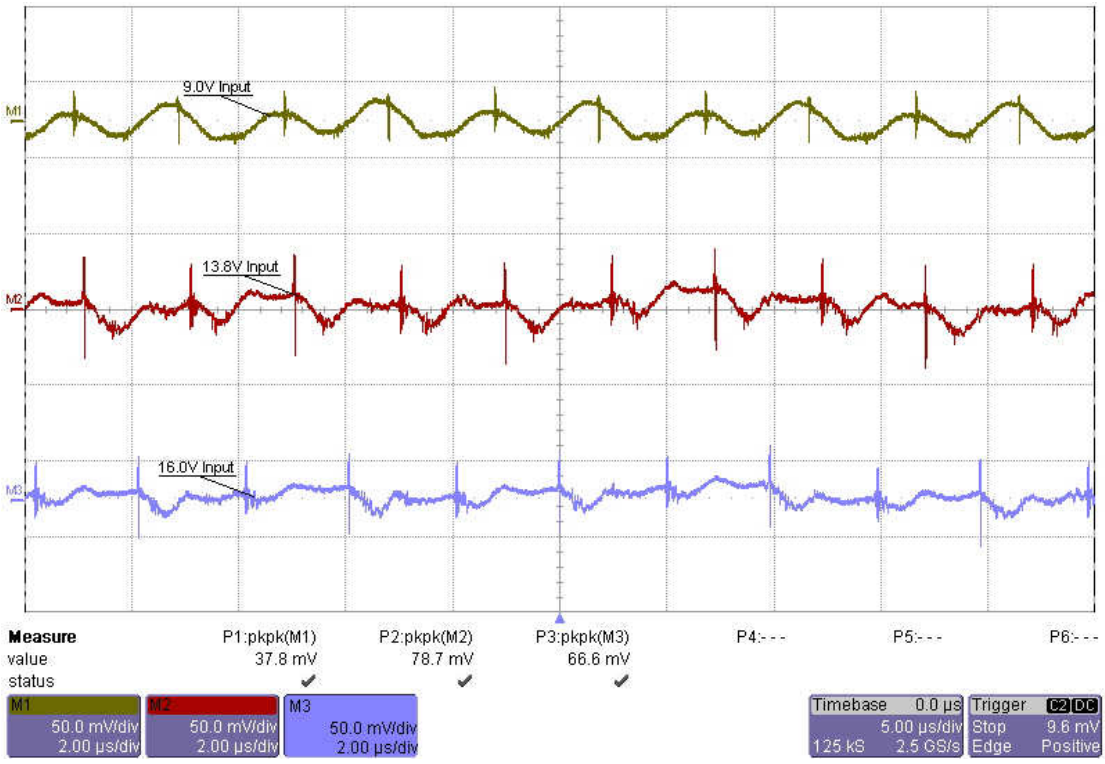


Figure 16

1.13 Thermal Measurement

The thermal image of the top side (Figure 17) shows the circuit at an ambient temperature of 21 °C with an input voltage of 13.8V and a load of 5.0A without heatsink or active cooling.

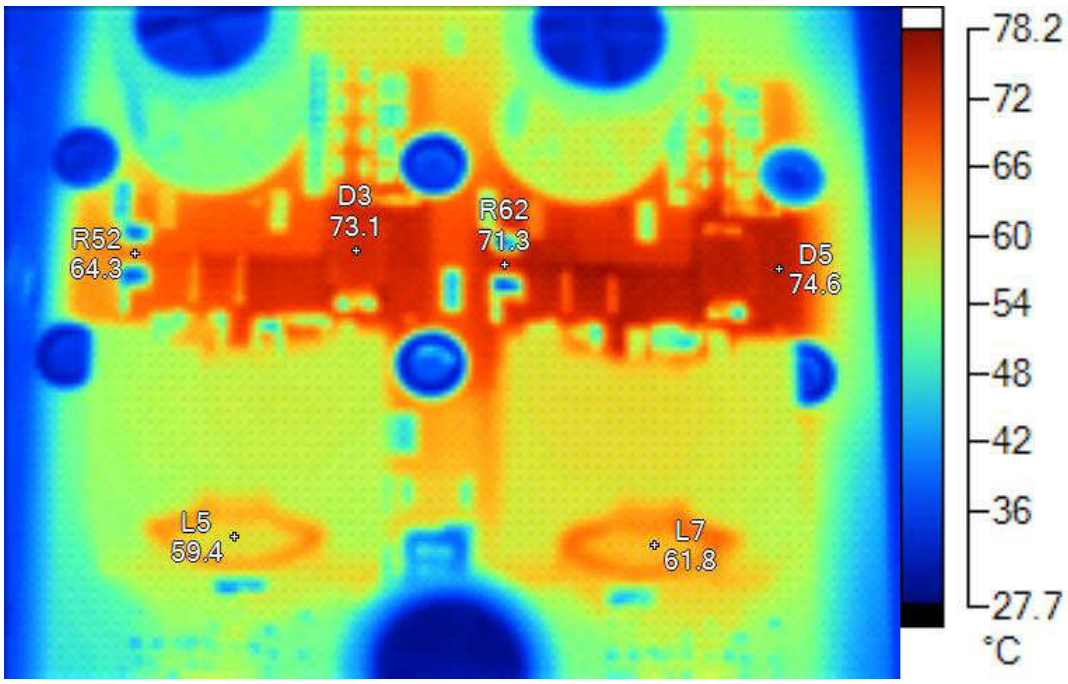


Figure 17

Name	Temperature	Emissivity	Background
L5	59.4°C	0.95	21.0°C
L7	61.8°C	0.95	21.0°C
R52	64.3°C	0.95	21.0°C
D3	73.1°C	0.95	21.0°C
R62	71.3°C	0.95	21.0°C
D5	74.6°C	0.95	21.0°C

The thermal image of the bottom side (Figure 18) shows the circuit at an ambient temperature of 21 °C with an input voltage of 13.8V and a load of 5.0A without heatsink or active cooling.

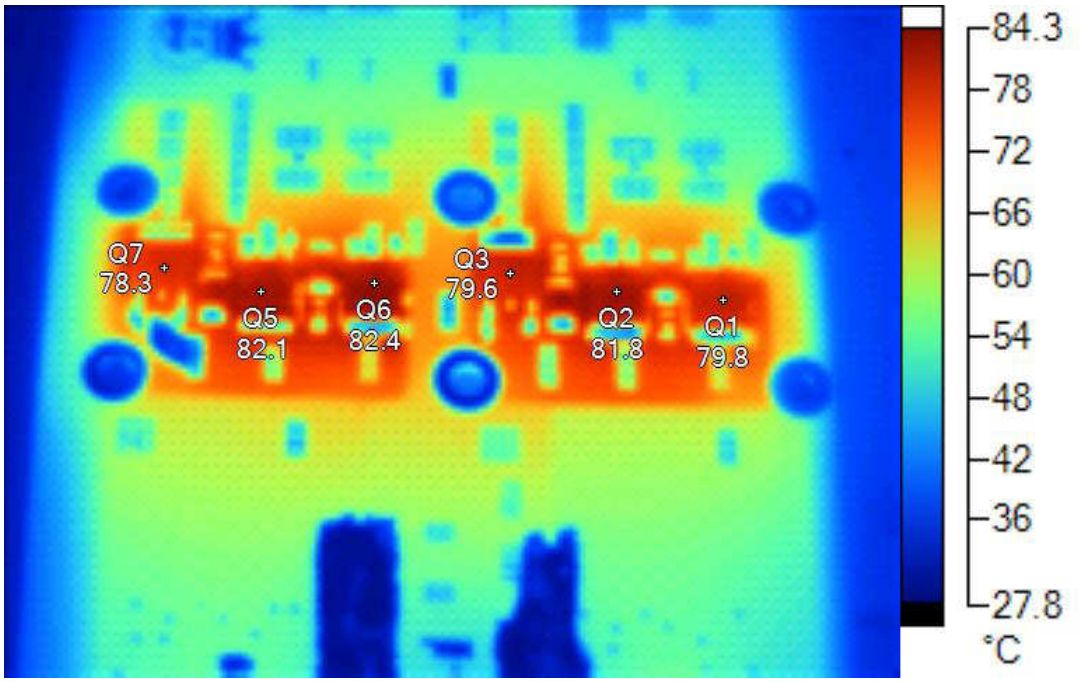


Figure 18

Name	Temperature	Emissivity	Background
Q7	78.3°C	0.95	21.0°C
Q5	82.1°C	0.95	21.0°C
Q6	82.4°C	0.95	21.0°C
Q3	79.6°C	0.95	21.0°C
Q2	81.8°C	0.95	21.0°C
Q1	79.8°C	0.95	21.0°C

2 Buck with LM2841X-Q1

Auxiliary supply providing +12.0V @ 200mA from 36.0V input voltage.
Figure 19 shows the loop response at 200mA load.

- 36.0V input 71 deg phase margin, 3.5 kHz bandwidth, -17 dB gain margin

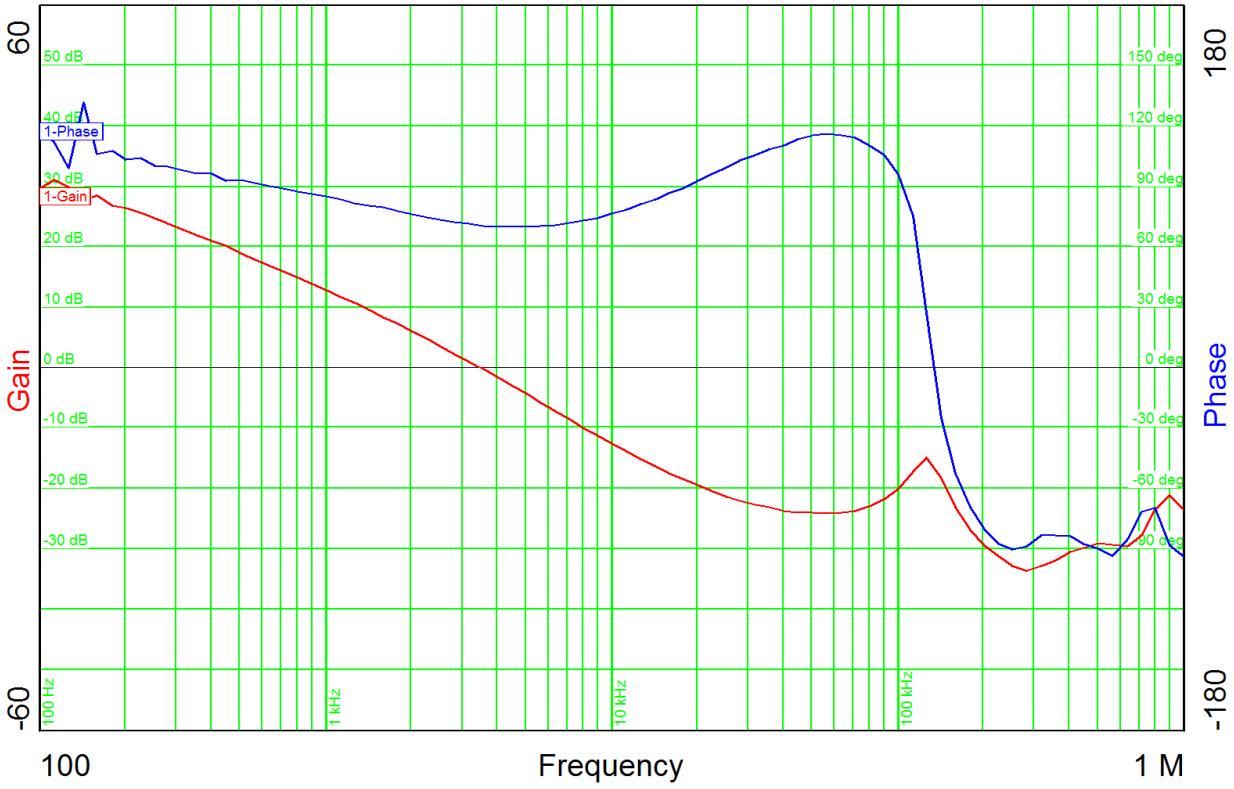


Figure 19

3 Inverting Buck-Boost with LM2841X-Q1

Auxiliary supply providing -12.0V @ 50mA from 36.0V input voltage.
Figure 20 shows the loop response at 50mA load.

- 36.0V input 61 deg phase margin, 4.7 kHz bandwidth, -10 dB gain margin

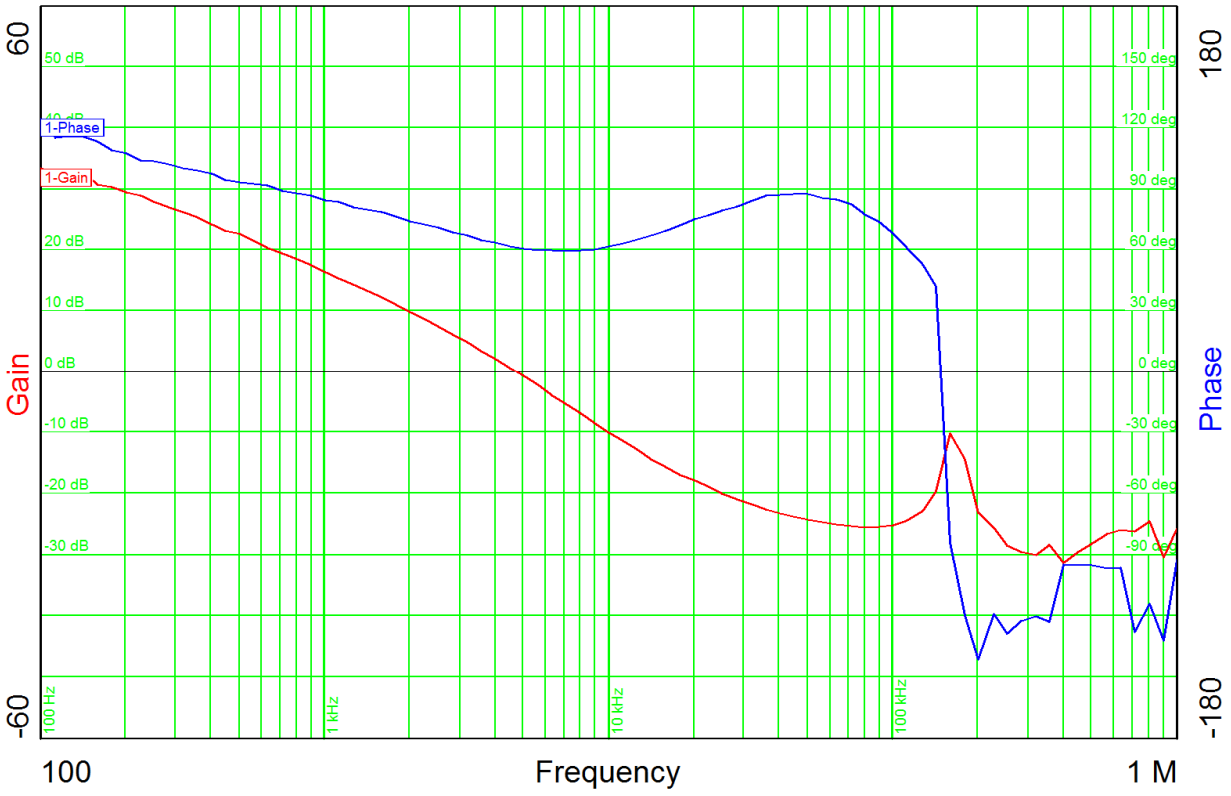


Figure 20

4 TPA3251D2 in Stereo Mode

Figure 21, Figure 22, Figure 23 and Figure 24 show one channel in stereo mode at 4 Ohm load (resistor).
The input signal was adjusted such that the amplifier was not yet clipping.

- 10 Hz 55.7V / 97W
- 100 Hz 57.0V / 102W
- 1 kHz 55.7 V / 97W
- 10 kHz 54.4 V / 92W

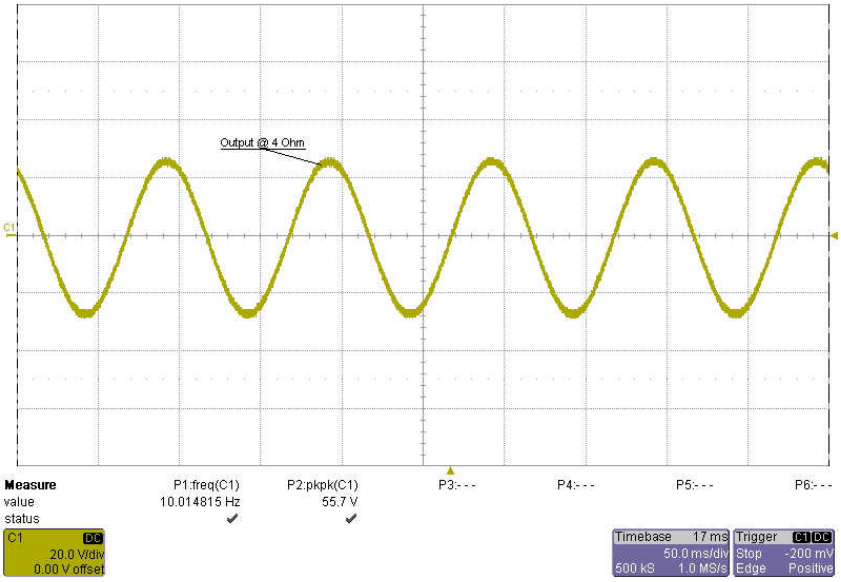


Figure 21

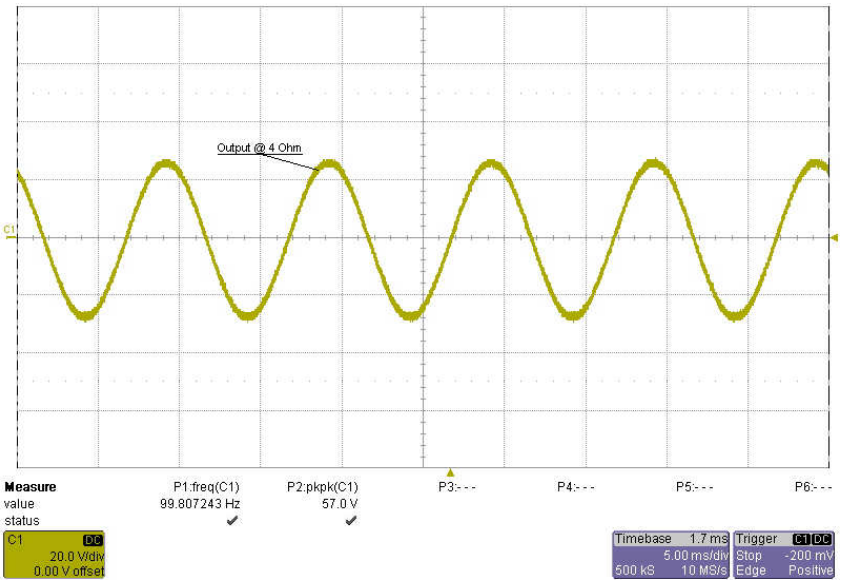


Figure 22

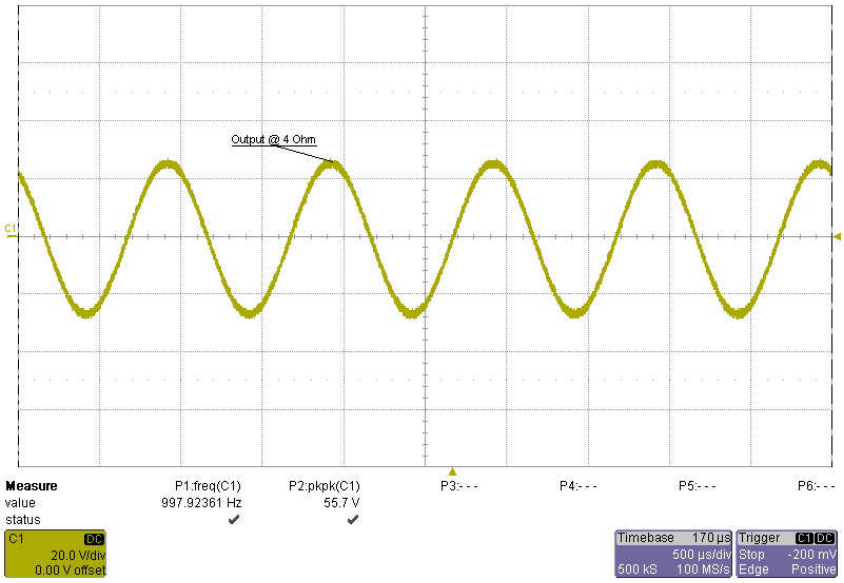


Figure 23

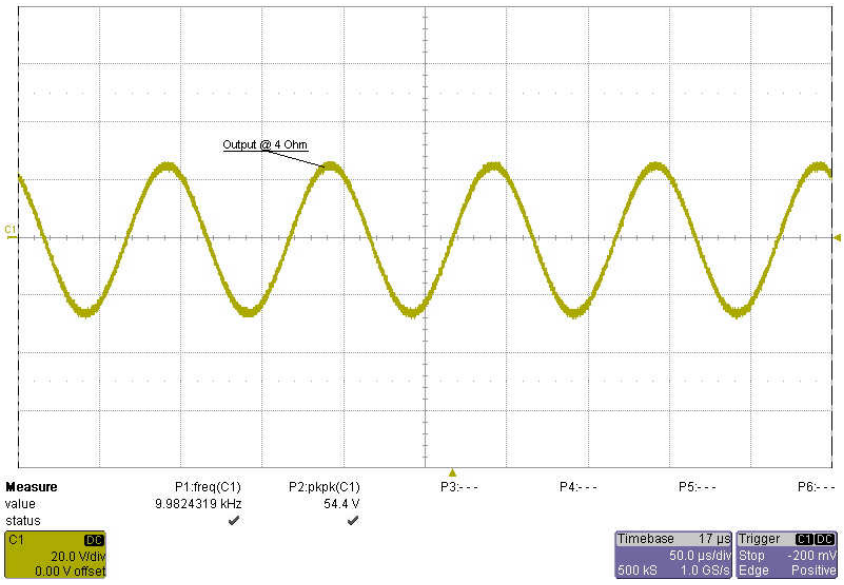


Figure 24

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