LM5175 42V 宽 V_{IN} 同步 4 开关 降压 - 升压控制器

1 特性

- 单电感降压-升压控制器，用于升压/降压 DC/DC 转换
- 宽 V_{IN} 范围：3.5V 至 42V，最大值为 60V
- 灵活的 V_{OUT} 范围：0.8V 至 55V
- V_{OUT} 短路保护
- 高效降压-升压转换
- 可调开关频率
- 可选频率同步和抖动
- 集成 2A 金属氧化物半导体场效应晶体管 (MOSFET) 栅极驱动器
- 逐周期电流限制和可选断续模式
- 可选输入或输出平均电流限制
- 可编程的输入欠压闭锁 (UVLO) 和软启动
- 电源正常和输出过压保护
- 可利用脉冲跳跃来选择连续导通模式 (CCM) 或断续导通模式 (DCM)
- 采用 HTSSOP-28 和 QFN-28 封装

2 应用

- 汽车起停系统
- 备用电池和超级电容充电
- 工业 PC 用电源
- USB 供电
- LED 照明

3 说明

LM5175 是一款同步四开关降压-升压 DC/DC 控制器，能够将输出电压稳定在输入电压、高于输入电压或者低于输入电压的某一电压值上。LM5175 具有 3.5V 至 42V 的宽输入电压范围（最大值为 60V），支持各类 应用。

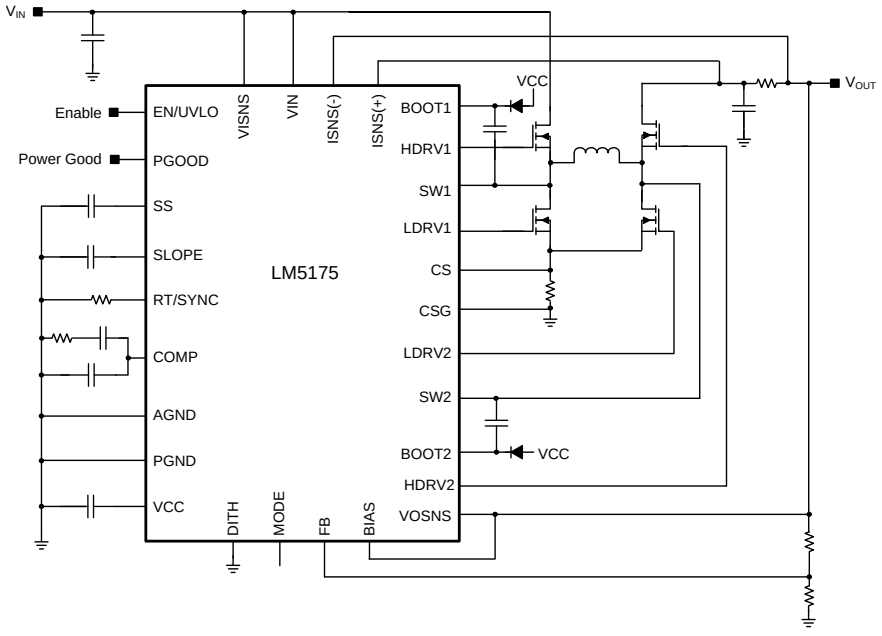
LM5175 在降压和升压工作模式下均采用电流模式控制，以提供出色的负载和线路调节性能。开关频率可通过外部电阻进行编程，并且可与外部时钟信号同步。

该器件还 具有 可编程的软启动功能，并且提供 诸如逐周期电流限制、输入欠压锁定 (UVLO)、输出过压保护 (OVP) 和热关断等各类保护特性。此外，LM5175 特有 可选择的连续导通模式 (CCM) 或断续导通模式 (DCM)、可选平均输入或输出电流限制、可降低峰值电磁干扰 (EMI) 的可选扩展频谱、以及应对持续过载情况的可选断续模式保护。

器件信息

订货编号	封装	封装尺寸
LM5175PWP	HTSSOP-28	9.7mm x 4.4mm
LM5175RHF	QFN-28	4.0mm x 5.0mm

4 简化电路原理图



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5 修订历史记录

Changes from Original (October 2015) to Revision A **Page**

- 已添加 QFN-28 封装 ... 1
- 已添加 LM5175RHF 信息 ... 1
- Added RHF package ... 3
- Added QFN pins ... 4
- Changed first plus to minus ... 18
- Changed all 1.22 V to 1.23 V ... 19
- Changed equation ... 23
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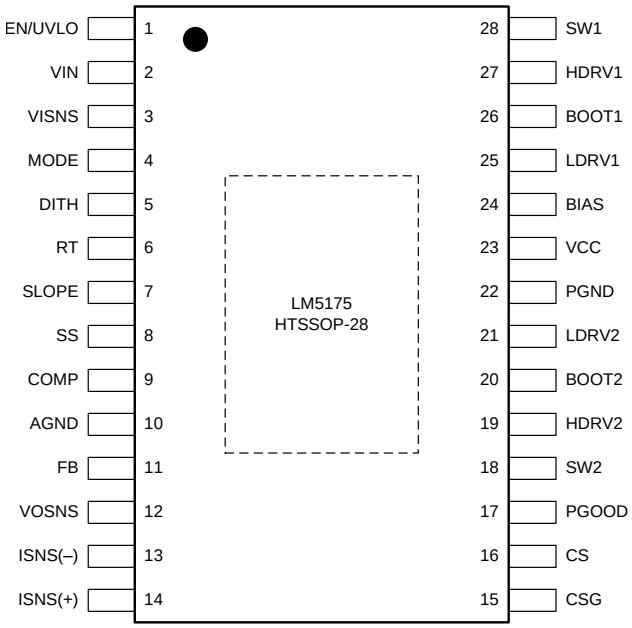
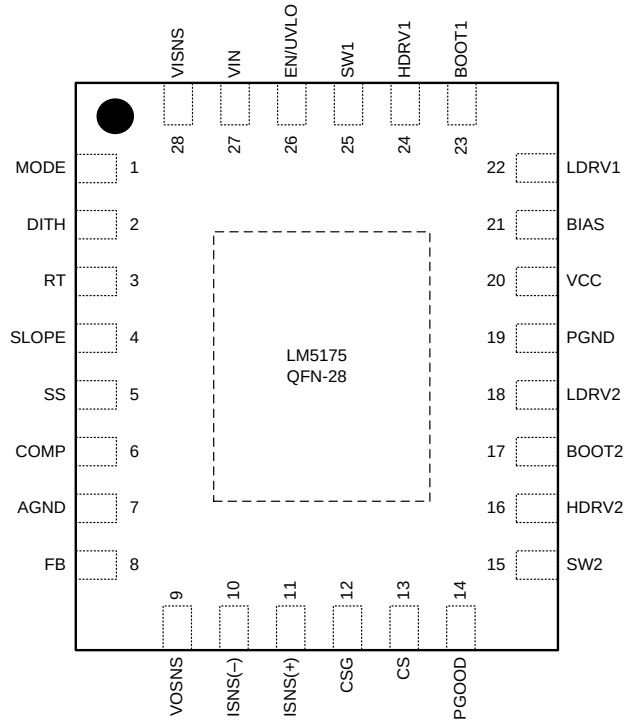
- Changed equation ... 25

6 Pin Configuration and Functions

HTSSOP-28
PWP Package
Top View



QFN-28
RHF Package
Top View



Pin Functions

PIN			DESCRIPTION
NAME	HTSSOP	QFN	
EN/UVLO	1	26	Enable pin. For EN/UVLO < 0.4 V, the LM5175 is in a low current shutdown mode. For 0.7 V < EN/UVLO < 1.23 V, the controller operates in standby mode in which the VCC regulator is enabled but the PWM controller is not switching. For EN/UVLO > 1.23 V, the PWM function is enabled, provided VCC exceeds the VCC UV threshold.
VIN	2	27	The input supply pin to the IC. Connect V_{IN} to a supply voltage between 3.5 V and 42 V.
VISNS	3	28	V_{IN} sense input. Connect to the input capacitor.
MODE	4	1	Mode = GND, DCM, Hiccup Disabled (Set R_{MODE} resistor to GND = 0 Ω)
			Mode = 1.00 V, DCM, Hiccup Enabled (Set R_{MODE} resistor to GND = 49.9 kΩ)
			Mode = 1.85 V, CCM, Hiccup Enabled (Set R_{MODE} resistor to GND = 93.1 kΩ)
			Mode = VCC, CCM, Hiccup Disabled (Set R_{MODE} resistor to VCC = 0 Ω)
DITH	5	2	A capacitor connected between the DITH pin and AGND is charged and discharged with a 10 uA current source. As the voltage on the DITH pin ramps up and down the oscillator frequency is modulated between –5% and +5% of the nominal frequency set by the RT resistor. Grounding the DITH pin will disable the dithering feature. In the external Sync mode, the DITH pin voltage is ignored.
RT/SYNC	6	3	Switching frequency programming pin. An external resistor is connected to the RT/SYNC pin and AGND to set the switching frequency. This pin can also be used to synchronize the PWM controller to an external clock.
SLOPE	7	4	A capacitor connected between the SLOPE pin and AGND provides the slope compensation ramp for stable current mode operation in both buck and boost mode.
SS	8	5	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start time.
COMP	9	6	Output of the error amplifier. An external RC network connected between COMP and AGND compensates the regulator feedback loop.
AGND	10	7	Analog ground of the IC.
FB	11	8	Feedback pin for output voltage regulation. Connect a resistor divider network from the output of the converter to the FB pin.
VOSNS	12	9	V_{OUT} sense input. Connect to the output capacitor.
ISNS(–) ISNS(+)	13 14	10 11	Input or Output Current Sense Amplifier inputs. An optional current sense resistor connected between ISNS(+) and ISNS(–) can be located either on the input side or on the output side of the converter. If the sensed voltage across the ISNS(+) and ISNS(-) pins reaches 50 mV, a slow Constant Current (CC) control loop becomes active and starts discharging the soft-start capacitor to regulated the drop across ISNS(+) and ISNS(-) to 50 mV. Short ISNS(+) and ISNS(-) together to disable this feature.
CSG	15	12	The negative or ground input to the PWM current sense amplifier. Connect directly to the low-side (ground) of the current sense resistor.
CS	16	13	The positive input to the PWM current sense amplifier.
PGOOD	17	14	Power Good open drain output. PGOOD is pulled low when FB is outside a 0.8 V ±10% regulation window.
SW2 SW1	18 28	15 25	The boost and the buck side switching nodes respectively.
HDRV2 HDRV1	19 27	16 24	Output of the high-side gate drivers. Connect directly to the gates of the high-side MOSFETs.
BOOT2 BOOT1	20 26	17 23	An external capacitor is required between the BOOT1, BOOT2 pins and the SW1, SW2 pins respectively to provide bias to the high-side MOSFET gate drivers.
LDRV2 LDRV1	21 25	18 22	Output of the low-side gate drivers. Connect directly to the gates of the low-side MOSFETs.
PGND	22	19	Power ground of the IC. The high current ground connection to the low-side gate drivers.
VCC	23	20	Output of the VCC bias regulator. Connect capacitor to ground.
BIAS	24	21	Optional input to the VCC bias regulator. Powering VCC from an external supply instead of V_{IN} can reduce power loss at high V_{IN}. For V_{BIAS} > 8 V, the VCC regulator draws power from the BIAS pin. The BIAS pin voltage must not exceed 40 V.
PowerPAD™	-	-	The PowerPAD should be soldered to the analog ground. If possible, use thermal vias to connect to a PCB ground plane for improved power dissipation.

7 Specifications

7.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
VIN, EN/UVLO, VISNS, VOSNS, ISNS(+), ISNS(–)	–0.3	60	V
BIAS	–0.3	40	
FB, SS, DITH, RT/SYNC, SLOPE, COMP	–0.3	3.6	
SW1, SW2	–1	60	
SW1, SW2 (20 ns transient)	–3.0	65	
VCC, MODE, PGOOD	–0.3	8.5	
LDRV1, LDRV2	–0.3	8.5	
BOOT1, HDRV1 with respect to SW1	–0.3	8.5	
BOOT2, HDRV2 with respect to SW2	–0.3	8.5	
BOOT1, BOOT2	–0.3	68	
CS, CSG	–0.3	0.3	
Operating junction temperature	–40	150	°C
Storage temperature, T_{stg}	-65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
V_{ESD}(1)	Human body model (HBM) ESD stress voltage(2)	±2000	V
	Charged device model (CDM) ESD stress voltage(3)	±750	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	3.5		42	V
BIAS	Bias supply voltage range	8		36	
V_{OUT}	Output voltage range	0.8		55	
EN/UVLO	Enable voltage range	0		42	
ISNS(+), ISNS(-)	Average current sense common mode range	0		55	
T_J	Operating temperature range(2)	–40		125	°C
F_{sw}	Operating frequency range	100		600	kHz

(1) *Recommended Operating Conditions* are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics* .
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.4 Thermal Information

THERMAL METRIC(1)		LM5175		UNIT
		HTSSOP	QFN	
		28 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.1	34.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.7	26.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	14.9	6.3	
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.3	
ψ_{JB}	Junction-to-board characterization parameter	14.7	6.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	2.0	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 24 V unless otherwise stated.(1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (V_{IN})						
V_{IN}	Operating input voltage		3.5		42	V
I_Q	V_{IN} shutdown current	$V_{EN/UVLO}$ = 0 V		1.4	10	µA
	V_{IN} standby current	$V_{EN/UVLO}$ = 1.1 V, non-switching		0.7	2	
	V_{IN} operating current	$V_{EN/UVLO}$ = 2 V, V_{FB} = 0.9 V		1.65	4	mA
VCC						
$V_{VCC(VIN)}$	Regulation voltage	V_{BIAS} = 0 V, VCC open	6.95	7.35	7.88	V
$V_{UV(VCC)}$	VCC Undervoltage lockout	VCC increasing	3.11	3.27	3.43	
	Undervoltage hysteresis			160		mV
I_{VCC}	VCC current limit	V_{VCC} = 0 V	65			mA
$R_{OUT(VCC)}$	VCC regulator output impedance	I_{VCC} = 30 mA, V_{IN} = 3.5 V		9.3	16	Ω
BIAS						
$V_{BIAS(SW)}$	BIAS switchover voltage	V_{IN} = 24 V	7.25	8	8.75	V
EN/UVLO						
$V_{EN(STBY)}$	Standby threshold	EN/UVLO rising	0.55	0.79	0.97	V
$I_{EN(STBY)}$	Standby source current	$V_{EN/UVLO}$ = 1.1 V	1	2	3	µA
$V_{EN(OP)}$	Operating threshold	EN/UVLO rising	1.17	1.23	1.29	V
$\Delta I_{HYS(OP)}$	Operating hysteresis current	$V_{EN/UVLO}$ = 2.4 V	1.5	3.5	5.5	µA
SS						
I_{SS}	Soft-start pull up current	V_{SS} = 0 V	4.30	5.65	7.25	µA
$V_{SS(CL)}$	SS clamp voltage	SS open		1.27		V
V_{FB} - V_{SS}	FB to SS offset	V_{SS} = 0 V		-15		mV
EA (ERROR AMPLIFIER)						
V_{REF}	Feedback reference voltage	FB = COMP	0.788	0.800	0.812	V
gm_{EA}	Error amplifier gm			1.27		mS
I_{SINK}/I_{SOURCE}	COMP sink/source current	V_{FB}=V_{REF} ± 300 mV		280		µA
R_{OUT}	Amplifier output resistance			20		MΩ
BW	Unity gain bandwidth			2		MHz
$I_{BIAS(FB)}$	Feedback pin input bias current	FB in regulation			100	nA
FREQUENCY						
$f_{SW(1)}$	Switching Frequency 1	RT = 133 kΩ	180	200	220	kHz
$f_{SW(2)}$	Switching Frequency 2	RT = 47 kΩ	430	500	565	

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 24 V unless otherwise stated.(1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DITHER						
I_{DITHER}	Dither source/sink current			10.5		µA
V_{DITHER}	Dither high threshold			1.27		V
	Dither low threshold			1.16		
SYNC						
V_{SYNC}	Sync input high threshold		2.1			V
	Sync input low threshold				1.2	
PW_{SYNC}	Sync input pulse width		75		500	ns
CURRENT LIMIT						
$V_{CS(BUCK)}$	Buck current limit threshold (Valley)	V_{IN} = V_{VISNS} = 24 V, V_{VOSNS} = 12 V, V_{SLOPE} = 0 V, T_J = 25°C	53.2	76	98	mV
$V_{CS(BOOST)}$	Boost current limit threshold (Peak)	V_{IN} = V_{VISNS} = 12 V, V_{VOSNS} = 18 V, V_{SLOPE} = 0 V, T_J = 25°C	119	170	221	
$I_{BIAS(CS/CSG)}$	CS/CSG pin bias current	V_{CS} = V_{CSG} = 0 V		-75		µA
$I_{OFFSET(CS/CSG)}$	CSG pin bias current	V_{CS} = V_{CSG} = 0 V			14	
CONSTANT CURRENT LOOP						
V_{SNS}	Average current loop regulation target	$V_{ISNS(-)}$ = 24 V, sweep ISNS(+), V_{SS} = 0.8 V	43	50	57	mV
I_{SNS}	ISNS(+)/ISNS(–) pin bias currents	$V_{ISNS(+)}$ = $V_{ISNS(–)}$ = V_{IN} = 24 V		7		µA
Gm	gm of soft-start pull down amplifier	$V_{ISNS(+)}$–$V_{ISNS(–)}$ = 55 mV, V_{SS} = 0.5 V		1		mS
SLOPE						
I_{SLOPE}	Buck adaptive slope current	V_{IN} = V_{VINSNS} = 24 V, V_{VOSNS} = 12 V, V_{SLOPE} = 0 V	24	30	35	µA
	Boost adaptive slope current	V_{IN} = V_{VINSNS} = 12 V, V_{VOSNS} = 18 V, V_{SLOPE} = 0 V	13	17	21	
gm_{SLOPE}	Slope compensation amplifier gm			2		µS
MODE						
I_{MODE}	Source current out of MODE pin		17	20	23	µA
V_{DCM_HIC}	DCM with hiccup threshold		0.60	0.7	0.76	V
V_{CCM_HIC}	CCM with hiccup threshold		1.18	1.28	1.38	
V_{CCM}	CCM no hiccup threshold		2.22	2.4	2.6	

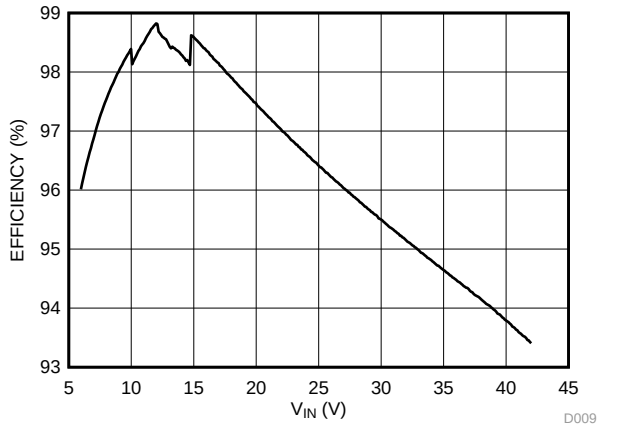
Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 24 V unless otherwise stated.(1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PGOOD						
V_{PGD}	PGOOD trip threshold for falling FB	Measured with respect to V_{REF}		–9		%
	PGOOD trip threshold for rising FB	Measured with respect to V_{REF}		10		%
	Hysteresis			1.6		%
$I_{LEAK(PGD)}$	PGOOD leakage current				100	nA
$I_{SINK(PGD)}$	PGOOD sink current	V_{PGOOD} = 0.4 V	2	4.2	6.5	mA
OUTPUT OVP						
V_{OVP}	Output overvoltage threshold	At the FB pin		0.86		V
	Hysteresis			21		mV
NMOS DRIVERS						
$I_{HDRV1,2}$	Driver peak source current	V_{BOOT} - V_{SW} = 7 V		1.8		A
	Driver peak sink current	V_{BOOT} - V_{SW} = 7 V		2.2		
$I_{LDRV1,2}$	Driver peak source current			1.8		
	Driver peak sink current			2.2		
$R_{HDRV1,2}$	Driver pull up resistance	V_{BOOT} - V_{SW} = 7 V		1.9		Ω
	Driver pull down resistance	V_{BOOT} - V_{SW} = 7 V		1.3		
$V_{UV(BOOT1,2)}$	BOOT1,2 to SW1,2 UVLO threshold	HDRV1,2 shut off		2.73		V
	BOOT1,2 to SW1,2 UVLO hysteresis	HDRV1,2 start switching		280		mV
	BOOT1,2 to SW1,2 threshold for refresh pulse			4.45		V
$R_{LDRV1,2}$	Driver pull up resistance	$I_{DRV1,2}$ = 0.1 A		2		Ω
	Driver pull down resistance	$I_{DRV1,2}$ = 0.1 A		1.5		
t_{DT1}	Dead time HDRV1,2 off to LDRV1,2 on			55		ns
t_{DT2}	Dead time LDRV1,2 off to HDRV1,2 on			55		
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			165		°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis			15		

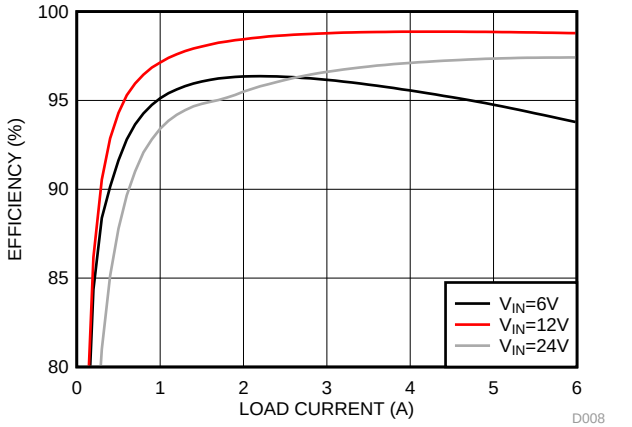
7.6 Typical Characteristics

At T_A = 25°C, unless otherwise stated.



V_{OUT}=12 V Fsw=300 kHz L1=4.7 µH
I_{OUT}=3 A

Figure 1. Efficiency vs V_{IN}



V_{OUT} =12 V Fsw=300 kHz L1=4.7 µH

Figure 2. Efficiency vs Load

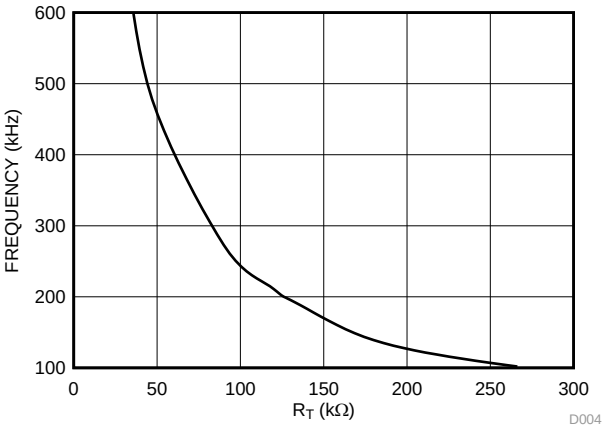


Figure 3. Oscillator Frequency

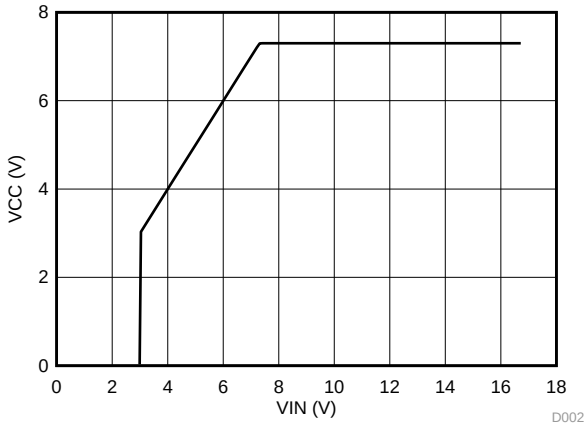


Figure 4. VCC vs V_{IN}

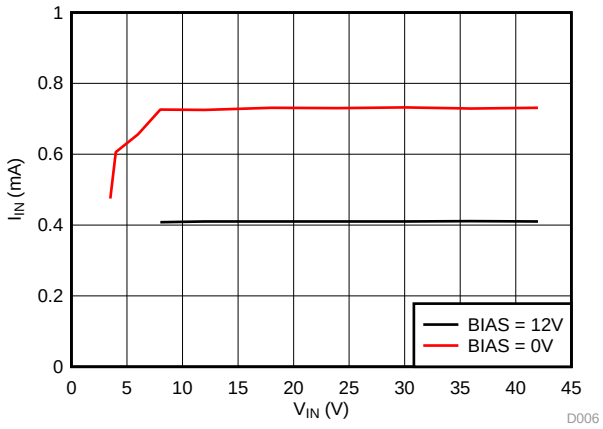


Figure 5. I_{IN} Standby

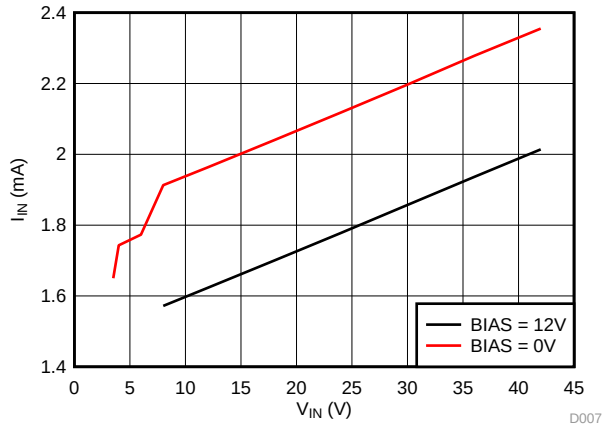


Figure 6. I_{IN} Operating vs V_{IN}

Typical Characteristics (continued)

At T_A = 25°C, unless otherwise stated.

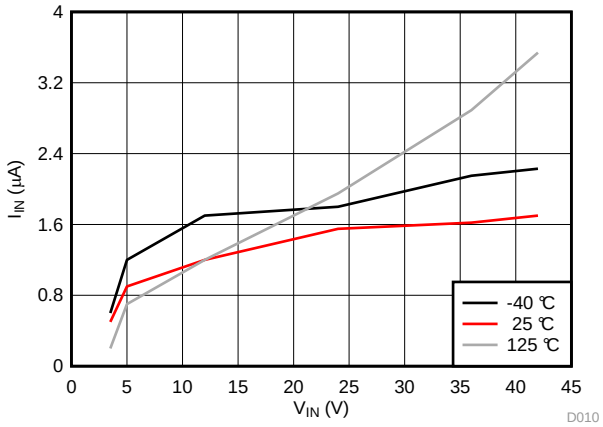


Figure 7. I_{IN} Shutdown vs V_{IN}

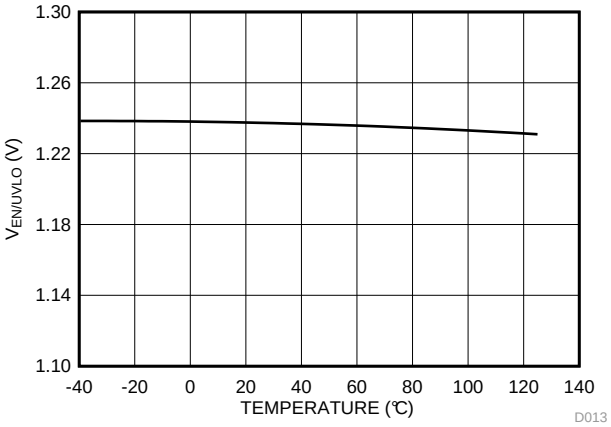


Figure 8. ENABLE/UVLO Rising Threshold vs Temperature

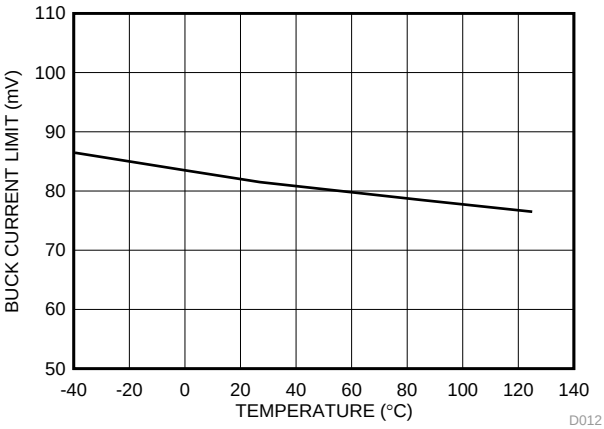


Figure 9. Buck Current Limit vs Temperature

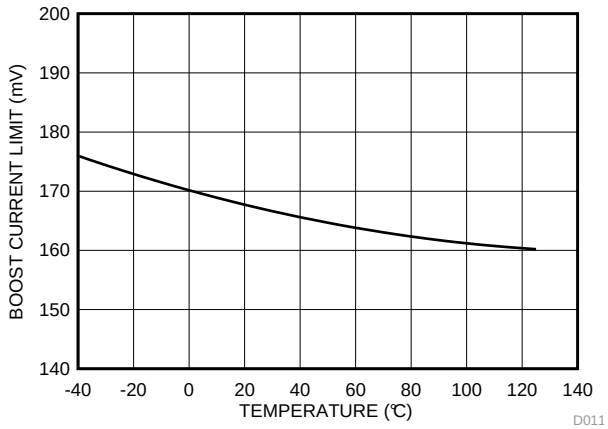


Figure 10. Boost Current Limit vs Temperature

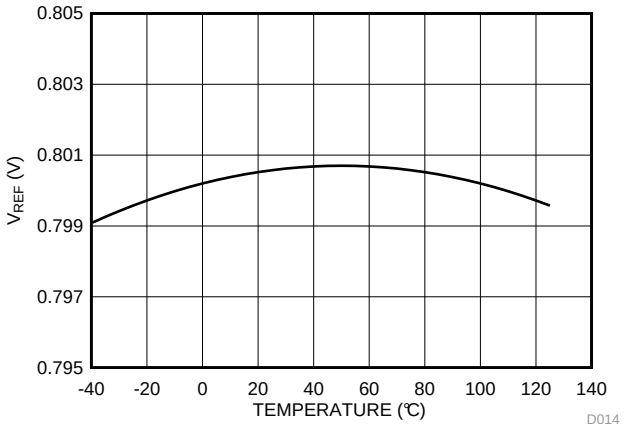
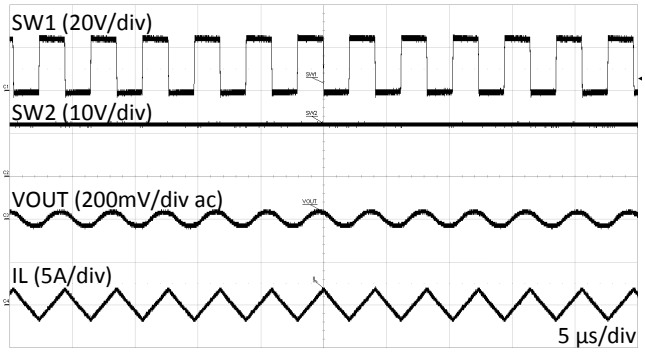


Figure 11. V_{REF} vs Temperature



VOUT=12 V VIN=24 V

Figure 12. Forced CCM Operation (Buck)

Typical Characteristics (continued)

At T_A = 25°C, unless otherwise stated.

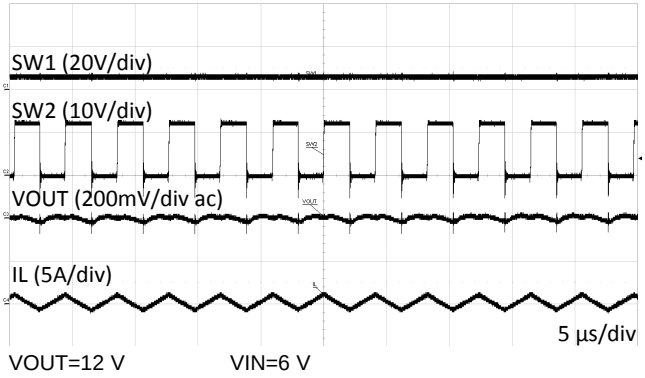


Figure 13. Forced CCM Operation (Boost)

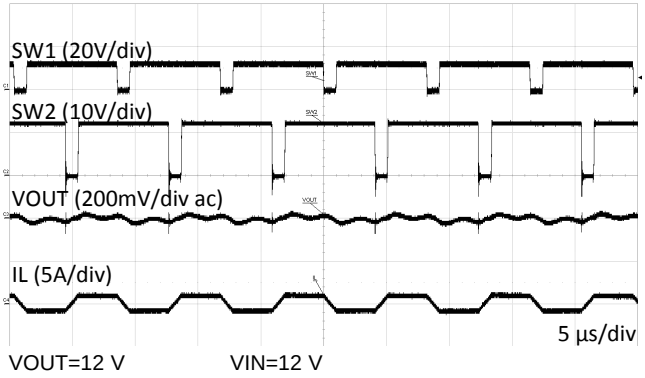


Figure 14. Forced CCM Operation (Buck-Boost)

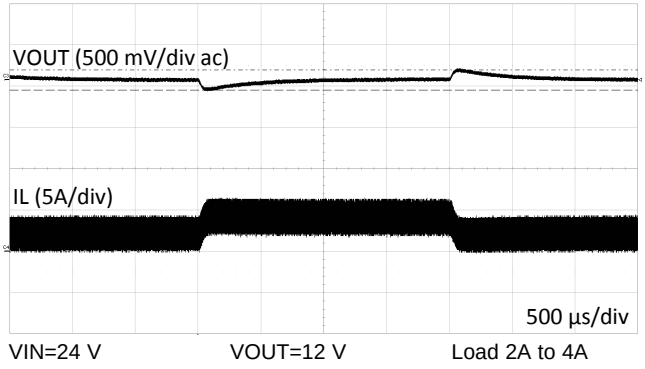


Figure 15. Load Step (Buck)

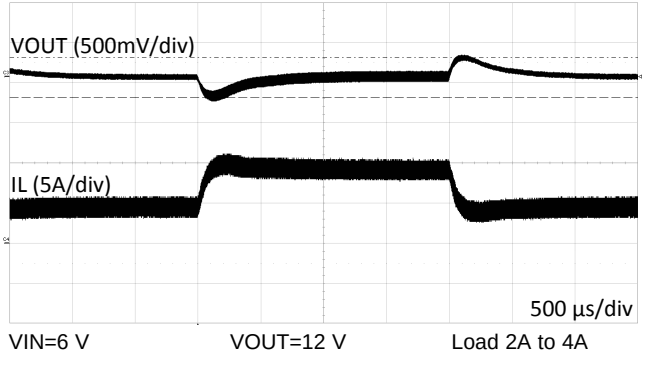


Figure 16. Load Step (Boost)

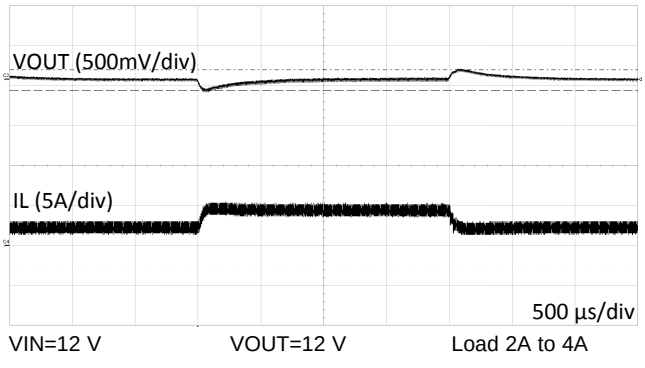


Figure 17. Load Step (Buck-Boost)

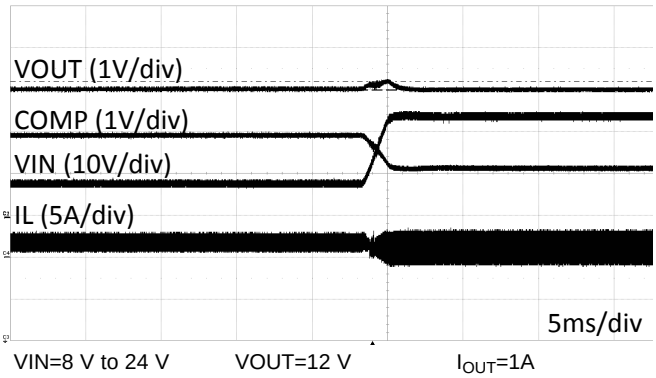


Figure 18. Line Transient

Typical Characteristics (continued)

At T_A = 25°C, unless otherwise stated.

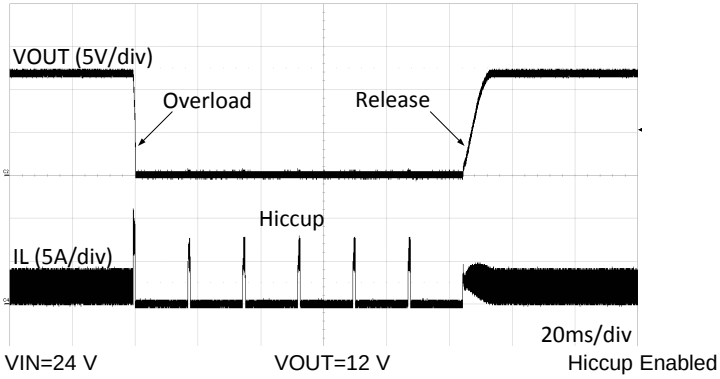


Figure 19. Hiccup Mode Current Limit

8 Detailed Description

8.1 Overview

The LM5175 is a wide input voltage four-switch buck-boost controller IC with integrated drivers for N-channel MOSFETs. It operates in the buck mode when V_{IN} is greater than V_{OUT} and in the boost mode when V_{IN} is less than V_{OUT}. When V_{IN} is close to V_{OUT}, the device operates in a proprietary transition buck or boost mode. The control scheme provides smooth operation for any input/output combination within the specified operating range. The buck or boost transition control scheme provides a low ripple output voltage when V_{IN} equals V_{OUT} without compromising the efficiency.

The LM5175 integrates four N-Channel MOSFET drivers including two low-side drivers and two high-side drivers, eliminating the need for external drivers or floating bias supplies. The internal VCC regulator supplies internal bias rails as well as the MOSFET gate drivers. The VCC regulator is powered either from the input voltage through the VIN pin or from the output or an external supply through the BIAS pin for improved efficiency.

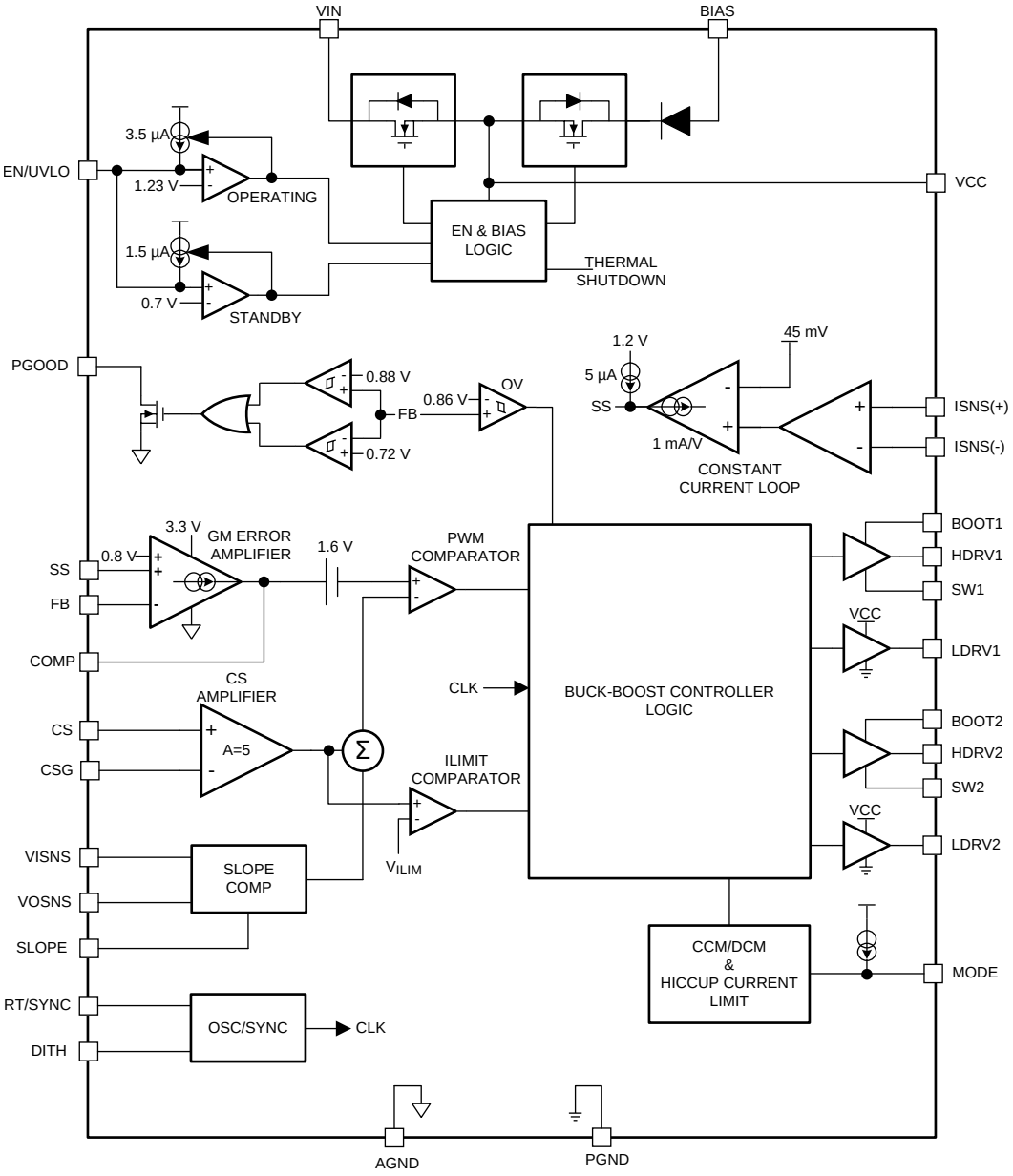
The PWM control scheme is based on valley current mode control for buck operation and peak current mode control for boost operation. The inductor current is sensed through a single sense resistor in series with the low-side MOSFETs. The sensed current is also monitored for cycle-by-cycle current limit. The behavior of the LM5175 during an overload condition is dependent on the MODE pin programming (see *MODE Pin Configuration*). If hiccup mode fault protection is selected, the controller turns off after a fixed number of switching cycles in cycle-by-cycle current limit and restarts after another fixed number of clock cycles. The hiccup mode reduces the heating in the power components in a sustained overload condition. If hiccup mode is disabled through the MODE pin, the controller remains in a cycle-by-cycle current limit condition until the overload is removed. The MODE pin also selects continuous conduction mode (CCM) for noise sensitive applications or discontinuous conduction mode (DCM) for higher light load efficiency.

In addition to the cycle-by-cycle current limiting, the LM5175 also provides an optional average current regulation loop that can be configured for either input or output current limiting. This is useful for battery charging or other applications where a constant current behavior may be required.

The soft-start time of LM5175 is programmed by a capacitor connected to the SS pin to minimize the inrush current and overshoot during startup.

The precision EN/UVLO pin supports programmable input undervoltage lockout (UVLO) with hysteresis. The output overvoltage protection (OVP) feature turns off the high-side drivers when the voltage at the FB pin is 7.5% above the nominal 0.8-V V_{REF}. The PGOOD output indicates when the FB voltage is inside a ±10% regulation window centered at V_{REF}.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency Valley/Peak Current Mode Control with Slope Compensation

The LM5175 implements a fixed frequency current mode control of both the buck and boost switches. The output voltage, scaled down by the feedback resistor divider, appears at the FB pin and is compared to the internal reference (V_{REF}) by an internal error amplifier. The error amplifier produces an error voltage by driving the COMP pin. An adaptive slope compensation signal based on V_{IN}, V_{OUT}, and the capacitor at the SLOPE pin is added to the current sense signal measured across the CS and CSG pins. The result is compared to the COMP error voltage by the PWM comparator.

Feature Description (continued)

The LM5175 regulates the output using valley current mode control in buck mode and peak current mode control in boost mode. For valley current mode control, the high-side buck MOSFET controlled by HDRV1 is turned on by the PWM comparator at the valley of the inductor ripple current and turned off by the oscillator clock signal. Valley current mode control is advantageous for buck converters where the PWM controller must resolve very short on-times. For peak current mode control in the boost mode, the low-side boost MOSFET controlled by LDRV2 is turned on by the clock signal in each switching cycle and turned off by the PWM comparator at the peak of the inductor ripple current.

The low-side gate drive LDRV1, complementary to the HDRV1 drive signal, controls the synchronous rectification MOSFET of the buck stage. The high-side gate drive HDRV2, complementary to the low-side gate drive LDRV2, controls the high-side synchronous rectifier of the boost stage. For operation with V_{IN} close to V_{OUT}, the LM5175 uses a proprietary buck or boost transition scheme to achieve smooth, low ripple transition zone behavior.

Peak and valley current mode controllers require slope compensation for stable current loop operation at duty cycle greater than 50% in peak current mode control and less than 50% in valley current mode control. The LM5175 provides a SLOPE pin to program optimum slope for any V_{IN} and V_{OUT} combination using an external capacitor.

8.3.2 VCC Regulator and Optional BIAS Input

The VCC regulator provides a regulated 7.5-V bias supply to the gate drivers. When EN/UVLO is above the 0.7-V (typical) standby threshold, the VCC regulator is turned on. For V_{IN} less than 7.5 V, the VCC voltage tracks V_{IN} with a small voltage drop as shown in Figure 4. If the EN/UVLO input is above the 1.23 V operating threshold and VCC exceeds the 3.3 V (typical) VCC UV threshold, the controller is enabled and switching begins.

The VCC regulator draws power from V_{IN} when there is no supply voltage connected to the BIAS pin. If the BIAS pin is connected to an external voltage source that exceeds VCC by one diode drop, the VCC regulator draws power from the BIAS input instead of V_{IN}. Connecting the BIAS pin to V_{OUT} in applications with V_{OUT} greater than 8.5 V improves the efficiency of the regulator in the buck mode. The BIAS pin voltage should not exceed 36 V.

For low V_{IN} operation, ensure that the VCC voltage is sufficient to fully enhance the MOSFETs. Use an external bias supply if V_{IN} dips below the voltage required to sustain the VCC voltage. For these conditions, use a series blocking diode between the input supply and the VIN pin (Figure 20). This prevents VCC from back-feeding into V_{IN} through the body diode of the VCC regulator.

A 1-µF capacitor to PGND is required to supply the VCC regulator load transients.

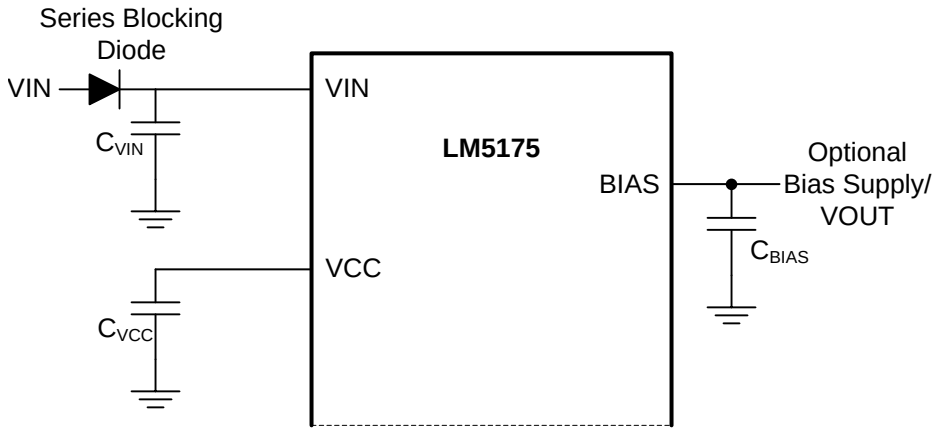


Figure 20. VCC Regulator

Feature Description (continued)

8.3.3 Enable/UVLO

The LM5175 has a dual function enable and undervoltage lockout (UVLO) circuit. The EN/UVLO pin has three distinct voltage ranges: shutdown, standby, and operating (see *Shutdown, Standby, and Operating Modes*). When the EN/UVLO pin is below the standby threshold (0.7 V typical), the converter is held in a low power shutdown mode. When EN/UVLO voltage is greater than the standby threshold but less than the 1.23 V operating threshold, the internal bias rails and the VCC regulator are enabled but the soft-start (SS) pin is held low and the PWM controller is disabled. A 1.5 µA pull-up current is sourced out of the EN/UVLO pin in standby mode to provide hysteresis between the shutdown mode and the standby mode. When EN/UVLO is greater than the 1.23 V operating threshold, the controller commences operation if VCC is above VCC UV threshold (3.3 V). A hysteresis current of 3.5 µA is sourced into the EN/UVLO pin when the EN/UVLO input exceeds the 1.23 V operation threshold to provide hysteresis that prevents on/off chattering in the presence of noise with a slowly changing input voltage.

The V_{IN} undervoltage lockout turn-on threshold is typically set by a resistor divider from the VIN pin to AGND with the mid-point of the divider connected to EN/UVLO. The turn-on threshold VIN_{UV} is calculated using Equation 1 where R_{UV2} is the upper resistor and R_{UV1} is the lower resistor in the EN/UVLO resistor divider:

$$V_{IN(UV)} = 1.23\ V \times \left(1 + \frac{R_{UV2}}{R_{UV1}}\right) - R_{UV2} \times 1.5\ \mu A \quad (1)$$

The hysteresis between the UVLO turn-on threshold and turn-off threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by:

$$\Delta V_{HYS(UV)} = 3.5\ \mu A \times R_{UV2} \quad (2)$$

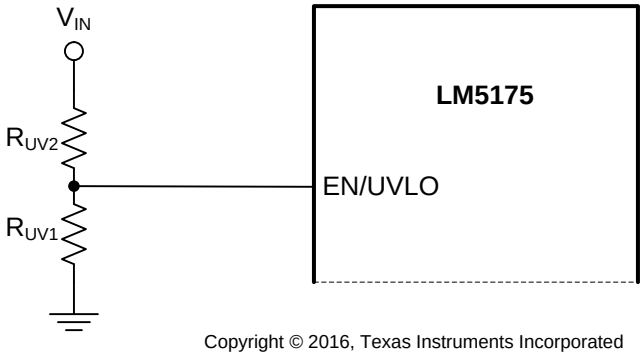


Figure 21. UVLO Threshold Programming

8.3.4 Soft-Start

The LM5175 soft-start time is programmed using a soft-start capacitor from the SS pin to AGND. When the converter is enabled, an internal 5-µA current source charges the soft-start capacitor. When the SS pin voltage is below the 0.8-V feedback reference voltage V_{REF}, the soft-start pin controls the regulated FB voltage. Once SS exceeds V_{REF}, the soft-start interval is complete and the error amplifier is referenced to V_{REF}. The soft-start time is given by Equation 3:

$$t_{ss} = \frac{C_{SS} \times 0.8\ V}{5\ \mu A} \quad (3)$$

The soft-start capacitor is internally discharged when the converter is disabled because of EN/UVLO falling below the operation threshold or VCC falling below the VCC UV threshold. The soft-start pin is also discharged when the converter is in hiccup mode current limiting or in thermal shutdown. When average input or output current limiting is active, the soft-start capacitor is discharged by the constant current loop transconductance (gm) amplifier to limit either input or output current.

Feature Description (continued)

8.3.5 Overcurrent Protection

The LM5175 provides cycle-by-cycle current limit to protect against overcurrent and short circuit conditions. In buck operation, the sensed valley voltage across the CSG and CS pins is limited to 76 mV. The high-side buck switch skips a cycle if the sensed voltage does not fall below this threshold during the buck switch off time. In boost operation, the maximum peak voltage across CS and CSG is limited to 170mV. If the peak current in the low-side boost switch causes the CS pin to exceed this threshold voltage, the boost switch is turned off for the remainder of the clock cycle.

Applying the appropriate voltage to the MODE pin of the LM5175 enables hiccup mode fault protection (see *MODE Pin Configuration*). In the hiccup mode, the controller shuts down after detecting cycle-by-cycle current limiting for 128 consecutive cycles and the soft-start capacitor is discharged. The soft-start capacitor is automatically released after 4000 oscillator clock cycles and the controller restarts. If hiccup mode protection is not enabled through the MODE pin, the LM5175 will operate in cycle-by-cycle current limiting as long as the overload condition persists.

8.3.6 Average Input/Output Current Limiting

The LM5175 provides optional average current limiting capability to limit either the input or the output current of the DC/DC converter. The average current limiting circuit uses an additional current sense resistor connected in series with the input supply or output voltage of the converter. A current sense gm amplifier with inputs at the ISNS(+) and ISNS(-) pins monitors the voltage across the sense resistor and compares it with an internal 50 mV reference. If the drop across the sense resistor is greater than 50 mV, the gm amplifier gradually discharges the soft-start capacitor. When the soft-start capacitor discharges below the 0.8-V feedback reference voltage V_{REF}, the output voltage of the converter decreases to limit the input or output current. The average current limiting feature can be used in applications requiring a regulated current from the input supply or into the load. The target constant current is given by Equation 4:

$$I_{CL(AVG)} = \frac{50\ mV}{R_{SNS}} \tag{4}$$

The average current loop can be disabled by shorting the ISNS(+) and ISNS(-) pins together.

8.3.7 CCM/DCM Operation

The LM5175 allows selection of continuous conduction mode (CCM) or discontinuous conduction mode (DCM) operation using the MODE pin (see *MODE Pin Configuration*). In CCM operation the inductor current can flow in either direction and the controller switches at a fixed frequency regardless of the load current. This mode is useful for noise-sensitive applications where a fixed switching eases filter design. In DCM operation the synchronous rectifier MOSFETs emulate diodes as LDRV1 or HDRV2 turn-off for the remainder of the PWM cycle when the inductor current reaches zero. The DCM mode results in reduced frequency operation at light loads, which lowers switching losses and increases light load efficiency of the converter.

8.3.8 Frequency and Synchronization (RT/SYNC)

The LM5175 switching frequency can be programmed between 100 kHz and 600 kHz using a resistor from the RT/SYNC pin to AGND. The R_T resistor is related to the nominal switching frequency (F_{sw}) by the following equation:

$$R_T = \frac{\left(\frac{1}{F_{sw}}\right) - 200\ ns}{37\ pF} \tag{5}$$

Figure 3 in the *Typical Characteristics* shows the relationship between the programmed switching frequency (F_{sw}) and the R_T resistor.

The RT/SYNC pin can also be used for synchronizing the internal oscillator to an external clock signal. The external synchronization pulse is ac coupled using a capacitor to the RT/SYNC pin. The voltage at the RT/SYNC pin must not exceed 3.3 V peak. The external synchronization pulse frequency should be higher than the internally set oscillator frequency and the pulse width should be between 75 ns and 500 ns.

Feature Description (continued)

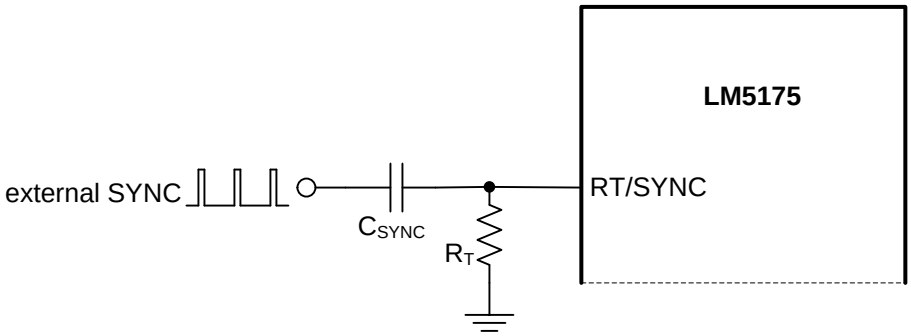


Figure 22. Using External SYNC

8.3.9 Frequency Dithering

The LM5175 provides an optional frequency dithering function that is enabled by connecting a capacitor from DITH to AGND. Figure 23 illustrates the dithering circuit. A triangular waveform centered at 1.22 V is generated across the C_{DITH} capacitor. This triangular waveform modulates the oscillator frequency by ±5% of the nominal frequency set by the R_T resistor. The C_{DITH} capacitance value sets the rate of the low frequency modulation. A lower C_{DITH} capacitance will modulate the oscillator frequency at a faster rate than a higher capacitance. For the dithering circuit to effectively reduce peak EMI, the modulation rate must be much less than the oscillator frequency (F_{sw}). Equation 6 calculates the DITH pin capacitance required to set the modulation frequency, F_{MOD}. Connecting the DITH pin directly to AGND disables frequency dithering, and the internal oscillator operates at a fixed frequency set by the RT resistor. Dither is disabled when external SYNC is used.

$$C_{DITH} = \frac{10\ \mu A}{F_{MOD} \times 0.24\ V} \tag{6}$$

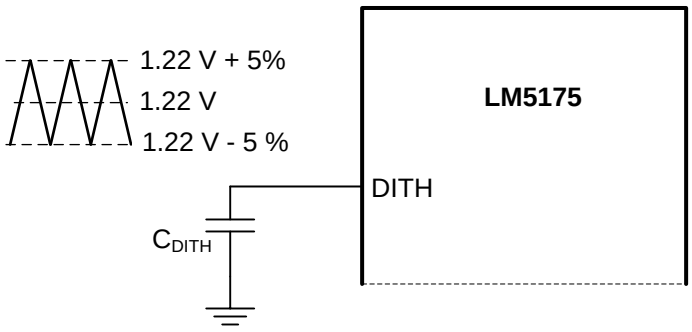


Figure 23. Dither Operation

8.3.10 Output Overvoltage Protection (OVP)

The LM5175 provides an output overvoltage protection (OVP) circuit that turns off the gate drives when the feedback voltage is 7.5% above the 0.8 V feedback reference voltage V_{REF}. Switching resumes once the output falls within 5% of V_{REF}.

8.3.11 Power Good (PGOOD)

PGOOD is an open drain output that is pulled low when the voltage at the FB pin is outside -9% / +10% of the nominal 0.8-V reference voltage. The PGOOD internal N-Channel MOSFET pull-down strength is typically 4.2 mA. This pin can be connected to a voltage supply of up to 8 V through a pull-up resistor.

Feature Description (continued)

8.3.12 Gm Error Amplifier

The LM5175 has a gm error amplifier for loop compensation. The gm amplifier output (COMP) range is 0.3 V to 3 V. Connect an R_{c1}-C_{c1} compensation network between COMP and ground for type II (PI) compensation (see Figure 24). Another pole is usually added using C_{c2} to suppress higher frequency noise.

The COMP output voltage (V_{COMP}) range limits the possible V_{IN} and I_{OUT} range for a given design. In buck mode, the maximum V_{IN} for which the converter can regulate the output at no load is when V_{COMP} reaches 0.3 V. Equation 7 gives V_{COMP} as a function of V_{IN} at no load in CCM buck mode:

$$V_{COMP(BUCK)} = 1.6\ V - A_{CS} \cdot R_{SENSE} \cdot \frac{V_{OUT}}{2 \cdot L1 \cdot F_{sw}} \cdot (1 - D_{BUCK}) - \frac{2\ \mu S \cdot (V_{IN} - V_{OUT}) + 6\ \mu A}{C_{SLOPE} \cdot F_{sw}} \cdot (1 - D_{BUCK}) \quad (7)$$

Where D_{BUCK} in the equation Equation 7 is the buck duty cycle given by:

$$D_{BUCK} = \frac{V_{OUT}}{V_{IN}} \quad (8)$$

A larger L1, lower slope ripple (higher C_{SLOPE}), smaller sense resistor (R_{SENSE}), and higher frequency can increase the maximum V_{IN} range for buck operation.

For boost mode, the minimum V_{IN} for which the converter can regulate the output at full load is when V_{COMP} reaches 3 V. Equation 9 gives V_{COMP} as a function of V_{IN} in boost mode:

$$V_{COMP(BOOST)} = 1.6\,V + A_{CS} \cdot R_{SENSE} \cdot \left(I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} + \frac{V_{IN}}{2 \cdot L1 \cdot F_{sw}} \cdot D_{BOOST} \right) + \frac{2\,\mu S \cdot (V_{OUT} - V_{IN}) + 5\,\mu A}{C_{SLOPE} \cdot F_{sw}} \cdot D_{BOOST} \quad (9)$$

Where D_{BOOST} in the Equation 9 is the boost duty cycle given by:

$$D_{BOOST} = 1 - \frac{V_{IN}}{V_{OUT}} \quad (10)$$

A larger L1, lower slope ripple (higher C_{SLOPE}), smaller sense resistor (R_{SENSE}), and higher frequency can extend the minimum V_{IN} range for boost operation.

8.3.13 Integrated Gate Drivers

The LM5175 provides four N-channel MOSFET gate drivers: two floating high-side gate drivers at the HDRV1 and HDRV2 pins, and two ground referenced low-side drivers at the LDRV1 and LDRV2 pins. Each driver is capable of sourcing 1.5 A and sinking 2 A peak current. In buck operation, LDRV1 and HDRV1 are switched by the PWM controller while HDRV2 remains continuously on. In boost operation, LDRV2 and HDRV2 are switched while HDRV1 remains continuously on.

In DCM buck operation, LDRV1 and HDRV2 turn off when the inductor current drops to zero (diode emulation). In a DCM boost operation, HDRV2 turns off when inductor current drops to zero.

The gate drive output HDRV2 remains off during soft-start to prevent reverse current flow from a pre-biased output.

The low-side gate drivers are powered from VCC and the high-side gate drivers HDRV1 and HDRV2 are powered from bootstrap capacitors C_{BOOT1} (between BOOT1 and SW1) and C_{BOOT2} (between BOOT2 and SW2) respectively. The C_{BOOT1} and C_{BOOT2} capacitors are charged through external Schottky diodes connected to the VCC pin as shown in Figure 24.

8.3.14 Thermal Shutdown

The LM5175 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 165°C (typical). The soft-start capacitor is discharged when thermal shutdown is triggered and the gate drivers are disabled. The converter automatically restarts when the junction temperature drops by the thermal shutdown hysteresis of 15°C below the thermal shutdown threshold.

8.4 Device Functional Modes

Please refer to *Enable/UVLO* section for the description of EN/UVLO pin function. *Shutdown, Standby, and Operating Modes* section lists the shutdown, standby, and operating modes for LM5175 as a function of EN/UVLO and VCC voltages.

8.4.1 Shutdown, Standby, and Operating Modes

EN/UVLO	VCC	DEVICE MODE
EN/UVLO < 0.7 V	—	Shutdown: VCC off, No switching
0.7 V < EN/UVLO < 1.23 V	—	Standby: VCC on, No switching
EN/UVLO > 1.23 V	VCC < 3.3 V	Standby: VCC on, No switching
EN/UVLO > 1.23 V	VCC > 3.3 V	Operating: VCC on, Switching enabled

8.4.2 MODE Pin Configuration

The MODE pin is used to select CCM/DCM operation and hiccup mode current limit. Mode is latched at startup.

MODE PIN CONNECTION	LIGHT LOAD MODE	HICCUP FAULT PROTECTION
Connect to VCC	CCM	No Hiccup
RMODE to AGND = 93.1 kΩ	CCM	Hiccup Enabled
RMODE to AGND = 49.9 kΩ	DCM	Hiccup Enabled
Connect to AGND	DCM	No Hiccup

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM5175 is a four-switch buck-boost controller. A quick-start tool on the LM5175 product webpage can be used to design a buck-boost converter using the LM5175. Alternatively, Webench®software can create a complete buck-boost design using the LM5175 and generate bill of materials, estimate efficiency, solution size, and cost of the complete solution. The following sections describe a detailed step-by-step design procedure for a typical application circuit.

9.2 Typical Application

A typical application example is a buck-boost converter operating from a wide input voltage range of 6 V to 36 V and providing a stable 12 V output voltage with current capability of 6 A.

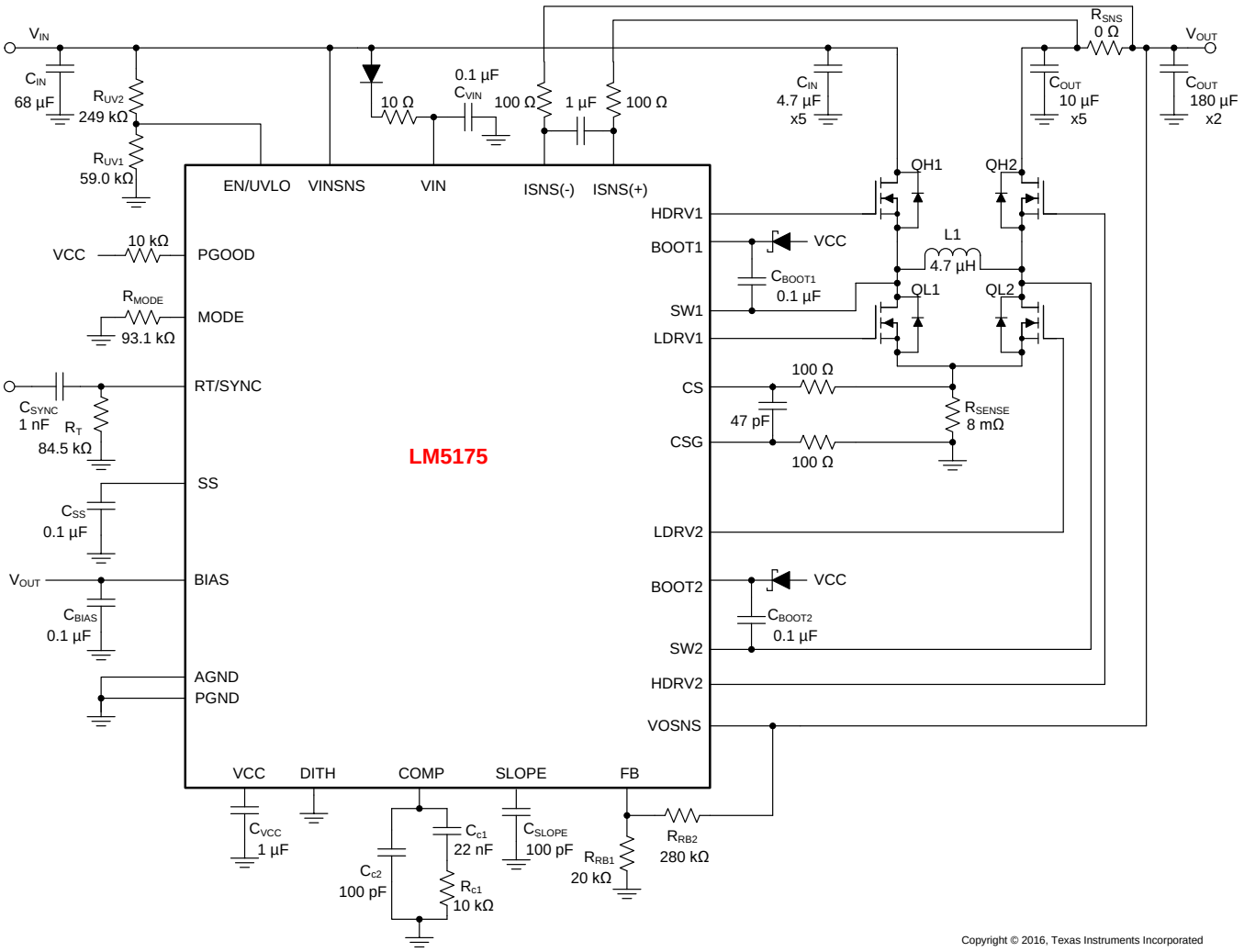


Figure 24. LM5175 Four-Switch Buck Boost Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

For this design example, the following are used as the input parameters.

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	6 V to 36 V
Output	12 V
Load Current	6 A
Switching Frequency	300 kHz
Mode	CCM, Hiccup

9.2.2 Detailed Design Procedure

9.2.2.1 Frequency

The switching frequency of LM5175 is set by an R_T resistor connected from RT/SYNC pin to AGND. The R_T resistor required to set the desired frequency is calculated using Equation 5 or Figure 3 . A 1% standard resistor of 84.5 kΩ is selected for F_{sw} = 300 kHz.

9.2.2.2 V_{OUT}

The output voltage is set using a resistor divider to the FB pin. The internal reference voltage is 0.8 V. Normally the bottom resistor in the resistor divider is selected to be in the 1 kΩ to 100 kΩ range. Select

$$R_{FB1} = 20\ k\Omega \tag{11}$$

The top resistor in the feedback resistor divider is selected using Equation 12:

$$R_{FB2} = \frac{V_{OUT} - 0.8\ V}{0.8\ V} \times R_{FB1} = 280\ k\Omega \tag{12}$$

9.2.2.3 Inductor Selection

The inductor selection is based on consideration of both buck and boost modes of operation. For the buck mode, inductor selection is based on limiting the peak to peak current ripple ΔI_L to ~40% of the maximum inductor current at the maximum input voltage. The target inductance for the buck mode is:

$$L_{BUCK} = \frac{(V_{IN(MAX)} - V_{OUT}) \times V_{OUT}}{0.4 \times I_{OUT(MAX)} \times F_{sw} \times V_{IN(MAX)}} = 11.1\ \mu H \tag{13}$$

For the boost mode, the inductor selection is based on limiting the peak to peak current ripple ΔI_L to ~40% of the maximum inductor current at the minimum input voltage. The target inductance for the boost mode is:

$$L_{BOOST} = \frac{V_{IN(MIN)}^2 \times (V_{OUT} - V_{IN(MIN)})}{0.4 \times I_{OUT(MAX)} \times F_{sw} \times V_{OUT}^2} = 2.1\ \mu H \tag{14}$$

In this particular application, the buck inductance is larger. Choosing a larger inductance reduces the ripple current but also increases the size of the inductor. A larger inductor also reduces the achievable bandwidth of the converter by moving the right half plane zero to lower frequencies. Therefore a judicious compromise should be made based on the application requirements. For this design a 4.7-µH inductor is selected. With this inductor selection, the inductor current ripple is 5.7 A, 4.3 A, and 2.1 A, at V_{IN} of 36 V, 24 V, and 6 V respectively.

The maximum average inductor current occurs at the minimum input voltage and maximum load current:

$$I_{L(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{0.9 \times V_{IN(MIN)}} = 13.3\ A \tag{15}$$

where a 90% efficiency is assumed. The peak inductor current occurs at minimum input voltage and is given by:

$$I_{L(PEAK)} = I_{L(MAX)} + \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{2 \times L1 \times F_{sw} \times V_{OUT}} = 14.4\ A \tag{16}$$

To ensure sufficient output current, the current limit threshold must be set to allow the maximum load current in boost operation. To ensure that the inductor does not saturate in current limit, the peak saturation current of the inductor should be higher than the maximum current limit. Adjusting for a ±20% current limit threshold tolerance, the peak inductor current limit is:

$$I_{L(SAT)} = \frac{1.2 \times I_{L(PEAK)}}{0.8} = 21.6 \text{ A} \quad (17)$$

Therefore, the inductor saturation current should be greater than 21.6 A. If hiccup mode protection is not enabled, the RMS current rating of the inductor should be sufficient to tolerate continuous operation in cycle-by-cycle current limiting.

9.2.2.4 Output Capacitor

In the boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by Equation 18 where the minimum V_{IN} corresponds to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (18)$$

In this example the maximum output ripple RMS current is $I_{COUT(RMS)}$ = 6 A. A 5-mΩ output capacitor ESR causes an output ripple voltage of 60 mV as given by:

$$\Delta V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN(MIN)}} \times ESR \quad (19)$$

A 400 µF output capacitor causes a capacitive ripple voltage of 25 mV as given by:

$$\Delta V_{RIPPLE(COUT)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)}{C_{OUT} \times F_{sw}} \quad (20)$$

Typically a combination of ceramic and bulk capacitors is needed to provide low ESR and high ripple current capacity. The complete schematic in Figure 24 at the end of this section shows a good starting point for C_{OUT} for typical applications.

9.2.2.5 Input Capacitor

In the buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitor is given by:

$$I_{CIN(RMS)} = I_{OUT} \sqrt{D \times (1 - D)} \quad (21)$$

The maximum RMS current occurs at D = 0.5, which gives $I_{CIN(RMS)} = I_{OUT}/2$ = 3 A. A combination of ceramic and bulk capacitors should be used to provide short path for high di/dt current and to reduce the output voltage ripple. The complete schematic in Figure 24 is a good starting point for C_{IN} for typical applications.

9.2.2.6 Sense Resistor (R_{SENSE})

The current sense resistor between the CS and CSG pins should be selected to ensure that current limit is set high enough for both buck and boost modes of operation. For the buck operation, the current limit resistor is given by:

$$R_{SENSE(BUCK)} = \frac{76 \text{ mV} \times 70\%}{I_{OUT(MAX)}} = 8.8 \text{ m}\Omega \quad (22)$$

For the boost mode of operation, the current limit resistor is given by:

$$R_{SENSE(BOOST)} = \frac{170 \text{ mV} \times 70\%}{I_{L(PEAK)}} = 8.2 \text{ m}\Omega \quad (23)$$

The closest standard value of R_{SENSE} = 8 mΩ is selected based on the boost mode operation.

The maximum power dissipation in R_{SENSE} happens at $V_{IN(MIN)}$:

$$P_{RSENSE(MAX)} = \left(\frac{170\,mV}{R_{SENSE}}\right)^2 \cdot R_{SENSE} \cdot \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right) = 1.8\,W \quad (24)$$

Based on this, select the current sense resistor with power rating of 2 W or higher.

For some application circuits, it may be required to add a filter network to attenuate noise in the CS and CSG sense lines. Please see Figure 24 for typical values. The filter resistance should not exceed 100 Ω.

9.2.2.7 Slope Compensation

For stable current loop operation and to avoid sub-harmonic oscillations, the slope capacitor should be selected based on Equation 25:

$$C_{SLOPE} = gm_{SLOPE} \times \frac{L1}{R_{SENSE} \times A_{CS}} = 2\,\mu S \times \frac{4.7\,\mu H}{8\,m\Omega \times 5} = 235\,pF \quad (25)$$

This slope compensation results in “dead-beat” operation, in which the current loop disturbances die out in one switching cycle. Theoretically a current mode loop is stable with half the “dead-beat” slope (twice the calculated slope capacitor value in Equation 25). A smaller slope capacitor results in larger slope signal which is better for noise immunity in the transition region (V_{IN}~V_{OUT}). A larger slope signal, however, restricts the achievable input voltage range for a given output voltage, switching frequency, and inductor. For this design C_{SLOPE} = 100 pF is selected for better transition region behavior while still providing the required V_{IN} range. This selection of slope capacitor, inductor, switching frequency, and inductor satisfies the COMP range limitation explained in Gm Error Amplifier section.

9.2.2.8 UVLO

The UVLO resistor divider must be designed for turn-on below 6V. Selecting a R_{UV2} = 249 kΩ gives a UVLO hysteresis of 0.8 V. The lower UVLO resistor is the selected using Equation 26:

$$R_{UV1} = \frac{R_{UV2} \times 1.23\,V}{V_{IN(UV)} + 1.5\,\mu A \times R_{UV2} - 1.23\,V} = 59.5\,k\Omega \quad (26)$$

A standard value of 59.0 kΩ is selected for R_{UV1}.

When programming the UVLO threshold for lower input voltage operation, it is important to choose MOSFETs with gate (Miller) plateau voltage lower than the minimum V_{IN}.

9.2.2.9 Soft-Start Capacitor

The soft-start time is programmed using the soft-start capacitor. The relationship between C_{SS} and the soft-start time is given by:

$$t_{ss} = \frac{0.8\,V \times C_{SS}}{5\,\mu A} \quad (27)$$

C_{SS} = 0.1 µF gives a soft-start time of 16 ms.

9.2.2.10 Dither Capacitor

The dither capacitor sets the modulation frequency of the frequency dithering around the nominal switching frequency. A larger C_{DITH} results in lower modulation frequency. For proper operation the modulation frequency (F_{MOD}) must be much lower than the switching frequency. Use Equation 28 to select C_{DITH} for the target modulation frequency.

$$C_{DITH} = \frac{10\,\mu A}{F_{MOD} \times 0.24\,V} \quad (28)$$

For the current design dithering is not being implemented. Therefore a 0 Ω resistor from the DITH pin to AGND disables this feature.

9.2.2.11 MOSFETs QH1 and QL1

The input side MOSFETs QH1 and QL1 need to withstand the maximum input voltage of 36 V. In addition they must withstand the transient spikes at SW1 during switching. Therefore QH1 and QL1 should be rated for 60 V. The gate plateau voltages of the MOSFETs should be smaller than the minimum input voltage of the converter, otherwise the MOSFETs may not fully enhance during startup or overload conditions.

The power loss in QH1 in the boost mode of operation is approximated by:

$$P_{COND(QH1)} = \left(I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} \right)^2 \cdot R_{DSON(QH1)} \tag{29}$$

The power loss in QH1 in the buck mode of operation consists of both conduction and switching loss components given by Equation 30 and Equation 31 respectively:

$$P_{COND(QH1)} = \left(\frac{V_{OUT}}{V_{IN}} \right) \cdot {I_{OUT}}^2 \cdot R_{DSON(QH1)} \tag{30}$$

$$P_{SW(QH1)} = \frac{1}{2} \cdot V_{IN} \cdot I_{OUT} \cdot \left(t_r + t_f \right) \cdot F_{sw} \tag{31}$$

The rise (t_r) and the fall (t_f) times are based on the MOSFET datasheet information or measured in the lab. Typically a MOSFET with smaller R_{DSON} (smaller conduction loss) will have longer rise and fall times (larger switching loss).

The power loss in QL1 in the buck mode of operation is given by the following equation:

$$P_{COND(QL1)} = \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot {I_{OUT}}^2 \cdot R_{DSON(QL1)} \tag{32}$$

9.2.2.12 MOSFETs QH2 and QL2

The output side MOSFETs QH2 and QL2 see the output voltage of 12 V and additional transient spikes at SW2 during switching. Therefore QH2 and QL2 should be rated for 20 V or more. The gate plateau voltages of the MOSFETs should be smaller than the minimum input voltage of the converter, otherwise the MOSFETs may not fully enhance during startup or overload conditions.

The power loss in QH2 in the buck mode of operation is approximated by:

$$P_{COND(QH2)} = {I_{OUT}}^2 \cdot R_{DSON(QH2)} \tag{33}$$

The power loss in QL2 in the boost mode of operation consists of both conduction and switching loss components given by Equation 34 and Equation 35 respectively:

$$P_{COND(QL2)} = \left(1 - \frac{V_{IN}}{V_{OUT}} \right) \cdot \left(I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} \right)^2 \cdot R_{DSON(QL2)} \tag{34}$$

$$P_{SW(QL2)} = \frac{1}{2} \cdot V_{OUT} \cdot \left(I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} \right) \cdot \left(t_r + t_f \right) \cdot F_{sw} \tag{35}$$

The rise (t_r) and the fall (t_f) times can be based on the MOSFET datasheet information or measured in the lab. Typically a MOSFET with smaller R_{DSON} (lower conduction loss) has longer rise and fall times (larger switching loss).

The power loss in QH2 in the boost mode of operation is given by the following equation:

$$P_{COND(QH2)} = \frac{V_{IN}}{V_{OUT}} \cdot \left(I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} \right)^2 \cdot R_{DSON(QH2)} \tag{36}$$

9.2.2.13 Frequency Compensation

This section presents the control loop compensation design procedure for the LM5175 buck-boost controller. The LM5175 operates mainly in buck or boost modes, separated by a transition region, and therefore the control loop design is done for both buck and boost operating modes. Then a final selection of compensation is made based on the mode that is more restrictive from a loop stability point of view. Typically for a converter designed to go deep into both buck and boost operating regions, the boost compensation design is more restrictive due to the presence of a right half plane zero (RHPZ) in the boost mode.

The boost power stage output pole location is given by:

$$f_{p1(boost)} = \frac{1}{2\pi}\left(\frac{2}{R_{OUT} \times C_{OUT}}\right) = 398\ \text{Hz} \tag{37}$$

where R_{OUT} = 2 Ω corresponds to the maximum load of 6 A.

The boost power stage ESR zero location is given by:

$$f_{z1} = \frac{1}{2\pi}\left(\frac{1}{R_{ESR} \times C_{OUT}}\right) = 79.6\ \text{kHz} \tag{38}$$

The boost power stage RHP zero location is given by:

$$f_{RHP} = \frac{1}{2\pi}\left(\frac{R_{OUT} \times (1 - D_{MAX})^2}{L1}\right) = 16.9\ \text{kHz} \tag{39}$$

where D_{MAX} is the maximum duty cycle at the minimum V_{IN}.

The buck power stage output pole location is given by:

$$f_{p1(buck)} = \frac{1}{2\pi}\left(\frac{1}{R_{OUT} \times C_{OUT}}\right) = 199\ \text{Hz} \tag{40}$$

The buck power stage ESR zero location is the same as the boost power stage ESR zero.

It is clear from Equation 39 that RHP zero is the main factor limiting the achievable bandwidth. For a robust design the crossover frequency should be less than 1/3 of the RHP zero frequency. Given the position of the RHP zero, a reasonable target bandwidth in boost operation is around 4 kHz:

$$f_{bw} = 4\ \text{kHz} \tag{41}$$

For some power stages, the boost RHP zero might not be as restrictive. This happens when the boost maximum duty cycle (D_{MAX}) is small, or when a really small inductor is used. In those cases, compare the limits posed by the RHP zero (f_{RHP}/3) with 1/20 of the switching frequency and use the smaller of the two values as the achievable bandwidth.

The compensation zero can be placed at 1.5 times the boost output pole frequency. Keep in mind that this locates the zero at 3 times the buck output pole frequency which results in approximately 30 degrees of phase loss before crossover of the buck loop and 15 degrees of phase loss at intermediate frequencies for the boost loop:

$$f_{zc} = 600\ \text{Hz} \tag{42}$$

If the crossover frequency is well below the RHP zero and the compensation zero is placed well below the crossover, the compensation gain resistor R_{c1} is calculated using the approximation:

$$R_{c1} = \frac{2\pi \times f_{bw}}{gm_{EA}} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \times \frac{A_{CS} \times R_{SENSE} \times C_{OUT}}{1 - D_{MAX}} = 9.49\ \text{k}\Omega \tag{43}$$

where D_{MAX} is the maximum duty cycle at the minimum V_{IN} in boost mode and A_{CS} is the current sense amplifier gain. The compensation capacitor C_{c1} is then calculated from:

$$C_{c1} = \frac{1}{2 \times \pi \times f_{zc} \times R_{c1}} = 27.9\ \text{nF} \tag{44}$$

The standard values of compensation components are selected to be R_{c1} = 10 kΩ and C_{c1} = 22 nF.

A high frequency pole is added to suppress switching noise using a 100 pF capacitor (C_{c2}) in parallel with R_{c1} and C_{c1}. These values provide a good starting point for the compensation design. Each design should be tuned in the lab to achieve the desired balance between stability margin across the operating range and transient response time.

9.2.3 Application Curves

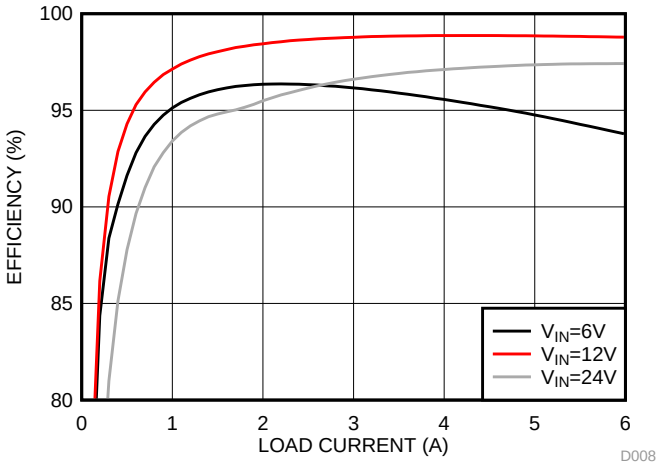


Figure 25. Efficiency vs Load

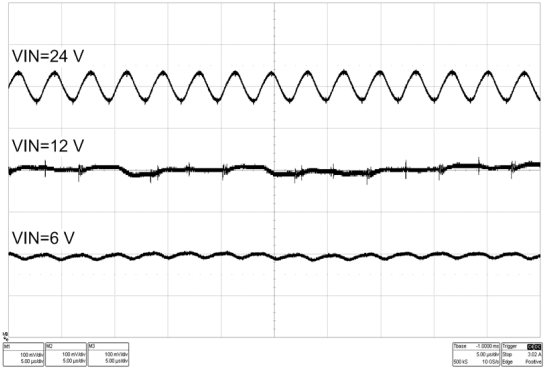


Figure 26. Output Voltage Ripple

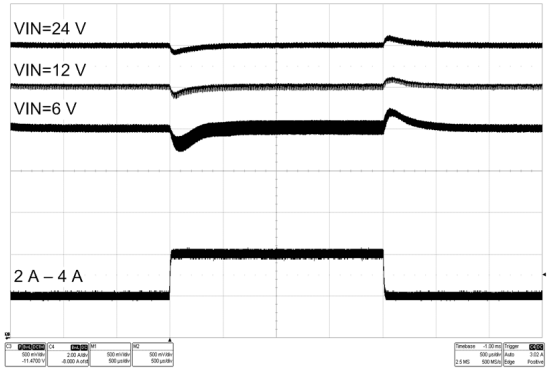


Figure 27. Load Transient Response

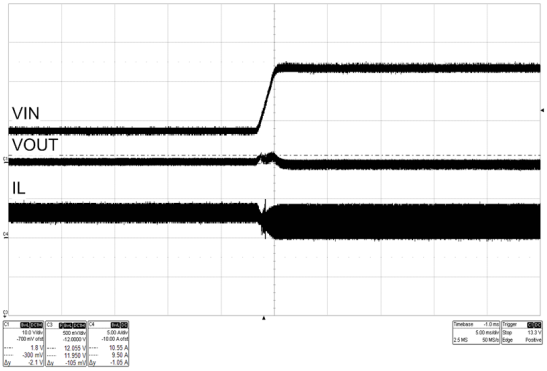


Figure 28. Line Transient Response (8 V - 24 V, I_{OUT} = 2 A)

10 Power Supply Recommendations

The LM5175 is a power management device. The power supply for the device is any dc voltage source within the specified input range. The supply should also be capable of supplying sufficient current based on the maximum inductor current in boost mode operation. The input supply should be bypassed with additional electrolytic capacitor at the input of the application board to avoid ringing due to parasitic impedance of the connecting cables.

11 Layout

11.1 Layout Guidelines

The basic PCB board layout requires separation of sensitive signal and power paths. The following checklist should be followed to get good performance for a well designed board.

- Place the power components including the input filter capacitor C_{IN}, the power MOSFETs QL1 and QH1, and the sense resistor R_{SENSE} close together to minimize the loop area for input switching current in buck operation.
- Place the power components including the output filter capacitor C_{OUT}, the power MOSFETs QL2 and QH2, and the sense resistor R_{SENSE} close together to minimize the loop area for output switching current in boost operation.
- Use a combination of bulk capacitors and smaller ceramic capacitors with low series impedance for the input and output capacitors. Place the smaller capacitors closer to the IC to provide a low impedance path for high di/dt switching currents.
- Minimize the SW1 and SW2 loop areas as these are high dv/dt nodes.
- Layout the gate drive traces and return paths as directly as possible. Layout the forward and return traces close together, either running side by side or on top of each other on adjacent layers to minimize the inductance of the gate drive path.
- Use Kelvin connections to R_{SENSE} for the current sense signals CS and CSG and run lines in parallel from the R_{SENSE} terminals to the IC pins. Avoid crossing noisy areas such as SW1 and SW2 nodes or high-side gate drive traces. Place the filter capacitor for the current sense signal as close to the IC pins as possible.
- Place the C_{IN}, C_{OUT}, and R_{SENSE} ground pins as close as possible with thick ground trace and/or planes on multiple layers.
- Place the VCC bypass capacitor close to the controller IC, between the VCC and PGND pins. A 1-µF ceramic capacitor is typically used.
- Place the BIAS bypass capacitor close to the controller IC, between the BIAS and PGND pins. A 0.1-µF ceramic capacitor is typically used.
- Place the BOOT1 bootstrap capacitor close to the IC and connect directly to the BOOT1 to SW1 pins.
- Place the BOOT2 bootstrap capacitor close to the IC and connect directly to the BOOT2 to SW2 pins.
- Bypass the V_{IN} pin to AGND with a low ESR ceramic capacitor located close to the controller IC. A 0.1 µF ceramic capacitor is typically used. When using external BIAS, use a diode between input rails and V_{IN} pins to prevent reverse conduction when V_{IN} < VCC.
- Connect the feedback resistor divider between the C_{OUT} positive terminal and AGND pin of the IC. Place the components close to the FB pin.
- Use care to separate the power and signal paths so that no power or switching current flows through the AGND connections which can either corrupt the COMP, SLOPE, or SYNC signals, or cause dc offset in the FB sense signal. The PGND and AGND traces can be connected near the PGND pin, near the VCC capacitor PGND connection, or near the PGND connection of the CS, CSG pin current sense resistor.
- When using the average current loop, divide the overall capacitor (C_{IN} or C_{OUT}) between the two sides of the sense resistor to ensure small cycle-by-cycle ripple. Place the average current loop filter capacitor close to the IC between the ISNS(+) and ISNS(-) pins.

11.2 Layout Example

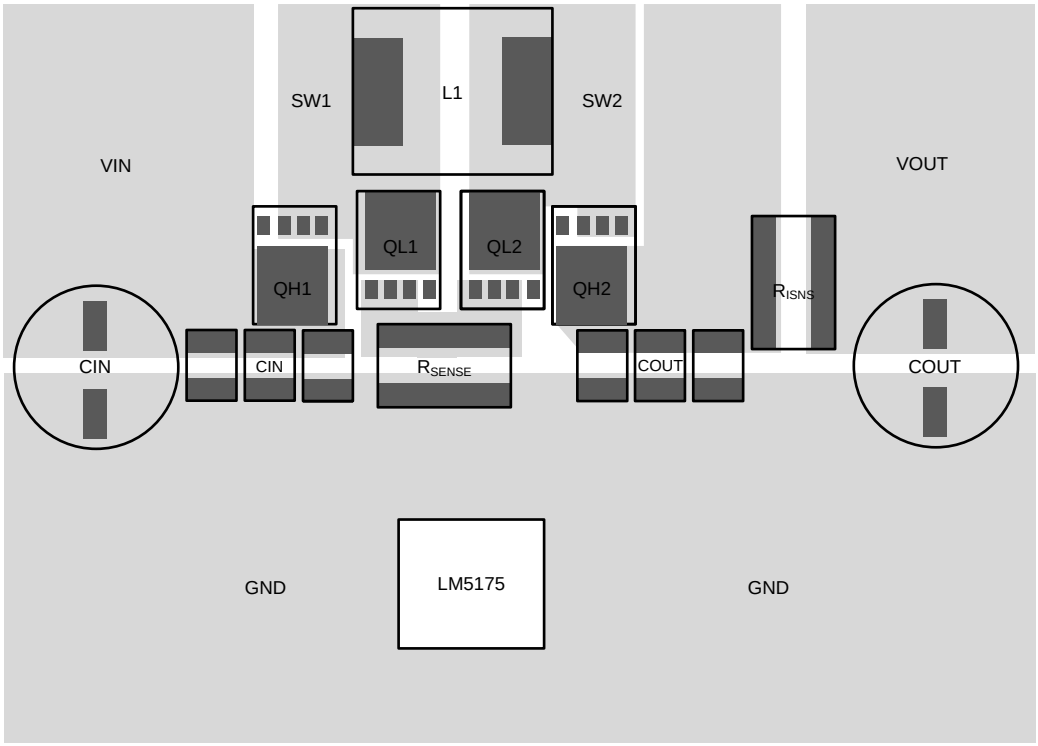


Figure 29. LM5175 Power Stage Layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请访问德州仪器 (TI) 主页以获取最新技术文档，包括应用笔记、用户指南和参考设计。

应用报告《IC 封装热指标》，SPRA953.

12.2 社区资源

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏

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时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
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无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5175PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	LM5175	Samples
LM5175PWPT	ACTIVE	HTSSOP	PWP	28	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	LM5175	Samples
LM5175RHFR	ACTIVE	VQFN	RHF	28	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM5175	Samples
LM5175RHFT	ACTIVE	VQFN	RHF	28	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM5175	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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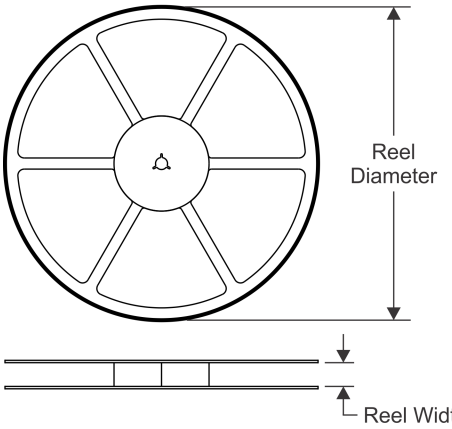
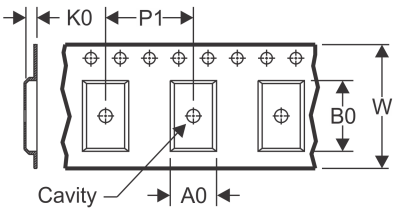
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

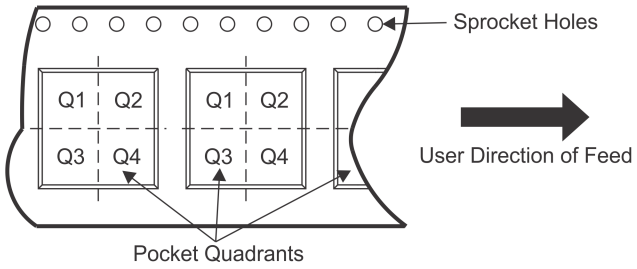


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

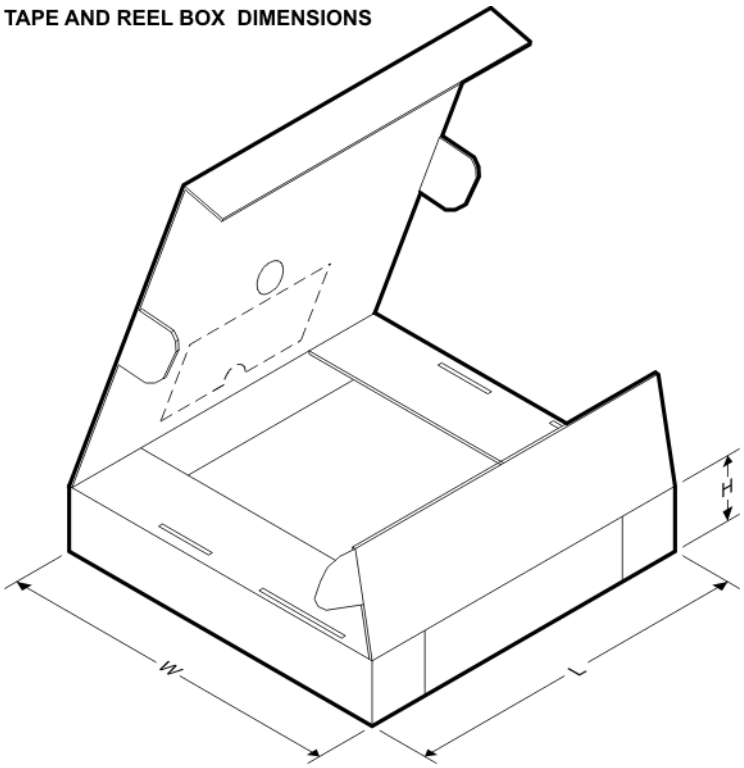
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5175PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
LM5175PWPT	HTSSOP	PWP	28	250	180.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
LM5175RHFR	VQFN	RHF	28	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM5175RHFT	VQFN	RHF	28	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

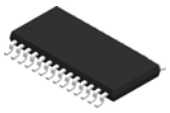


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5175PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
LM5175PWPT	HTSSOP	PWP	28	250	213.0	191.0	55.0
LM5175RHFR	VQFN	RHF	28	3000	367.0	367.0	35.0
LM5175RHFT	VQFN	RHF	28	250	210.0	185.0	35.0

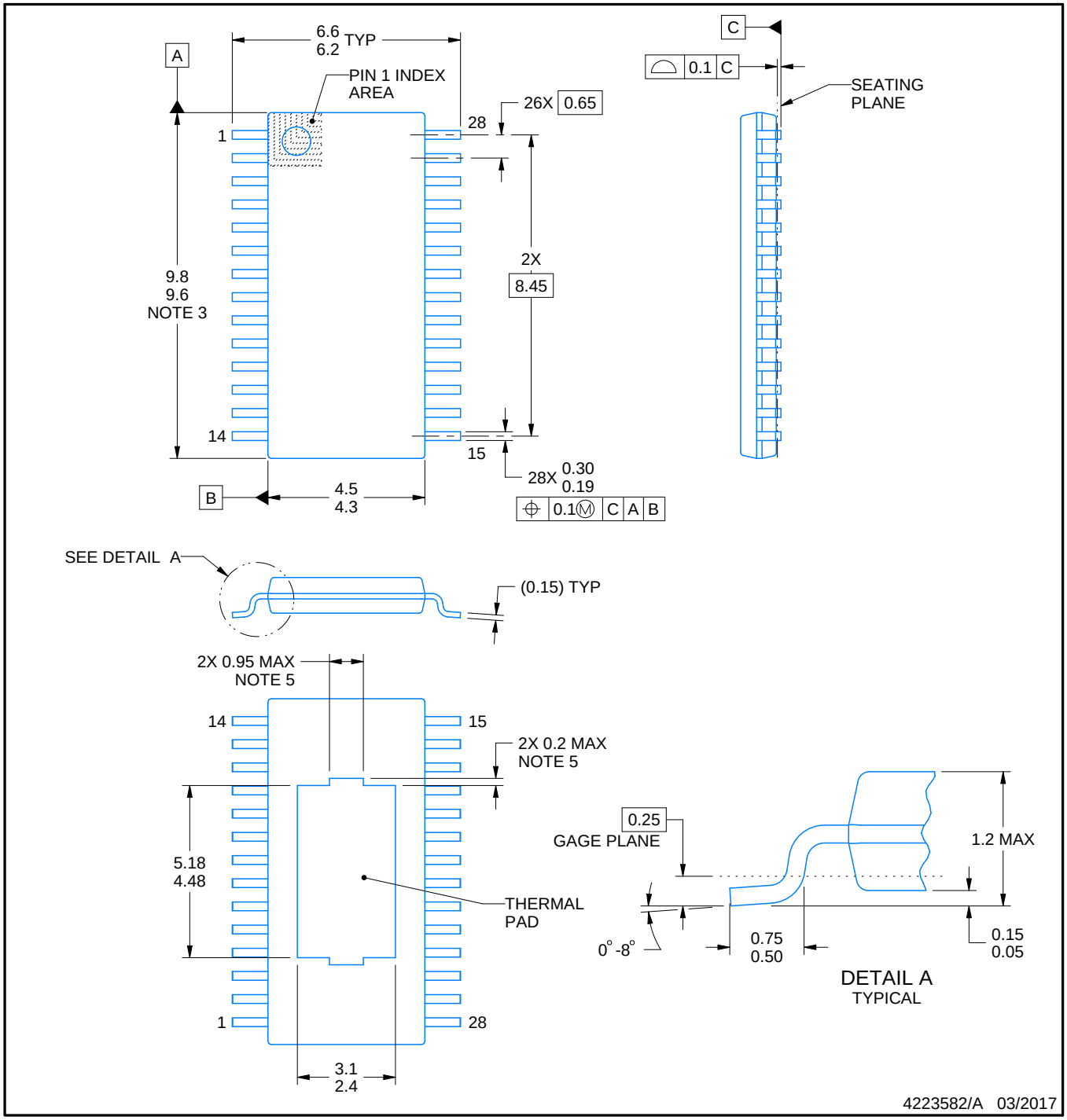
PACKAGE OUTLINE

PWP0028C



PowerPAD™ TSSOP - 1.2 mm max height

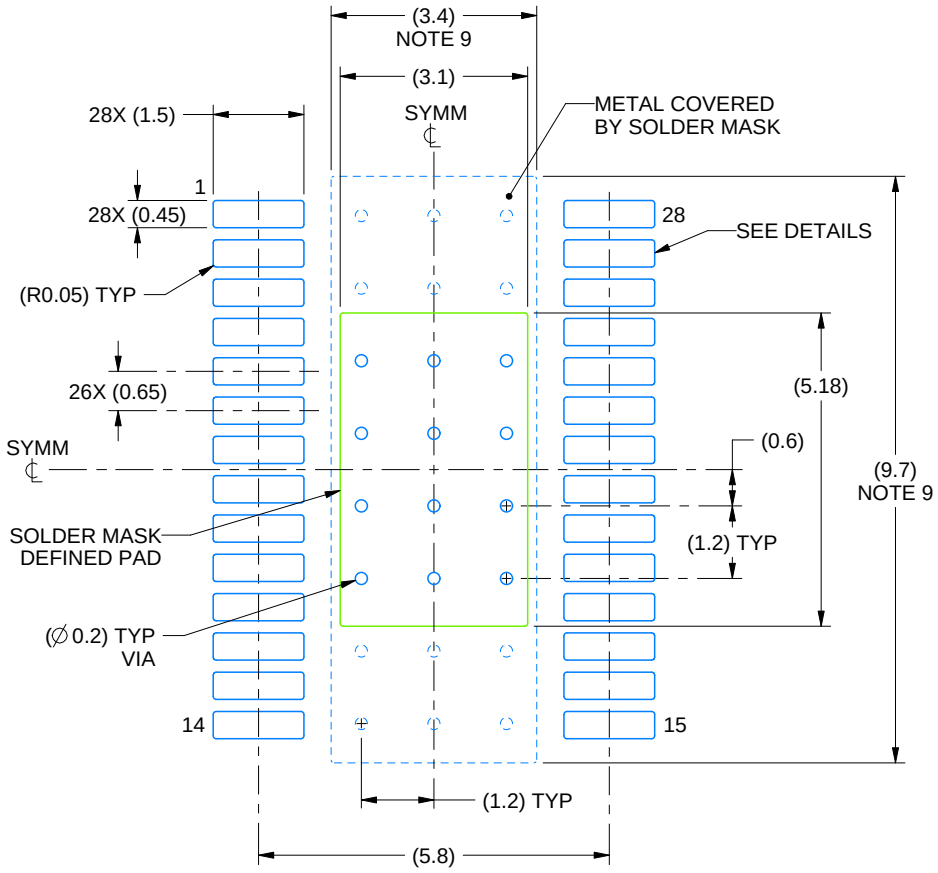
SMALL OUTLINE PACKAGE



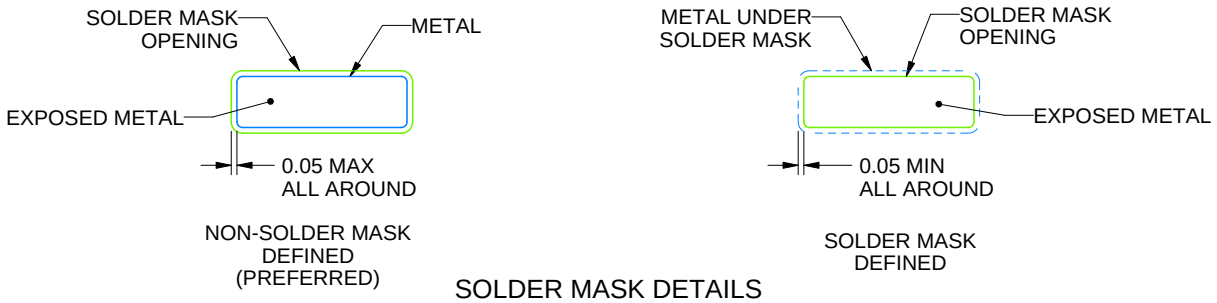
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

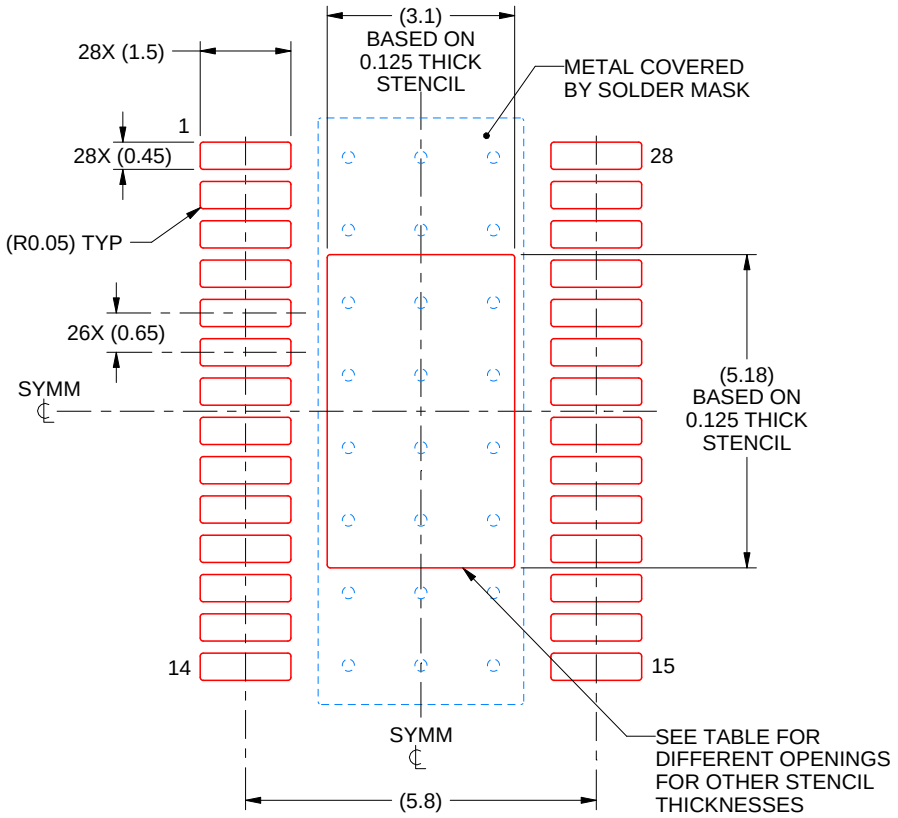


SOLDER MASK DETAILS

4223582/A 03/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 5.79
0.125	3.10 X 5.18 (SHOWN)
0.15	2.83 X 4.73
0.175	2.62 X 4.38

4223582/A 03/2017

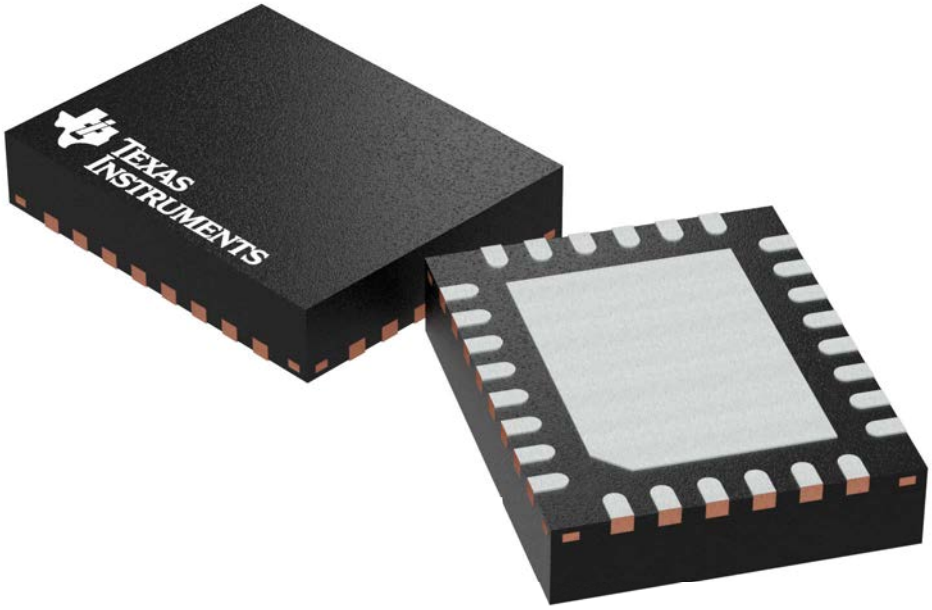
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

RHF 28

VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



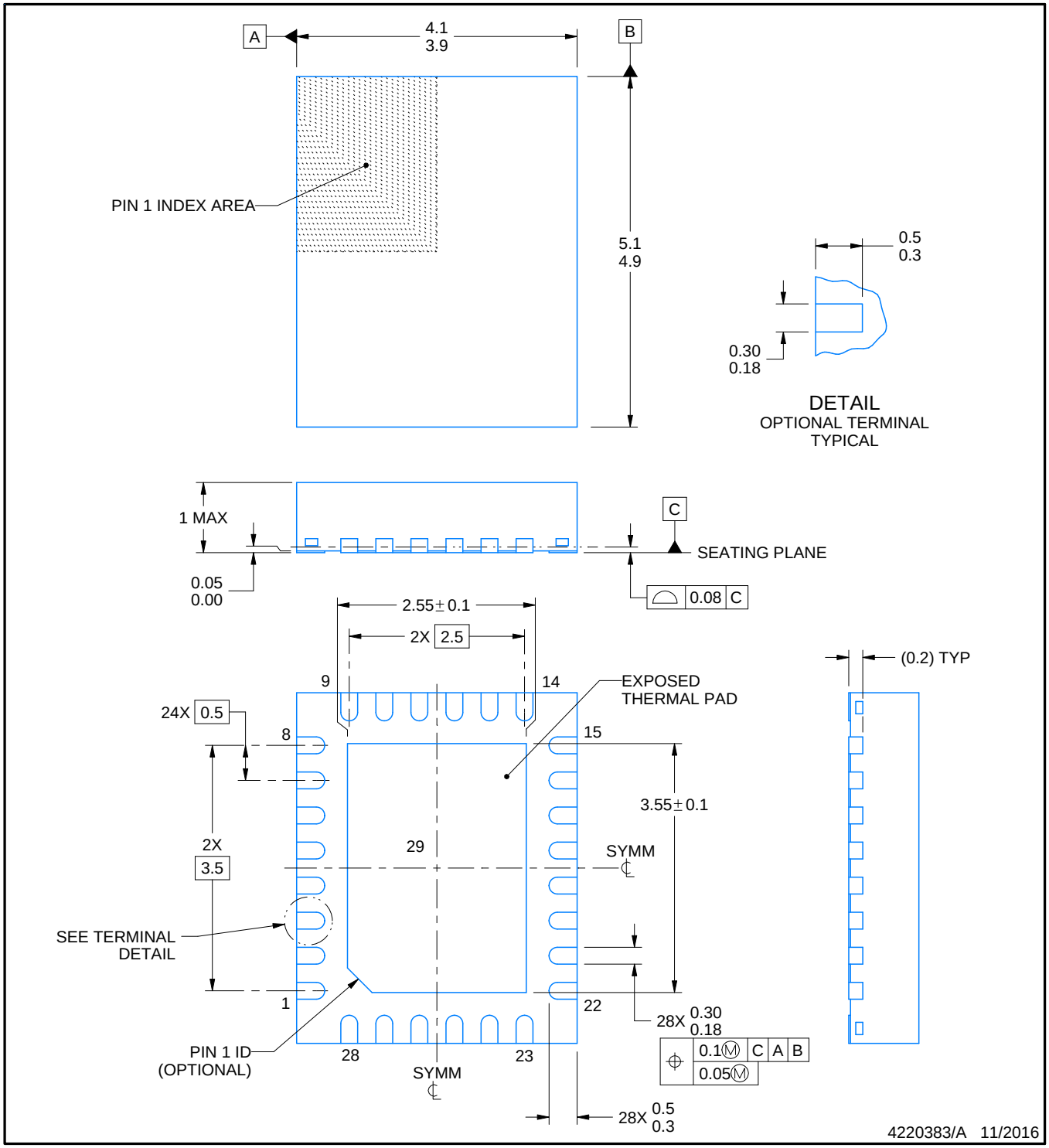
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RHF0028A

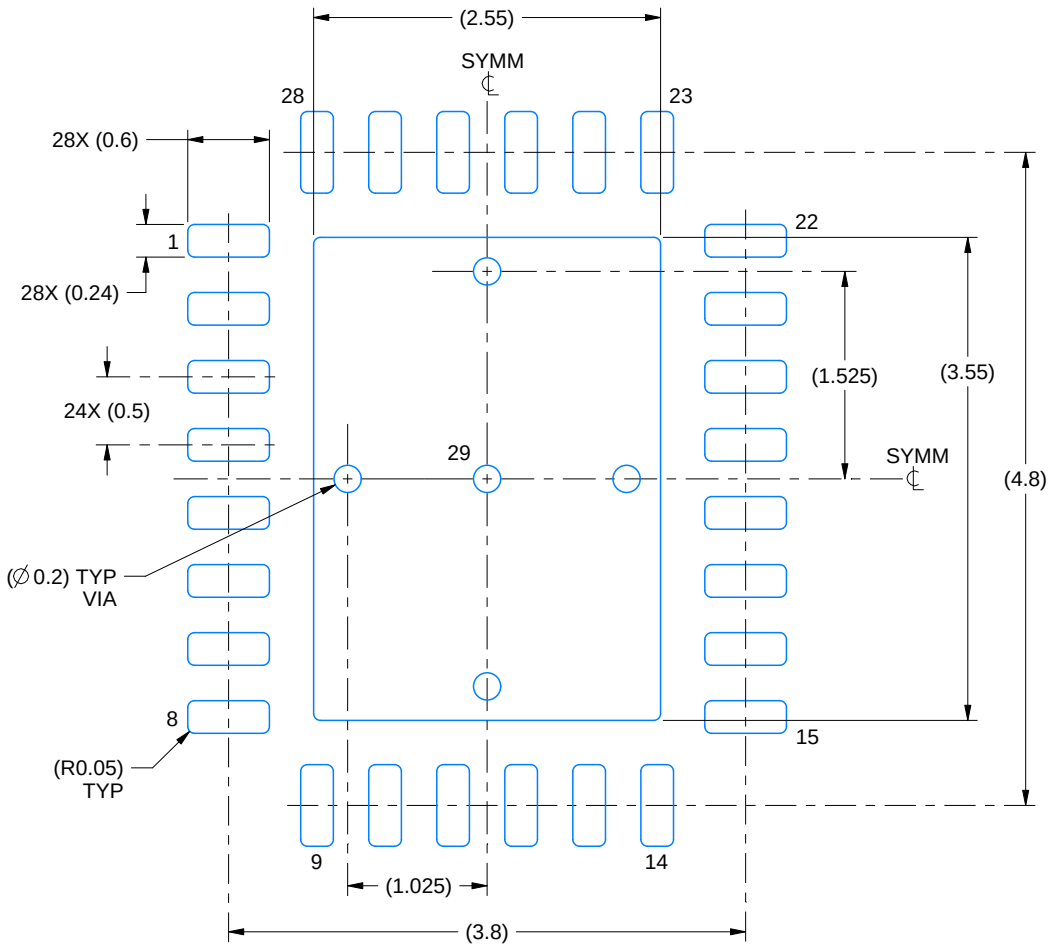
VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

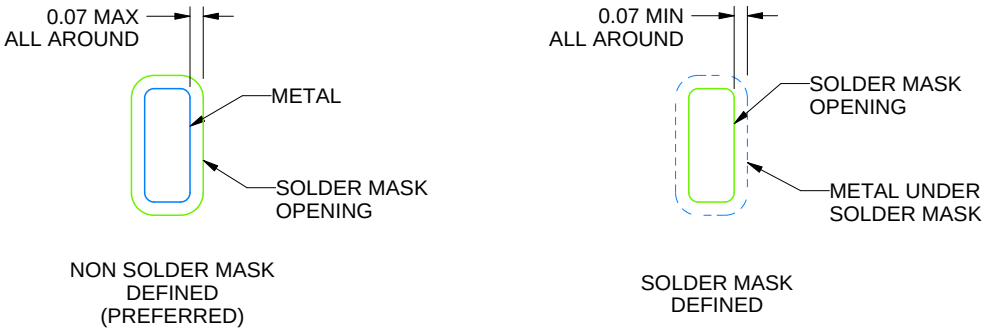


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

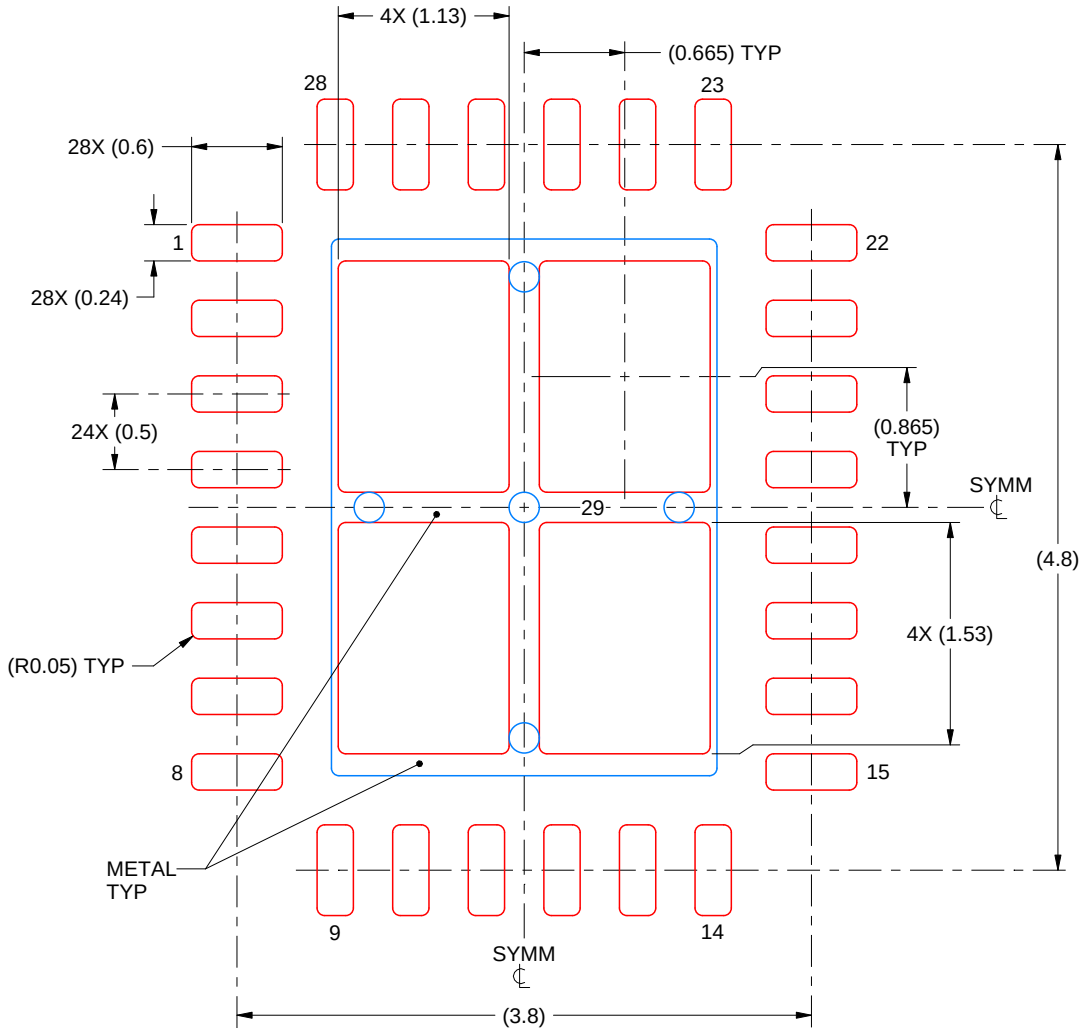


SOLDER MASK DETAILS

4220383/A 11/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 29
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4220383/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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