Application Report
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bq77905 20S Cell Stacking Configuration

Taylor Vogt *BMS: Monitoring and Protection*

ABSTRACT

The bq77905 is a *3–5S Low Power Protector* with easy stacking capabilities for higher than 5S cell battery packs. This document provides an example for setting up a stacking configuration with the bq77905 and exhibits detailed analysis of the stacking functionality.

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Trademarks

1 Configuration

The following stacking configuration represents a battery pack protection system for a 20S cell pack. Therefore, the setup requires four stacked bq77905 devices supporting 5 cells each. Each device is numbered and labeled as a device under test (DUT) in the high-level block diagram illustrated in Figure 1.

NOTE: For other configurations where one or more devices on the stack supports a lower cell count (for example, 3 or 4) than the rest of the stacked devices, TI recommends using the upper-most device on the stack to support the highest cell count. For example, if the user wants to protect a 9S cell pack, DUT#2 shown in Figure 1 supports 5 cells while DUT#1 would support 4 cells. In that case, DUT#2 supports more cells because it is the higher and upper-most device on the stack. Furthermore, If the user wants to protect a 17S cell pack, DUT#4 would support 5 cells while DUT#1–3 would support 4. When possible, configure each DUT to support the same number of cells.

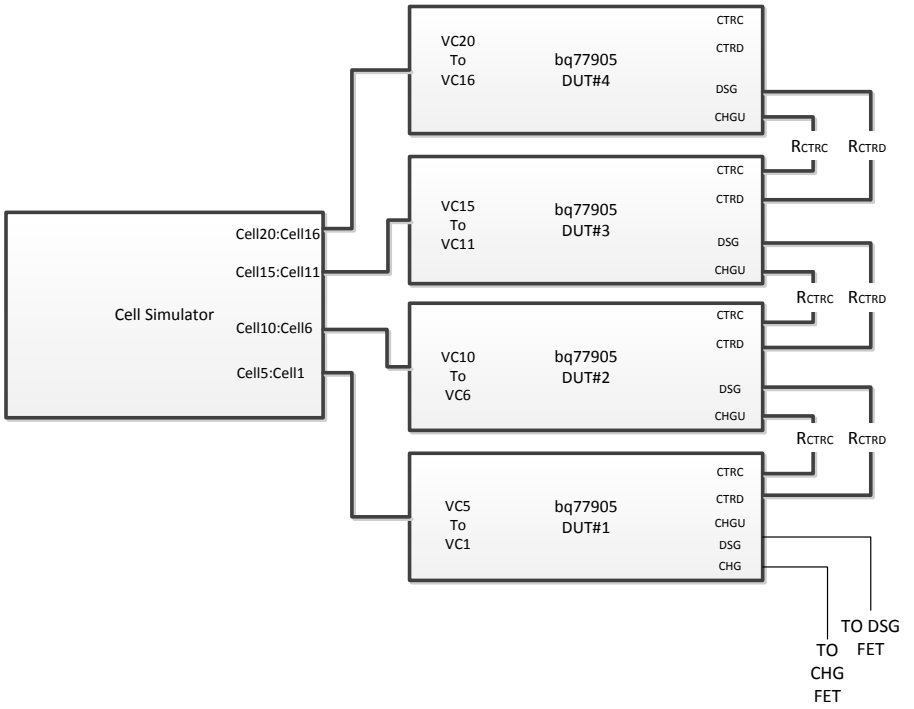

Figure 1. Block Diagram

1.1 General Setup Instructions

The following instructions are useful when constructing any stacking configuration with the bq77905. The instructions refer to DUTs #1–4 shown in Figure 1 representing the devices labeled U1–U4, respectively, in the detailed schematic in Figure 11. Many of the steps refer to pin connections that can best be understood by observing the schematic. Further information on the setup of Stacking Implementations can be found on the bq77904 / bq77905: 3-5S Low Power Protector data sheet (SLUSCM3).

1. For the bottom device (DUT#1 or U1), use the CHG pin to drive the CHG FET, and leave the CHGU pin unconnected.
2. For the upper devices (all except DUT#1 or U1), connect the CHGU pin to the CTRC pin of the immediately lower device with a R_{CTRC} and leave the CHG pin unconnected.
3. Connect the DSG pins of the upper devices with a R_{CTRD} to the CTRD pin of the immediate lower devices.
4. Ensure that the SRP and SRN pins of the upper devices are connected to its corresponding AVSS pin. Each device should have its own separate plane for referencing the AVSS/DVSS pin or any other pins.
5. Ensure that the CCFG pin for each device is connected appropriately (5 cells = floating, 4 cells = AVDD, 3 cells = AVSS)
6. Ground the CTRC and CTRD pins of the upper-most device (in this case DUT#4 or U4) to its corresponding reference plane.
7. If load removal is not used for UV recovery, connect the LD pin of the upper devices to its corresponding reference plane. Otherwise, refer to the data sheet link (SLUSCM3).

2 Functionality

The following sections describe a fault detected by a DUT and displays the results in several images. Each device in the stack is functional in protecting OV, UV, OTC, OTD, UTC, and UTD faults, but the following results display protection of cell 17 on the upper-most device (DUT#4). This is so the data can focus on FET switching time in response to a fault on the top of the stack. Typically this was recorded within a few ms of the response time of faults on the bottom device, so the bq77905 functions efficiently across a stack.

2.1 Undervoltage (UV)

The UV fault test focuses on the DSG turn-off time as cell 17 is monitored below the desired threshold. In Figure 2, it is clear that DSG will fall and stay low while any cell has a UV fault detected. When examining the delay of DSG rise/fall by measuring the delta between the UV fault threshold (red arrows in Figure 2 and Figure 3) and DSG rise/fall, both figures display a similar response time of close to 1s due to the large R_{GS}. This is expected for the bq77905 and will need to be accounted for appropriately in any system.

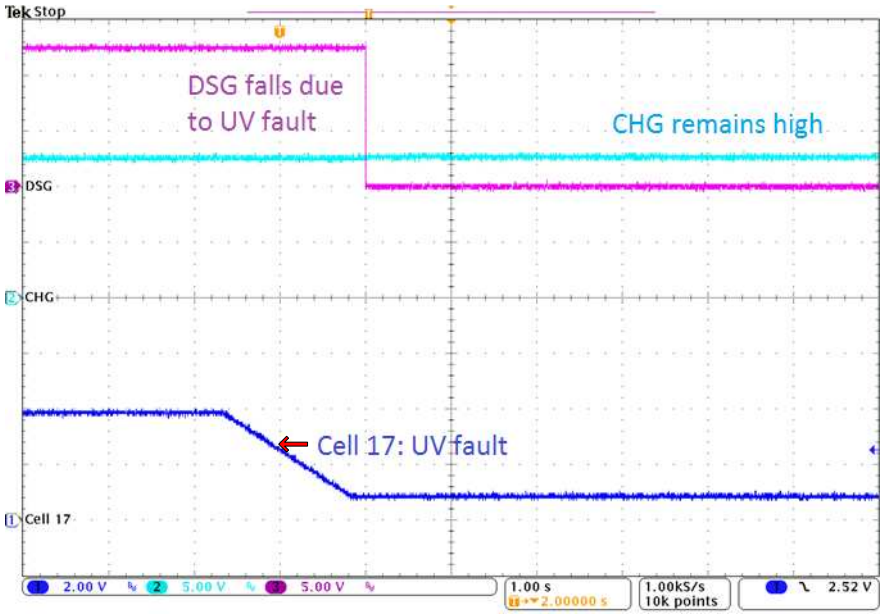

Figure 2. UV Detection

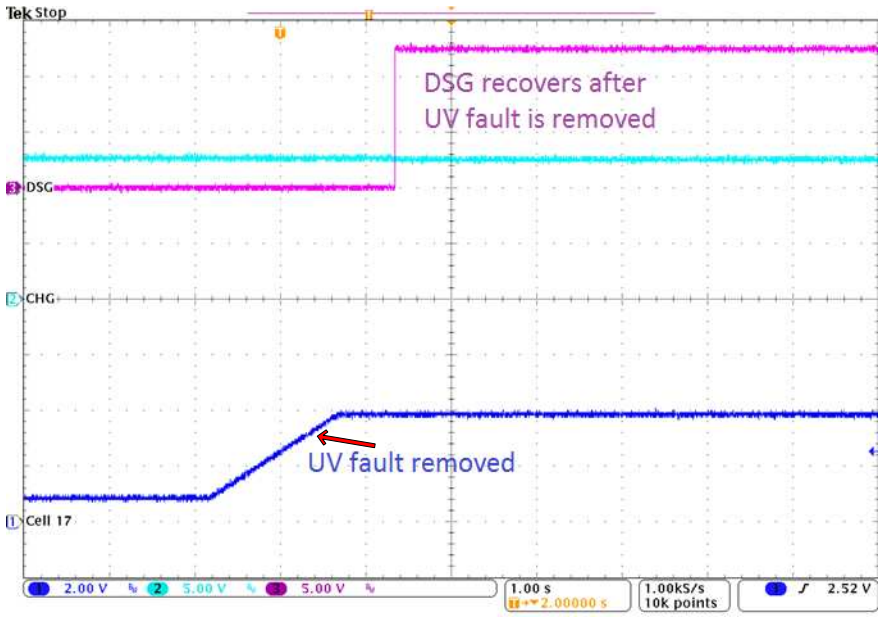

Figure 3. UV Recovery

2.2 Overvoltage (OV)

The OV fault test is almost identical to the UV fault test, but instead focuses on the CHG turn-off time as a cell is monitored above the desired threshold. As shown in Figure 4, the CHG pin falls due to the OV fault (threshold designated by red arrows in Figure 4 and Figure 5) after a delay of approximately 400–600 ms.

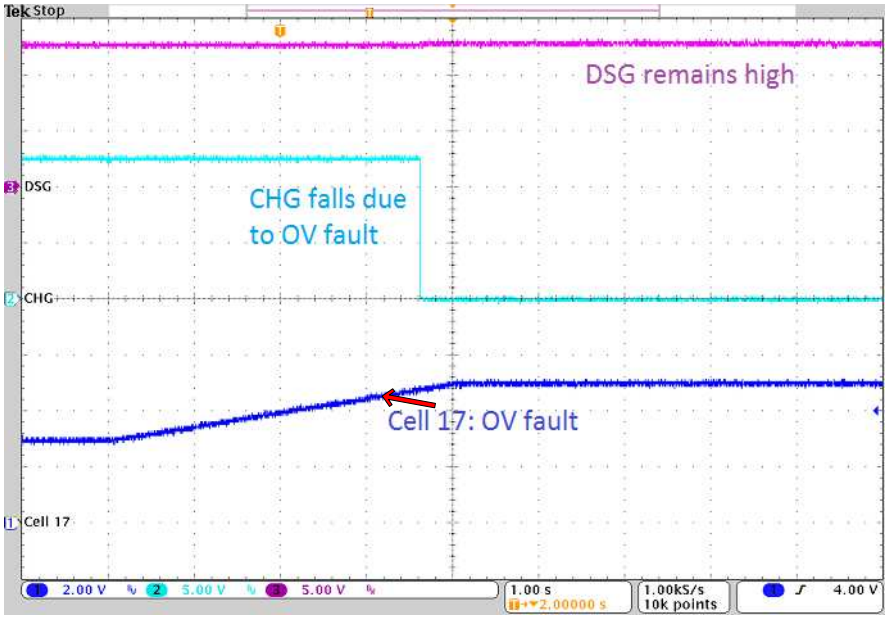

Figure 4. OV Detection

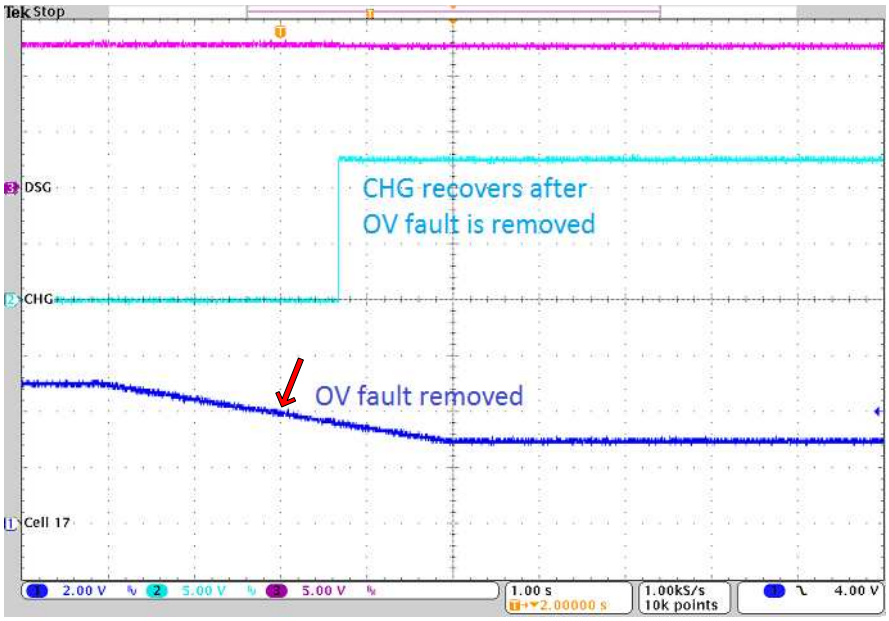

Figure 5. OV Recovery

3 Load Current

In the data sheet stacking schematics and Figure 11, the bottom device has the load of the FET gate-source resistors while the upper devices have only the load from the R_{CTRD} and R_{CTRC} resistors. Since the load is needed for the FETs, add load to the upper devices to more closely match the load between the devices. Adding the load on the CHG or CHGU and DSG output allows the load to match the mode of the battery rather than simply adding a load to the cells. Figure 6 shows currents into the FETs and stacking interface pins.

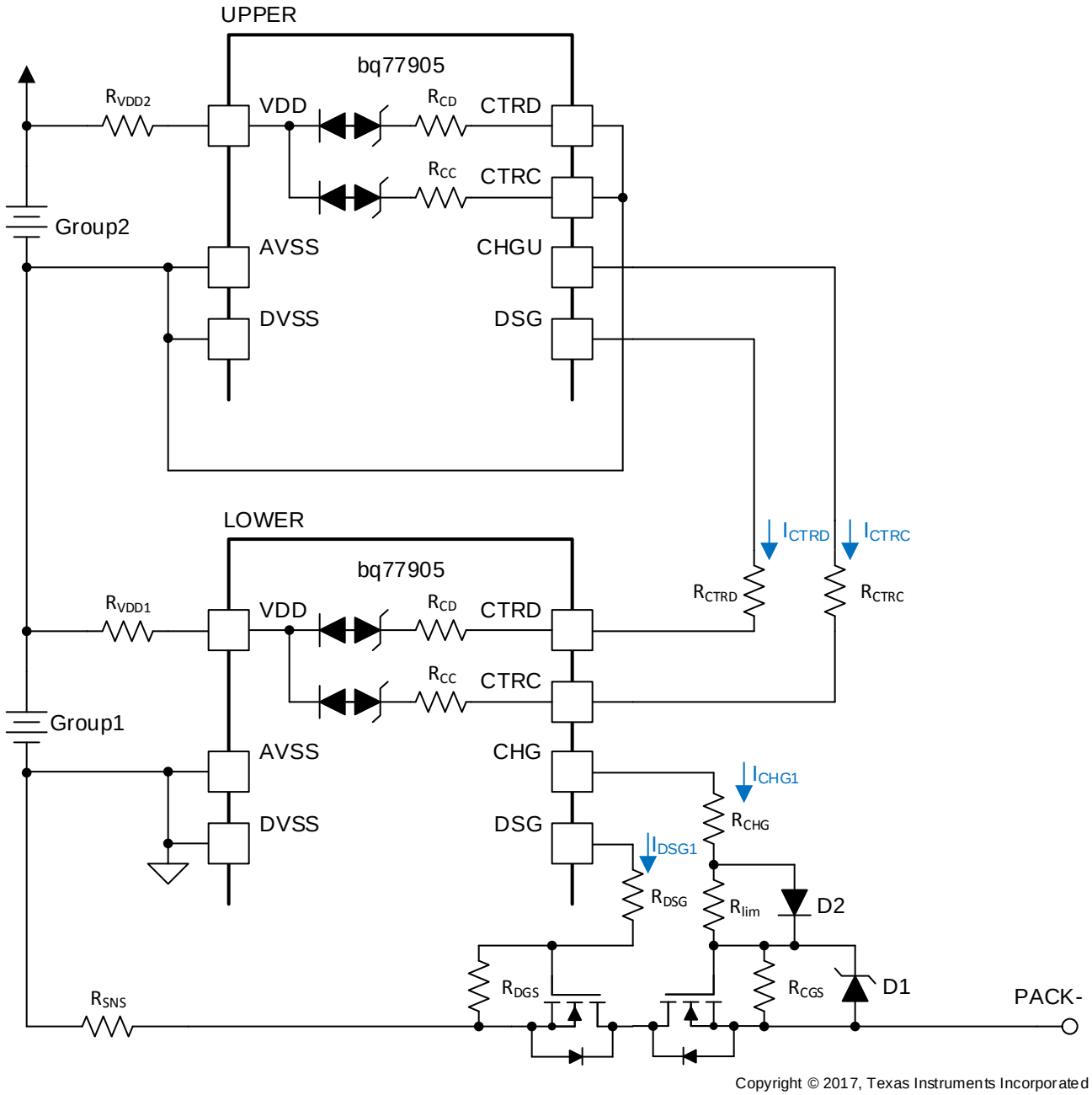

Figure 6. Loading for Stacked Devices

Since the R_{DSG} and R_{CHG} are small with respect to the gate resistors, these can usually be neglected when estimating current and are omitted from the following equations. The currents for the DSG and CHG FET drive:

$$I_{DSG1} = \frac{V_{(FETON)}}{R_{DGS}} \quad (1)$$

$$I_{CHG1} = \frac{\left(V_{(FETON)} - V_{D2}\right)}{R_{CGS}} \quad (2)$$

The CTRC and CTRD pins have an internal resistance which will limit the current into the clamp at the maximum pin voltage. The clamp voltage is shown at a specific test current in the data sheet, $V_{CTR(MAXV)}$. The internal resistance $R_{CD} = R_{CC}$ or R_{Cx} has a nominal value of 440 kΩ but may vary significantly and is not a characterized value in the data sheet. The CTRC and CTRD characteristic for an example device is shown in Figure 7.

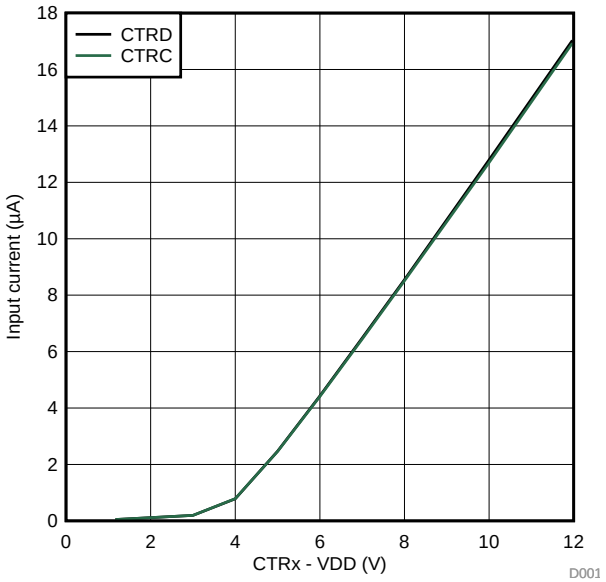

Figure 7. Example CTRx pin Characteristic

At low currents the data sheet test conditions may be a good representation of the control input operating point and the equation for the input current is:

$$I_{CTRx} = \frac{\left(V_{(FETON)} - V_{CTR(MAXV)}\right)}{R_{CTRx}} \quad (3)$$

Using typical values in the data sheet and 10 MΩ for R_{CTRx}, I_{CTRx} would be 800 nA, near the 600 nA data sheet test current.

One method to match the load of the FETs would be to adjust R_{CTRx}. However, at much higher currents it is better to consider the internal resistance and an internal clamp value V_C in an equation for I_{CTRx}:

$$I_{CTRx} = \frac{\left(V_{(FETON)} - V_C\right)}{\left(R_{Cx} + R_{CTRx}\right)} \quad (4)$$

As R_{CTRx} is decreased to increase the current, the current becomes more sensitive to the internal R_{Cx} resistance variation. A designer may want to avoid using the R_{CTRx} resistor to match the current of the FET unless the R_{xGS} resistance were very large.

A better method to match the FET load current on the upper device would be to add resistors from the upper device FET outputs to the VSS reference, R_{DLD} and R_{CLD} as shown in Figure 8.

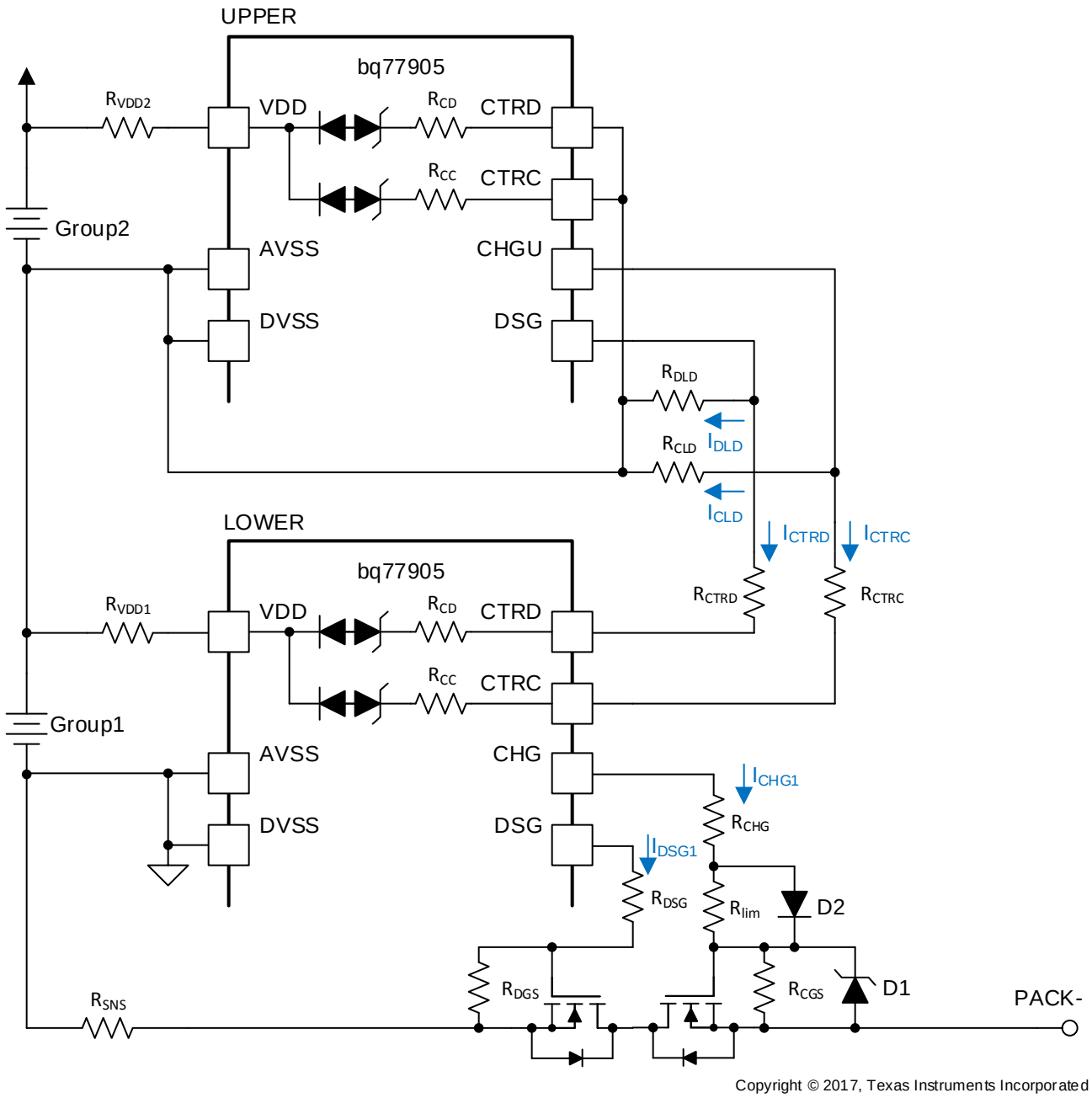

Figure 8. Load Matching Resistors

The currents in these load matching resistances are added to the stacking interface currents to match the FET drive currents of the lower device:

$$I_{DLD} + I_{CTRD} = I_{DSG1} \quad (5)$$

$$I_{CLD} + I_{CTRC} = I_{CHG1} \quad (6)$$

These R_{xLD} load resistances receive the full $V_{(FETON)}$ voltage and are unaffected by the clamp voltage for a predictable load current.

$$R_{xLD} = \frac{V_{(FETON)}}{I_{xLD}} \quad (7)$$

Since I_{CTRx} provides some load, R_{DLD} and R_{CLD} will be larger than the R_{xGS} resistance of the lower device. The designer would solve for the equations and select a suitable load resistance from available values. Example calculations in Table 1 and Table 2 show that load matching resistors can improve the capacity mismatch caused by the FET load.

Table 1. Example DSG Load Calculations

Parameter	Source	Value
$V_{(FETON)}$	Data sheet	12 V
R_{DGS}	Figure 11 R47	1 MΩ
I_{DSG1}	Equation 1	12 µA
$V_{CTR(MAXV)}$	Data sheet	4 V
R_{CTRD}	Figure 11 R32	10 MΩ
I_{CTRD}	Equation 3	0.8 µA
I_{DLD} desired	Equation 5	11.2 µA
Capacity difference without matching load	Load mismatch current × 24 hours per day × 365 days per year	98 mAH per year
R_{DLD} desired	Equation 7	1.07 MΩ
R_{DLD} selected	Standard 5% value	1.1 MΩ
Nominal current error	12 × (1 / 1.07 – 1 / 1.1)	0.305 µA
Capacity difference with 5% matching load resistor value	Load mismatch current × 24 hours per day × 365 days per year	2.68 mAH per year

Table 2. Example CHG Load Calculations

Parameter	Source	Value
$V_{(FETON)}$	Data sheet	12 V
V_{D2}	Estimate from data sheet	0.4 V
R_{CGS}	Figure 11 R48	3.3 MΩ
I_{CHG1}	Equation 2	3.52 µA
$V_{CTR(MAXV)}$	Data sheet	4 V
R_{CTRC}	Figure 11 R33	10 MΩ
I_{CTRC}	Equation 3	0.8 µA
I_{CLD} desired	Equation 6	2.72 µA
Capacity difference without matching load	Load mismatch current × 24 hours per day × 365 days per year	24 mAH per year
R_{CLD} desired	Equation 7	4.41 MΩ
R_{CLD} selected	Standard 5% value	4.3 MΩ
Nominal current error	12 × (1 / 4.41 – 1 / 4.3)	–70.7 nA
Capacity difference with 5% matching load resistor value	Load mismatch current × 24 hours per day × 365 days per year	–0.62 mAH per year

The previous calculations assume the $V_{(FETON)}$ voltage is in regulation as would be the case with 5 cell stacks and high voltage cells. With lower cell counts and voltages, the FET drive voltage will drop out of regulation as shown in Figure 9. When each device supports the same number of cells, the voltages should match and not be a concern. When the devices have different numbers of cells, use the $V_{(FETON)}$ from the normal system condition in calculations to equalize currents.

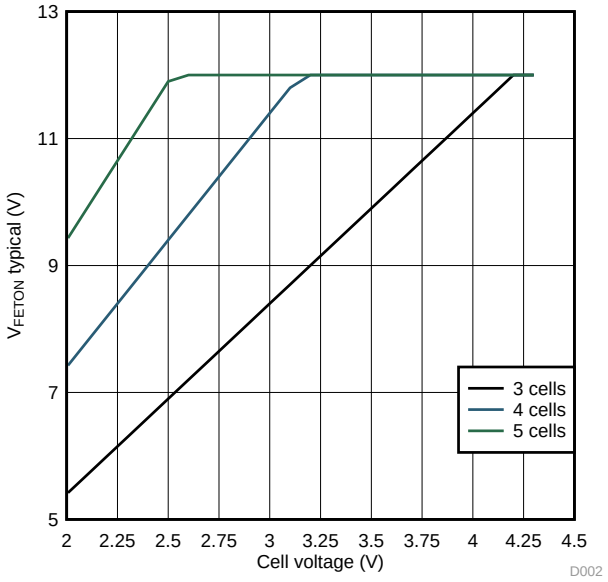

Figure 9. FET Drive Voltage With Cell Variation

4 Troubleshooting FAQ

Q: What is the limit to how many devices you can stack?

A: The bq77905 has no technical limitation on the number of devices in a stack. However, keep in mind that the larger the stack becomes, the greater the noise impact on the CTRC/D signal strength and the greater the total delay time from the top to bottom of the stack. This delay time is not an increase in the individual DUT protections, but it is a minimal increase due to logic propagation across each device in the stack. Typically, this is only 1–10 ms per device added to the stack, so it must be decided if this is a small enough margin for the application.

Q: What will happen if I make a lower device support more cells than an upper device (for example, if you made DUT#1 support 5 cells and DUT#4 support 3 cells)?

A: The system should function appropriately, but this is not recommended as doing so could impact CTRC/D signal strength across the stack. However, the tradeoff would be lower gate voltage on the FETs, so determine if one option is better than the other.

Q: What changes need to be made for a DUT to support only 3 or 4 cells?

A: As mentioned in Section 1.1 and in the data sheet, the CCFG pin must be configured appropriately, and the unused cells must always be chosen as the upper-most cells and shorted to the immediate lower cell (for example, in an 8S cell stack configuration, C4 could be shorted to C3 for 4 cells in DUT#1).

Q: How do I implement *Load Detect* for *UV Fault Recovery* on upper devices?

A: As shown in Figure 11, connect the LD pins of all devices to PACK– through a R_{LD} (R8, R18, R28, R44) equal to 300 kΩ and a blocking diode. Also, the R_{GS_CHG} (R48) should be increased from the typical 1 MΩ to 3.3 MΩ. Refer to the data sheet (SLUSCM3) for further detail and explanations.

Q: How would I decrease the CHG FET turn off time without affecting the *UV Load Detect?*

A: Instead of decreasing the value of the R_{GS_CHG} (R48), it is more effective to implement a CHG FET turn off speed circuit. Further detail is explained in Section 3 of the bq77905 Using Multiple FETs (SLUA773) Application Note.

Q: With a small battery the cells on the bottom device have a lower voltage than the cells of an upper device. Why is this and how can it be avoided?

A: The bottom device has a greater load than the upper device due to the FET drive load of the gate-source resistors (Figure 11) R47 and R48 being smaller than the stacking interface load on the upper device, RCTR resistors R32 and R33 for example. See Section 3.

Q: The FETs turn on, but the voltage measured at CTRC or CTRD indicates the FETs should be off. Why is this?

A: The CTRC and CTRD nodes have a high impedance source. When a meter is attached such as in Figure 10 the meter becomes part of the circuit forming a voltage divider and alters the voltage at CTRx. If the gate voltage is measured at the same time the FETs may be observed to turn off. Measuring CTRx with respect to VDD will reduce the influence of the meter. If the meter input can be set to high impedance, a better measurement will be obtained, but loading will still occur.

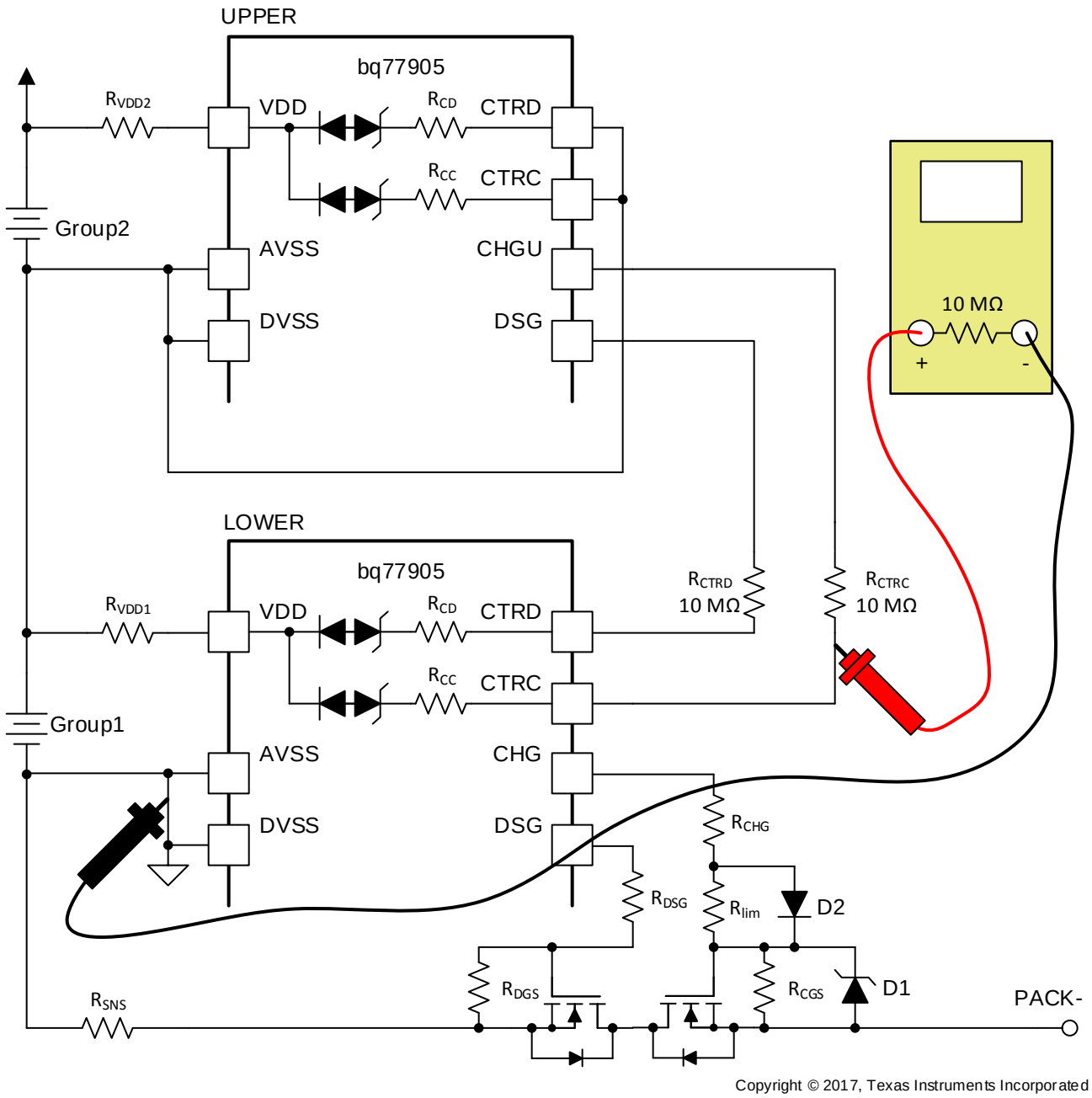

Figure 10. Measurement Loading Example on CTRC

5 References

For additional information, refer to the following documents available at www.ti.com:

- bq77904 / bq77905: 3-5S Low Power Protector data sheet (SLUSCM3)
- bq77905 EVM User's Guide (SLVUAN2)
- bq77905 Using Multiple FETs (SLUA773)
- bq77905 Separate Current Paths (SLUA772)

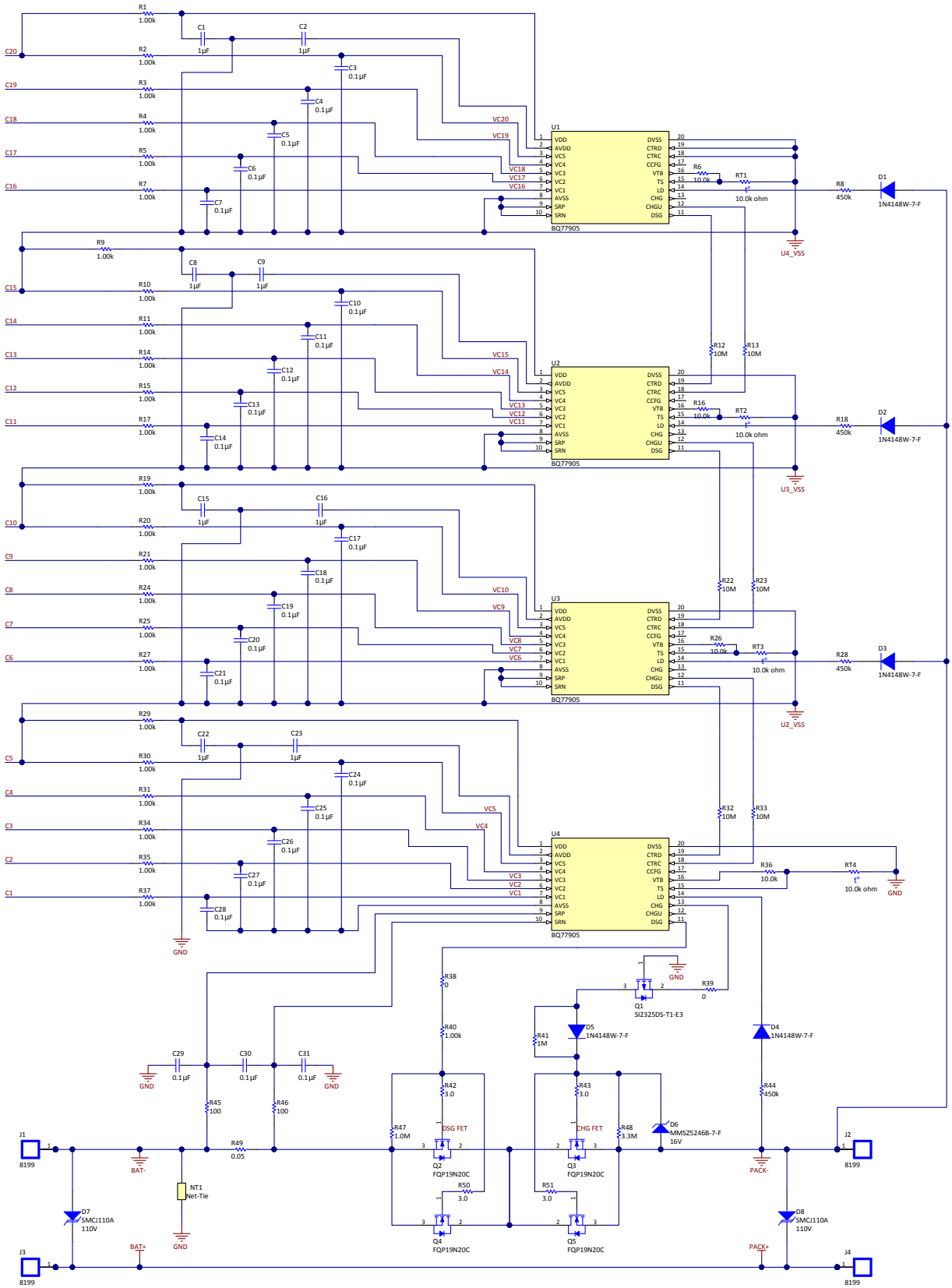

Figure 11. Schematic

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2016) to A Revision	Page
• Added *Load Current* section.	5
• Added FAQ about lower voltage in the lower device.	10
• Added FAQ on CTRx measurement with image.	10

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