适用于能量收集器供电应用的 bq25570 微功率升压充电器与降压 转换器

1 特性

- 超低功耗直流/直流升压充电器
  - 冷启动电压：V_{IN} ≥ 600mV
  - 能够在 VIN 低至 100mV 时持续能量意大利 将特性从：能够在输入源低至 120mV 时持续能量意大利改为：能够在输入源低至 100mV 时持续能量意大利
  - 输入电压稳压防止高阻抗输入源故障
  - 488nA（典型值）的完全运行静态电流
  - 电池电流 < 5nA 的运输节电模式
- 储能
  - 可将能量存储在可再充电锂离子电池、薄膜电池、超大电容器或传统电容器中
- 电池充电和保护
  - 内部设定欠压电平
  - 用户可编程过压电平
- 电池正常输出标志
  - 可编程阈值和滞后
  - 功率损耗待定的随附报警功能的微控制器
  - 可被用来启用或禁用系统负载
- 可编程降压调节输出（降压）
  - 效率到达 93%
  - 支持 110mA 的峰值输出电流（典型值）
- 可编程最大功率点跟踪 (MPPT)
  - 从多种能量意大利器件中提供最佳能量提取，其中包括太阳能电池板、热电和压电发电机

2 应用

- 能量意大利
- 太阳能充电器
- 热电发电机 (TEG) 能量意大利
- 无线传感器网络 (WSN)
- 低功耗无线监测
- 环境监测
- 桥梁和结构健康监测 (SHM)
- 智能楼宇控制
- 便携式和可佩戴式健康器件
- 娱乐系统遥控

3 说明

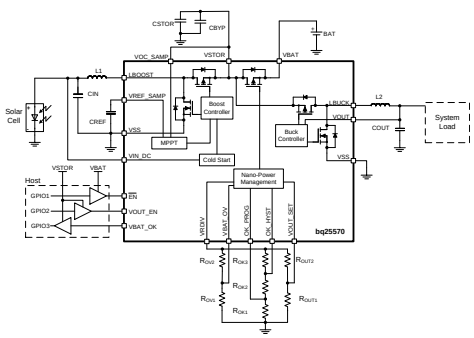
bq25570 器件经过专门设计，可以有效地提取光电（太阳能）或热电发电机 (TEG) 等各种高输出阻抗直流源产生的微瓦 (µW) 至毫瓦 (mW) 级的电能，而不会导致这些输入源发生故障。电池管理 特性 确保可充电电池不会因为所提取的能量而过充，不会出现电压升高或损耗超出系统负载安全限制范围的情况。除高效升压充电器外，bq25570 还集成了高效率、微功耗的降压转换器，可为系统（例如有严格功率和操作要求的无线传感器网络 (WSN)）提供第二个电源轨。bq25570 的所有功能都采用 20 引线 3.5mm x 3.5mm QFN 小尺寸封装 (RGR)。

器件信息(1)

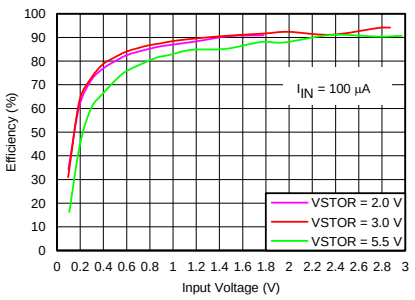
器件型号	封装	封装尺寸（标称值）
bq25570	超薄四方扁平无引线封装 (VQFN) (20)	3.50mm x 3.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用原理图



充电器效率与输入电压



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (December 2018) to Revision G — **Page**

- Changed From: "330 mV typical,.." To: "600 mV typical,.." in the second paragraph of the *Overview* section ... 13
- Changed Figure 21 ... 16
- Changed From: "VIN(CS) = 330 mV typical." To: "VIN(CS) = 600 mV typical." in the last paragraph of the *Cold-Start Operation* section ... 19

Changes from Revision E (March 2015) to Revision F — **Page**

- 将特性从“冷启动电压：V_{IN} ≥ 330mV（典型）”更改为“冷启动电压：V_{IN} ≥ 600mV” ... 1
- Changed the RGR Package appearance ... 4
- Increased $V_{IN(CS)}$ From: TYP = 330 mV and MAX = 450 mV To: TYP = 600 mV and MAX = 700 mV in *Electrical Characteristics* table ... 6

Changes from Revision D (December 2014) to Revision E — **Page**

- Changed the Test Condition for $P_{IN(CS)}$ in the *Electrical Characteristics* ... 6
- Changed the values for $P_{IN(CS)}$ in the *Electrical Characteristics* From: TYP = 5 To: TYP = 15 ... 6
- Changed CBYP = 0.1 µF To: CBYP = 0.01 µF in *Detailed Design Procedure* ... 25
- Changed CBYP = 0.1 µF To: CBYP = 0.01 µF in *Detailed Design Procedure* ... 28
- Changed CBYP = 0.1 µF To: CBYP = 0.01 µF in *Detailed Design Procedure* ... 31

Changes from Revision C (December 2013) to Revision D — **Page**

- 已添加 添加了 *ESD 额定值* 表、*特性* *说明*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Revision B (September 2013) to Revision C **Page**

- 1
- 将特性从：效率高达 98% 改为：效率高达 93%..... 1
- 将 说明 部分的文本从“继续收集低至 V_{IN} = 120mV 的能量。” 更改为“继续收集低至 V_{IN} = 100mV 的能量。” 1
- Changed Peak Input Power n the Absolute Maximum Ratings table From: MAX = 400 mW To: MAX = 510 mW..... 5
- Changed VIN(DC) in the Recommended Operating Conditions table From: MIN = 0.12 V MAX = 4 V To: MIN = 0.1 V MAX = 5.1 V..... 5
- Changed VIN(DC) in the Electrical Characteristics table From: MIN = 120 mV MAX = 4000 mV To: MIN = 100 mV MAX = 5100 mV 6
- Changed PIN in the Electrical Characteristics table From: MAX = 400 mW To: MAX = 510 mW..... 6
- Added VDELTA, VBAT_OV - VIN(DC to the ELECTRICAL CHARACTERISTICS table..... 7
- Changed VOUT_EN(H) From: VSTOR - 0.2 To: VSTOR - 0.4 in the ELECTRICAL CHARACTERISTICS table..... 7

Changes from Revision A (September 2013) to Revision B **Page**

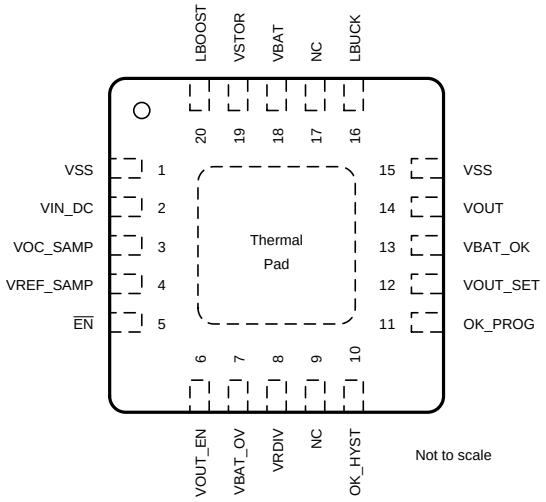
- Changed values in the *Thermal Information* table..... 6

Changes from Original (March 2013) to Revision A **Page**

- Changed the data sheet from a Product Brief to Production data 4

5 Pin Configuration and Functions

RGR Package
20 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	5	I	Active low digital programming input for enabling/disabling the IC. Connect to GND to enable the IC.
LBOOST	20	I/O	Inductor connection for the boost charger switching node. Connect a 22 µH inductor between this pin and pin 2 (VIN_DC).
LBUCK	16	I/O	Inductor connection for the buck converter switching node. Connect at least a 4.7 µH inductor between this pin and pin 14 (VOUT).
NC	9	I	Connect to ground using the IC's PowerPAD™.
NC	17	I	Connect to ground using the IC's PowerPAD.
OK_HYST	10	I	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT_OK hysteresis threshold. If not used, connect this pin to GND.
OK_PROG	11	I	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT_OK threshold. If not used, connect this pin to GND.
VBAT	18	I/O	Connect a rechargeable storage element with at least 100uF of equivalent capacitance between this pin and either VSS pin.
VBAT_OK	13	O	Digital output for battery good indicator. Internally referenced to the VSTOR voltage. Leave floating if not used.
VBAT_OV	7	I	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT overvoltage threshold.
VIN_DC	2	I	DC voltage input from energy harvesting source. Connect at least a 4.7 µF capacitor as close as possible between this pin and pin 1.
VOC_SAMP	3	I	Sampling pin for MPPT network. Connect to VSTOR to sample at 80% of input source open circuit voltage. Connect to GND for 50% or connect to the mid-point of external resistor divider between VIN_DC and GND.
VOUT	14	O	Buck converter output. Connect at least 22 µF output capacitor between this pin and pin 15 (VSS).
VOUT_EN	6	I	Active high digital programming input for enabling/disabling the buck converter. Connect to VSTOR to enable the buck converter.
VOUT_SET	12	I	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VOUT regulation set point.
VREF_SAMP	4	I	Connect a 0.01-µF low-leakage capacitor from this pin to GND to store the voltage to which VIN_DC will be regulated. This voltage is provided by the MPPT sample circuit.
VRDIV	8	O	Connect high side of resistor divider networks to this biasing voltage.
VSS	1	I	Power ground for the boost charger.
VSS	15	—	Power ground for the buck converter and analog/signal ground for the resistor dividers and VREF_SAMP capacitor.
VSTOR	19	O	Connection for the output of the boost charger. Connect at least a 4.7 µF capacitor in parallel with a 0.1 µF capacitor as close as possible to between this pin and pin 1 (VSS).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN_DC, VOC_SAMP, VREF_SAMP, VBAT_OV, VRDIV, OK_HYST, OK_PROG, VBAT_OK, VBAT, VSTOR, LBOOST, $\overline{EN}$, VOUT_EN, VOUT_SET, LBUCK, VOUT (2)	–0.3	5.5	V
Peak Input Power, PIN_PK			510	mW
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}/ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VIN(DC)	DC input voltage into VIN_DC (1)	0.1		5.1	V
VBAT, VOUT	Voltage range (2)	2		5.5	V
CIN	Capacitance on VIN_DC pin	4.7			µF
CSTOR	Capacitance on VSTOR pin	4.7			µF
COUT	Capacitance on VOUT pin	10	22		µF
CBAT	Capacitance or battery with at least the same equivalent capacitance on VBAT pin	100			µF
CREF	Capacitance on VREF_SAMP that stores the samped VIN reference	9	10	11	nF
$R_{OC1} + R_{OC2}$	Total resistance for setting for MPPT reference if needed	18	20	22	MΩ
$R_{OK\ 1} + R_{OK\ 2} + R_{OK3}$	Total resistance for setting VBAT_OK threshold voltage.	11	13	15	MΩ
$R_{OUT1} + R_{OUT2}$	Total resistance for setting VOUT threshold voltage.	11	13	15	MΩ
$R_{OV1} + R_{OV2}$	Total resistance for setting VBAT_OV voltage.	11	13	15	MΩ
L1	Inductance on LBOOST pin	22			µH
L2	Inductance on LBUCK pin	4.7	10		µH
T_A	Operating free air ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		105	°C

(1) Maximum input power ≤ 400 mW. Cold start has been completed
(2) VBAT_OV setting must be higher than VIN_DC

6.4 Thermal Information

THERMAL METRIC(1)		bq25570 RGR 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	12.5	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	12.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over recommended temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for conditions of V_{STOR} = 4.2 V, V_{OUT} = 1.8 V. External components, C_{IN} = 4.7 µF, L1 = 22 µH, C_{STOR} = 4.7 µF, L2 = 10 µH, C_{OUT} = 22 µF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST CHARGER						
$V_{IN(DC)}$	DC input voltage into VIN_DC	Cold-start completed	100		5100	mV
$I_{CHG(CBC\_LIM)}$	Cycle-by-cycle current limit of charger	0.5V < V_{IN} < 4.0 V; VSTOR = 4.2 V		230	285	mA
P_{IN}	Input power range for normal charging	VBAT_OV > VSTOR > VSTOR_CHGEN	0.005		510	mW
$V_{IN(CS)}$	Minimum input voltage for cold start circuit to start charging VSTOR	VBAT < VBAT_UV; VSTOR = 0 V; 0°C < T_A < 85°C		600	700	mV
$VSTOR_{(CHGEN)}$	Voltage on VSTOR when cold start operation ends and normal charger operation commences		1.6	1.73	1.9	V
$P_{IN(CS)}$	Minimum cold-start input power for VSTOR to reach $VSTOR_{(CHGEN)}$ and allow normal charging to commence	VSTOR < $VSTOR_{(CHGEN)}$ VIN_DC clamped to $V_{IN(CS)}$ by cold start circuit VBAT = 100 µF		15		µW
$t_{BAT\_HOT\_PLUG}$	Time for which switch between VSTOR and VBAT closes when battery is hot plugged into VBAT	Battery resistance = 300 Ω, Battery voltage = 3.3V		50		ms
QUIESCENT CURRENTS						
I_Q	$\overline{EN}$ = 0, VOUT_EN = 1 - Full operating mode	VIN_DC = 0V; VSTOR = 2.1V; T_J = 25°C		488	700	nA
		VIN_DC = 0V; VSTOR = 2.1V; –40°C < T_J < 85°C			900	
	$\overline{EN}$ = 0, VOUT_EN = 0 - Partial standby mode	VIN_DC = 0V; VSTOR = 2.1V; T_J = 25°C		445	615	
		VIN_DC = 0V; VSTOR = 2.1V; –40°C < T_J < 85°C			815	
	$\overline{EN}$ = 1, VOUT_EN = x - Ship mode	VBAT = 2.1 V; T_J = 25°C; VSTOR = VIN_DC = 0 V		1	5	
		VBAT = 2.1 V; –40°C < T_J < 85°C; VSTOR = VIN_DC = 0 V			30	
MOSFET RESISTANCES						
$R_{DS(ON)-BAT}$	ON resistance of switch between VBAT and VSTOR	VBAT = 4.2 V		0.95	1.50	Ω

Electrical Characteristics (continued)

Over recommended temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for conditions of V_{STOR} = 4.2 V, V_{OUT} = 1.8 V. External components, C_{IN} = 4.7 µF, L1 = 22 µH, C_{STOR} = 4.7 µF, L2 = 10 µH, C_{OUT} = 22 µF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(ON)\_CHG}$	Charger low side switch ON resistance	VBAT = 4.2 V		0.70	0.90	Ω
	Charger high side switch ON resistance			2.30	3.00	
	Charger low side switch ON resistance	VBAT = 2.1 V		0.80	1.00	
	Charger high side switch ON resistance			3.70	4.80	
$R_{DS(ON)\_BUCK}$	Buck low side switch ON resistance	VBAT = 4.2 V		0.80	1.00	Ω
	Buck high side switch ON resistance			1.60	2.00	
	Buck low side switch ON resistance	VBAT = 2.1 V		1.00	1.20	
	Buck high side switch ON resistance			2.40	2.90	
f_{SW_CHG}	Maximum charger switching frequency			1		MHz
f_{SW_BUCK}	Maximum buck switching frequency			500		kHz
T_{TEMP_SD}	Junction temperature when charging is discontinued	VBAT_OV > VSTOR > 1.8V		125		C
BATTERY MANAGEMENT						
VBAT_OV	Programmable voltage range for overvoltage threshold	VBAT increasing	2.2		5.5	V
VBAT_OV_HYST	Battery over-voltage hysteresis (internal)	VBAT decreasing; VBAT_OV = 5.25V		24	55	mV
VDELTA	VBAT_OV - VIN(DC)	Main boost charger on; MPPT not sampling VOC	400			mV
VBAT_UV	Under-voltage threshold	VBAT decreasing	1.91	1.95	2.0	V
VBAT_UV_HYST	Battery under-voltage hysteresis (internal)	VBAT increasing		15	32	mV
VBAT_OK_HYST	Programmable voltage range of digital signal indicating VSTOR (=VBAT) is OK	VBAT increasing	VBAT_UV		VBAT_OV	V
VBAT_OK_PROG	Programmable voltage range of digital signal indicating VSTOR (=VBAT) is OK	VBAT decreasing	VBAT_UV		VBAT_OK_HYST – 50	mV
VBAT_ACCURACY	Overall Accuracy for threshold values VBAT_OV, VBAT_OK	Selected resistors are 0.1% tolerance	-2%		2%	
VBAT_OK(H)	VBAT_OK (High) threshold voltage	Load = 10 µA			VSTOR – 200	mV
VBAT_OK(L)	VBAT_OK (Low) threshold voltage	Load = 10 µA			100	mV
ENABLE THRESHOLDS						
$\overline{EN}$(H)	Voltage for $\overline{EN}$ high setting. Relative to VBAT.	VBAT = 4.2V	VBAT – 0.2			V
$\overline{EN}$(L)	Voltage for $\overline{EN}$ low setting	VBAT = 4.2V			0.3	V
VOUT_EN(H)	Voltage for VOUT_EN High setting.	VSTOR = 4.2V	VSTOR – 0.4			V
VOUT_EN(L)	Voltage for VOUT_EN Low setting.	VSTOR = 4.2V			0.3	V
BIAS and MPPT CONTROL STAGE						
VOC_SAMPLE	Time period between two MPPT samples			16		s
VOC_STLG	Settling time for MPPT sample measurement of VIN_DC open circuit voltage	Device not switching		256		ms
VIN_REG	Regulation of VIN_DC during charging	0.5 V < VIN < 4 V; IIN(DC) = 10 mA			10%	
MPPT_80	Voltage on VOC_SAMP to set MPPT threshold to 0.80 of open circuit voltage of VIN_DC		VSTOR – 0.015			V

Electrical Characteristics (continued)

Over recommended temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for conditions of V_{STOR} = 4.2 V, V_{OUT} = 1.8 V. External components, C_{IN} = 4.7 µF, L1 = 22 µH, C_{STOR} = 4.7 µF, L2 = 10 µH, C_{OUT} = 22 µF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MPPT_50	Voltage on VOC_SAMP to set MPPT threshold to 0.50 of open circuit voltage of VIN_DC				15	mV
VBIAS	Internal reference for the programmable voltage thresholds	VSTOR ≥ VSTOR_CHGEN	1.205	1.21	1.217	V

6.6 Electrical Characteristics

Over recommended ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for conditions of VSTOR = 4.2 V, V_{OUT} = 1.8 V. External components, C_{IN} = 4.7 µF, L1 = 22 µH, CSTOR = 4.7 µF, L2 = 10 µH, C_{OUT} = 22 µF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK CONVERTER						
VOUT	Output regulation (excluding resistor tolerance error)	I_{OUT} = 10 mA; 1.3 V < V_{OUT} < 3.3 V	–2%		2%	
	Output line regulation	I_{OUT} = 10 mA; VSTOR = 2.1 V to 5.5 V, C_{OUT} = 22 µF		0.09		%/V
	Output load regulation	I_{OUT} = 100 µA to 95 mA, VSTOR = 3.6 V, C_{OUT} = 22 µF		-0.01		%/mA
	Output ripple	VSTOR = 4.2V, I_{OUT} = 1 mA, C_{OUT} = 22 µF		30		mVpp
	Programmable voltage range for output voltage threshold		1.3		VSTOR – 0.2 (1)	V
IOUT	Output Current	VSTOR = 3.3V; V_{OUT} = 1.8 V	93	110		mA
$t_{START-STBY}$	Startup time with $\overline{EN}$ low and VOUT_EN transition to high (Standby Mode)	C_{OUT} = 22 µF		250		µs
$t_{START-SHIP}$	Startup time with VOUT_EN high and $\overline{EN}$ transition from high to low (Ship Mode)	C_{OUT} = 22 µF		100		ms
I-BUCK(CBC-LIM)	Cycle-by-cycle current limit of buck converter	2.4 V < VSTOR < 5.5 V; 1.3 V < V_{OUT} < 3.3 V	160	185	205	mA

(1) The dropout voltage can be computed as the maximum output current times the buck high side resistance.

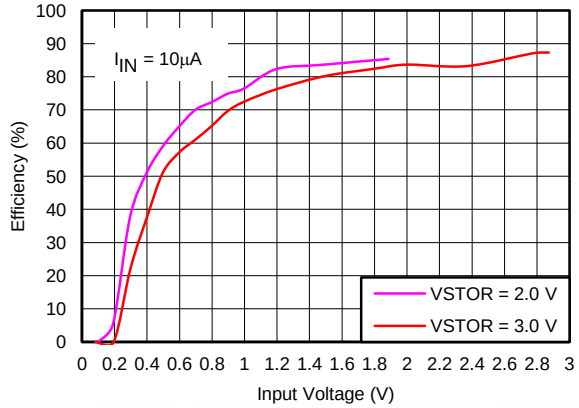
6.7 Typical Characteristics

Unless otherwise noted, graphs were taken using Figure 24 with CIN = 4.7µF, L1 = Coilcraft 22µH LPS4018, CSTOR = 4.7µF, L2 = Toko 10 µH DFE252012C, COUT = 22µF, VBAT_OV=4.2V, VOUT=1.8V

Table 1. Table of Graphs

			FIGURE
Charger Efficiency (η)(1)	vs. Input Voltage	IN= 10 µA	Figure 1
		IN= 100 µA	Figure 2
		IIN = 10 mA	Figure 3
	vs. Input Current	VIN = 2.0 V	Figure 4
		VIN = 1.0 V	Figure 5
		VIN = 0.5 V	Figure 6
		VIN = 0.2 V	Figure 7
VSTOR Quiescent Current	vs. VSTOR Voltage	$\overline{EN}$ = 1, VOUT_EN = X (Ship Mode)	Figure 8
		$\overline{EN}$ = 0, VOUT_EN = 0 (Standby Mode)	Figure 9
VBAT Quiescent Current	vs. VBAT Voltage	$\overline{EN}$ = 0, VOUT_EN = 1 (Active Mode)	Figure 10
Buck Efficiency (η)		vs. Output Current	Figure 11
		vs. Input Voltage	Figure 12
Normalized Buck Output Voltage		vs. Output Current	Figure 13
		vs. Input Voltage	Figure 14
		vs. Temperature	Figure 15
Buck Maximum Output Current vs. Input Voltage	VOUT = 1.8V - 100mV		Figure 16
Buck Major Switching Frequency		vs. Output Current	Figure 17
		vs. Input Voltage	Figure 18
Buck Output Ripple		vs.Output Current	Figure 19
		vs. Input Voltage	Figure 20

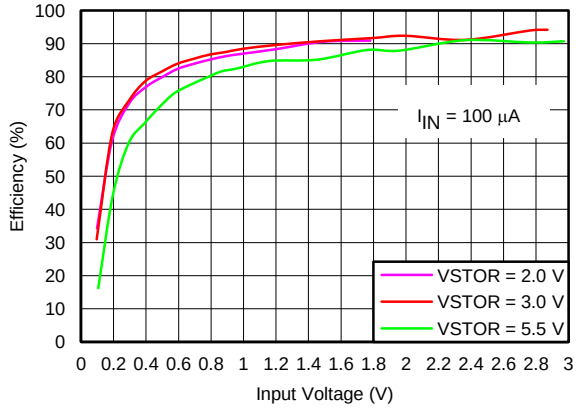
(1) See SLUA691 for an explanation on how to take these measurements. Because the MPPT feature cannot be disabled on the bq25570, these measurements need to be taken in the middle of the 16 s sampling period.



VIN_DC = sourcemeter configured with I_{COMP} = 10 µA and outputing 0 to 3.0 V

VSTOR = sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 2.0 V or 3.0 V

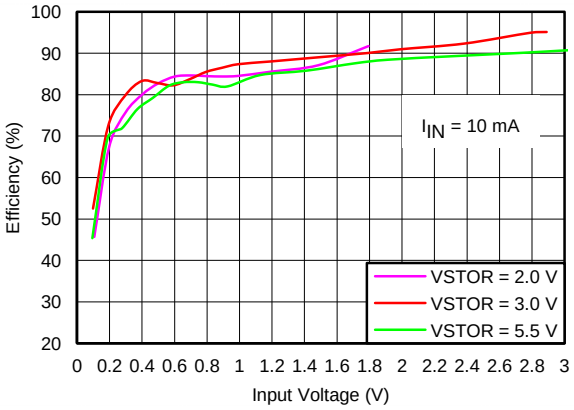
Figure 1. Charger Efficiency vs Input Voltage



VIN_DC = Keithley Source Meter configured with I_{COMP} = 100 µA and voltage source varied from 0.1 V to 3.0 V s

VSTOR = Keithley Sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 2.0 V, 3.0 V or 5.5 V

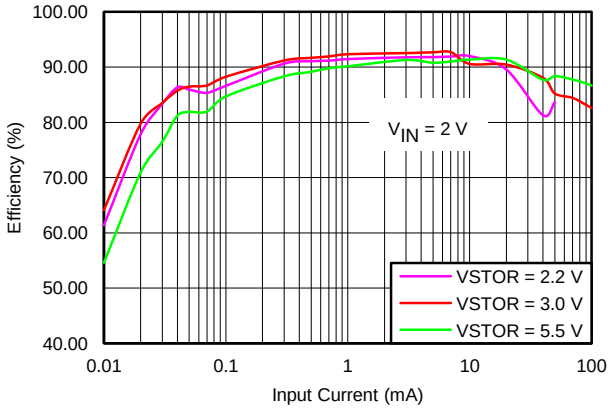
Figure 2. Charger Efficiency vs Input Voltage



VIN_DC = sourcemeter configured with I_{COMP} = 10 mA and voltage source varied from 0.1 V to 3.0 V

VSTOR = sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 2.0 V, 3.0 V or 5.5 V

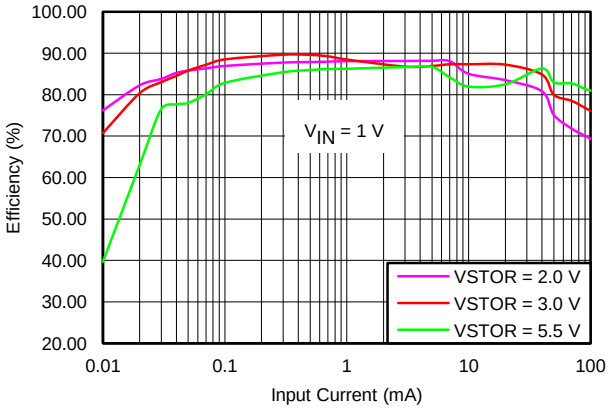
Figure 3. Charger Efficiency vs Input Voltage



VIN_DC = sourcemeter configured with voltage source = 2.0 V and I_{COMP} varied from 0.01 mA to 100 mA

VSTOR = sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 2.2 V , 3.0 V or 5.5 V

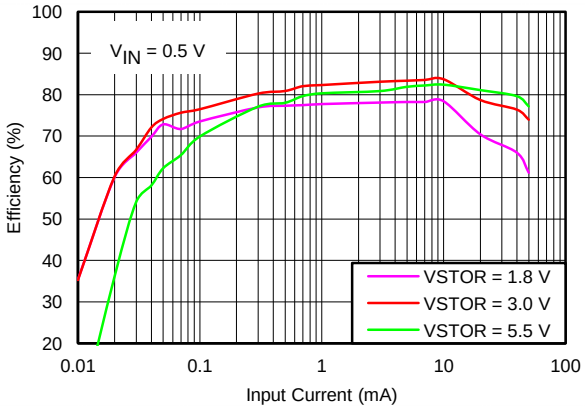
Figure 4. Charger Efficiency vs Input Current



VIN_DC = sourcemeter configured with voltage source = 1.0 V and I_{COMP} varied from 0.01 mA to 100 mA

VSTOR = sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 2.0 V, 3.0 V or 5.5 V

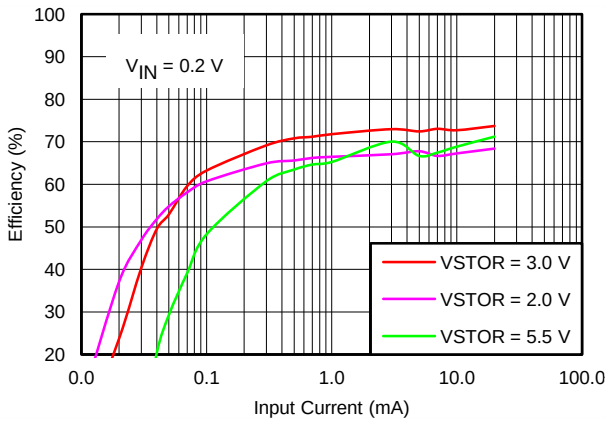
Figure 5. Charger Efficiency vs Input Current



VIN_DC = sourcemeter configured with voltage source = 0.5 V and I_{COMP} varied from 0.01 mA to 100 mA

VSTOR = sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 1.8 V, 3.0 V or 5.5 V

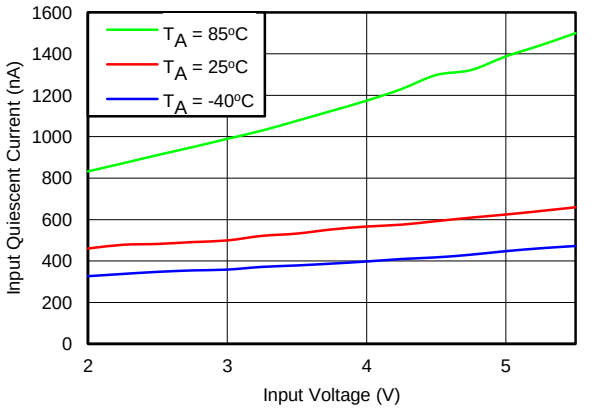
Figure 6. Charger Efficiency vs Input Current



VIN_DC = souremeter configured with voltage source = 0.2 V and I_{COMP} varied from 0.01 mA to 100 mA

VSTOR = sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 2.0 V, 3.0 V or 5.5 V

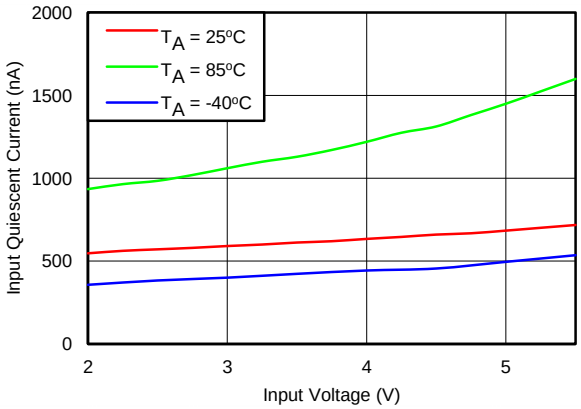
Figure 7. Charger Efficiency vs Input Current



VIN_DC = floating and $\overline{EN}$ = VOUT_EN = GND

VSTOR = sourcemeter configured to measure current and voltage source varied from 2.0 V or 5.5 V

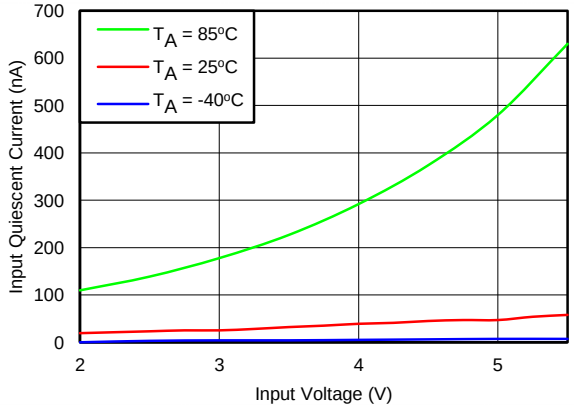
Figure 8. VSTOR Quiescent Current vs VSTOR Voltage: Standby Mode



VIN_DC = floating and $\overline{EN}$ = GND and VOUT_EN=VSTOR

VSTOR= sourcemeter configured to measure current and voltage source varied from 2.0 V or 5.5 V

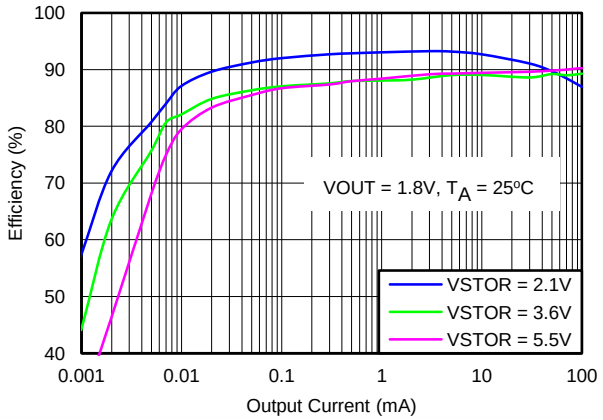
Figure 9. VSTOR Quiescent Current vs VSTOR Voltage: Active Mode



VIN_DC = floating and $\overline{EN}$ = VSTOR

VSTOR = sourcemeter configured to measure current and voltage source varied from 2.0 V or 5.5 V

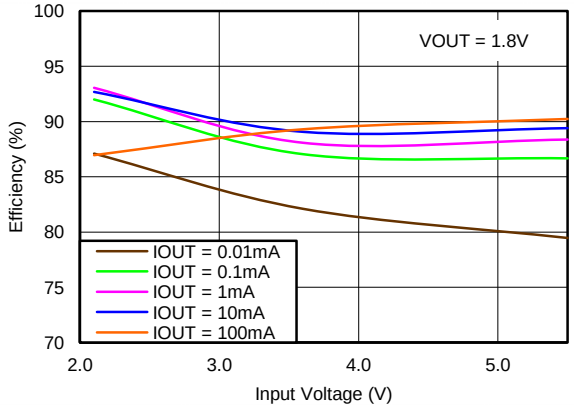
Figure 10. VBAT Quiescent Current vs VBAT Voltage: Ship Mode



VSTOR = sourcemeter configured as a voltage source, measuring current

OUT = sourcemeter configured to sink current with VCOMP>V(OUT)

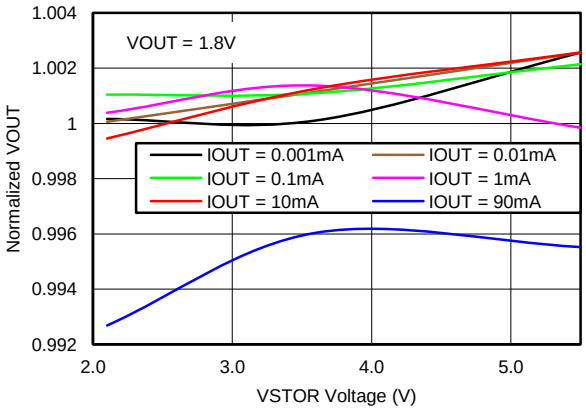
Figure 11. Buck Efficiency vs Output Current



VSTOR = sourcemeter configured as a voltage source, measuring current

OUT = sourcemeter configured sink current with VCOMP>V(OUT)

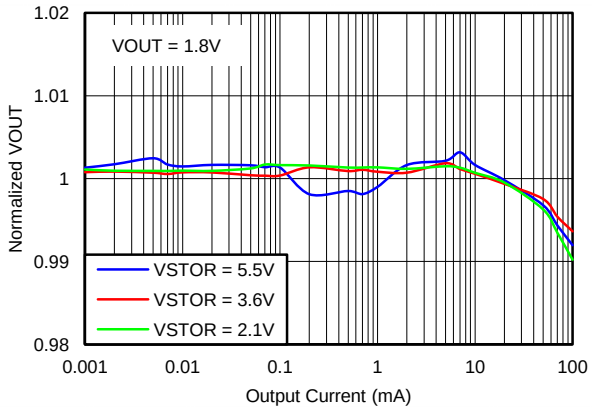
Figure 12. Buck Efficiency vs Input Voltage



VSTOR = sourcemeter configured as a voltage source

OUT = sourcemeter configured to sink current with VCOMP>V(OUT) and measuring voltage

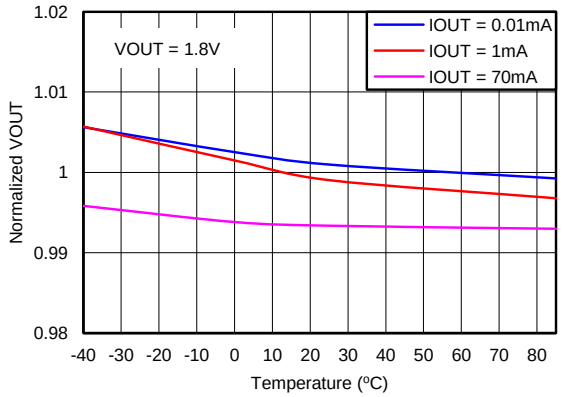
Figure 13. Normalized Buck Output Voltage vs Input Voltage



VSTOR = sourcemeter configured as a voltage source

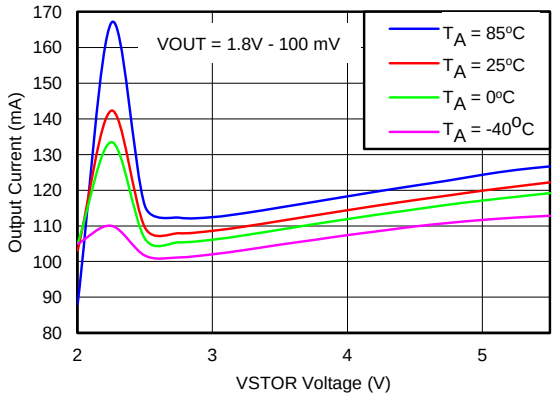
OUT = sourcemeter configured to sink current with VCOMP>V(OUT) and measuring voltage

Figure 14. Normalized Buck Output Voltage vs Output Current



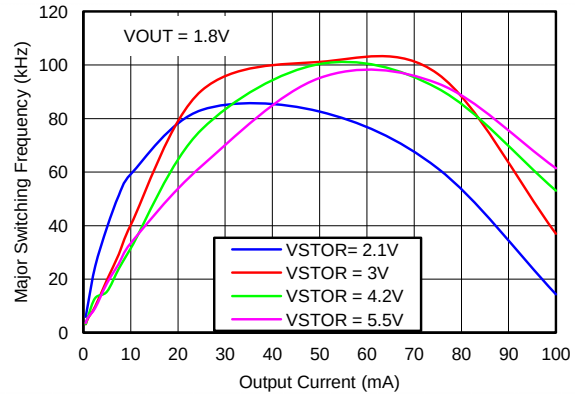
VSTOR = sourcemeter configured as a voltage source
OUT = sourcemeter configured to sink current with VCOMP>V(OUT) and measuring voltage
Thermal stream for temperature variation

Figure 15. Normalized Buck Output Voltage vs Temperature



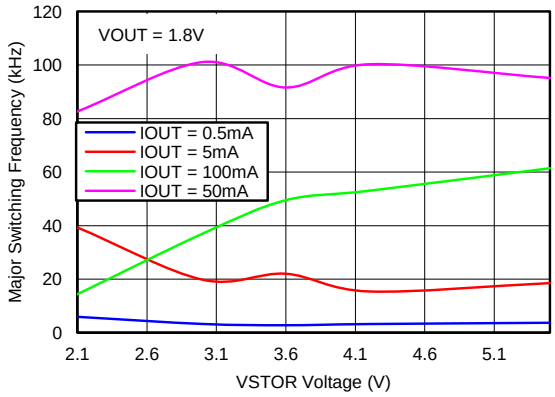
VSTOR = sourcemeter configured as a voltage source
OUT = sourcemeter configured to increasingly sink current with VCOMP>V(OUT) until V(OUT) < VOUT - 100 mV
Thermal stream for temperature variation

Figure 16. Buck Maximum Output Current vs Input Voltage



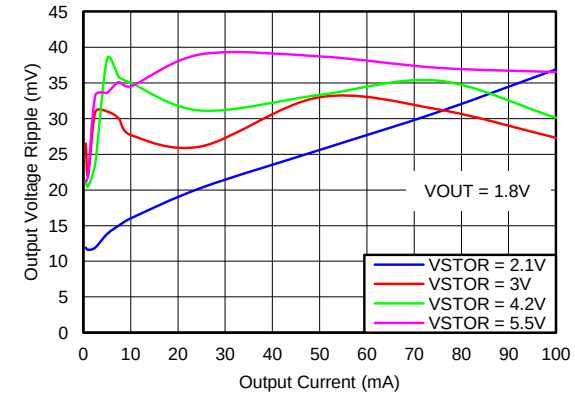
VSTOR = sourcemeter configured as a voltage source
OUT = sourcemeter configured to sink current with VCOMP>V(OUT) and measuring voltage
Oscilloscope used to measure switching frequency at LBOOST

Figure 17. Buck Major Switching Frequency vs Output Current



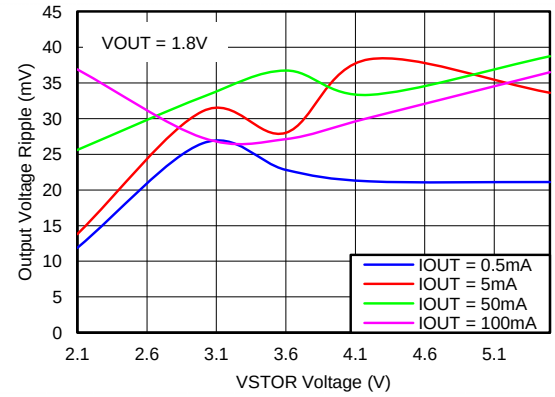
VSTOR = sourcemeter configured as a voltage source
OUT = sourcemeter configured to sink current with VCOMP>V(OUT) and measuring voltage
Oscilloscope used to measure switching frequency at LBOOST

Figure 18. Buck Major Switching Frequency vs Input Voltage



VSTOR = sourcemeter configured as a voltage source
OUT = sourcemeter configured to sink current with VCOMP>V(OUT) and measuring voltage
Oscilloscope used to measure voltage ripple at OUT

Figure 19. Buck Output Voltage Ripple vs Output Current



VSTOR = sourcemeter configured as a voltage source
OUT = sourcemeter configured to sink current with VCOMP>V(OUT) and measuring voltage
Oscilloscope used to measure voltage ripple at OUT

Figure 20. Buck Output Voltage Ripple vs Input Voltage

7 Detailed Description

7.1 Overview

The bq25570 device is a highly integrated energy harvesting Nano-Power management solution that is well suited for meeting the special needs of ultra low-power applications. The product is specifically designed to efficiently acquire and manage the microwatts (µW) to milliwatts (mW) of power generated from a variety of DC sources like photovoltaic (solar) or thermal electric generators. targeted toward products and systems, such as wireless sensor networks (WSN) which have stringent power and operational demands.

The main boost charger is powered from the boost output, VSTOR. Once the VSTOR voltage is above VSTOR_CHGEN (1.8 V typical), for example, after a partially discharged battery is attached to VBAT, the boost charger can effectively extract power from low voltage output harvesters such as TEGs or single or dual cell solar panels outputting voltages down to VIN(DC) (100 mV minimum). When starting from VSTOR = VBAT < 100 mV, the cold start circuit needs at least VIN(CS), 600 mV typical, to charge VSTOR up to 1.8 V.

The bq25570 also implements a programmable maximum power point tracking sampling network to optimize the transfer of power into the device. The fraction of open circuit voltage that is sampled and held can be controlled by pulling VOC_SAMP high or low (80% or 50% respectively) or by using external resistors. This sampled voltage is maintained via internal sampling circuitry and held with an external capacitor (CREF) on the VREF_SAMP pin. For example, solar cells typically operate with a maximum power point (MPP) of 80% of their open circuit voltage. Connecting VOC_SAMP to VSTOR sets the MPPT threshold to 80% and results in the IC regulating the voltage on the solar cell to ensure that the VIN_DC voltage does not fail below the voltage on CREF which equals 80% of the solar panel's open circuit voltage. Alternatively, an external reference voltage can be provided by a MCU to produce a more complex MPPT algorithm.

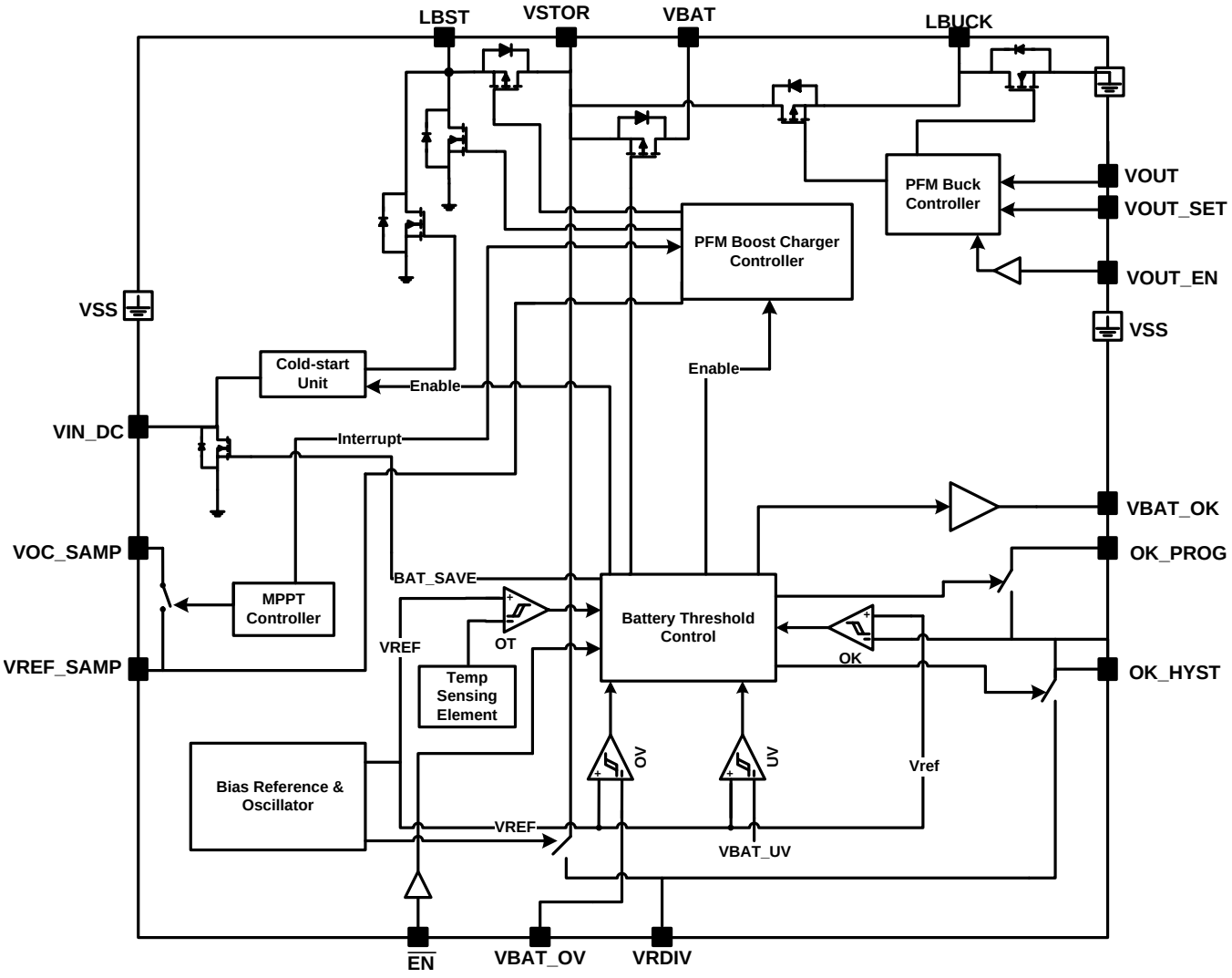
The bq25570 is designed with the flexibility to support a variety of energy storage elements. The availability of the sources from which harvesters extract their energy can often be sporadic or time-varying. Systems will typically need some type of energy storage element, such as a re-chargeable battery, super capacitor, or conventional capacitor. The storage element provides constant power to the system. The storage element also allows the system to handle any peak currents that can not directly come from the input source. To prevent damage to a customer’s storage element, both maximum and minimum voltages are monitored against the internally set under-voltage (UV) and user programmable over-voltage (OV) levels.

To further assist users in the strict management of their energy budgets, the bq25570 toggles the battery good (VBAT_OK) flag to signal an attached microprocessor when the voltage on an energy storage battery or capacitor has dropped below a pre-set critical level. This should trigger the reduction of load currents to prevent the system from entering an under voltage condition. There is also independent enable signals to allow the system to control when to run the regulated output or even put the whole IC into an ultra-low quiescent current sleep state.

In addition to the boost charging front end, the bq25570 provides the system with an externally programmable regulated supply via the buck converter. The regulated output has been optimized to provide high efficiency across low output currents (< 10 µA) to high currents (~110 mA).

All the capabilities of bq25570 are packed into a small foot-print 20-lead 3.5-mm x 3.5-mm QFN package (RGR).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Maximum Power Point Tracking

Maximum power point tracking (MPPT) is implemented in order to maximize the power extracted from an energy harvester source. The boost charger indirectly modulates the input impedance of the main boost charger by regulating the charger's input voltage, as sensed by the VIN_DC pin, to the sampled reference voltage, as stored on the VREF_SAMP pin. The MPPT circuit obtains a new reference voltage every 16 s (typical) by periodically disabling the charger for 256 ms (typical) and sampling a fraction of the open-circuit voltage (VOC). For solar harvesters, the maximum power point is typically 70%-80% and for thermoelectric harvesters, the MPPT is typically 50%. Tying VOC_SAMP to VSTOR internally sets the MPPT regulation point to 80% of VOC. Tying VOC_SAMP to GND internally sets the MPPT regulation point to 50% of VOC. If input source does not have either 80% or 50% of VOC as its MPP point, the exact ratio for MPPT can be optimized to meet the needs of the input source being used by connecting external resistors R_{OC1} and R_{OC2} between VRDIV and GND with mid-point at VOC_SAMP.

The reference voltage is set by the following expression:

$$VREF\_SAMP = VIN\_DC(OpenCircuit)\left(\frac{R_{OC1}}{R_{OC1} + R_{OC2}}\right) \quad (1)$$

Feature Description (continued)

7.3.2 Battery Undervoltage Protection

To prevent rechargeable batteries from being deeply discharged and damaged, and to prevent completely depleting charge from a capacitive storage element, the boost charger has an internally set undervoltage (VBAT_UV) threshold plus an internal hysteresis voltage (VBAT_UV_HYST). The VBAT_UV threshold voltage when the battery voltage is decreasing is internally set to 1.95V (typical). The undervoltage threshold when battery voltage is increasing is given by VBAT_UV plus VBAT_UV_HYST. For the VBAT_UV feature to function properly, the system load should be connected to the VSTOR pin while the storage element should be connected to the VBAT pin. Once the VSTOR pin voltage goes above VBAT_UV plus VBAT_UV_HYST threshold, the VSTOR pin and the VBAT pins are effectively shorted through an internal PMOS FET. The switch remains closed until the VSTOR pin voltage falls below the VBAT_UV threshold. The VBAT_UV threshold should be considered a fail safe to the system and the system load should be removed or reduced based on the VBAT_OK threshold which should be set above the VBAT_UV threshold.

7.3.3 Battery Overvoltage Protection

To prevent rechargeable batteries from being exposed to excessive charging voltages and to prevent over charging a capacitive storage element, the over-voltage (VBAT_OV) threshold level must be set using external resistors. This is also the voltage value to which the charger will regulate the VSTOR/VBAT pin when the input has sufficient power. The VBAT_OV threshold when the battery voltage is rising is given by Equation 2:

$$VBAT\_OV = \frac{3}{2} VBIAS \left(1 + \frac{R_{OV2}}{R_{OV1}} \right) \quad (2)$$

The sum of the resistors is recommended to be no higher than 13 MΩ that is, R_{OV1} + R_{OV2} = 13 MΩ. Spreadsheet SLUC484 provides help on sizing and selecting the resistors. The overvoltage threshold when battery voltage is decreasing is given by VBAT_OV minus VBAT_OV_HYST. Once the voltage at the battery exceeds VBAT_OV threshold, the boost charger is disabled. The charger will start again once the battery voltage drops by VBAT_OV_HYST. When there is excessive input energy, the VBAT pin voltage will ripple between the VBAT_OV and the VBAT_OV_HYST levels.

CAUTION

If VIN_DC is higher than VSTOR and VSTOR is equal to VBAT_OV, the input VIN_DC is pulled to ground through a small resistance to stop further charging of the attached battery or capacitor. It is critical that if this case is expected, the impedance of the source attached to VIN_DC be higher than 20 Ω and not a low impedance source.

7.3.4 Battery Voltage within Operating Range (VBAT_OK Output)

The charger allows the user to set a programmable voltage independent of the overvoltage and undervoltage settings to indicate whether the VSTOR voltage (and therefore the VBAT voltage when the PFET between the two pins is turned on) is at an acceptable level. When the battery voltage is decreasing the threshold is set by Equation 3:

$$VBAT\_OK\_PROG = VBIAS \left(1 + \frac{R_{OK2}}{R_{OK1}} \right) \quad (3)$$

When the battery voltage is increasing, the threshold is set by Equation 4:

$$VBAT\_OK\_HYST = VBIAS \left(1 + \frac{R_{OK2} + R_{OK3}}{R_{OK1}} \right) \quad (4)$$

The sum of the resistors is recommend to be no higher than approximately i.e., R_{OK1} + R_{OK2} + R_{OK3}= 13 MΩ. Spreadsheet SLUC484 provides help on sizing and selecting the resistors. The logic high level of this signal is equal to the VSTOR voltage and the logic low level is ground. The logic high level has ~20 KΩ internally in series to limit the available current in order to prevent MCU damage until the MCU is fully powered. The VBAT_OK_PROG threshold must be greater than or equal to the UV threshold.

Feature Description (continued)

7.3.5 Storage Element / Battery Management

In this section the battery management functionality of the bq25570 integrated circuit (IC) is presented. The IC has internal circuitry to manage the voltage across the storage element and to optimize the charging of the storage element. For successfully extracting energy from the source, two different threshold voltages must be programmed using external resistors, namely battery good threshold (VBAT_OK) and over voltage (OV) threshold. The two user programmable threshold voltages and the internally set undervoltage threshold determine the IC's region of operation. Figure 21 shows the relative position of the various threshold voltages.

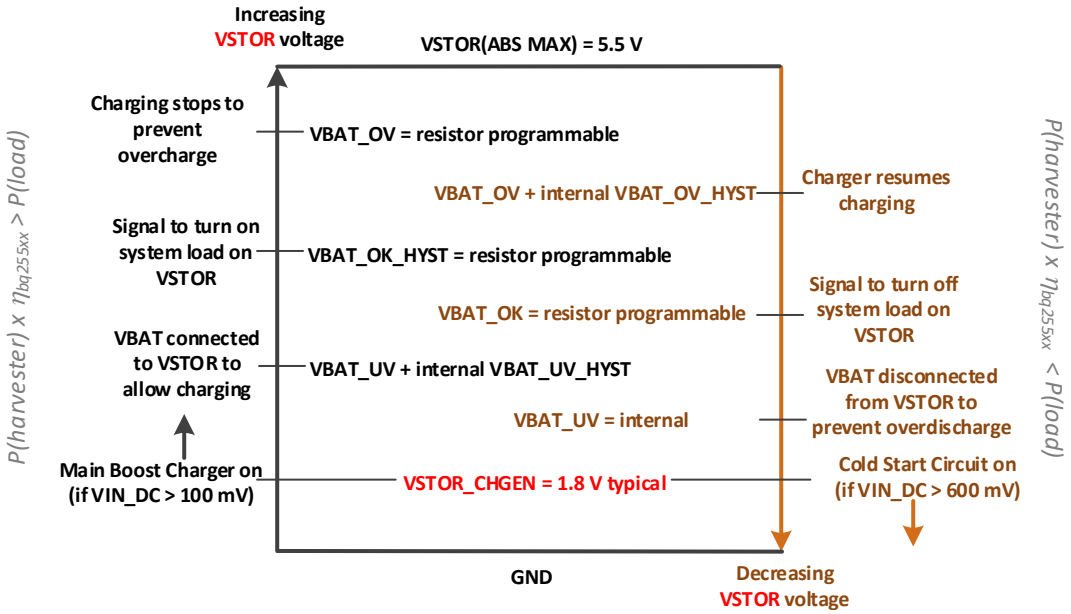


Figure 21. Summary of VSTOR Threshold Voltages

7.3.6 Programming OUT Regulation Voltage

To set the proper output regulation voltage and input voltage power good comparator, the external resistors must be carefully selected.

The OUT regulation voltage is then given by Equation 5:

$$VOUT = VBIAS\left(\frac{R_{OUT2} + R_{OUT1}}{R_{OUT1}}\right) \quad (5)$$

Note that VBIAS is nominally 1.21 V per the electrical specification table. The sum of the resistors is recommended to be no greater than 13 MΩ , that is, R_{OUT1} + R_{OUT2} = 13 MΩ. Higher resistors may result in poor output voltage regulation and/or input voltage power good threshold accuracies due to noise pickup via the high impedance pins or reduction of effective resistance due to parasitic resistances created from board assembly residue. See Layout Considerations section for more details. SLUC484 provides help on sizing and selecting the resistors.

Feature Description (continued)

7.3.7 Step Down (Buck) Converter

The buck regulator input power is internally connected to VSTOR and steps the VSTOR voltage down to a lower regulated voltage at the OUT pin. It employs pulse frequency modulation (PFM) control to regulate the voltage close to the desired reference voltage. The voltage regulated at the OUT pin is set by the user programmed resistor divider. The current through the inductor is controlled through internal current sense circuitry. The peak current in the inductor is controlled to maintain high efficiency of the converter across a wide input current range. The converter delivers an output current up to 110mA typical with a peak inductor current of 200 mA. The buck converter is disabled when the voltage on VSTOR drops below the VBAT_UV condition. The buck converter continues to operate in pass (100% duty cycle) mode, passing the input voltage to the output, as long as VSTOR is greater than VBAT_UV and less than VOUT.

7.3.8 Nano-Power Management and Efficiency

The high efficiency of the bq25570 charger is achieved through the proprietary Nano-Power management circuitry and algorithm. This feature essentially samples and holds the VSTOR voltage to reduce the average quiescent current. That is, the internal circuitry is only active for a short period of time and then off for the remaining period of time at the lowest feasible duty cycle. A portion of this feature can be observed in Figure 28 where the VRDIV node is monitored. Here the VRDIV node provides a connection to the VSTOR voltage (first pulse) and then generates the reference levels for the VBAT_OV and VBAT_OK resistor dividers for a short period of time. The divided down values at each pin are compared against VBIAS as part of the hysteretic control. Because this biases a resistor string, the current through these resistors is only active when the Nano-Power management circuitry makes the connection—hence reducing the overall quiescent current due to the resistors. This process repeats every 64 ms.

The efficiency of the bq25570 boost charger is shown for various input power levels in Figure 1 through Figure 7. All efficiency data points were captured by averaging 50 measurements of the input current in between MPPT sampling events. This must be done due to the pulsing currents of the hysteretic, discontinuous mode boost and buck converters. Quiescent currents into VSTOR, VBAT_SEC and VBAT_PRI over temperature and voltage are shown at Figure 8 through Figure 9.

7.4 Device Functional Modes

The bq25570 has five functional modes: cold start operation, main boost charger disabled (ship mode), main boost charger enabled, buck converter enabled mode and thermal shutdown. When VSTOR is greater than VSTOR_CHGEN (1.8 V typical), the bq25570's two enable pins allow for flexibility in controlling the system. The table below summarizes the functionality.

Table 2. Enable Functionality Table when VSTOR > VSTOR_CHGEN

$\overline{EN}$ PIN LOGIC LEVEL	VOUT_EN PIN LOGIC LEVEL	FUNCTIONAL MODE
0	0	Buck standby mode: boost charger and VBAT_OK are enabled. Buck converter is disabled.
0	1	Boost charger, buck converter and VBAT_OK enabled.
1	x	Ship mode (lowest leakage state): boost charger, PFET between VSTOR and VBAT is off, buck converter and VBAT_OK indication are disabled.

The $\overline{EN}$ high voltage is relative to the VBAT pin voltage. VOUT_EN high voltage is relative to VSTOR. If it is not desired to control $\overline{EN}$, it is recommended that this pin be tied to VSS, or system ground. When $\overline{EN}$ is low, VOUT_EN is used to enable and disable the buck converter. The high-level *Functional Block Diagram* highlights most of the major functional blocks inside the bq25570. The cold start circuitry is powered from VIN_DC. The main boost charger circuitry is powered from VSTOR while the boost power stage is powered from VIN_DC. Details of entering and exiting each mode are explained below.

7.4.1 Main Boost Charger Disabled (Ship Mode) - (VSTOR > VSTOR_CHGEN and $\overline{EN}$ = HIGH)

When taken high relative to the voltage on VBAT_SEC, the $\overline{EN}$ pin shuts down the IC including the boost charger, buck converter and battery management circuitry. It also turns off the PFET that connects VBAT_SEC to VSTOR. This can be described as ship mode, because it will put the IC in the lowest leakage state and provides a long storage period without significantly discharging the battery on VBAT. If there is no need to control $\overline{EN}$, it is recommended that this pin be tied to VSS, or system ground.

7.4.2 Cold-Start Operation (VSTOR < VSTOR_CHGEN, VIN_DC > VIN(CS) and PIN > PIN(CS), $\overline{EN}$ = don't care)

Whenever VSTOR < VSTOR_CHGEN, VIN_DC ≥ VIN(CS) and PIN > PIN(CS), the cold-start circuit is on. This could happen when there is not input power at VIN_DC to prevent the load from discharging the battery or during a large load transient on VSTOR. During cold start, the voltage at VIN_DC is clamped to VIN(CS) so the energy harvester's output current is critical to providing sufficient cold start input power, PIN(CS) = VIN(CS) X IIN(CS). The cold-start circuit is essentially an unregulated, hysteretic boost converter with lower efficiency compared to the main boost charger. None of the other features, including the EN pin, function during cold start operation. The cold start circuit's goal is to charge VSTOR higher than VSTOR_CHGEN so that the main boost charger can operate. When a depleted storage element is initially attached to VBAT, as shown in Figure 22 and the harvester can provide a voltage > VIN(CS) and total power at least > PIN(CS), assuming no system load or leakage at VSTOR and VBAT, the cold start circuit can charge VSTOR above VSTOR_CHGEN. Once the VSTOR voltage reaches the VSTOR_CHGEN threshold, the IC

1. first performs an initialization pulse on VRDIV to reset the feedback voltages,
2. then disables the charger for 32 ms (typical) to allow the VIN_DC voltage to rise to the harvester's open-circuit voltage which will be used as the input voltage regulation reference voltage until the next MPPT sampling cycle and
3. lastly performs its first feedback sampling using VRDIV, approximately 64 ms after the initialization pulse.

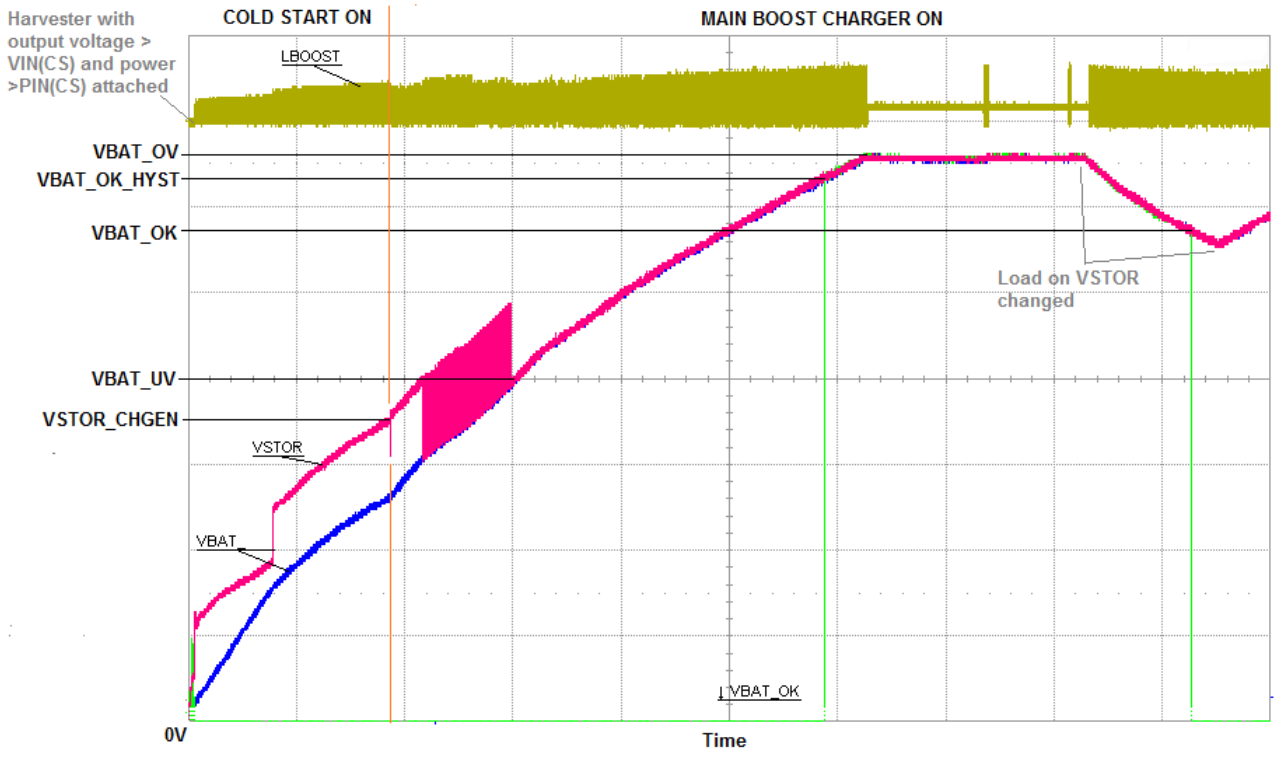


Figure 22. Charger Operation After a Depleted Storage Element is Attached and Harvester Power is Available

The energy harvester must supply sufficient power for the IC to exit cold start. Due to the body diode of the PFET connecting VSTOR and VBAT, the cold start circuit must charge both the capacitor on CSTOR up to the VSTOR_CHGEN and the storage element connected to VBAT up to VSTOR_CHGEN less a diode drop. When a rechargeable battery with an open protector is attached, the initial charge time is typically short due to the minimum charge needed to close the battery's protector FETs. When large, discharged super capacitors with high DC leakage currents are attached, the intial charge time can be significant.

When the VSTOR voltage reaches VSTOR_CHGEN, the main boost charger starts up. When the VSTOR voltage rises to the VBAT_UV threshold, the PMOS switch between VSTOR and VBAT turns on, which provides additional loading on VSTOR and could result in the VSTOR voltage dropping below both the VBAT_UV threshold and the VSTOR_CHGEN voltage, especially if system loads on VSTOR or VBAT are active during this time. Therefore, it is not uncommon for the VSTOR voltage waveform to have incremental pulses (for example, stair steps) as the IC cycles between cold-start and main boost charger operation before eventually maintaing VSTOR above VSTOR_CHGEN.

The cold start circuit initially clamps VIN_DC to VIN(CS) = 600 mV typical. If sufficient input power (that is, output current from the harvester clamped to VIN(CS)) is not available, it is possible that the cold start circuit cannot raise the VSTOR voltage above VSTOR_CHGEN in order for the main boost conveter to start up. It is highly recommended to add an external PFET between the system load and VSTOR. An inverted VBAT_OK signal provided by $\overline{\text{VB\_SEC\_ON}}$ can be used to drive the gate of this system-isolating, external PFET. See the Energy Harvester Selection applications section for guidance on minimum input power requirements.

7.4.3 Main Boost Charger Enabled (VSTOR > VSTOR_CHGEN and $\overline{\text{EN}}$ = LOW)

One way to avoid cold start is to attach a partially charged storage element as shown in Figure 23.

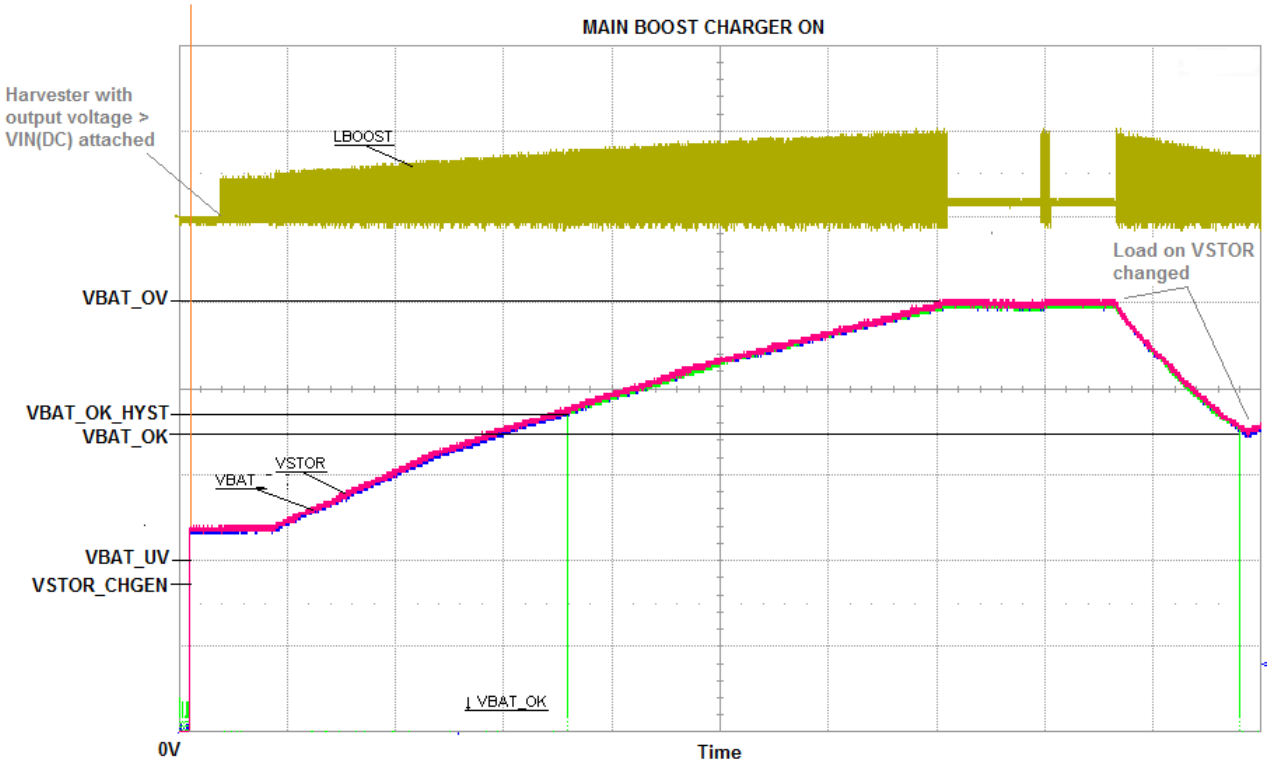


Figure 23. Charger Operation after a Partially Charged Storage Element is Attached and Harvester Power is Available

When no input source is attached, the VSTOR node should be discharged to ground before attaching a storage element. Hot-plugging a storage element that is charged (for example, the battery protector PFET is closed) and with the VSTOR node more than 100 mV above ground results in the PFET between VSTOR and VBAT remaining off until an input source is attached.

Assuming the voltages on VSTOR and VBAT are both below 100 mV, when a charged storage element is attached (that is, hot-plugged) to VBAT, the IC

1. first turns on the internal PFET between the VSTOR and VBAT pins for $t_{BAT\_HOT\_PLUG}$ (45 ms) in order to charge VSTOR to VSTOR_CHGEN then turns off the PFET to prevent the battery from overdischarge,
2. then performs an initialization pulse on VRDIV to reset the feedback voltages,
3. then disables the charger for 32 ms (typical) to allow the VIN_DC voltage to rise to the harvester's open-circuit voltage which will be used as the input voltage regulation reference voltage until the next MPPT sampling cycle and
4. lastly performs its first feedback sampling using VRDIV, approximately 64 ms after the initialization pulse.

If the VSTOR pin voltage remains above the internal under voltage threshold (VBAT_UV) for the additional 64 ms after the VRDIV initialization pulse (following the 45-ms PFET on time), the internal PFET turns back on and the main boost charger begins to charge the storage element assuming there is sufficient power available from the harvester at the VIN_DC pin. If VSTOR does not reach the VBAT_UV threshold, then the PFET remains off until the main boost charger can raise the VSTOR voltage to VBAT_UV. If a system load tied to VSTOR discharges VSTOR below VSTOR_GEN or below VBAT_UV during the 32 ms initial MPPT reference voltage measurement or within 110 ms after hot plug, it is recommended to add an external PFET between the system load and VSTOR. An inverted VBAT_OK signal provided by $\overline{\text{VB_SEC_ON}}$can be used to drive the gate of this system-isolating, external PFET. Otherwise, the VSTOR voltage waveform will have incremental pulses as the IC turns on and off the internal PFET controlled by VBAT_UV or cycles between cold-start and main boost charger operation.

Once VSTOR is above VSTOR_CHGEN but less than VBAT_V and VIN_DC > VIN(DC)-MIN = 100 mV, the main boost charger extracts power from its source by employing pulse frequency modulation (PFM) mode of control to regulate the voltage at VIN_DC close to the desired reference voltage. The reference voltage is set by the MPPT circuitry as described in the features section. Input voltage regulation is obtained by transferring charge from the input to VSTOR only when the input voltage is higher than the voltage on pin VREF_SAMP. The current through the inductor is controlled through internal current sense circuitry. The peak current in the inductor is incremented internally in three pre-determined levels (~50 mA, ~100 mA and finally I-CHG(CBC_LIM)) in order to maintain high efficiency of the charger across a wide input current range. When in discontinous mode, the boost charger can transfer up to a maximum of 100 mA average input current with I-CHG(CBC_LIM) = 230mA typical peak inductor current. The boost charger is disabled when the voltage on VSTOR reaches the user set VBAT_OV threshold to protect the battery connected at VBAT from overcharging. In order for the battery to charge to VBAT_OV, the input power must exceed the power needed for the load on VSTOR. See the Energy Harvester Selection applications section for guidance on minimum input power requirements.

Steady state operation for the boost charger is shown in Figure 23. These plots highlight the inductor current, the VSTOR voltage ripple, input voltage regulation and the LBOOST switching node. The cycle-by-cycle minor switching frequency is a function of each the converter's inductor value, peak current limit and voltage levels on each side of each inductor. Once the VSTOR capacitor, CSTOR, droops below a minimum value, the hysteretic switching repeats.

7.4.3.1 Buck Converter Enabled (VSTOR > VBAT_UV, $\overline{EN}$ = LOW and VOUT_EN = HIGH)

The bq25570 buck converter is hysteretic, peak current, discontinuous mode buck converter as summarized in *Step Down (Buck) Converter*. It has two startup responses: 1) from the ship-mode state ($\overline{EN}$ transitions from high to low with VOUT_EN already high), and 2) from the standby state (VOUT_EN transitions from low to high). The startup response out of ship-mode has the longest time duration due to the internal circuitry being disabled. This response is shown in Figure 35. The startup time takes approximately 100 ms due to the internal Nano-Power management circuitry needing to first complete the 64 ms sample and hold cycle.

Startup from the standby state is shown in Figure 37. This response is much faster due to the internal circuitry being pre-enabled. The startup time from this state is entirely dependent on the size of the output capacitor. The larger the capacitor, the longer it will take to charge during startup. With COUT = 22 µF, the startup time is approximately 400 µs. The buck converter can startup into a pre-biased output voltage.

The buck converter is disabled when the voltage on VSTOR drops below the VBAT_UV condition. The buck converter continues to operate in pass (100% duty cycle) mode, passing the input voltage to the output, as long as VSTOR is greater than VBAT_UV and less than VOUT.

7.4.4 Thermal Shutdown

Rechargeable Li-ion batteries need protection from damage due to operation at elevated temperatures. The application should provide this battery protection and ensure that the ambient temperature is never elevated greater than the expected operational range of 85°C.

The bq25570 uses an integrated temperature sensor to monitor the junction temperature of the device. Once the temperature threshold is exceeded, the boost charger and buck converter are disabled. Once the temperature of the device drops below this threshold, the boost charger and buck converter resume operation. To avoid unstable operation near the overtemperature threshold, a built-in hysteresis of approximately 5°C has been implemented. Care should be taken to not over discharge the battery in this condition since the boost charger is disabled. However, if the supply voltage drops to the VBAT_UV setting, the switch between VBAT and VSTOR will open and protect the battery even if the device is in thermal shutdown.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Energy Harvester Selection

The energy harvesting source (for example, solar panel, TEG, vibration element) must provide a minimum level of power for the IC to operate as designed. The IC's minimum input power required to exit cold start can be estimated as

$$PIN > PIN(CS) = VIN(CS) \times IIN(CS) > \frac{\left(I - STR\_ELM\_LEAK_{@1.8V} \times 1.8V\right) + \frac{(1.8V)^2}{RSTOR(CS)}}{0.05} \quad (6)$$

where I-STR_ELM_LEAK$_{@1.8V}$ is the storage element leakage current at 1.8 V and

RSTOR(CS) is the equivalent resitive load on VSTOR during cold start and 0.05 is an estimate of the worst case efficiency of the cold start circuit.

Once the IC is out of cold start and the system load has been activated (for example, using the VBAT_OK signal), the energy harvesting element must provide the main boost charger with at least enough power to meet the average system load. Assuming RSTOR(AVG) represents the average resistive load on VSTOR, the simplified equation below gives an estimate of the IC's minimum input power needed during system operation:

$$PIN \times \eta_{EST} > PLOAD = \frac{(VBAT\_OV)^2}{RSTOR(AVG)} + VBAT\_OV \times I - STR\_ELM\_LEAK_{@VBAT\_OV} \quad (7)$$

where η_{EST} can be derived from the datasheet efficiency curves for the given input voltage and current and VBAT_OV. The simplified equation above assumes that, while the harvester is still providing power, the system goes into low power or sleep mode long enough to charge the storage element so that it can power the system when the harvester eventually is down. Refer to SLUC461 for a design example that sizes the energy harvester.

8.1.2 Storage Element Selection

In order for the charge management circuitry to protect the storage element from over-charging or discharging, the storage element must be connected to VBAT pin and the system load tied to the VSTOR pin. Many types of elements can be used, such as capacitors, super capacitors or various battery chemistries. A storage element with 100 µF equivalent capacitance is required to filter the pulse currents of the PFM switching charger. The equivalent capacitance of a battery can be computed as computed as

$$C_{EQ} = \frac{2 \times mAHr_{BAT(CHRGD)} \times 3600\ s/Hr}{V_{BAT(CHRGD)}} \quad (8)$$

In order for the storage element to be able to charge VSTOR capacitor (CSTOR) within the $t_{VB\_HOT\_PLUG}$ (50 ms typical) window at hot-plug; therefore preventing the IC from entering cold start, the time constant created by the storage element's series resistance (plus the resistance of the internal PFET switch) and equivalent capacitance must be less than $t_{VB\_HOT\_PLUG}$. For example, a battery's resistance can be computed as:

$R_{BAT} = V_{BAT} / I_{BAT(CONTINUOUS)}$ from the battery specifications. (9)

The storage element must be sized large enough to provide all of the system load during periods when the harvester is no longer providing power. The harvester is expected to provide at least enough power to fully charge the storage element while the system is in low power or sleep mode. Assuming no load on VSTOR (i.e., the system is in low power or sleep mode), the following equation estimates charge time from voltage VBAT1 to VBAT2 for given input power is:

$PIN \times \eta_{EST} \times t_{CHRG} = 1/2 \times CEQ \times (VBAT2^2 - VBAT1^2)$ (10)

Application Information (continued)

Refer to SLUC461 for a design example that sizes the storage element.

Note that if there are large load transients or the storage element has significant impedance then it may be necessary to increase the CSTOR capacitor from the 4.7 µF minimum or add additional capacitance to VBAT in order to prevent a droop in the VSTOR voltage. Refer to Inductor Selection for sizing capacitors.

8.1.3 Inductor Selection

The boost charger and the buck converter each need an appropriately sized inductor for proper operation. The inductor's saturation current should be at least 25% higher than the expected peak inductor currents recommended below if system load transients on VSTOR and/or VOUT are expected. Since this device uses hysteretic control for both the boost charger and buck converter, both are considered naturally stable systems (single order transfer function).

8.1.3.1 Boost Charger Inductor Selection

For the boost charger to operate properly, an inductor of appropriate value must be connected between LBOOST, pin 20, and VIN_DC, pin 2. The boost charger internal control circuitry is designed to control the switching behavior with a nominal inductance of 22 µH ± 20%. The inductor must have a peak current capability of > 300 mA with a low series resistance (DCR) to maintain high efficiency.

A list of inductors recommended for this device is shown in Table 3.

Table 3. Boost Charger Inductor Selection

INDUCTANCE (µH)	DIMENSIONS (mm)	PART NUMBER	MANUFACTURER
22	4.0x4.0x1.7	LPS4018-223M	Coilcraft
22	3.8x3.8x1.65	744031220	Wuerth

8.1.3.2 Buck Converter Inductor Selection

For buck converter to operate properly, an inductor of appropriate value must be connected between LBUCK, pin 16, and VOUT, pin 14. The buck converter internal control circuitry is designed to control the switching behavior with a nominal inductance of 10 µH ± 20%. The inductor must have a peak current capability of > 200 mA with a low series resistance (DCR) to maintain high efficiency. The speed of the peak current detect circuit sets the inductor's lower bound to 4.7 µH. When using a 4.7 µH, the peak inductor current will increase when compared to that of a 10 µH inductor, resulting in slightly higher major frequency.

A list of inductors recommended for this device is shown in Table 4.

Table 4. Buck Converter Inductor Selection

INDUCTANCE (µH)	DIMENSIONS (mm)	PART NUMBER	MANUFACTURER
10	2.0 x 2.5 x 1.2	DFE252012C-H-100M	Toko
10	4.0x4.0x1.7	LPS4018-103M	Coilcraft
10	2.8x2.8x1.35	744029100	Wuerth
10	3.0x3.0x1.5	74438335100	Wuerth
10	2.5x2.0x1.2	74479889310	Wuerth
4.7	2.0 x 2.5 x 1.2	DFE252012R-H-4R7M	Toko

8.1.4 Capacitor Selection

In general, all the capacitors need to be low leakage. Any leakage the capacitors have will reduce efficiency, increase the quiescent current and diminish the effectiveness of the IC for energy harvesting.

8.1.4.1 VREF_SAMP Capacitance

The MPPT operation depends on the sampled value of the open circuit voltage and the input regulation follows the voltage stored on the CREF capacitor. This capacitor is sensitive to leakage since the holding period is around 16 seconds. As the capacitor voltage drops due to any leakage, the input regulation voltage also drops preventing proper operation from extraction the maximum power from the input source. Therefore, it is recommended that the capacitor be an X7R or COG low leakage capacitor.

8.1.4.2 VIN_DC Capacitance

Energy from the energy harvester input source is initially stored on a capacitor, CIN, connected to VIN_DC, pin 2, and VSS, pin 1. For energy harvesters which have a source impedance which is dominated by a capacitive behavior, the value of the harvester capacitor should scaled according to the value of the output capacitance of the energy source, but a minimum value of 4.7 µF is recommended.

8.1.4.3 VSTOR Capacitance

Operation of the bq25570 requires two capacitors to be connected between VSTOR, pin 19, and VSS, pin 1. A high frequency bypass capacitor of at 0.01 µF should be placed as close as possible between VSTOR and VSS. In addition, a low ESR capacitor of at least 4.7 µF should be connected in parallel.

8.1.4.4 VOUT Capacitance

The output capacitor is chosen based on transient response behavior and ripple magnitude. The lower the capacitor value, the larger the ripple will become and the larger the droop will be in the case of a transient response. It is recommended to use at least a 22 µF output capacitor between VOUT, pin 14 and VSS, pin 15, for most applications.

8.1.4.5 Additional Capacitance on VSTOR or VBAT

If there are large, fast system load transients and/or the storage element has high resistance, then the CSTOR capacitors may momentarily discharge below the VBAT_UV threshold in response to the transient. This causes the bq25570 to turn off the PFET switch between VSTOR and VBAT and turn on the boost charger. The CSTOR capacitors may further discharge below the VSTOR_CHGEN threshold and cause the bq25570 to enter Cold Start. For instance, some Li-ion batteries or thin-film batteries may not have the current capacity to meet the surge current requirements of an attached low power radio. To prevent VSTOR from drooping, either increasing the CSTOR capacitance or adding additional capacitance in parallel with the storage element is recommended. For example, if boost charger is configured to charge the storage element to 4.2 V and a 500 mA load transient of 50 µs duration infrequently occurs, then, solving I = C x dv/dt for CSTOR gives :

$$\text{CSTOR} \geq \frac{500\ \text{mA} \times 50\ \mu\text{s}}{(4.2\ \text{V} - 1.8\ \text{V})} = 10.5\ \mu\text{F} \tag{11}$$

Note that increasing CSTOR is the recommended solution but will cause the boost charger to operate in the less efficient cold start mode for a longer period at startup compared to using CSTOR = 4.7 µF. If longer cold start run times are not acceptable, then place the additional capacitance in parallel with the storage element.

8.2 Typical Applications

8.2.1 Solar Application Circuit

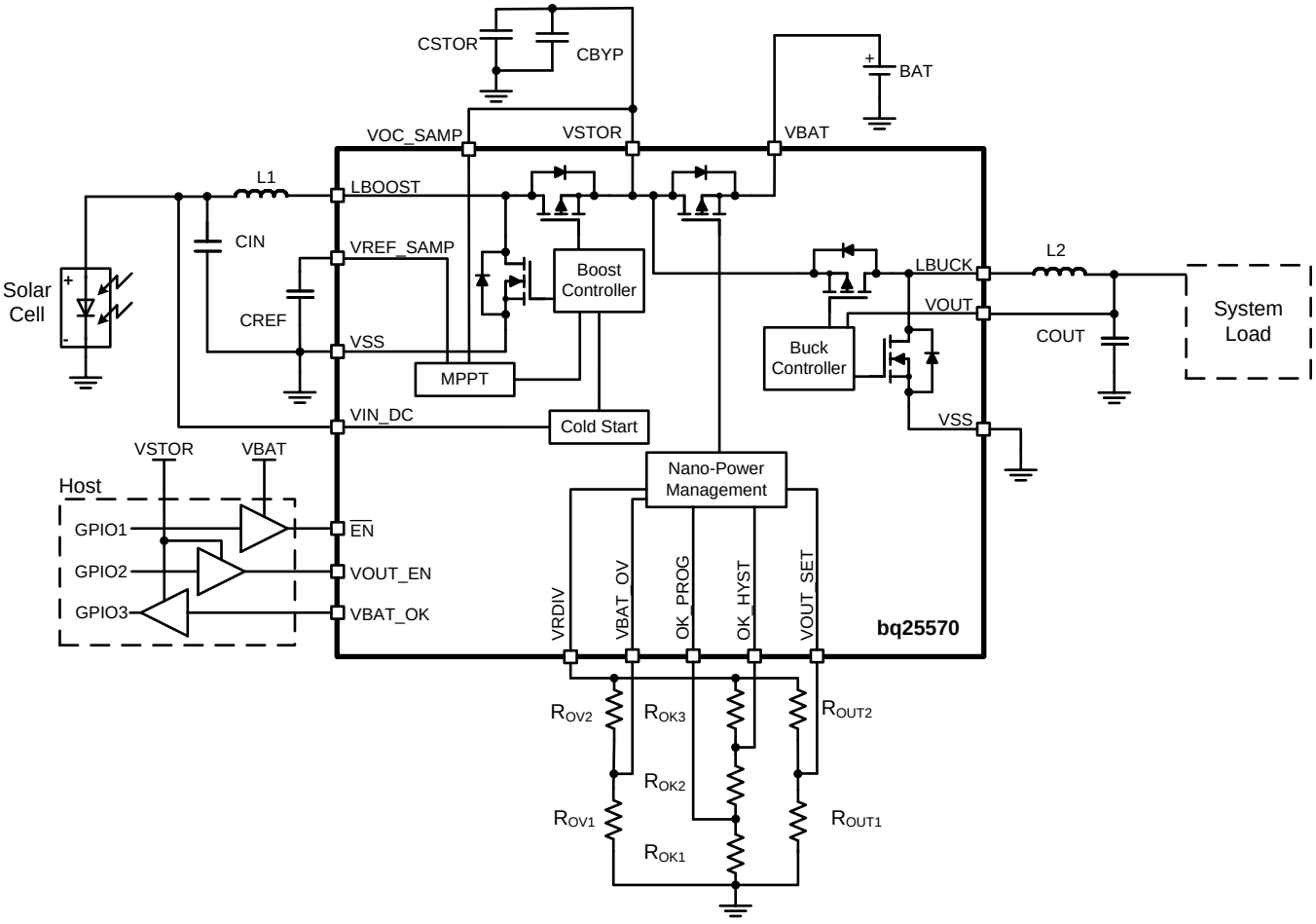


Figure 24. Typical Solar Application Circuit

8.2.1.1 Design Requirements

The desired voltage levels are VBAT_OV = 4.2 V, VBAT_OK = 2.39 V, VBAT_OK_HYST = 2.80 V and MPP (V_{OC}) = 80% which is typical for solar panels. A 1.8-V, up to 100-mA power rail is also needed. There are no large load transients expected on either rail.

8.2.1.2 Detailed Design Procedure

The recommended L1 = 22 µH with ISAT ≥ I-CHG(CBC_LIM)$_{MAX}$, L2 = 10 µH with ISAT ≥ I-BUCK(CBC_LIM)$_{MAX}$, CBYP = 0.01 µF and low leakage CREF = 10 nF are selected. In order to ensure the fastest recovery of the harvester output voltage to the MPPT level following power extraction, the minimum recommended CIN = 4.7 µF is selected. Because no large system load transients are expected and to ensure fast charge time during cold start, the minimum recommended CSTOR = 4.7 µF.

No MPPT resistors are required because VOC_SAMP can be tied to VSTOR to give 80% MPPT.

- Keeing in mind VBAT_UV < VBAT_OV ≤ 5.5 V, to size the VBAT_OV resistors, first choose $RSUM_{OV} = R_{OV1} + R_{OV2}$ = 13 MΩ then solve Equation 2 for

$$R_{OV1} = \frac{3}{2} \times \frac{RSUM_{OV} \times VBIAS}{VBAT\_OV} \times \frac{3}{2} \frac{13\ M\Omega \times 1.21\ V}{4.2\ V} = 5.61\ M\Omega \rightarrow 5.62\ M\Omega \text{ closest 1\% value then} \quad (12)$$

- $R_{OV2} = RSUM_{OV} - R_{OV1}$ = 13 MΩ - 5.62 MΩ = 7.38 MΩ → 7.32 MΩ resulting in VBAT_OV = 4.18V due to rounding to the nearest 1% resistor.

Typical Applications (continued)

- Keeping in mind VBAT_OV ≥ VBAT_OK_HYST > VBAT_OK ≥ VBAT_UV, to size the VBAT_OK and VBAT_OK_HYST resistors, first choose $RSUM_{OK} = R_{OK1} + R_{OK2} + R_{OK3}$ = 13 MΩ then solve Equation 3 and Equation 4 for

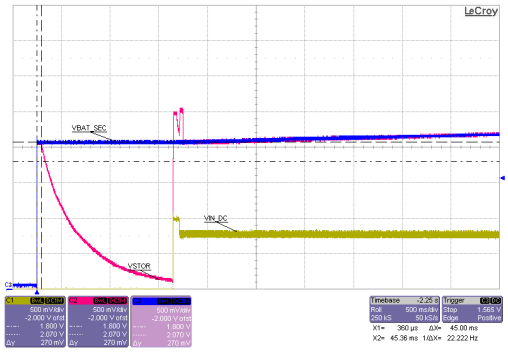
$$R_{OK1} = \frac{VBIAS \times RSUM_{OK}}{VBAT\_OK\_HYST} = \left(\frac{1.21\ V}{2.8\ V}\right) \times 13\ M\Omega = 5.62\ M\Omega \text{ then} \quad (13)$$

$$R_{OK2} = \left(\frac{VBAT\_OK}{VBIAS} - 1\right) \times R_{OK1} = \left(\frac{2.39\ V}{1.21\ V} - 1\right) \times 5.62\ M\Omega = 5.479\ M\Omega \rightarrow 5.49\ M\Omega, \text{ then} \quad (14)$$

- $R_{OK3} = RSUM_{OK} - R_{OK1} - R_{OK2}$ = 13 MΩ - 5.62 MΩ - 5.479 MΩ = 1.904 MΩ → 1.87 MΩ to give VBAT_OK = 2.39 V and VBAT_OK_HYST = 2.80 V.
- For VOUT, first choose $R_{OUT1} + R_{OUT2}$ = RSUMOUT = 13 MΩ, then solve Equation 5 for R_{OUT1} = VBIAS / VOUT x $RSUM_{OUT}$ = 1.21 V / 1.8 V x 13 MΩ = 8.74 MΩ → 8.66 MΩ after rounding to nearest 1% value.
- ROUT2 = RSUM - ROUT1 = 13 MΩ - 8.66 MΩ = 4.34 MΩ → 4.22 MΩ after rounding.

SLUC484 provides help on sizing and selecting the resistors.

8.2.1.3 Application Curves

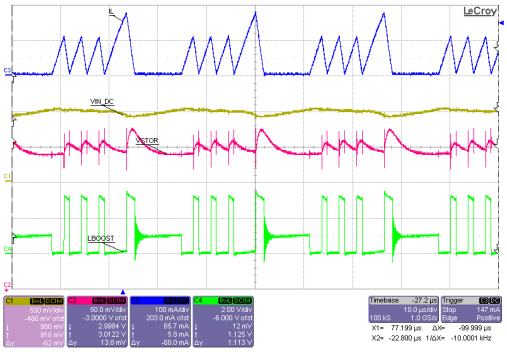


Sourcemeter with V_{SOURCE} = 1.0 V and compliance of 8.5 mA subsequently applied to VIN_DC

VBAT = 0.1 F capacitor charged to 2.0 V

Resistance on VSTOR = 100 kΩ

Figure 25. Startup by Battery Attach With Almost Depleted Storage Element

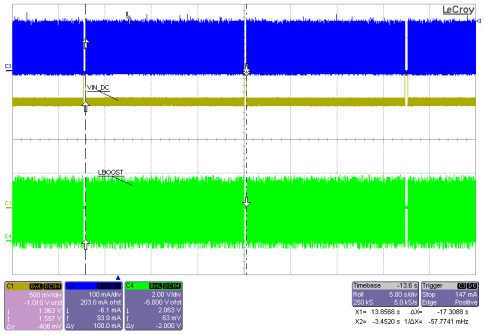


VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA

VBAT = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

IL = inductor current

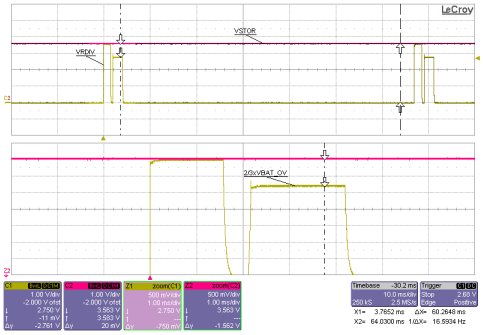
Figure 26. Boost Charger Operational Waveforms



VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA

VBAT = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

Figure 27. MPPT Operation

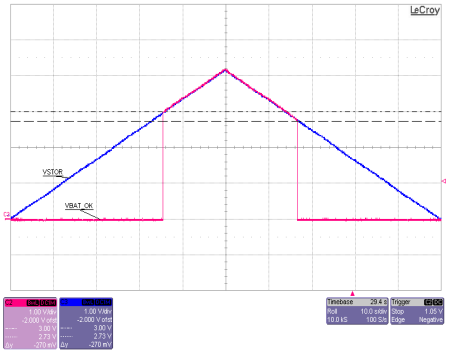


VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA

VBAT = sourcemeter with V_{SOURCE} = 3.6 V and compliance of 1 A

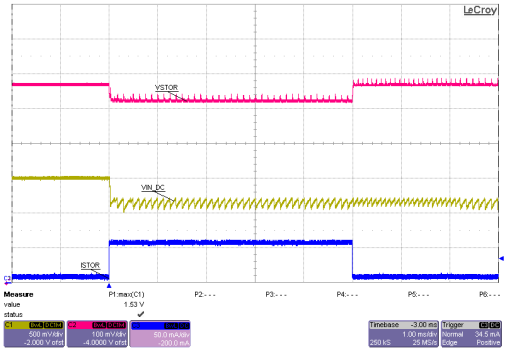
Figure 28. VRDIV Waveform

Typical Applications (continued)



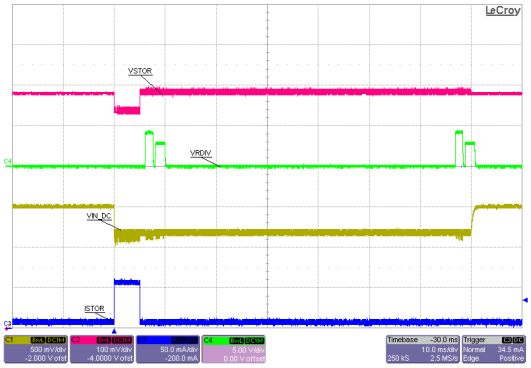
VIN_DC = 1.5 V with 75 Ω series resistance
No storage element on VBAT or VBAT_PRI
VSTOR artifically ramped from 0 V to 4.2 V to 0 V using a power amp driven by a function generator

Figure 29. VBAT_OK Operation



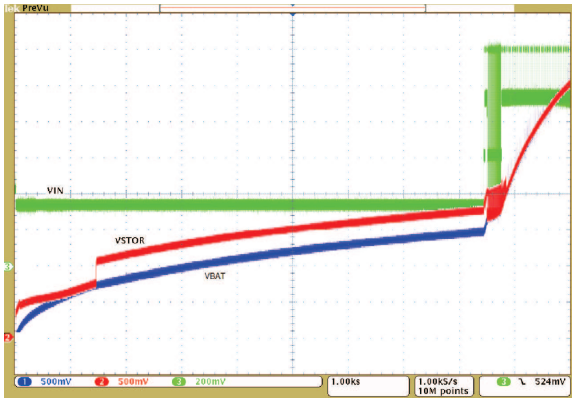
VIN_DC = 1.5 V with 75 Ω series resistance
VBAT = 4.2 V charged 0.5 F capacitor
R(VSTOR) = open to 84 Ω to open

Figure 30. 50 mA Load Transient on VSTOR



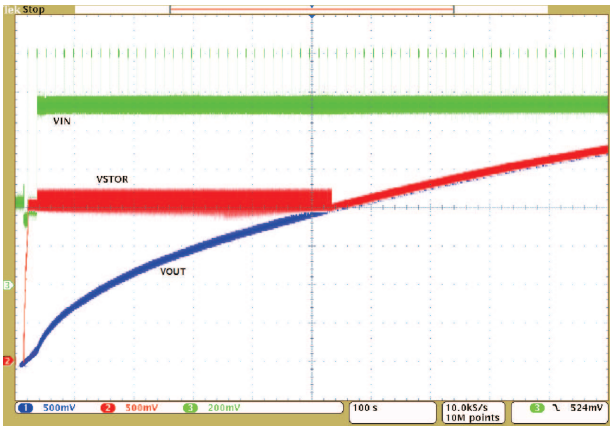
VIN_DC = 1.5 V with 75 Ω series resistance
VBAT = 4.2 V charged 0.5 F capacitor
R(VSTOR) = open to 84 Ω to open

Figure 31. 50 mA Load Transient on VSTOR - Zoom Out



VIN_DC = source meter with 1.2 V compliance and ISC = 1.0 mA
120 mF super capacitor on VBAT

Figure 32. Charging a Super Capacitor on VBAT



VIN_DC = source meter with 1.2 V compliance and ISC = 1.0 mA
120 mF super capacitor on VOUT with VOUT regulation voltage changed to 4.2 V.

Figure 33. Charging a Super Capacitor on VOUT

Typical Applications (continued)

8.2.2 TEG Application Circuit

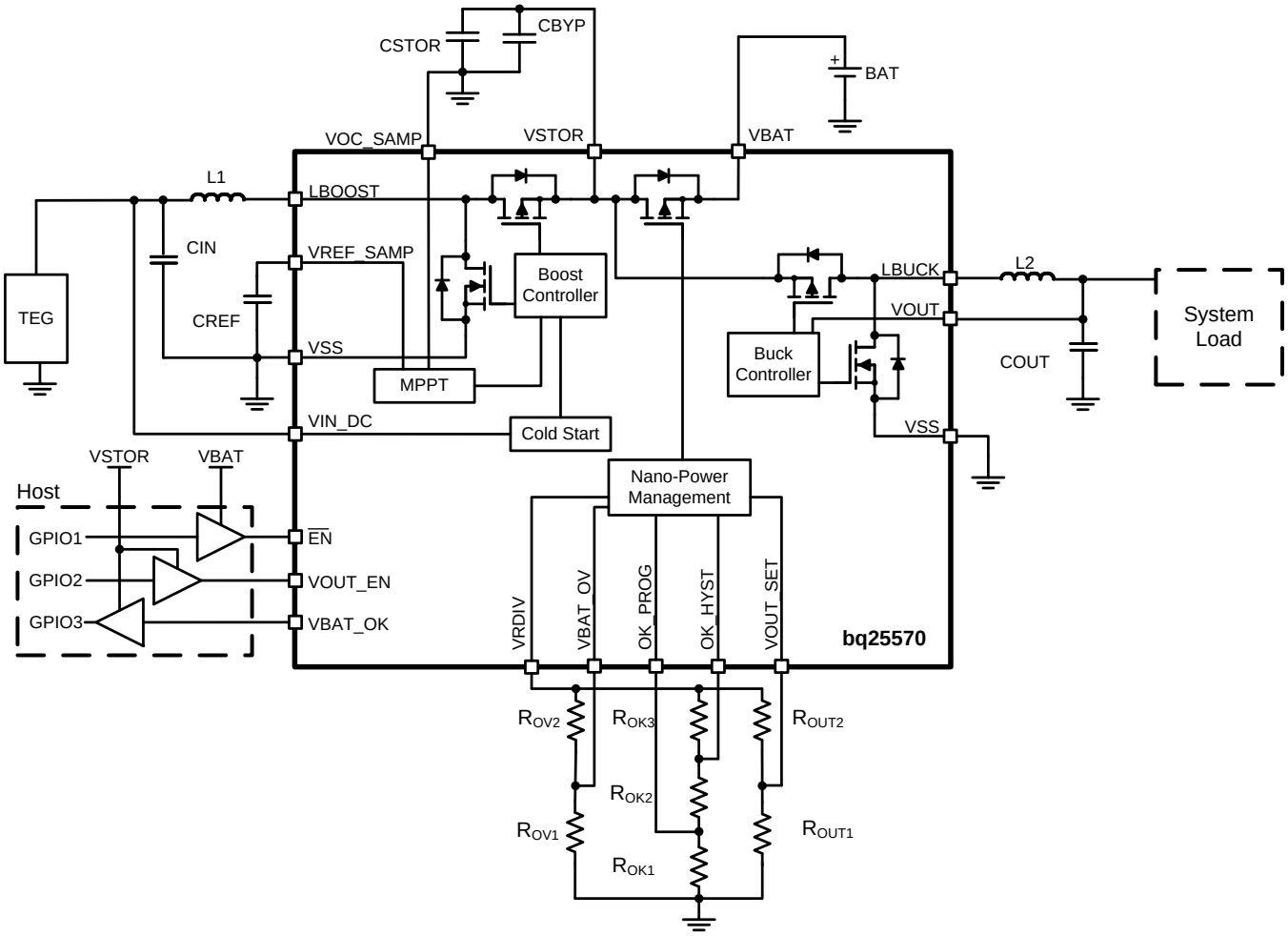


Figure 34. Typical TEG Application Circuit

8.2.2.1 Design Requirements

The desired voltage levels are VBAT_OV = 5.0 V, VBAT_OK = 3.5 V, VBAT_OK_HYST = 3.7 V and MPP (V_{OC}) = 50% which is typical for TEG harvesters. A 1.8-V, up to 100-mA power rail is also needed. There are no large load transients expected on either rail.

8.2.2.2 Detailed Design Procedure

The recommended L1 = 22 µH with ISAT ≥ I-CHG(CBC_LIM)$_{MAX}$, L2 = 10 µH with ISAT ≥ I-BUCK(CBC_LIM)$_{MAX}$, CBYP = 0.01 µF and low leakage CREF = 10 nF are selected. In order to ensure the fastest recovery of the harvester output voltage to the MPPT level following power extraction, the minimum recommended CIN = 4.7 µF is selected. Because no large system load transients are expected and to ensure fast charge time during cold start, the minimum recommended CSTOR = 4.7 µF.

No MPPT resistors are required because VOC_SAMP can be tied to GND to give 50% MPPT.

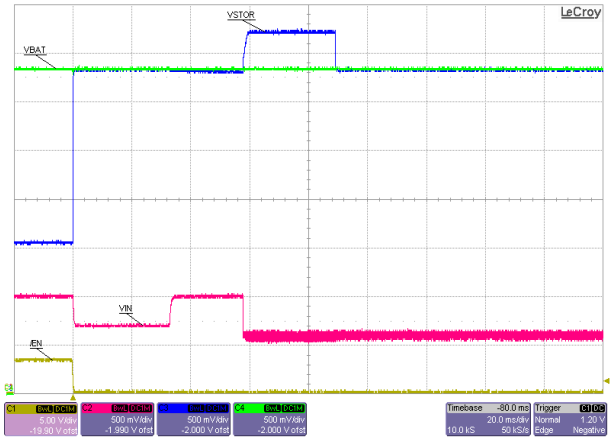
Referring back to the procedure in *Detailed Design Procedure* or using the spreadsheet calculator at SLUC484 gives the following values:

- R_{OV1} = 4.75 MΩ, R_{OV2} = 8.25 MΩ resulting in VBAT_OV = 4.97 V due to rounding to the nearest 1% resistor.
- R_{OK1} = 4.22 MΩ, R_{OK2} = 8.06 MΩ, R_{OK3} = 0.698 MΩ resulting in VBAT_OK = 3.5 V and VBAT_OK_HYST = 3.7 V after rounding.

Typical Applications (continued)

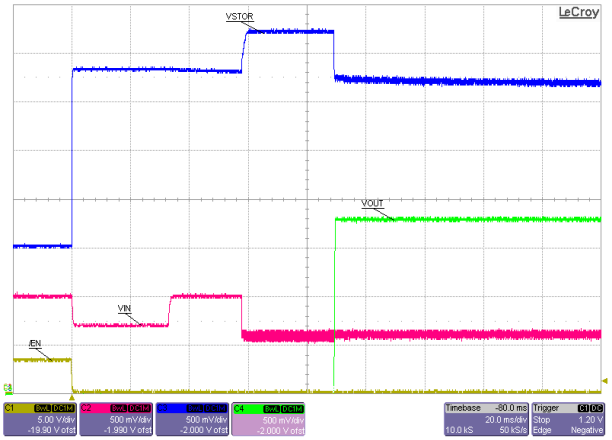
- R_{OUT1} = 8.66 MΩ and R_{OUT2} = 4.22 MΩ resulting in VOUT = 1.8V.

8.2.2.3 Application Curves



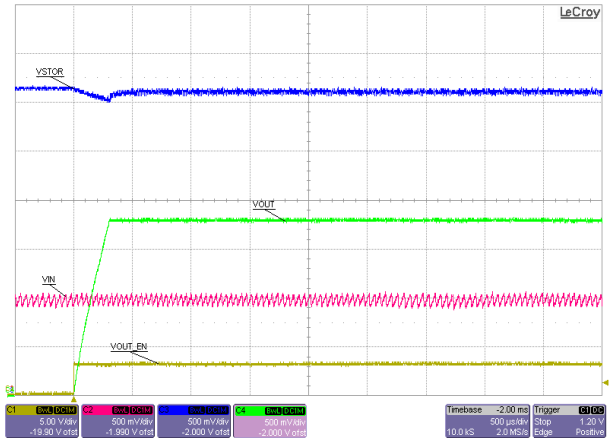
VIN_DC = 1.0 V power supply 100Ω series resistance
VBAT = 3.4-V charged Li coin cell

Figure 35. Startup by Taking $\overline{EN}$ Low (From Ship Mode)



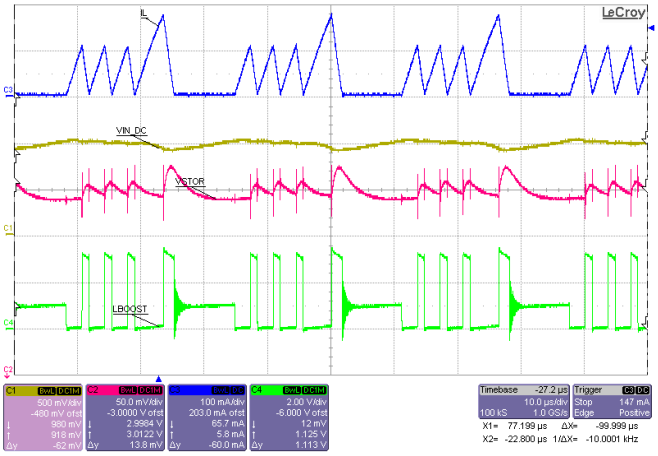
VIN_DC = 1.0 V power supply 100Ω series resistance
VBAT = 3.4-V charged Li coin cell

Figure 36. Startup by taking $\overline{EN}$ low (from Ship mode), including VOUT



VIN_DC = 2.0 V power supply 100Ω series resistance
VBAT = 3.1-V charged Li coin cell

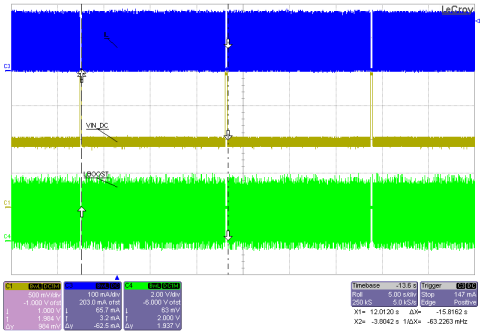
Figure 37. Startup by taking VOUT_EN high (from Standby mode)



VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA
VBAT = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

Figure 38. Boost Charger Operational Waveforms

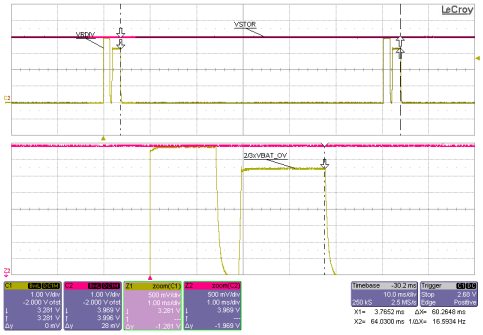
Typical Applications (continued)



VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA

VBAT = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

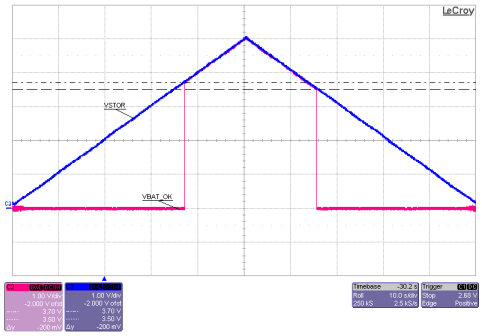
Figure 39. MPPT Operation



VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA

VBAT = sourcemeter with V_{SOURCE} = 4.0 V and compliance of 1 A

Figure 40. VRDIV Waveform



VIN_DC floating

No storage element on VBAT or VBAT_PRI

VSTOR artifically ramped from 0 V to 5.0 V to 0 V using a function generator

Figure 41. VBAT_OK Operation

Typical Applications (continued)

8.2.3 Piezoelectric Application Circuit

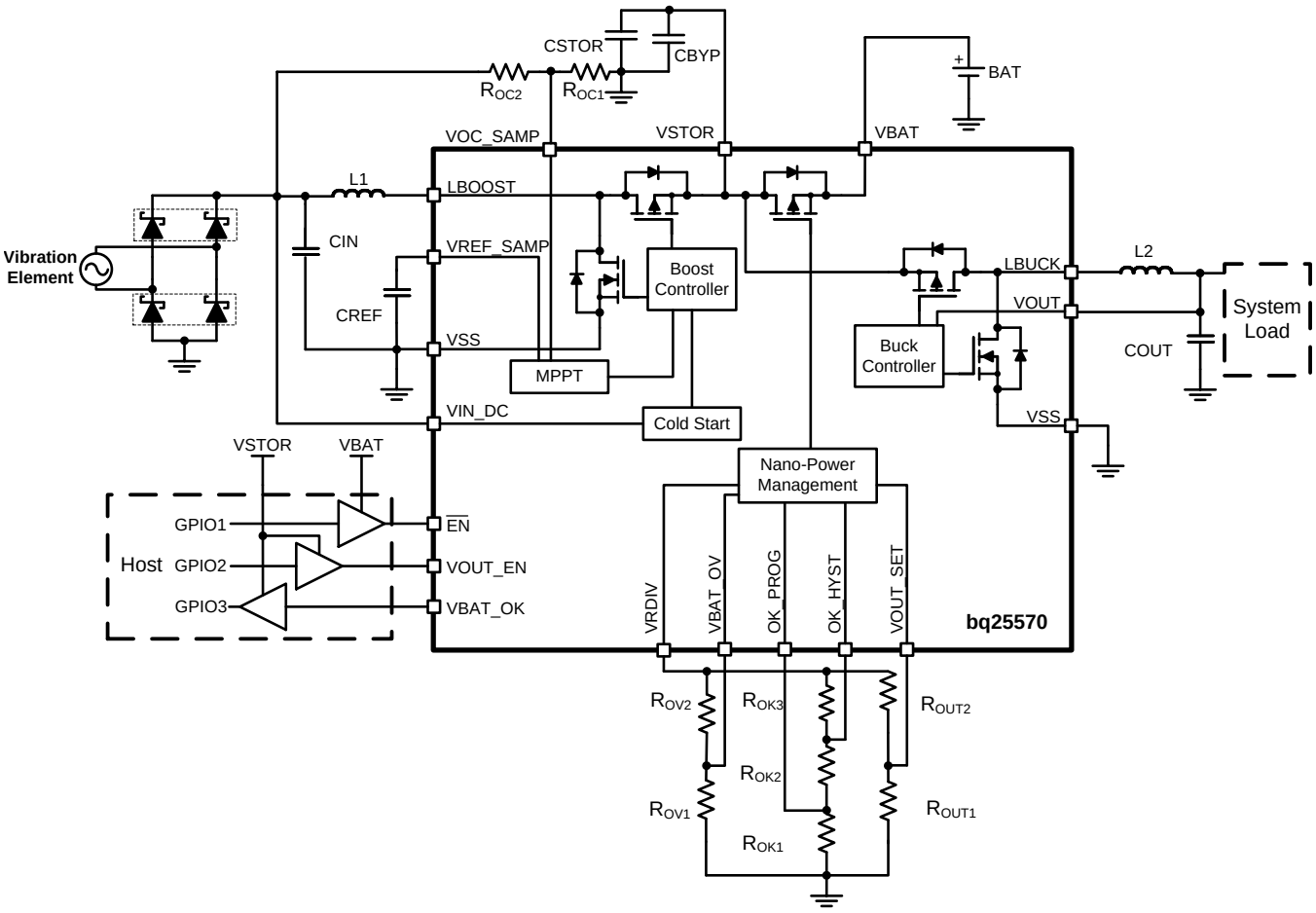


Figure 42. Typical Externally Set MPPT Application Circuit

8.2.3.1 Design Requirements

The desired voltage levels are VBAT_OV = 3.30 V, VBAT_OK = 2.80 V, VBAT_OK_HYST = 3.10 V, and MPP (V_{OC}) = 40% for the selected piezoelectric harvester which provides a rectified V_{OC} = 1 V. A 1.8-V, up to 100-mA power rail is also needed. There are no large load transients expected on either rail.

8.2.3.2 Detailed Design Procedure

The recommended L1 = 22 µH, CBYP = 0.01 µF and low leakage CREF = 10 nF are selected. The rectifier diodes are Panasonic DB3X316F0L. In order to ensure the fastest recovery of the harvester output voltage to the MPPT level following power extraction, the minimum recommended CIN = 4.7 µF is selected. Because no large system load transients are expected and to ensure fast charge time during cold start, the minimum recommended CSTOR = 4.7 µF.

- Keeping in mind that VREF_SAMP stores the MPP voltage for the harvester, first choose $RSUM_{OC} = R_{OC1} + R_{OC2}$ = 20 MΩ then solve Equation 1 for

$$R_{OC1} = \left(\frac{VREF\_SAMP}{VIN\_DC(OC)}\right) \times RSUM_{OC} = \frac{0.14}{1V} \times 20\ M\Omega = 8\ M\Omega \rightarrow 8.06\ M\Omega \text{ closest 1\% resistor, then} \quad (15)$$

- R_{OC2} = $RSUM_{OC}$ x (1 - VREF_SAMP / VIN_DC(OC) = 20 MΩ x (1 - 0.4 V / 1 V) = 12 MΩ → series 10 MΩ and
  2 MΩ easy to obtain 1% resistors.
- Referring back to the procedure in *Detailed Design Procedure* or using using the spreadsheet calculator at

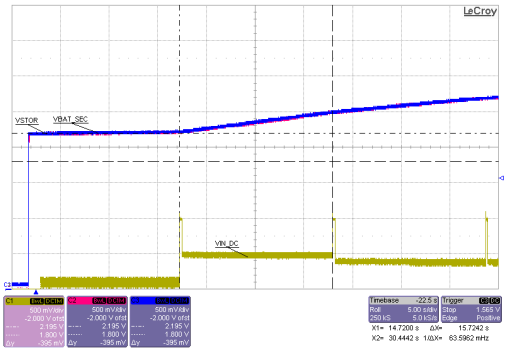
Typical Applications (continued)

SLUC484 gives the following values

– R_{OV1} = 7.15 MΩ, R_{OV2} = 5.90 MΩ resulting in VBAT_OV = 3.31V due to rounding to the nearest 1% resistor.

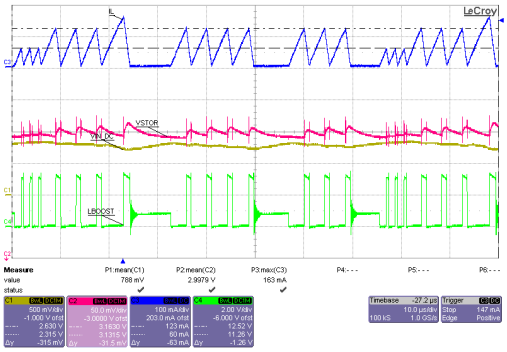
- R_{OK1} = 4.99 MΩ, R_{OK2} = 6.65 MΩ, R_{OK3} = 1.24 MΩ resulting in VBAT_OK = 2.82 V and VBAT_OK_HYST = 3.12 V after rounding to the nearest 1% resistor value.
- R_{OUT1} = 8.66 MΩ and R_{OUT2} = 4.22 MΩ resulting in VOUT = 1.8V.

8.2.3.3 Application Curves



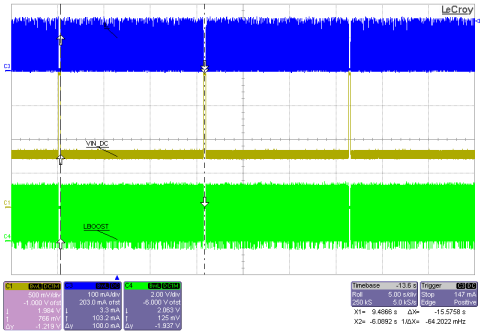
Sourcemeter with V_{SOURCE} = 1.0 V and compliance of 8.5 mA subsequently applied to VIN_DC
VBAT = 0.1 F capacitor charged to 2.2 V
Resistance on VSTOR = 100 kΩ

Figure 43. Startup by Battery Attach With Partially Charged Storage Element



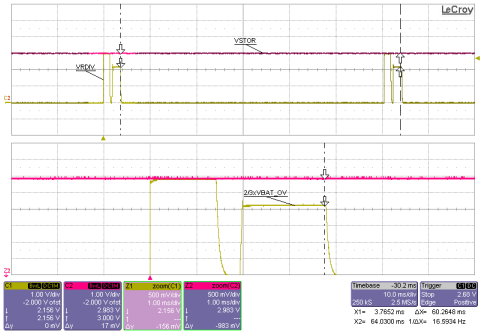
VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA
VBAT = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

Figure 44. Boost Charger Operational Waveforms



VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA
VBAT = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

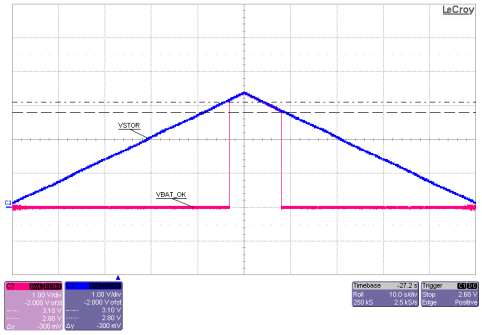
Figure 45. MPPT Operation



VIN_DC = sourcemeter with V_{SOURCE} = 2.0 V and compliance of 43 mA
VBAT = sourcemeter with V_{SOURCE} = 3.0 V and compliance of 1 A

Figure 46. VRDIV Waveform

Typical Applications (continued)



VIN_DC floating
No storage element on VBAT or VBAT_PRI
VSTOR artifically ramped from 0 V to 3.3 V to 0 V using a function generator

Figure 47. VBAT_OK Operation

9 Power Supply Recommendations

See *Energy Harvester Selection* and *Storage Element Selection* for guidance on sizing the energy harvester and storage elements for the system load.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the PCB layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the boost charger and buck converter could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitors as well as the inductors should be placed as close as possible to the IC. For the boost charger, first priority are the output capacitors, including the 0.1uF bypass capacitor (CBYP), followed by CSTOR, which should be placed as close as possible between VSTOR, pin 19, and VSS, pin 1. Next, the input capacitor, CIN, should be placed as close as possible between VIN_DC, pin 2, and VSS, pin 1. Last in priority is the boost charger's inductor, L1, which should be placed close to LBOOST, pin 20, and VIN_DC, pin 2. For the buck converter, the output capacitor COUT should be placed as close as possible between VOUT, pin 14, and VSS, pin 15. The buck converter inductor (L2) should be placed as close as possible beween the switching node LBUCK, pin 16, and VOUT, pin 14. It is best to use vias and bottom traces for connecting the inductors to their respective pins instead of the capacitors.

To minimize noise pickup by the high impedance voltage setting nodes (VBAT_OV, OK_PROG, OK_HYST, VOUT_SET), the external resistors should be placed so that the traces connecting the midpoints of each divider to their respective pins are as short as possible. When laying out the non-power ground return paths (for example, from resistors and CREF), it is recommended to use short traces as well, separated from the power ground traces and connected to VSS pin 15. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. The PowerPAD should not be used as a power ground return path.

The remaining pins are either NC pins, that should be connected to the PowerPAD as shown below, or digital signals with minimal layout restrictions. See the EVM user's guide for an example layout (SLUUAA7).

In order to maximize efficiency at light load, the use of voltage level setting resistors > 1 MΩ is recommended. In addition, the sample and hold circuit output capacitor on VREF_SAMP must hold the voltage for 16s. During board assembly, contaminants such as solder flux and even some board cleaning agents can leave residue that may form parasitic resistors across the physical resistors/capacitors and/or from one end of a resistor/capacitor to ground, especially in humid, fast airflow environments. This can result in the voltage regulation and threshold levels changing significantly from those expected per the installed components. Therefore, it is highly recommended that no ground planes be poured near the voltage setting resistors or the sample and hold capacitor. In addition, the boards must be carefully cleaned, possibly rotated at least once during cleaning, and then rinsed with de-ionized water until the ionic contamination of that water is well above 50 MOhm. If this is not feasible, then it is recommended that the sum of the voltage setting resistors be reduced to at least 5X below the measured ionic contamination.

10.2 Layout Example

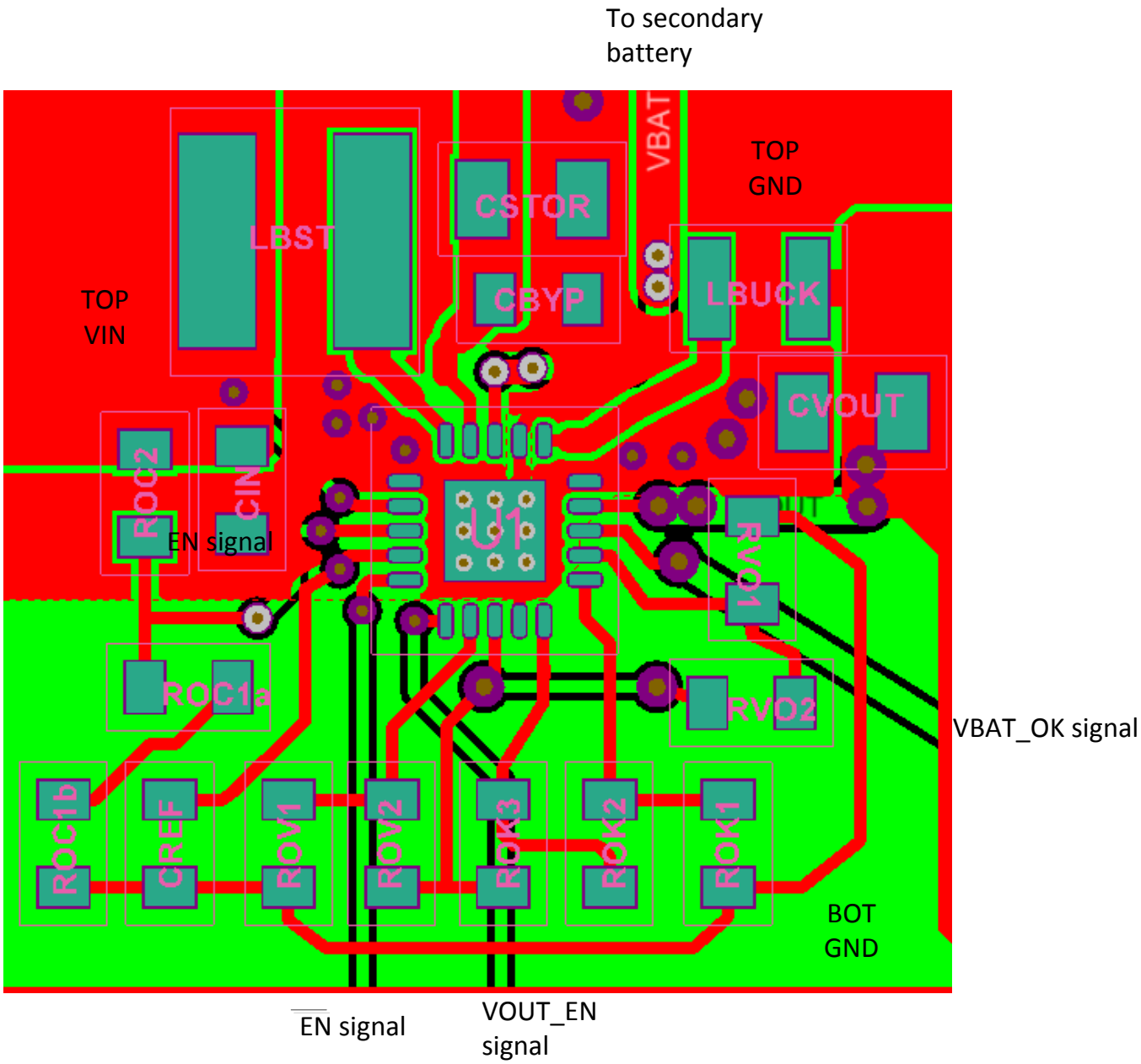


Figure 48. Layout Schematic

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power-dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

For more details on how to use the thermal parameters in the Thermal Table, check the *Thermal Characteristics Application Note* (SZZA017) and the *IC Package Thermal Metrics Application Note* (SPRA953).

11 器件和文档支持

11.1 器件支持

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11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- *EVM 用户指南*，SLUUAA7
- *《热工特性应用手册》*，SZZA017
- *《IC 封装热指标应用手册》*，SPRA953

11.3 接收文档更新通知

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这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25570RGRR	ACTIVE	VQFN	RGR	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQ570	Samples
BQ25570RGRT	ACTIVE	VQFN	RGR	20	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQ570	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

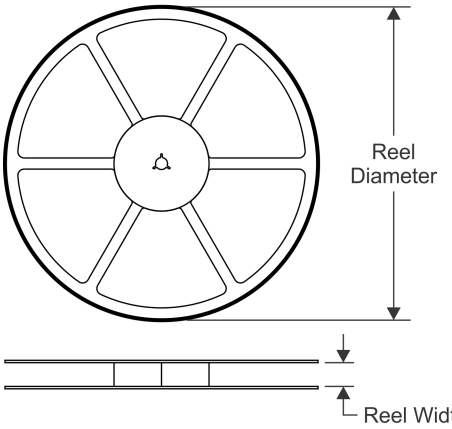
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

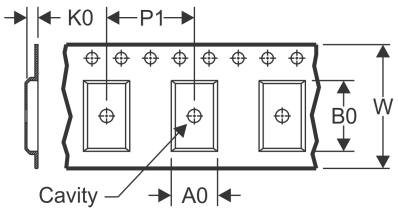
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

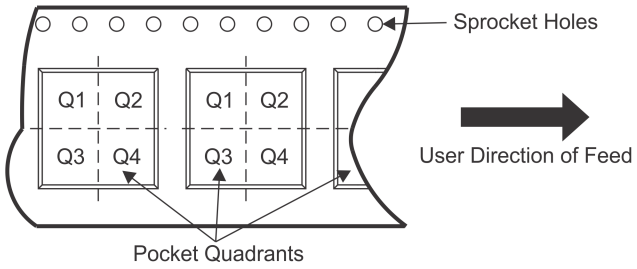


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

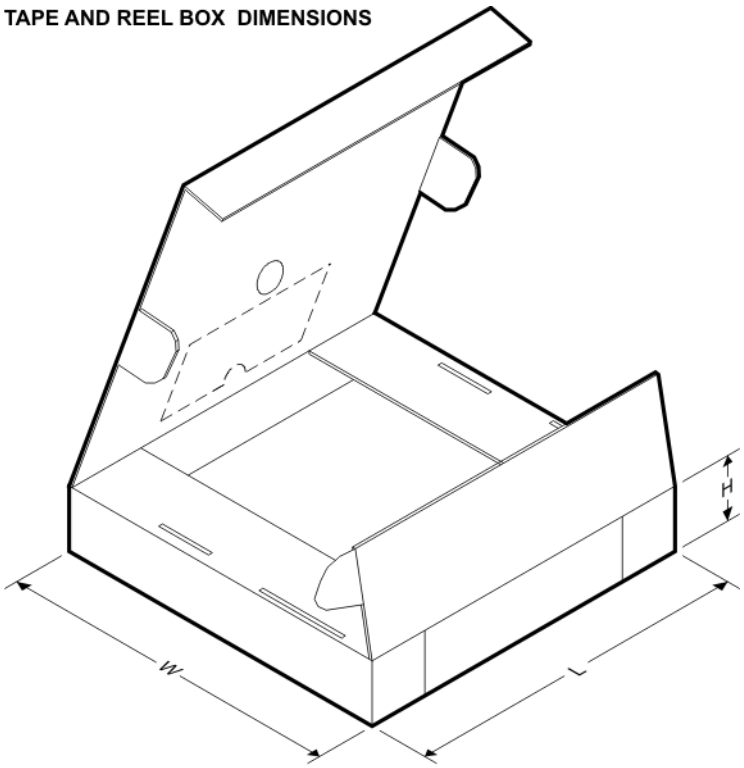
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25570RGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
BQ25570RGRT	VQFN	RGR	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2

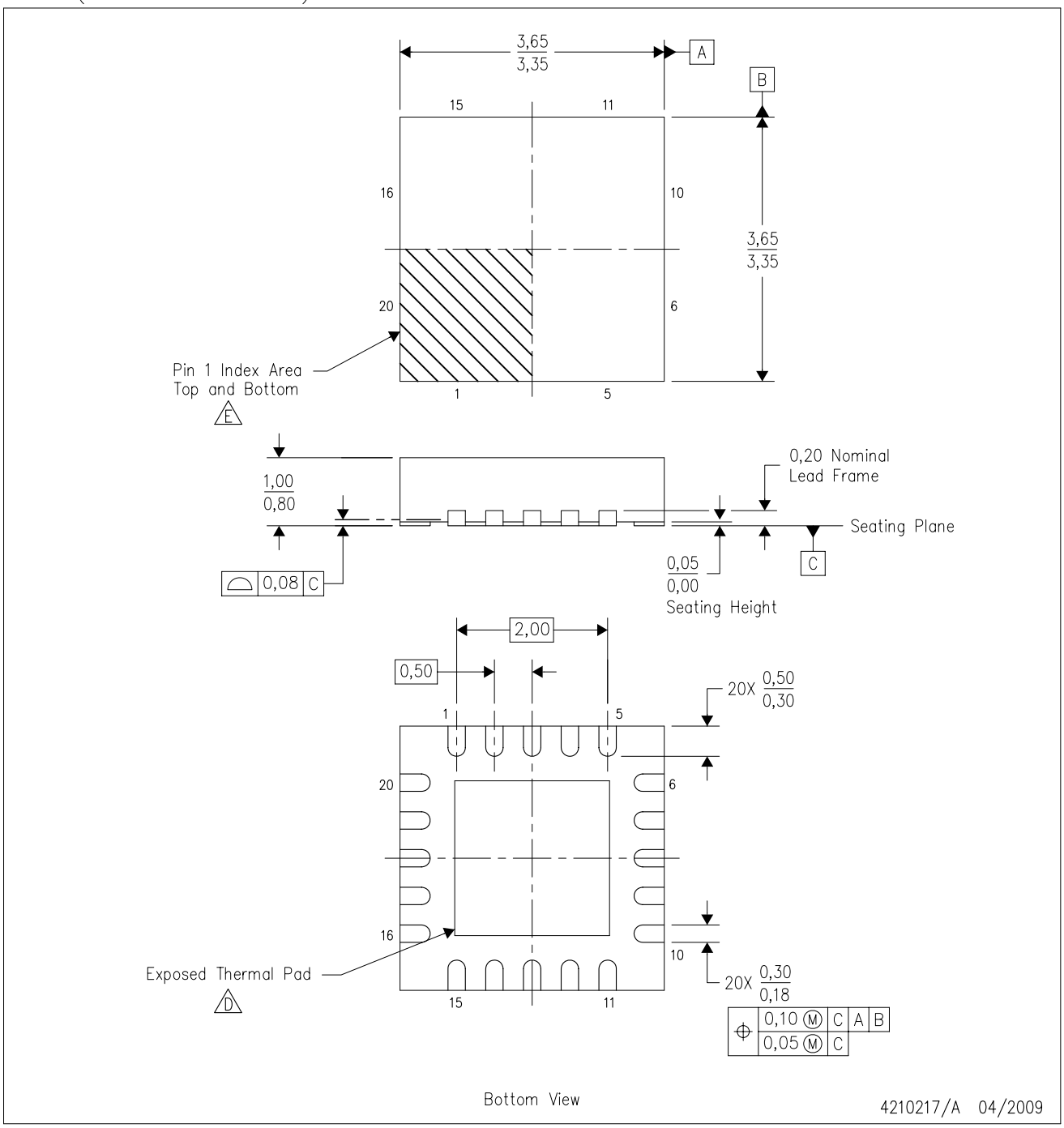
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25570RGRR	VQFN	RGR	20	3000	367.0	367.0	35.0
BQ25570RGRT	VQFN	RGR	20	250	210.0	185.0	35.0

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

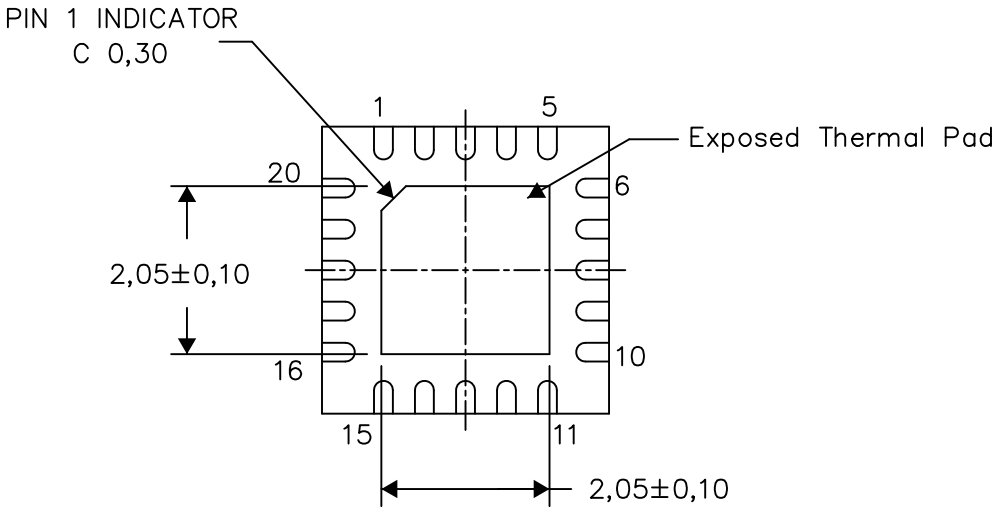
RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



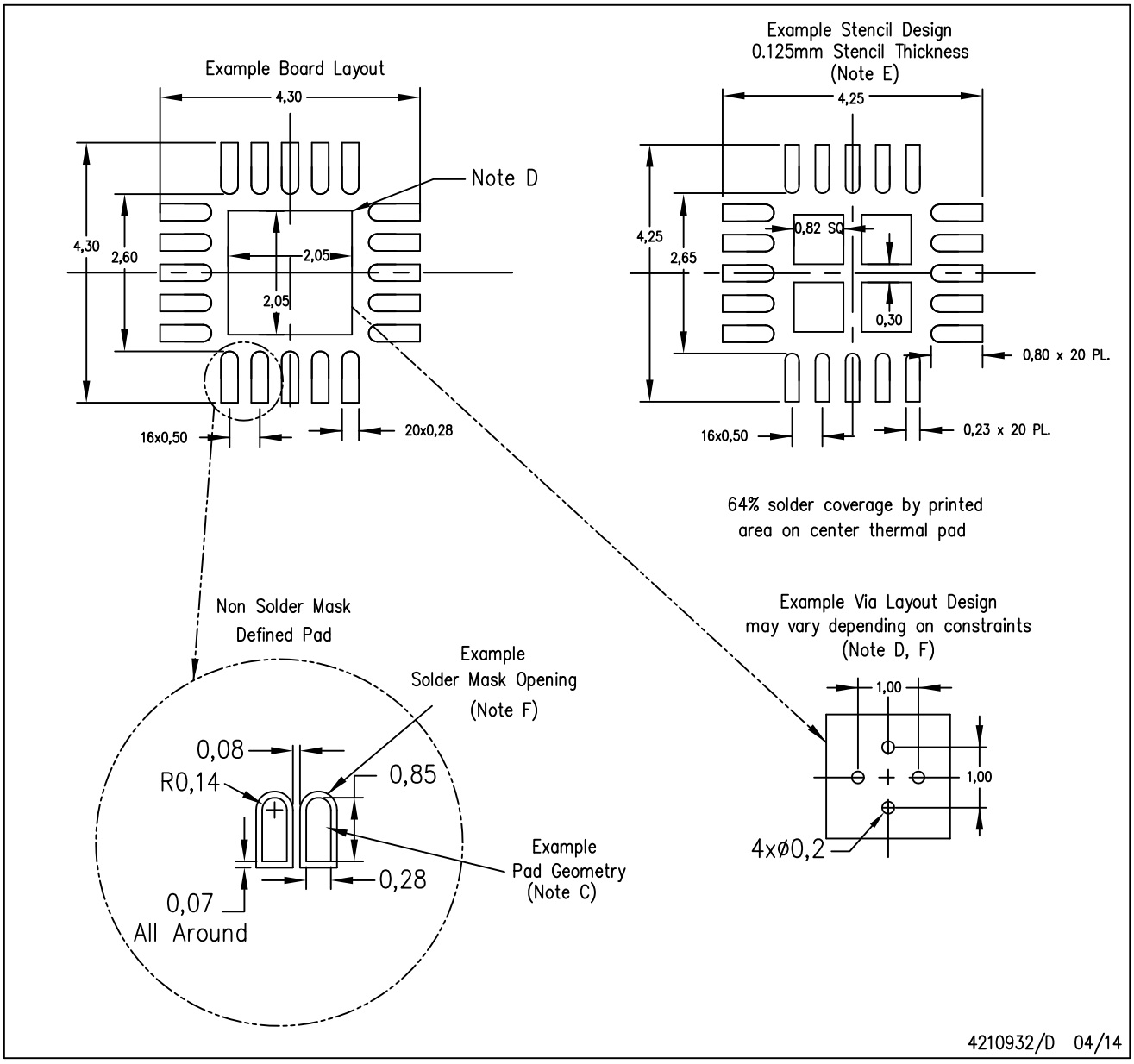
Bottom View

Exposed Thermal Pad Dimensions

4210218/E 04/14

NOTE: All linear dimensions are in millimeters

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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