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Intelligent System State Restoration After Power Failure With Compute Through Power Loss Utility

TEXAS INSTRUMENTS

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TI Designs provide the foundation that you need including methodology, testing, and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDM-FRAM-CTPL	Design Folder
MSP-EXP430FR6989	Tool Folder
MSP-FRAM-UTILITIES	Software Page
MSP430FR6989	Product Folder

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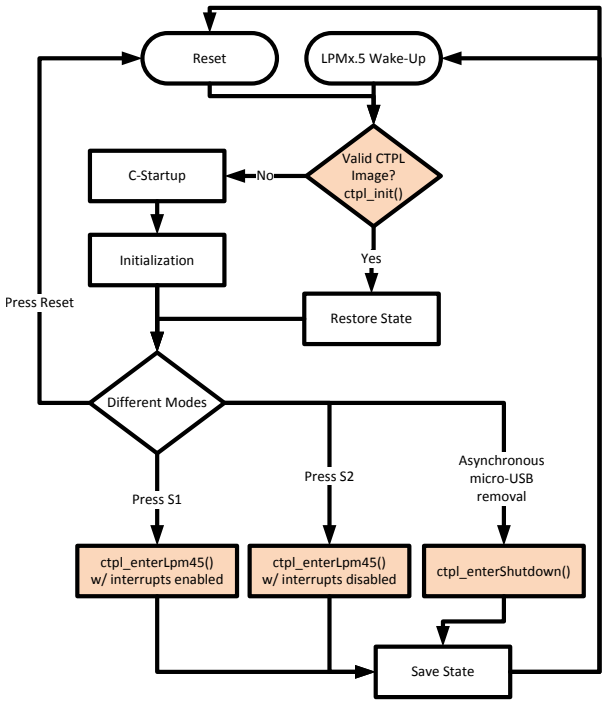
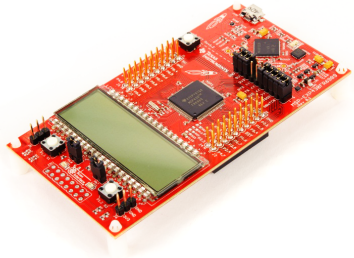
Design Features

- Uses Compute Through Power Loss (CTPL) Software Utility
- Offers Complete Shutdown With Software-State Retention Through VCC Monitoring
- Offers Ease-of-Use With Low-Power Modes (LPMx.5)
- Supports Energy Harvesting Applications

Featured Applications

- Home and Building Automation
- Portable Health and Fitness Products
- Smart Metering





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1 System Description

Compute Through Power Loss (CTPL) is a software-utility library for Ultra-Low-Power MSP430FRxx FRAM microcontrollers. The CPTL enables an application to easily save the CPU and peripheral states into nonvolatile FRAM before powering down or entering a deep-sleep mode like LPMx.5. When a CPU wakes up, the CTPL restores an application exactly where it last executed with context-save and restore. This TI design showcases the ease of integrating this utility library in an application. Bypassing the sometimes cycle intensive start-up routine, the CTPL enables a faster wake-up time from a cold start.

2 Block Diagram

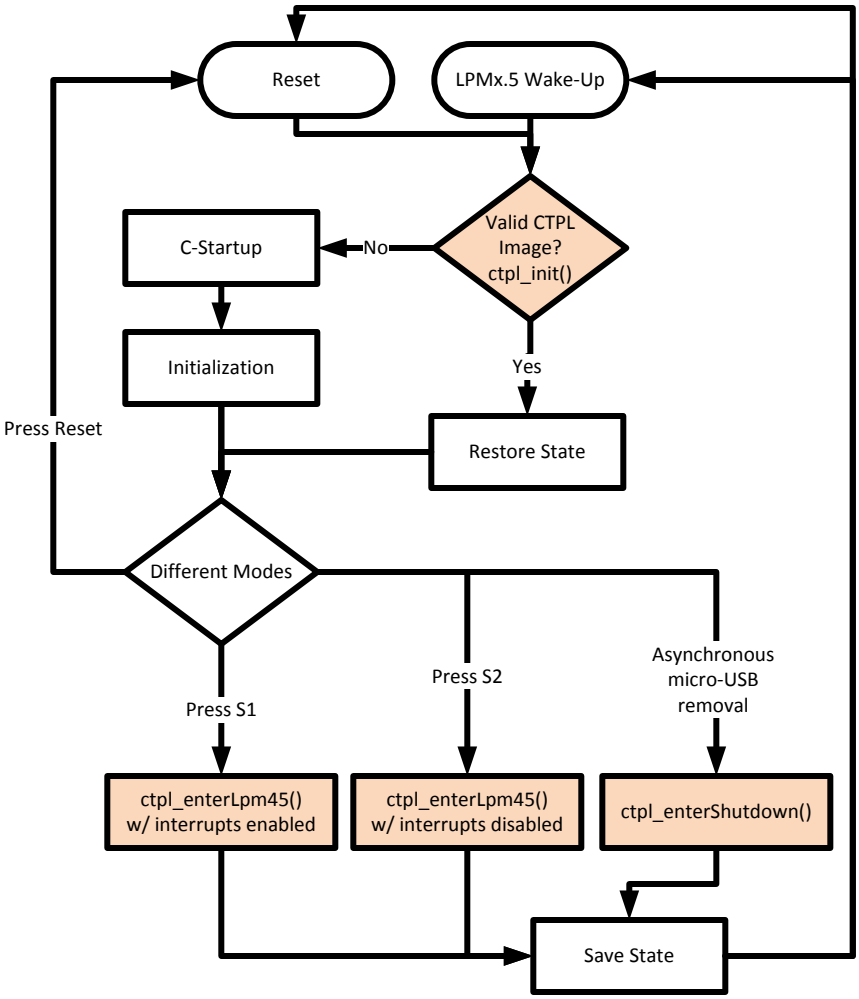

Figure 1. Block Diagram

3 System Design Theory

The CTPL saves the state of a microcontroller by storing the stack from RAM, key peripherals, and CPU states to Ferroelectric Random Access Memory (FRAM). Upon wakeup from low-power mode or a complete power-cycle, the CTPL checks for a signature in FRAM to determine if an application should execute the C start-up routine (part of the compiler C runtime library that runs before entering the application main() function) or return where the application left off. From a valid signature, the CTPL library restores the state of the CPU, key peripherals, and stack. The CPTL emulates the ease of use of a low-power mode LPM0-LPM3 function call.

Using CPTL to skip the C start-up routine, the application restarts quicker from a cold start. The CPTL can help avoid C start-up routine reinitialization and save significant energy for applications and large arrays.

In an MSP application, waking up from deep-sleep mode requires the software to restart. The application and its peripherals then need to reinitialize. The CTPL uses LPMx.5 to simplify the process of entering and exiting low-power mode and restoring the application.

NOTE: Only RTC, external interrupts, and/or a device reset can wake up the device from low-power mode 3.5.

To learn more about CTPL, see the FRAM Utilities for MSP Microcontrollers software page.

3.1 FRAM Technology

To save its states periodically during a power-down process or upon entering a low-power mode, an application requires a nonvolatile memory technology that offers extremely high endurance. With 10^{15} write cycles, FRAM stores and restores the state of an application without stressing or wearing out. Existing flash technology is typically limited to from 10,000 to 100,000 write cycles.

3.2 Simplifying the Use of LPM x.5 With MSP Microcontrollers

When the MSP microcontroller wakes up from LPMx.5, the following occurs:

1. The device resets.
2. The MSP application restarts while maintaining only the GPIO and RTC volatile content and peripheral states.
3. The application identifies whether the microcontroller is waking up from low-power mode or if it is waking up from a cold start.
4. The application reinitializes the peripherals of the MSP.
5. The application restores the GPIO state of the MSP.

These steps are also outlined in the *Enter LPMx.5 and Exit* and *Wake-Up from LPM3.5* sections of *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* (SLAU367).

By abstracting all checks and setups, the CTPL enables the MSP to do the following:

- Enter LPMx.5.
- Exit LPMx.5.
- Restore an application from LPMx.5.

The CPTL and FRAM simplify the process for an application to use low-power mode on MSP microcontrollers.

For a list of MSP430FRxx MCUs that have CTPL compatibility, see the FRAM Utilities for MSP Microcontrollers software page.

4 Hardware

For this design, you will need the following:

- The MSP-EXP430FR6989 LaunchPad

For information on LaunchPad, see the MSP-EXP430FR6989 LaunchPad Development Kit product folder. This folder contains the hardware schematics and other design resources.

4.1 Hardware Features

For information on applications that run on the MSP-EXP430FR6989, see Figure 2.

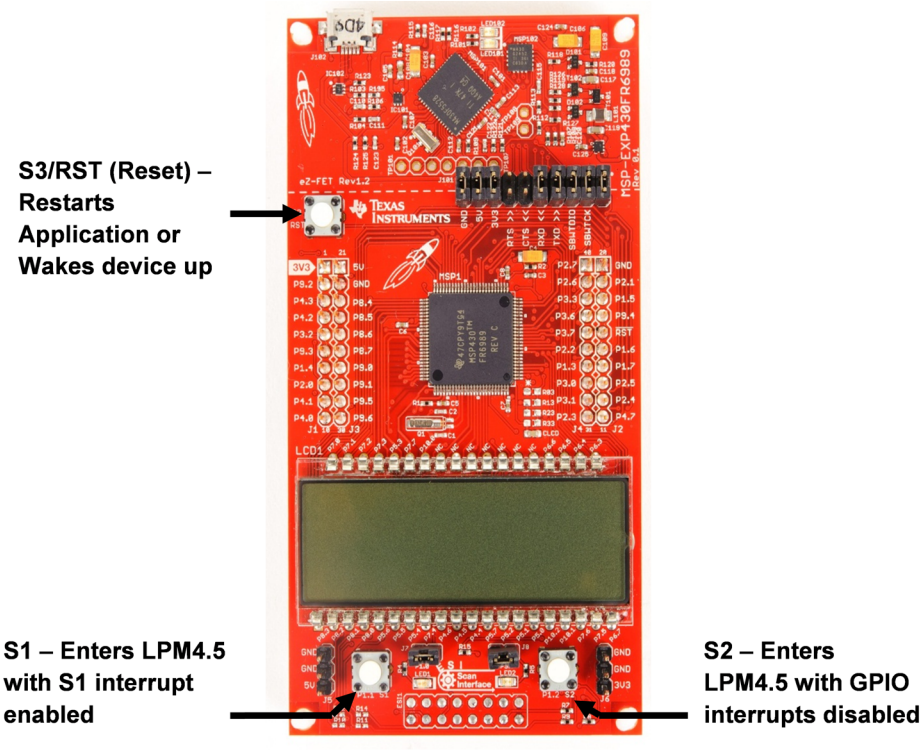

Figure 2. Application Functionality on MSP-EXP430FR6989

5 Software

For the software in this design, see TIDM-FRAM-CTPL.

This project requires Code Composer Studio™ v6.1 (or newer) or IAR Embedded Workbench v6.30 (or newer). For download and debug information, see Section 5.3.

5.1 Software Demonstration Description

After starting up from reset, the software application for CPTL displays a counter on the 6 alpha-numeric segment LCD and counts up every 500 ms.

The application offers the following four operating modes:

- Mode 1: Pressing S3/RST (reset) restarts the application by performing a cold start and counting up from zero (0). The application executes the C start-up routine because it lacks valid CTPL image.
- Mode 2: Pressing S1 enters LPM4.5 with S1 interrupts enabled to wake the device again. Upon wakeup, the counter does not start from zero (0) because CTPL resumes the application, bypassing the C start-up routine.
- Mode 3: Pressing S2 enters LPM4.5 with all GPIO interrupts disabled which emulates a CTPL shutdown with the lowest power state. Then, press S3/RST to wakeup. Realize that the counter does not start from zero (0) because CTPL resumes the application and bypasses the C start-up routine.
- Mode 4: Asynchronously removing Micro-USB power automatically enters CTPL shutdown when VCC reaches a level of below 2.6 V. Reapplying Micro-USB power will resume the application with a counter value that does not start from zero (0).

5.2 Monitoring VCC Voltage for Power Loss

Applications that must safely shut down and/or signal when VCC drops below a certain minimum operating threshold voltage must monitor VCC for a low-voltage condition or complete power loss. Choose the voltage threshold and power supply circuit (for example, onboard storage capacitors) based on the system requirements that provide a fair amount of leftover energy to safely shutdown.

The CPTL uses the ADC12_B built-in VCC measurement capability and window comparator mode of the MSP430FR6989 microcontroller to indicate to the application when there is a loss of power when VCC reaches 2.6 V. The CPTL samples the VCC at 1 kHz.

Aside from ADC12_B, you could also use the built-in Comparator_E peripheral module and employ an external resistor-based voltage divider to provide a reference voltage point for the comparator to trigger.

Figure 3 shows the VCC voltage drop when the Micro-USB of the LaunchPad™ is disconnected and ctpl_enterShutdown() is executed. Figure 3 shows that the device executes the shutdown routine when the VCC reaches 2.6 V. Figure 4 also shows the execution time of ctpl_enterShutdown() at a CPU operating frequency of 1 MHz or approximately 1.12 ms.

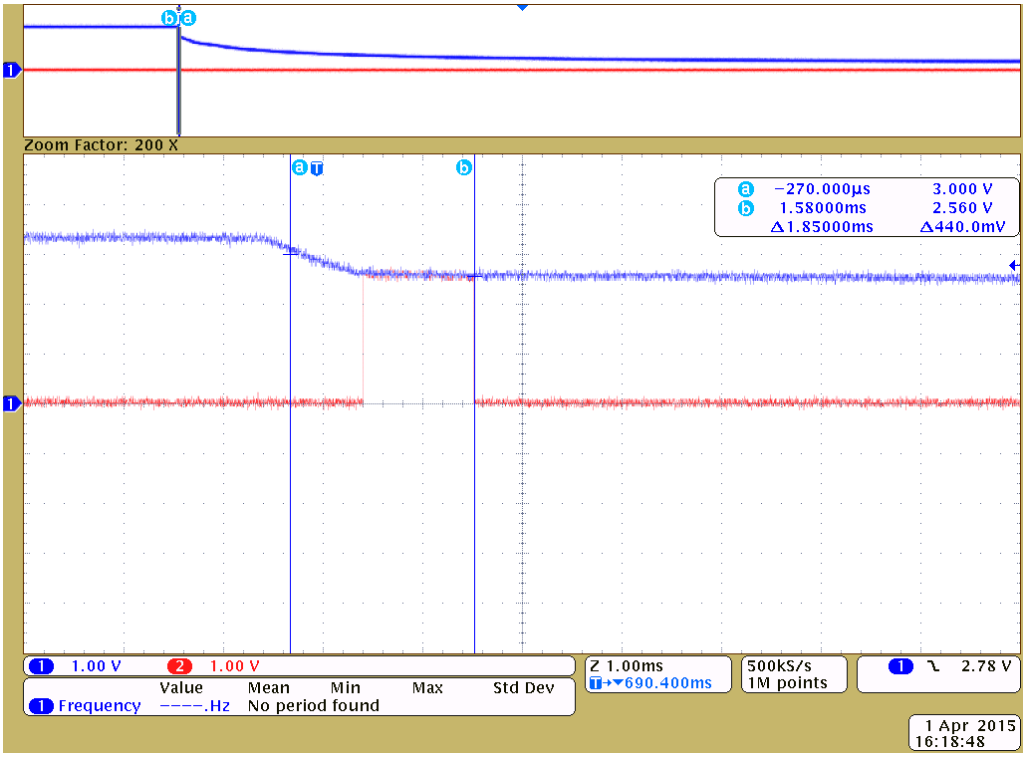

Figure 3. VCC Drop When Micro-USB is Disconnected

Figure 4 illustrates that the application enters shutdown mode (LPM4.5) at approximately 2.56 V; a significant margin before the device enters brownout reset (approximately 1.8 V). For more information, see *MSP430FR698x(1), MSP430FR598x(1) Mixed-Signal Microcontrollers* (SLAS789).

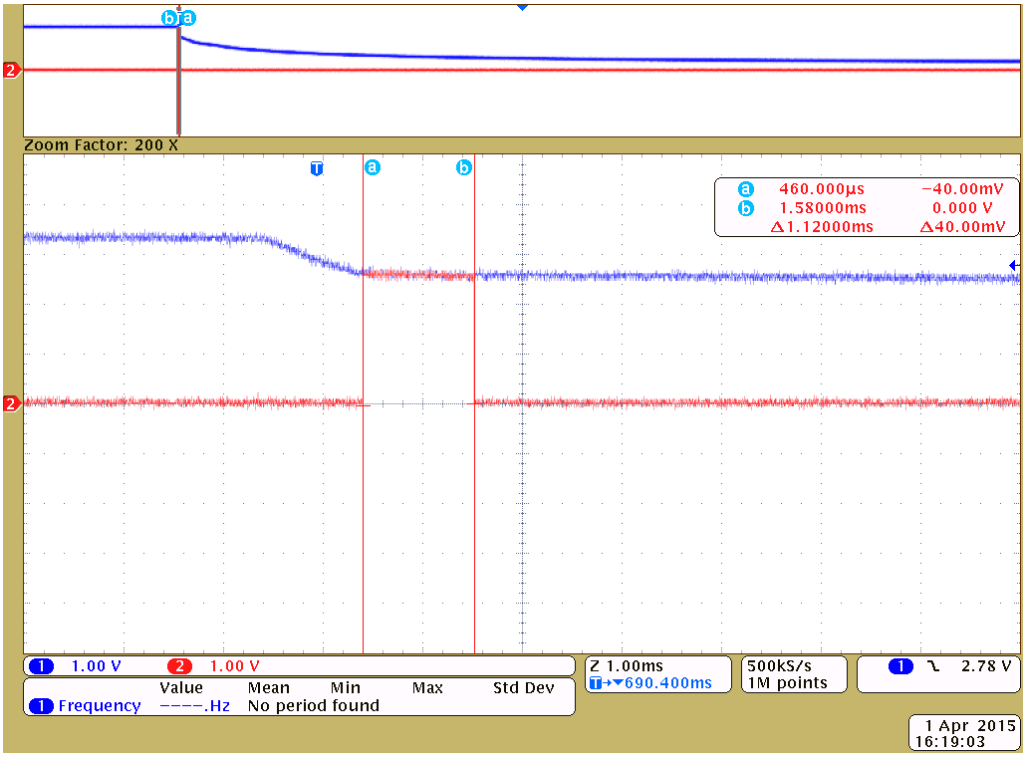

Figure 4. Ctpl_enterShutdown() Execution Time at 1 MHz

Figure 5 shows a graph of the voltage profile of an application on a powerup, a voltage-dip, and a powerdown. When a voltage-dip occurs during the application that crosses the 2.6-V VCC detection threshold, the application then starts the ctpl_shutdown() with a watchdog timer that has a 64-ms time-out. Because the ADC is disabled to monitor the VCC, TI designed the watchdog time-out to restart the application where it last executed if the VCC recovers its voltage. If a power loss occurs, the application detects the voltage drop and again triggers the watchdog time-out. Because the voltage continues to drop below the SVS threshold, the device resets and its functions are disabled.

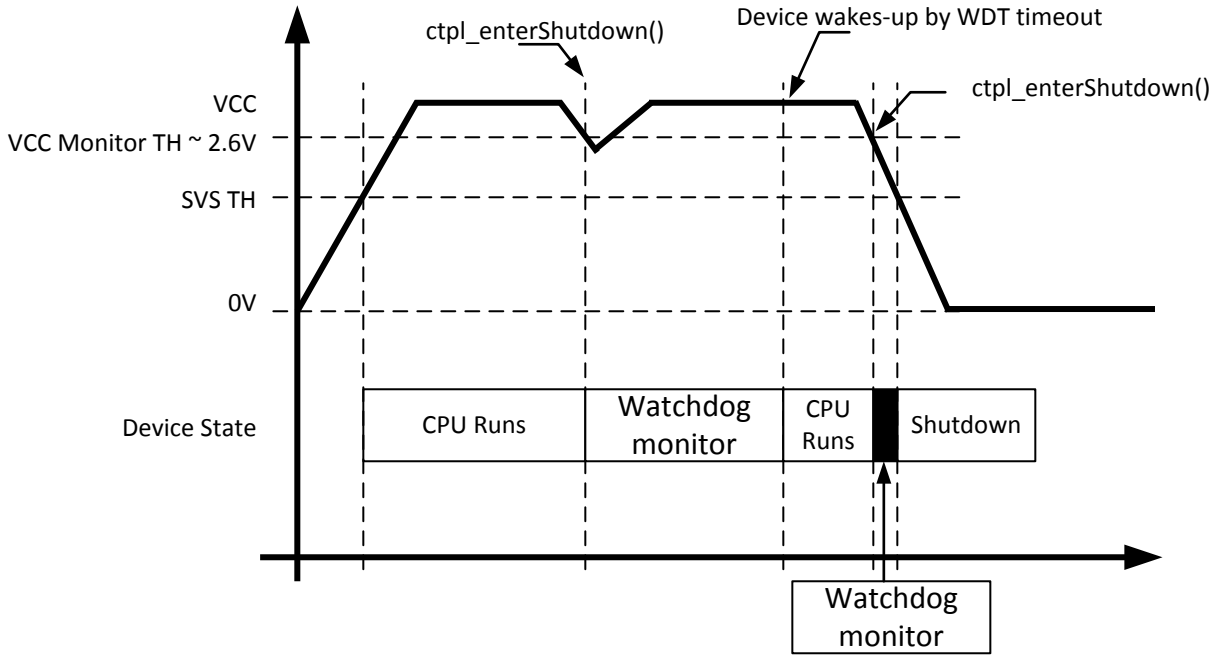

Figure 5. Power-Up and Down Conditions

You could also use an external ultra-low-power SVS device from the TI Supervisor Portfolio and connect the SVS output to an interruptible GPIO pin (not the reset pin) on the MSP430™. This SVS output would trigger a ctpl_enterLpm45() (with GPIO interrupts enabled) and wake up. When selecting the SVS, ensure the device has the right threshold voltage when it enters low-power mode or wake up. Design the system to ensure that it has enough energy to execute the CTPL utility. Using an ultra-low-power SVS device to sample VCC eliminates the need for an ADC or comparator. Depending on the profile of application-specific device activity, using an external ultralow power SVS can also save significant power compared to using the internal ADC12_B (in polling mode) or Comparator_E modules. This system might benefit certain energy harvesting applications.

The following list presents examples of TI SVS devices with various fixed threshold voltages and push-pull output drivers:

- TPS3839L30
- TPS3836H30
- TPS3836J25

5.3 Download and Debug

5.3.1 Code Composer Studio (CCS)

To use Code Composer Studio with this design, do the following:

1. Launch CCS.
2. Go to Project.
3. Go to Import CCS Project.
4. Click Browse.
5. Navigate to c:\ti\msp430\TIDM-FRAM-CTPL_xx_xx_xx_xx\CCS\ (see Figure 6).

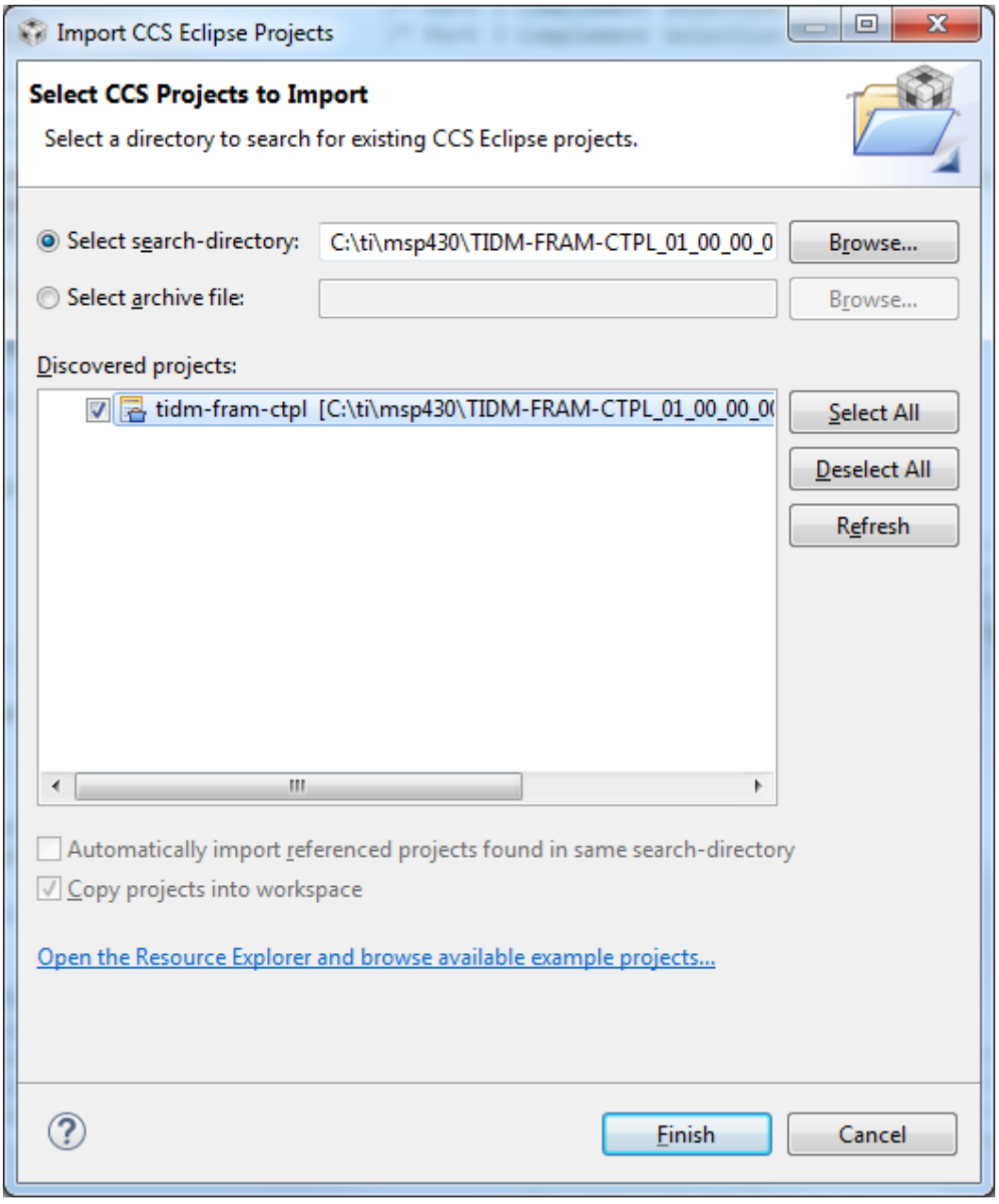

Figure 6. CCS Import Project

6. Build the project by clicking this hammer icon. 
7. Download and debug the application by clicking this bug icon. 

5.3.2 IAR Embedded Workbench

To use IAR Embedded Workbench with this design, do the following:

1. Launch IAR.
2. Click File.
3. Click Open.
4. Click Workspace.
5. Select c:\ti\msp430\TIDM-FRAM-CTPL_xx_xx_xx_xx\IAR\tidm-fram-ctpl.eww.
6. Click this icon to build and download the project. 

5.4 Functional Verification and Performance

EnergyTrace++™ software verified and debugged the functionality of the application states. This tool helped determine if the application entered the low-power-modes or if higher powered peripherals are enabled when needed. Only MSP430FR58x, MSP430FR59x, MSP430FR68x, and MSP430FR69x devices support EnergyTrace++ technology. For screen shots of the software captured over 10 seconds, see Figure 7, Figure 8, and Figure 9.

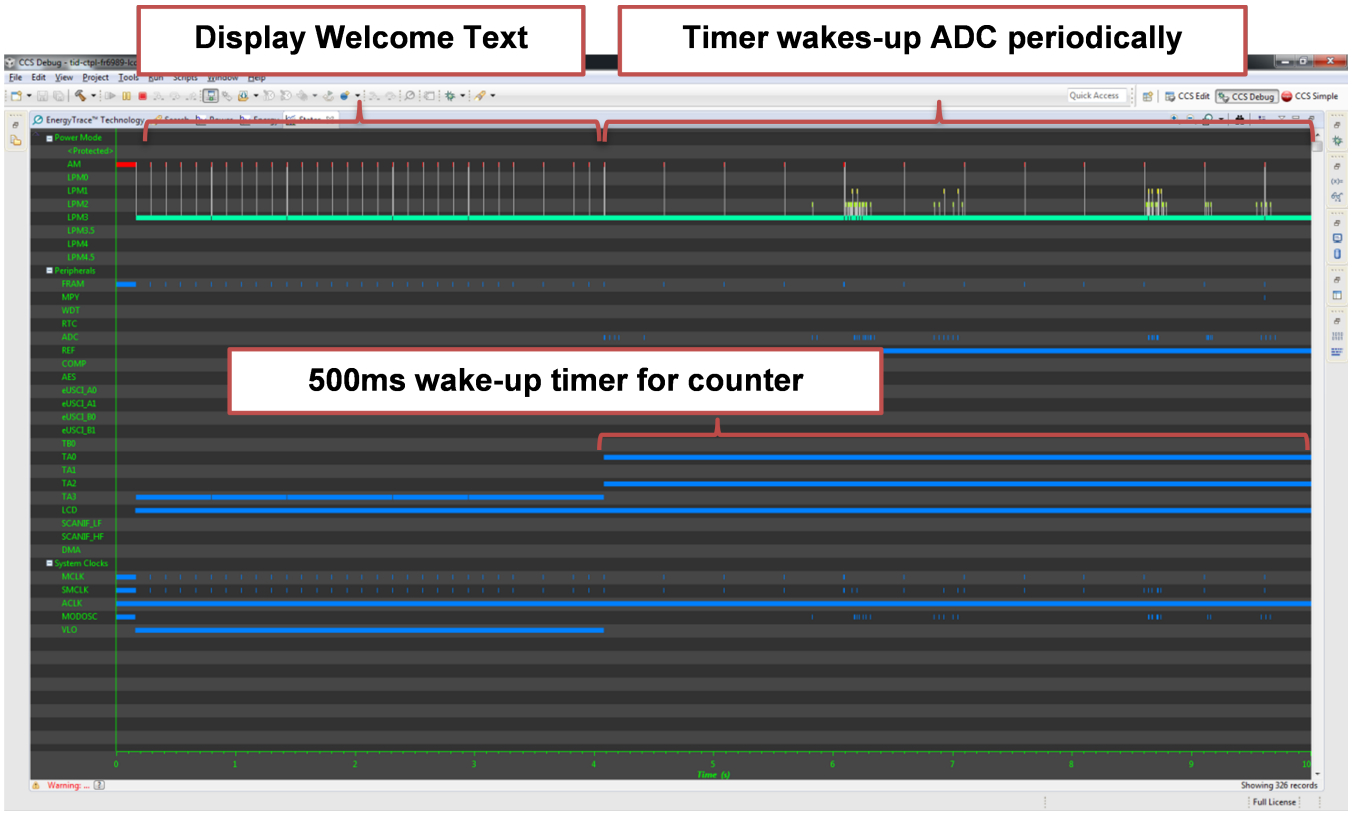

Figure 7. EnergyTrace++ Capture on Reset

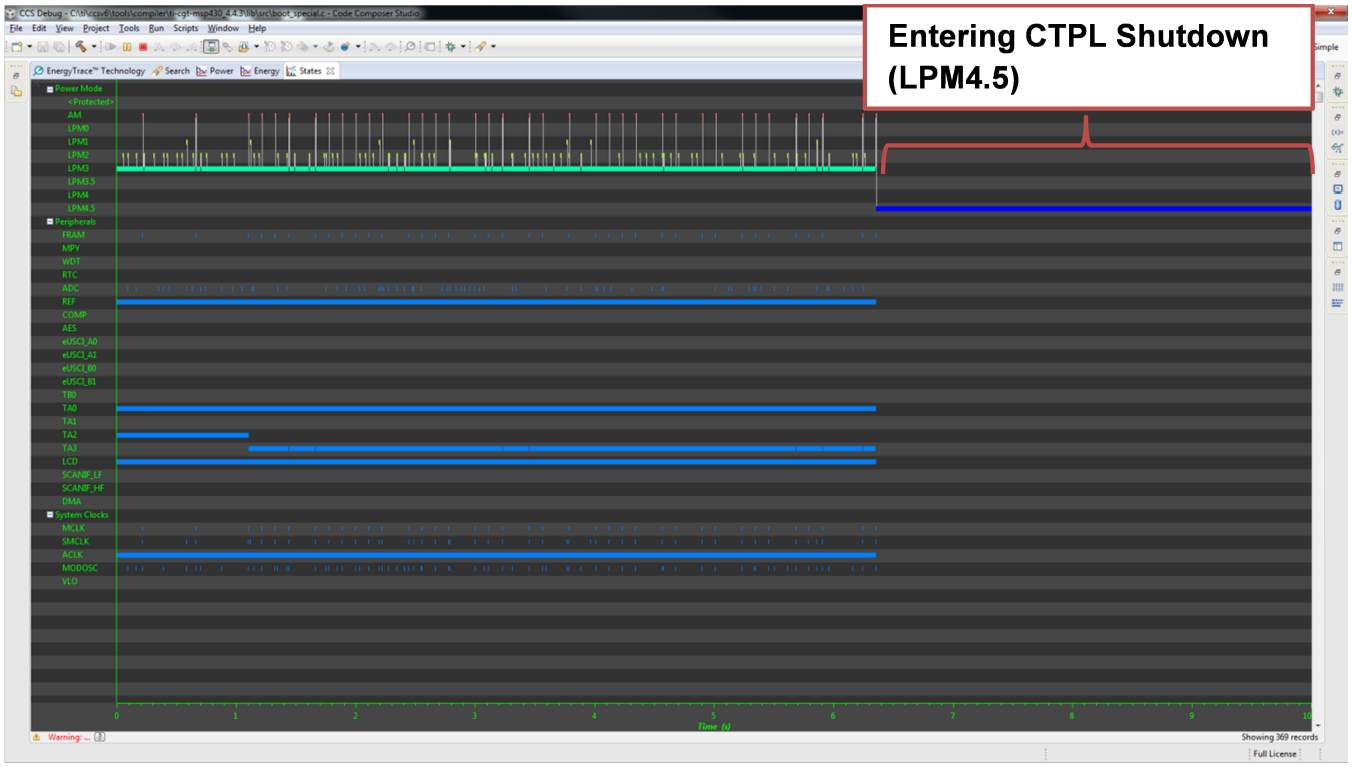

Figure 8. EnergyTrace++ Technology Capture of Application Entering CTPL Shutdown

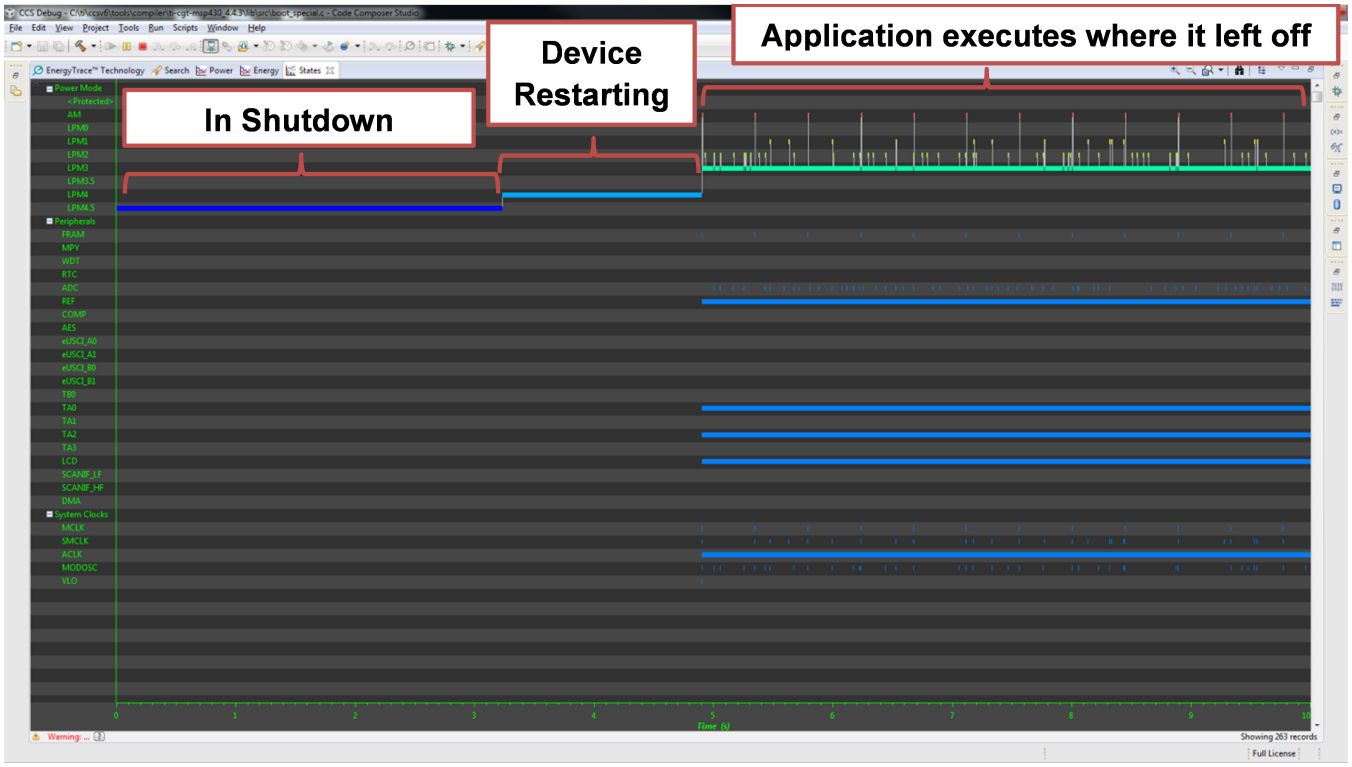

Figure 9. EnergyTrace++ Capture of Application Waking Up From CTPL Shutdown

5.5 Current Profile

See Figure 10, for a current profile of the CPTL:

- Executing in LPM3
- Running ADC and LCD
- Entering ctpl_enterLpm45()
- Running with all GPIO interrupts disabled
- Running with SVS enabled

When all the GPIOs are configured to the lowest-power state, the LPM4.5 current with SVS enabled should be approximately 200 nA.

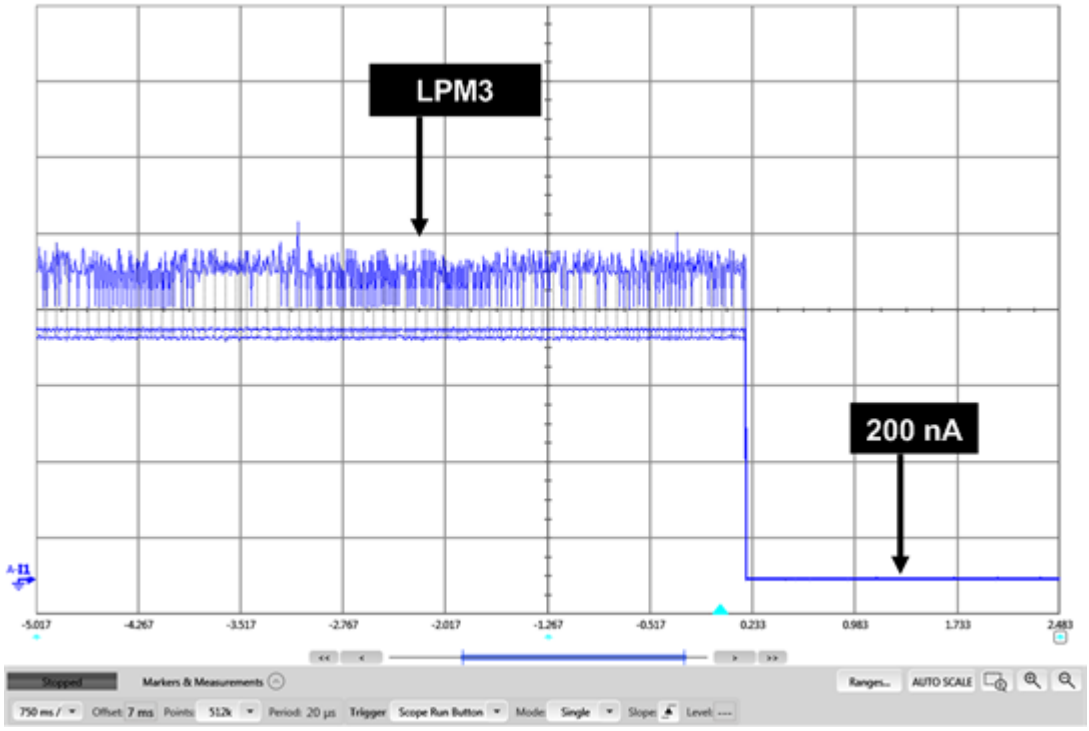

Figure 10. CTPL Enters Shutdown or LPM4.5 with Interrupts Disabled

For the current profile of a device waking up from LPM4.5 as it reinitializes the ADC, timers, and LCD before it returns to the application where it last executed while bypassing the C start-up routine, see Figure 11.

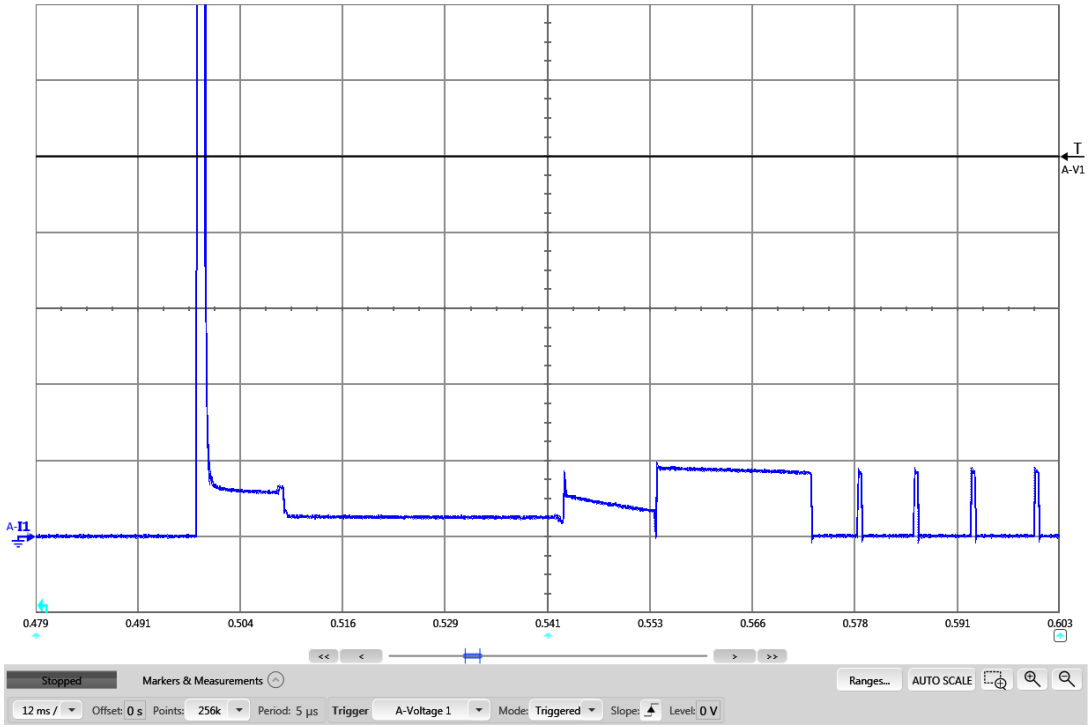

Figure 11. Wake-Up from CTPL Shutdown

6 References

1. MSP-FRAM-Utilities Software Page
2. *MSP430FR698x(1), MSP430FR598x(1) Mixed-Signal Microcontrollers* (SLAS789)
3. *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* (SLAU367)

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