Test Report: PMP30548

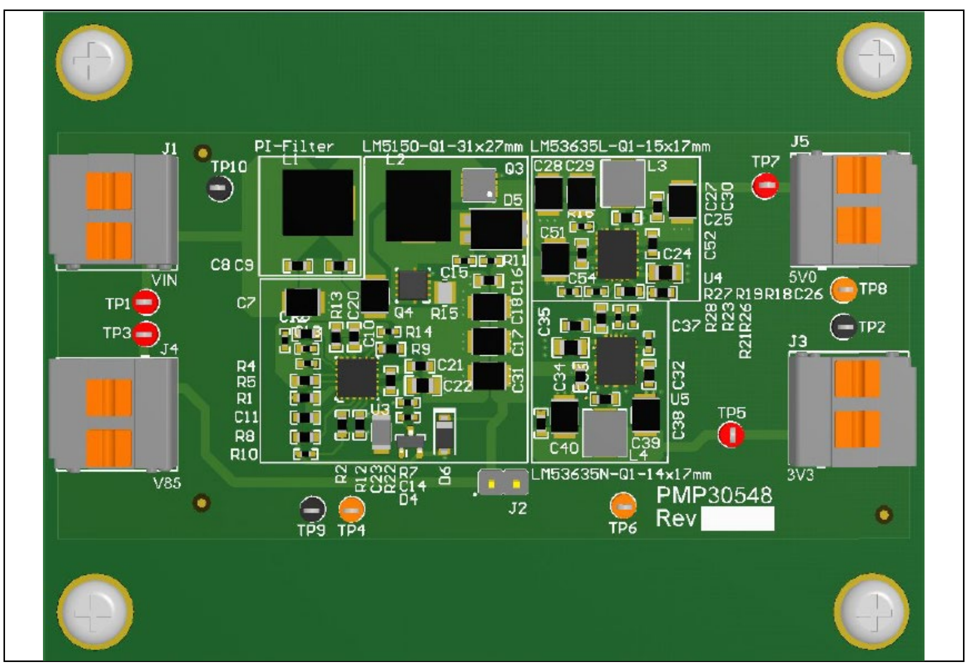
Small automotive front-end 16-W power reference design

Description

This reference design provides a non-isolated automotive power supply that can be directly connected to the battery. This simple solution uses a pre-boost stage to withstand cold cranking pulses and two downstream buck converters that provide a total output power of 16 W.
It offers a small footprint of less than 46 mm x 32 mm including input filter, pre-boost controller and two buck converters. No electrolytic capacitors are used thereby also offering a low profile solution.

Features

- Small Footprint Solution of 46 mm x 32 mm
- Designed to handle cold cranking operation at 3.2 V
- Wide-Vin buck supply to handle jump start operation of 40 V
- EMI friendly solution
- Output Power contains 5 V @ 1.6 A and 3.3 V @ 2.3 A
- Total Efficiency of up to 88 %
- AEC-Q100 Qualified



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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Ranges	3.2 V (min), 13.5 V (typ), 40 V (max)
Output Power LM5150-Q1	**8.5 V @ 2 A (2.5 A)**
Switching Frequency LM5150-Q1	2.1 MHz
Output Power LM53635L-Q1	**5 V @ 1.6 A**
Switching Frequency LM53635L-Q1	2.1 MHz
Output Power LM53635N-Q1	**3.3 V @ 2.3 A**
Switching Frequency LM53635L-Q1	2.1 MHz

1.2 Required Equipment*

- Power Supply: EA-PS-3032-10B
- Ohmic Load
- Frequency Response Analyzer: Venable Model 3120
- Digital Voltmeter
- Cold Crank Generator (HVL068A)

1.3 Considerations*

- Switching Frequency of all three power rails of 2.1 MHz
- Unless otherwise specified the measurements were performed at full load at all outputs
- The reference design has been tested at 3.2 V / 6 V / 13.5 V and 40 V

2 Testing and Results

2.1 Efficiency Graphs

The efficiency graphs are shown in Figure 1and Figure 2.

Figure 1 shows the efficiency dependent on the output current of the primary buck 3V3 with fixed load current on the primary buck 5V0.

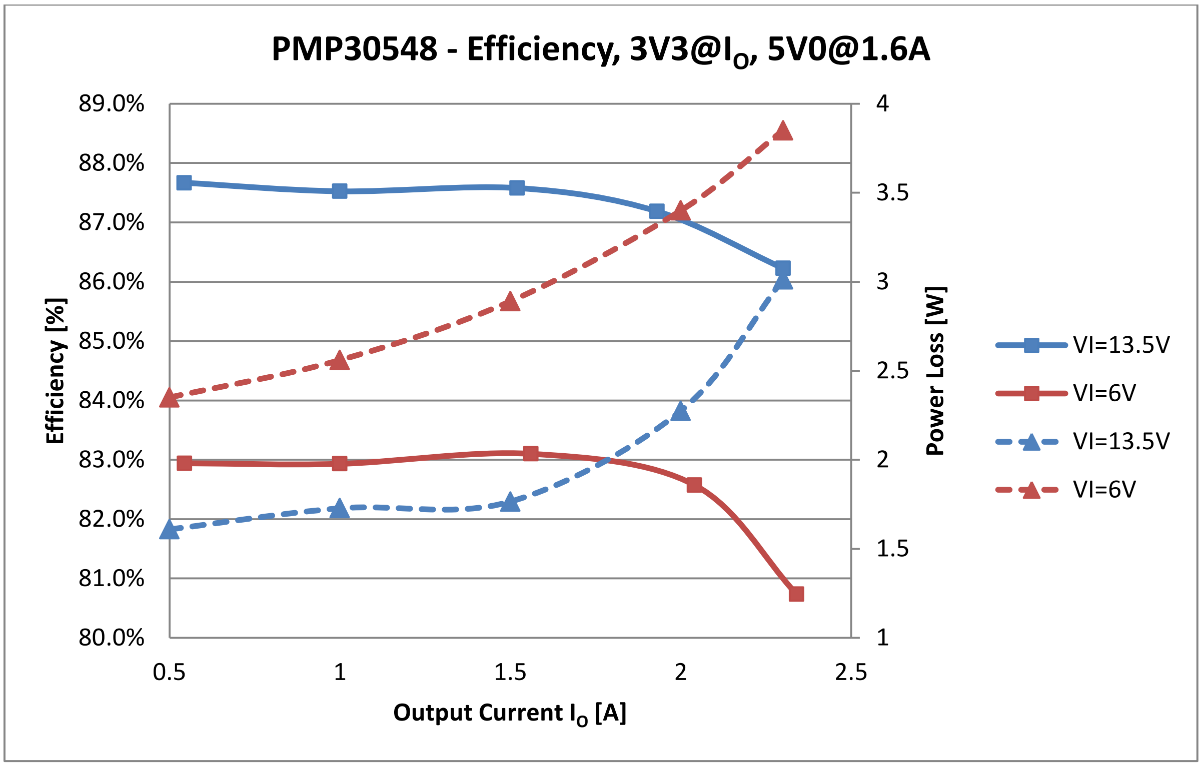

Figure 1: Efficiency Graph with variable load on 3V3 rail

Figure 2 shows the efficiency dependent on the output current of the primary buck 5V0 with fixed load current on the primary buck 3V3 at an input voltage of VIN = 13.5 V and VIN = 6 V.

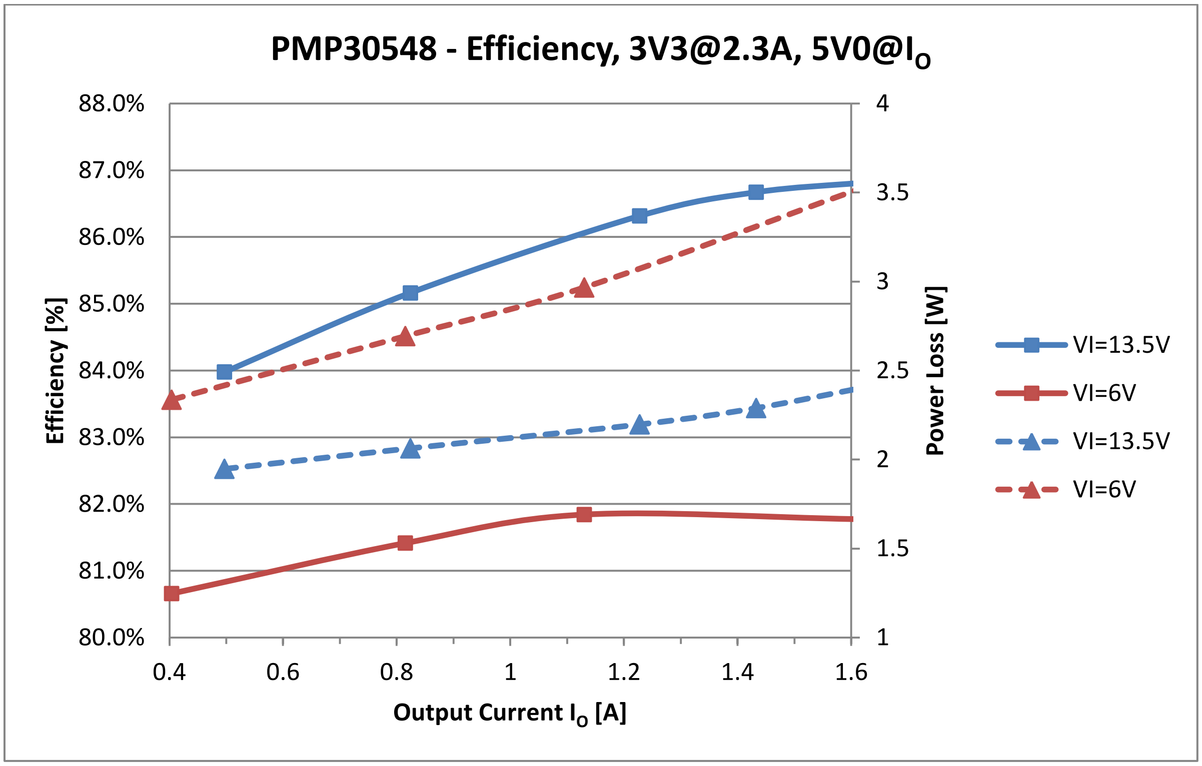

Figure 2: Efficiency Graph with variable load on 5V0 rail

2.2 Thermal Images

The thermal performance shows the circuit at an ambient temperature of 25°C. Figure 3 shows the circuit with an input voltage of 6 V and full load on all output rails.

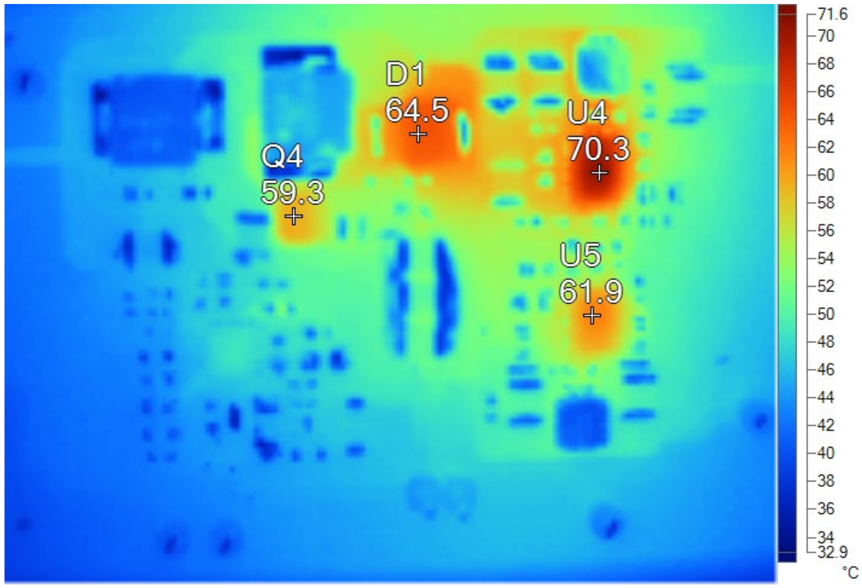

Figure 3: Thermal @ VIN = 6 V

Label	Emissivity	Background Temp	Min	Avg	Max
D1	0.97	25.5	64.5	64.5	64.5
Q4	0.97	25.5	59.3	59.3	59.3
U4	0.97	25.5	70.3	70.3	70.3
U5	0.97	25.5	61.9	61.9	61.9

3 Waveforms

3.1 Switching

Figure 5 through Figure 7 shows the switching node of the corresponding switching regulator at full load conditions.

3.1.1 LM5150 – 8V5 Switching Node

Figure 5 shows the switching node of the pre-boost voltage 8V5 at the minimum input voltage (3.2 V) and full load conditions on 3V3 rail and 5V0 rail.

Channel C4: Switching Node 8V5 (2 V/DIV), **9.3 V maximum**
Time Scale: 200 ns/DIV

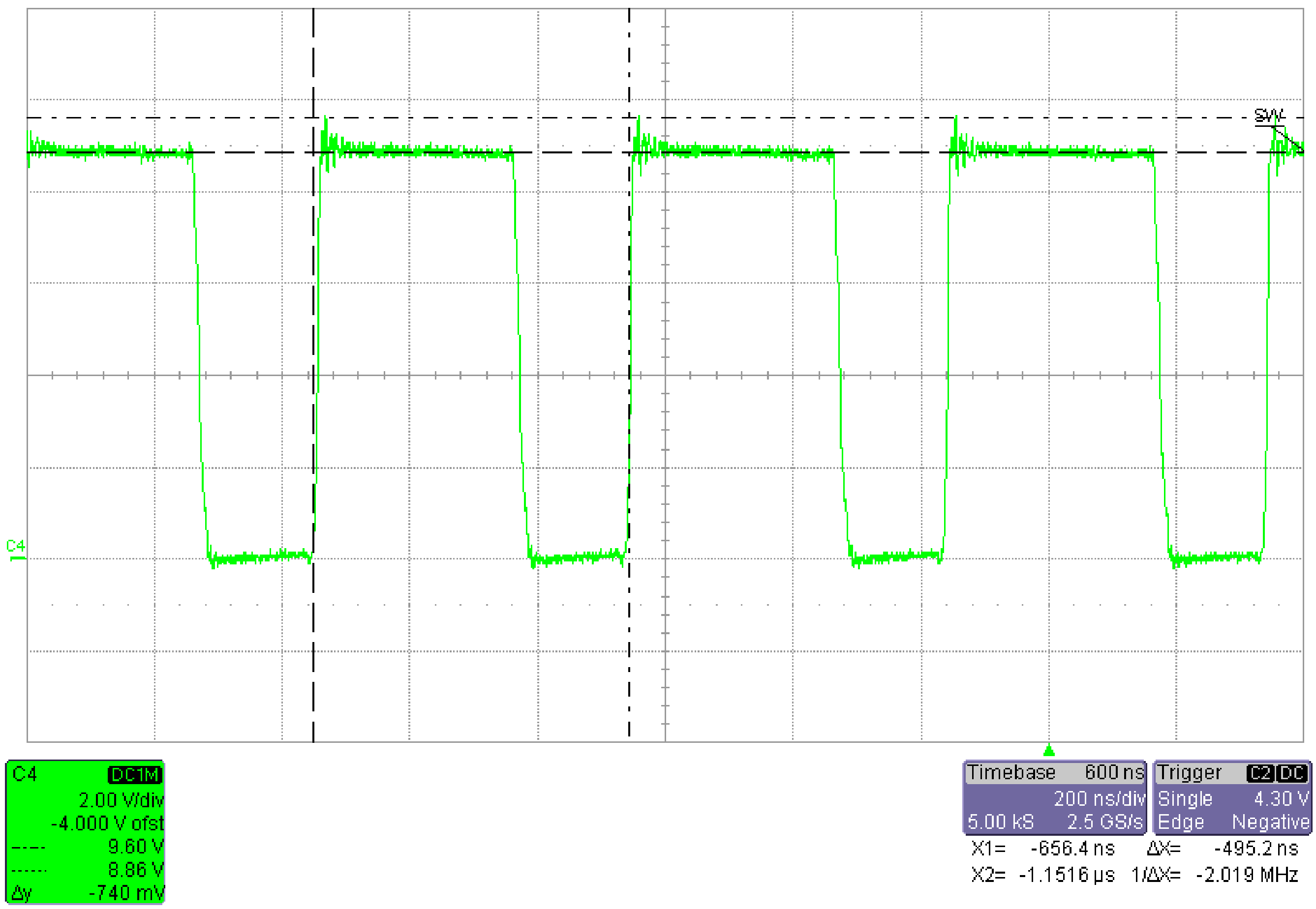

Figure 4: Switching Node 8V5 for VI = 3.2 V

3.1.2 LM53635L – 5V0 Switching Node

Figure 6 shows the switching node of the 5V0 rail at nominal input voltage of 13.5 V.

Channel C1: Output Voltage Ripple 5V0 (AC coupled, 20 mV/DIV), **13.5 V maximum**
Channel C4: Switching Node 5V0 (5 V/DIV)
Time Scale: 200 ns/DIV

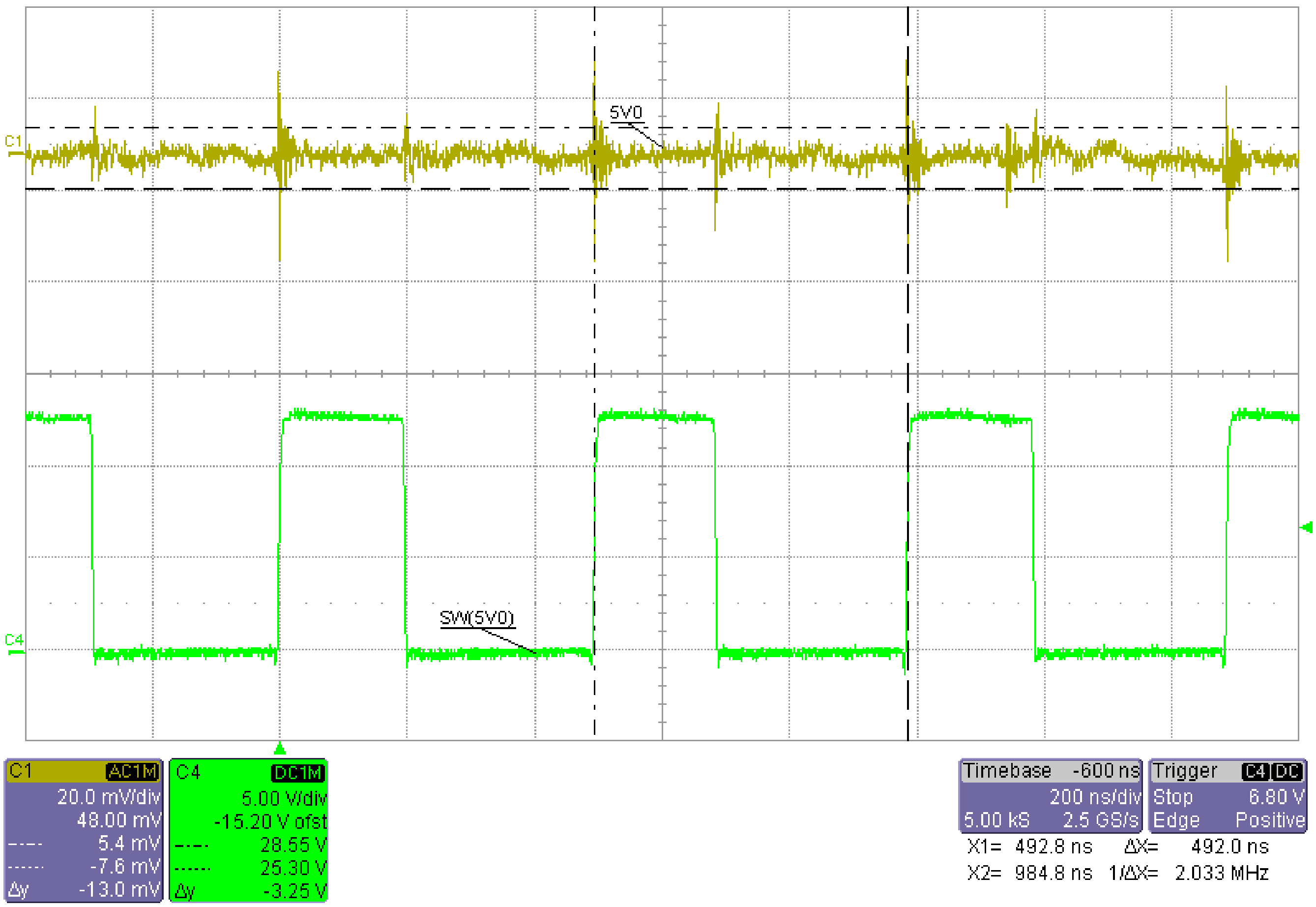

Figure 5: Switching Node for 5V0 at VI = 13.5 V

3.1.3 LM53635N – 3V3 Switching Node

Figure 7 shows the switching node of the 53V3 rail at nominal input voltage of 13.5 V.

Channel C3: Output Voltage Ripple 3V3 (AC coupled, 20 mV/DIV), **13.5 V maximum**
Channel C4: Switching Node 3V3 (5 V/DIV)
Time Scale: 200 ns/DIV

The maximum

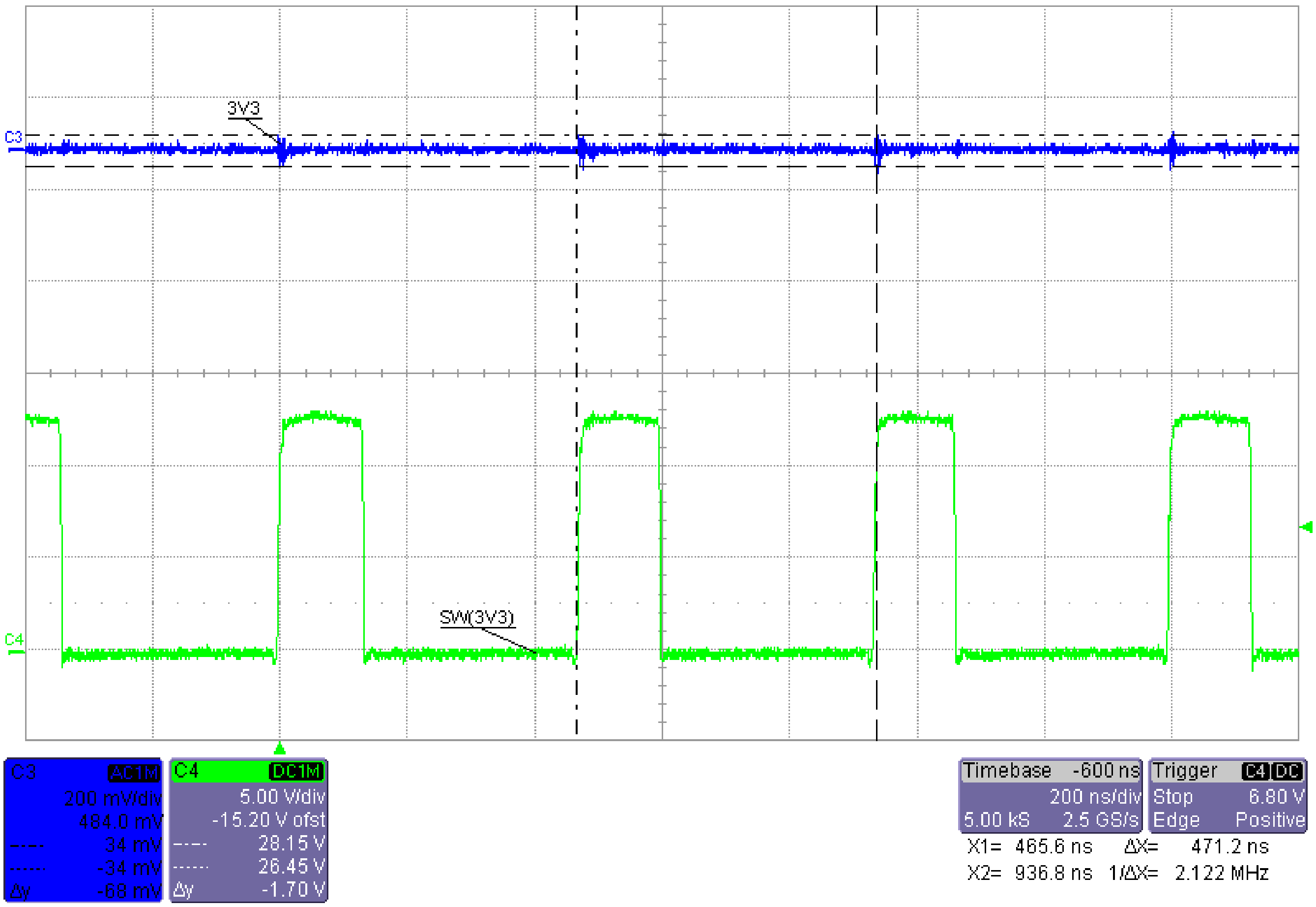

Figure 6: Switching Node for 3V3 at VI = 13.5 V

3.2 Output Voltage Ripple

Figure 8 through Figure 9 shows the output voltage ripple measurements of the circuit. The measurements were performed under full load conditions.

Channel C1: Output Voltage Ripple 5V0 (AC coupled, 50 mV/DIV), **13 mV maximum**
Channel C2: Output Voltage Ripple 3V3 (AC coupled, 50 mV/DIV), **10 mV maximum**
Channel C3: Output Voltage Ripple 8V5 (AC coupled, 100 mV/DIV), **108 mV maximum**
Time Scale: 200 ns/DIV

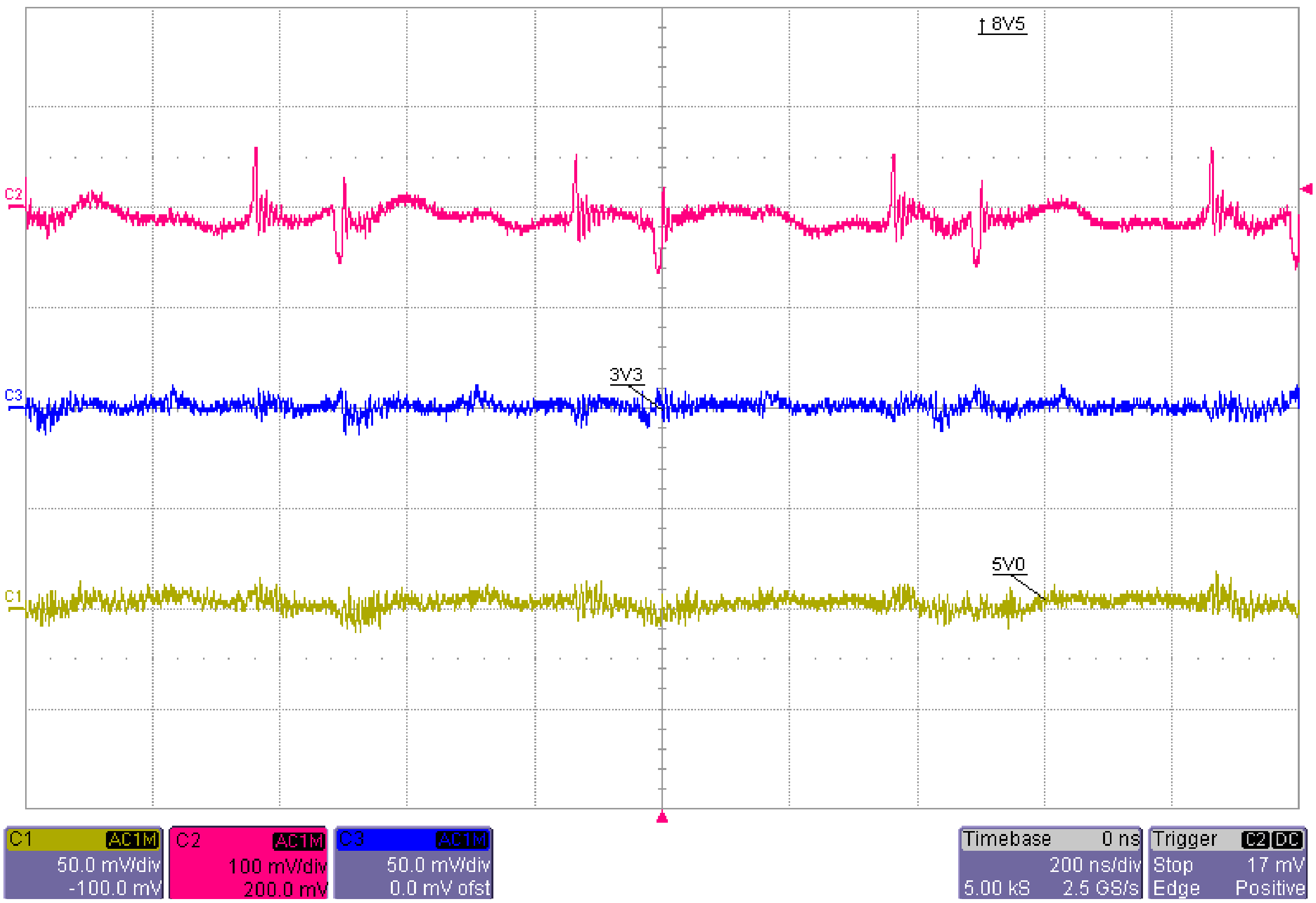

Figure 7: Output Voltage Ripple @ VIN = 3.2 V

Channel C1:	Output Voltage Ripple 5V0 (AC coupled, 50 mV/DIV), **13 mV maximum**
Channel C2:	Output Voltage Ripple 3V3 (AC coupled, 50 mV/DIV), **10 mV maximum**
Channel C3:	Output Voltage Ripple 8V5 (AC coupled, 100 mV/DIV), **d/c**
Time Scale:	200 ns/DIV

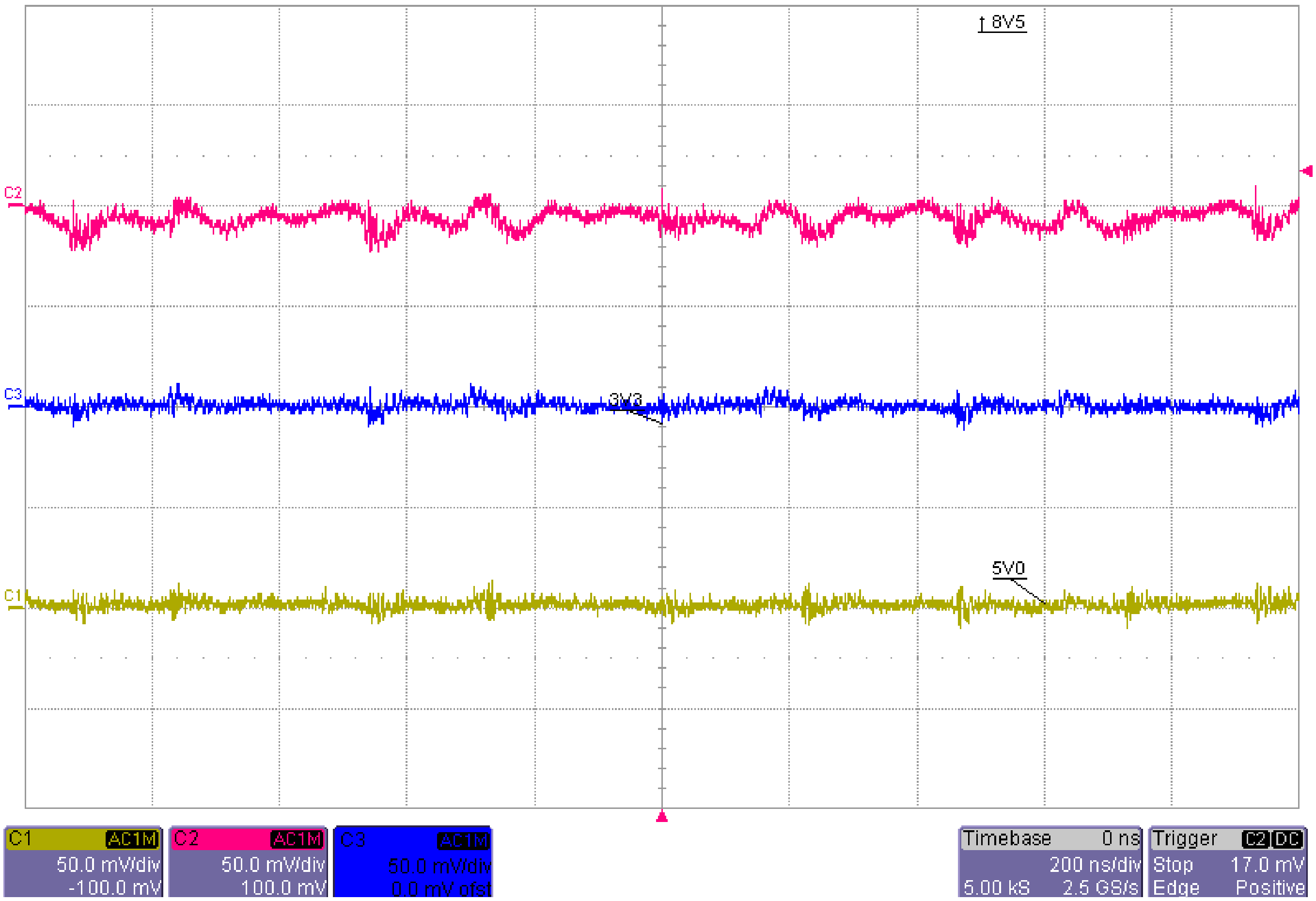

Figure 8: Output Voltage Ripple @ VIN = 13.5 V

3.3 Cold Cranking Response

The following graph shows the response of the pre-boost on a cold cranking pulse (HVAL068A, test pulse “severe”, VW80000)
Both buck stages are fully loaded.

Channel C1: Output Voltage pre-boost 8V5 (2 V /div)
Channel C2: Input Voltage VIN (2 V /div)
Time Scale: 5 ms/div

The maximum deviation of the output voltage 8V5 is at 920 mW which corresponds to 10.8%.

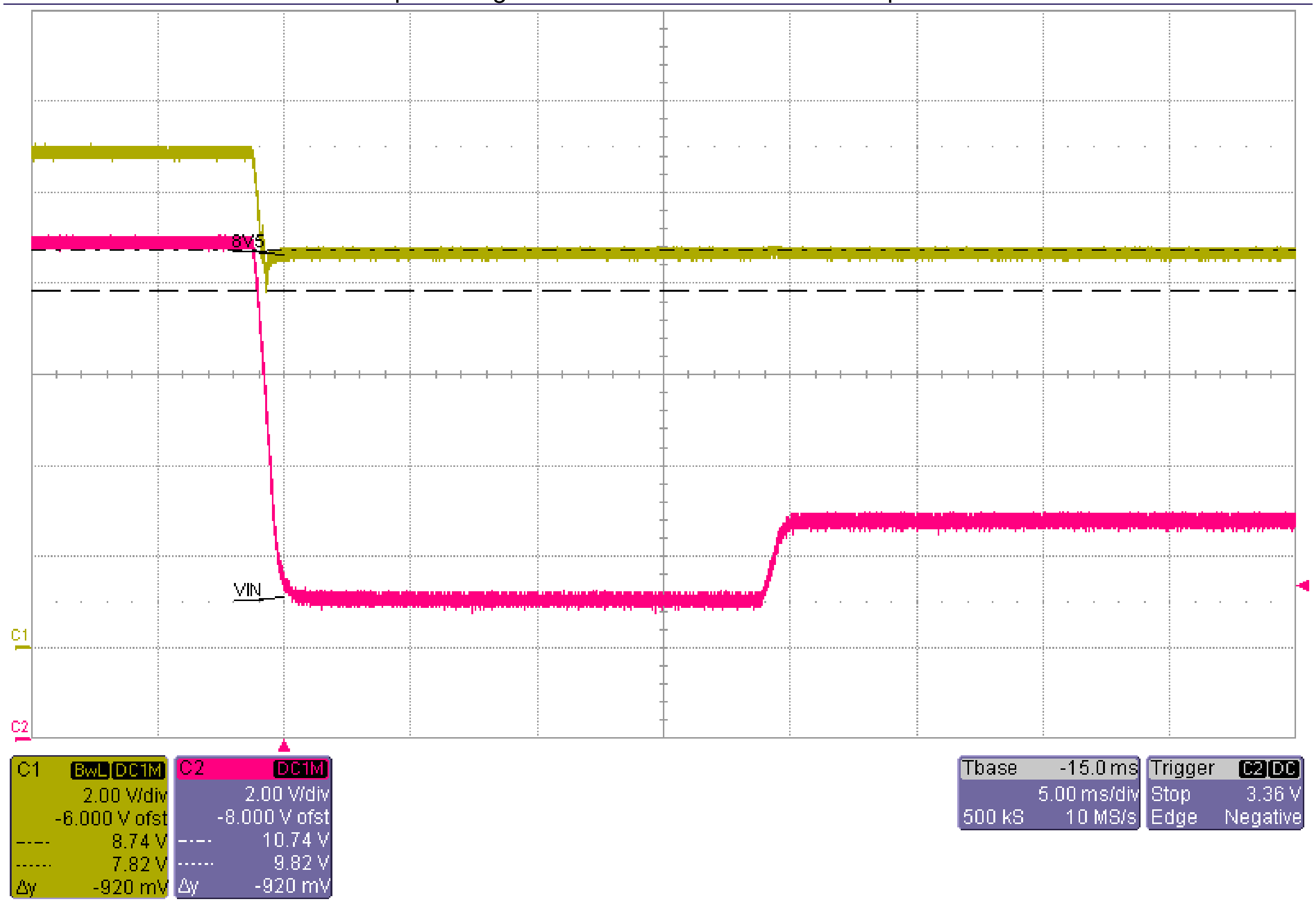

Figure 9: Cold Cranking Response (I) (Time Scale: 5 ms/div)

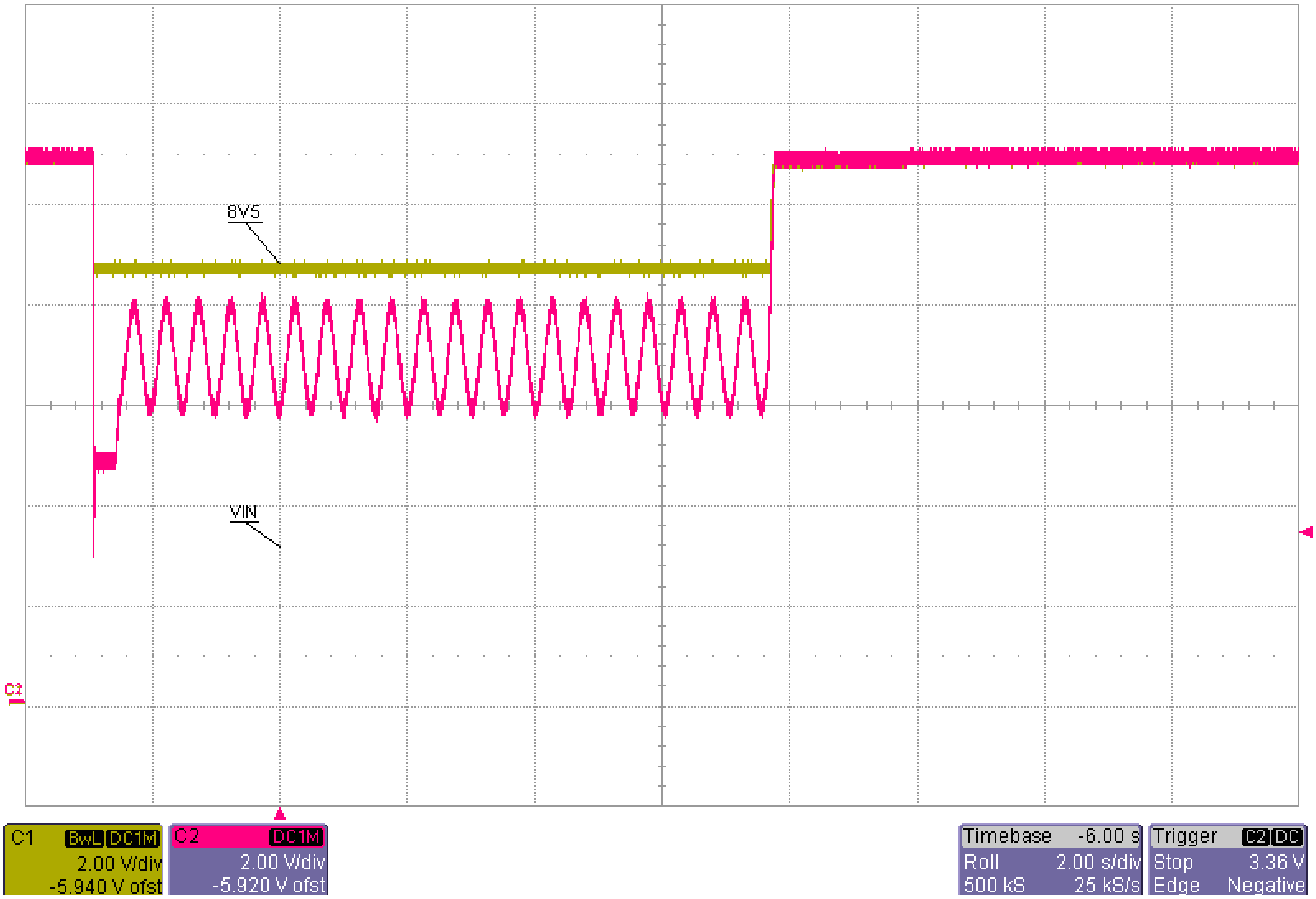

Figure 10: Cold Cranking Response (II) (Time Scale: 2s/div)

3.4 Bode Plot

3.4.1 LM5150-Q1 – 8.5V@2.3A

The following graph shows the loop response of the pre-boost at worst-case condition:

- VIN = 3.2 V
- VO = 8.5 V
- Both buck stages fully loaded
- Compensation Values:
  - C13 = 1 nF
  - C12 = 33 nF
  - R6 = 2430 Ohm

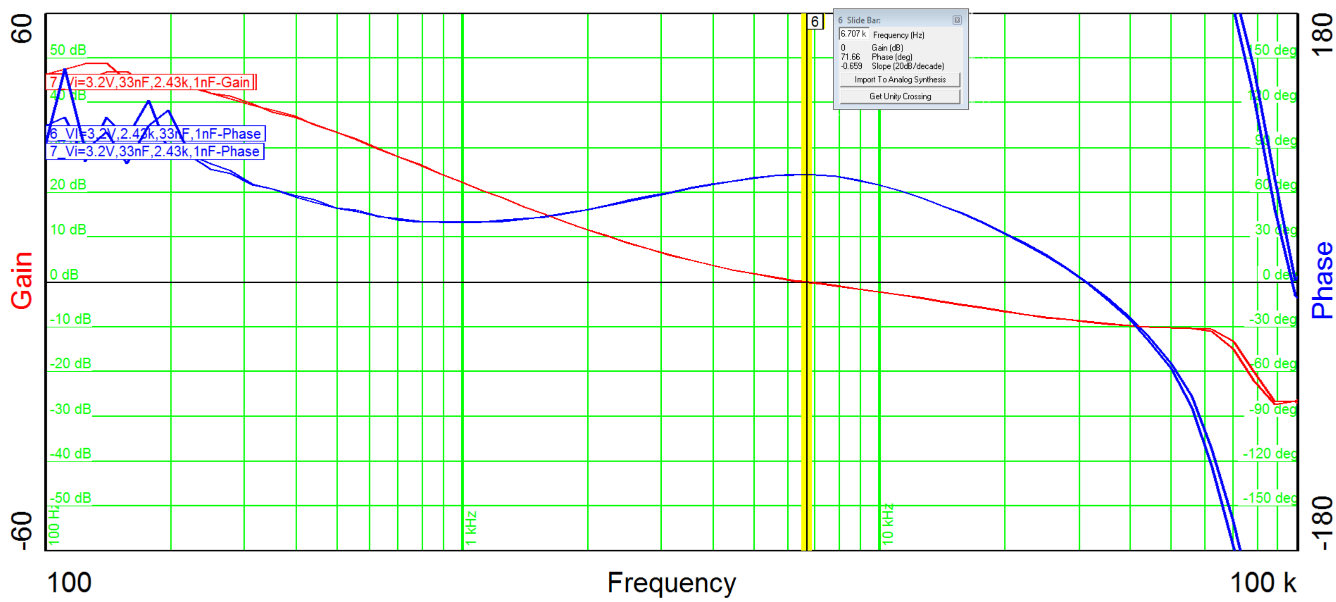

Figure 11: Loop Response – 8.5V@2.3A

Crossover Frequency (kHz)	Phase Margin (deg)	Slope (20 dB/decade)	Crossover Frequency (kHz)	Gain Margin (dB)	Slope (20 dB/decade)
6.7	71	-0.7	32	-9.2	-0.5

3.4.2 LM53635N-Q1 – 3.3V@2.3A

The following graph shows the loop response of the buck converter LM53635N-Q1 at full load condition:

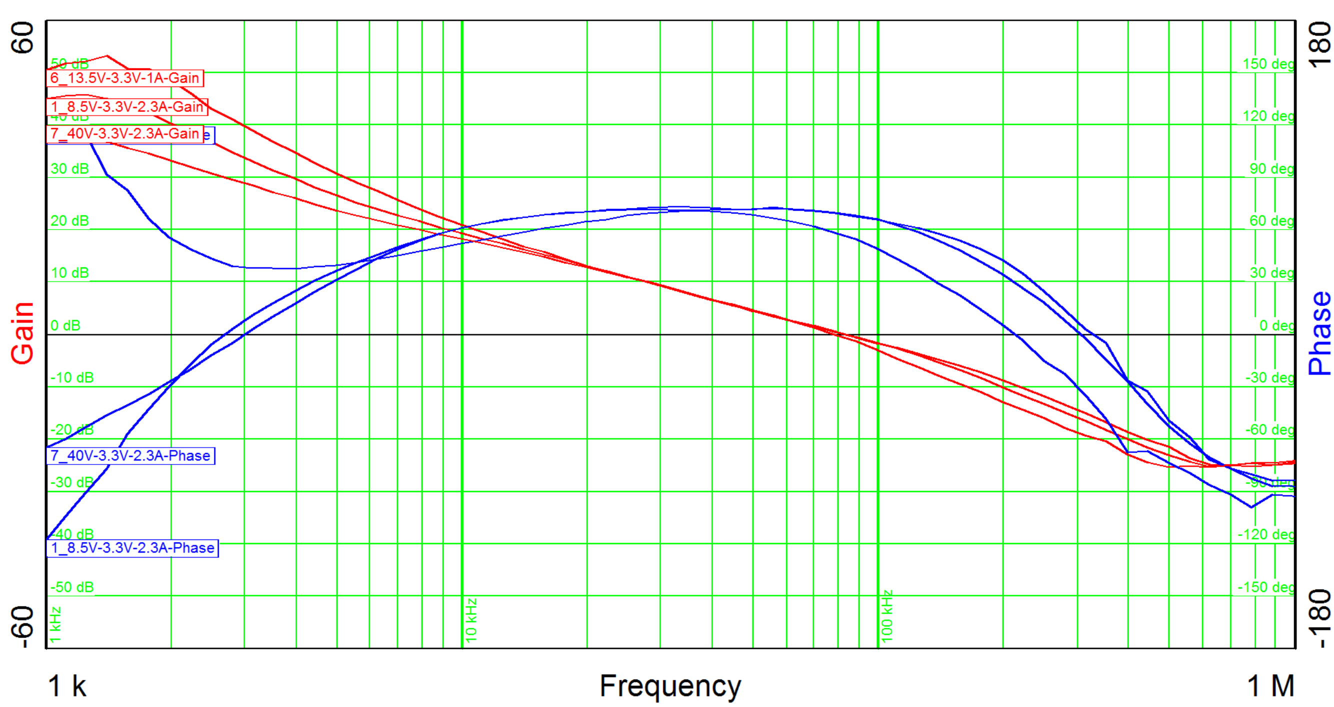

Figure 12: Loop Response – 3.3 V @ 2.3 A

VIN (V)	Crossover Frequency (kHz)	Phase Margin (deg)	Slope (20 dB/decade)	Crossover Frequency (kHz)	Gain Margin (dB)	Slope (20 dB/decade)
8.5	83.6	68.3	-1	327.4	-15.8	-1.8
13.5	82.7	69	-1	306.2	-16.3	-1.6
40	77.9	58.5	-1.4	212.6	-13.8	-1.6

3.4.3 LM53635L-Q1 – 5.0V@1.6A

The following graph shows the loop response of the buck converter LM53635N-Q1 at full load condition:

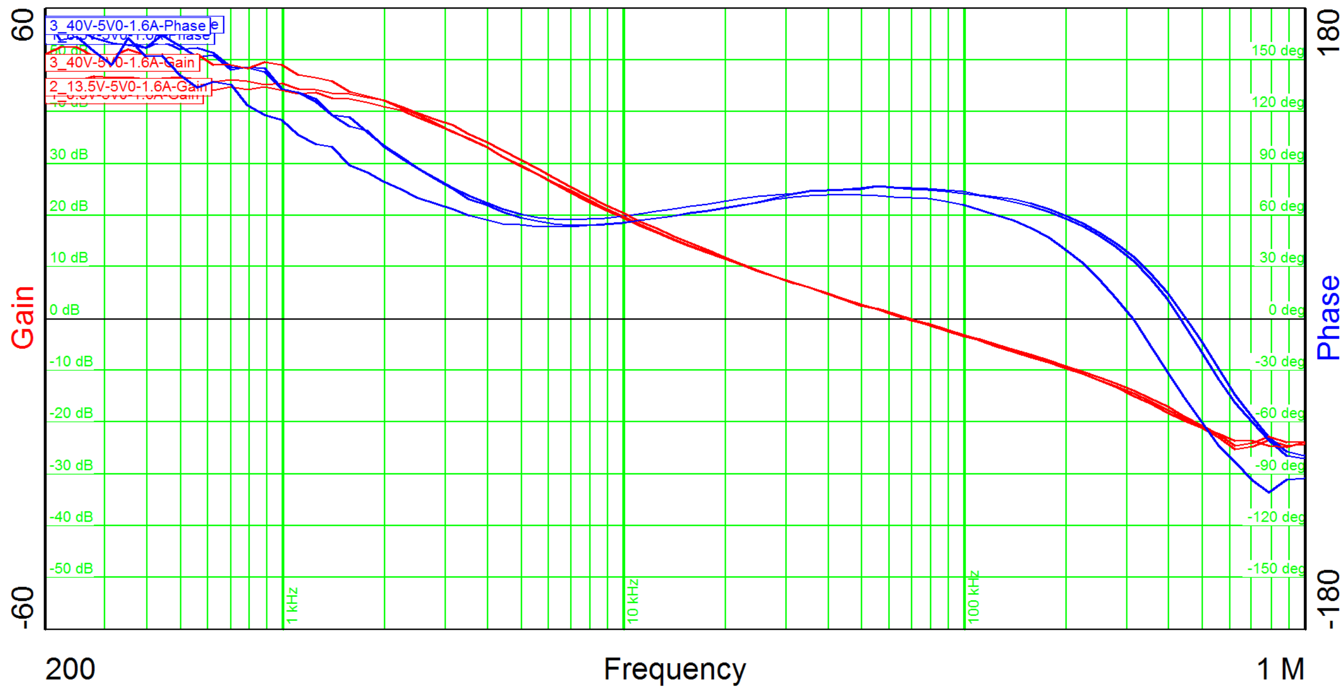

Figure 13: Loop Response – [5V@1.6A](#)

VIN (V)	Crossover Frequency (kHz)	Phase Margin (deg)	Slope (20 dB/decade)	Crossover Frequency (kHz)	Gain Margin (dB)	Slope (20 dB/decade)
8.5	67.8	76	-1.1	447.4	-19.4	-1.9
13.5	70.2	75	-1	431.4	-18.4	-1.8
40	68.7	70	-1	310.4	-14.8	-1.7

3.5 Load Transients

Figure 14 through Figure 16 shows the load transient responses.

3.5.1 LM5150 – 8V5 Load Transient Response

The response on a load step of 1 A to 2.4 A at an input voltage of 6 V is shown in Figure 14.

Channel C1: Output Voltage 8V5 (AC coupled, 20 mV/div),
410 mV undershoot (4.8%), 1.6 V overshoot (5.8%)
Channel C4: Output Current 8V5 (1 A/div)
Time Scale: 200 us/div

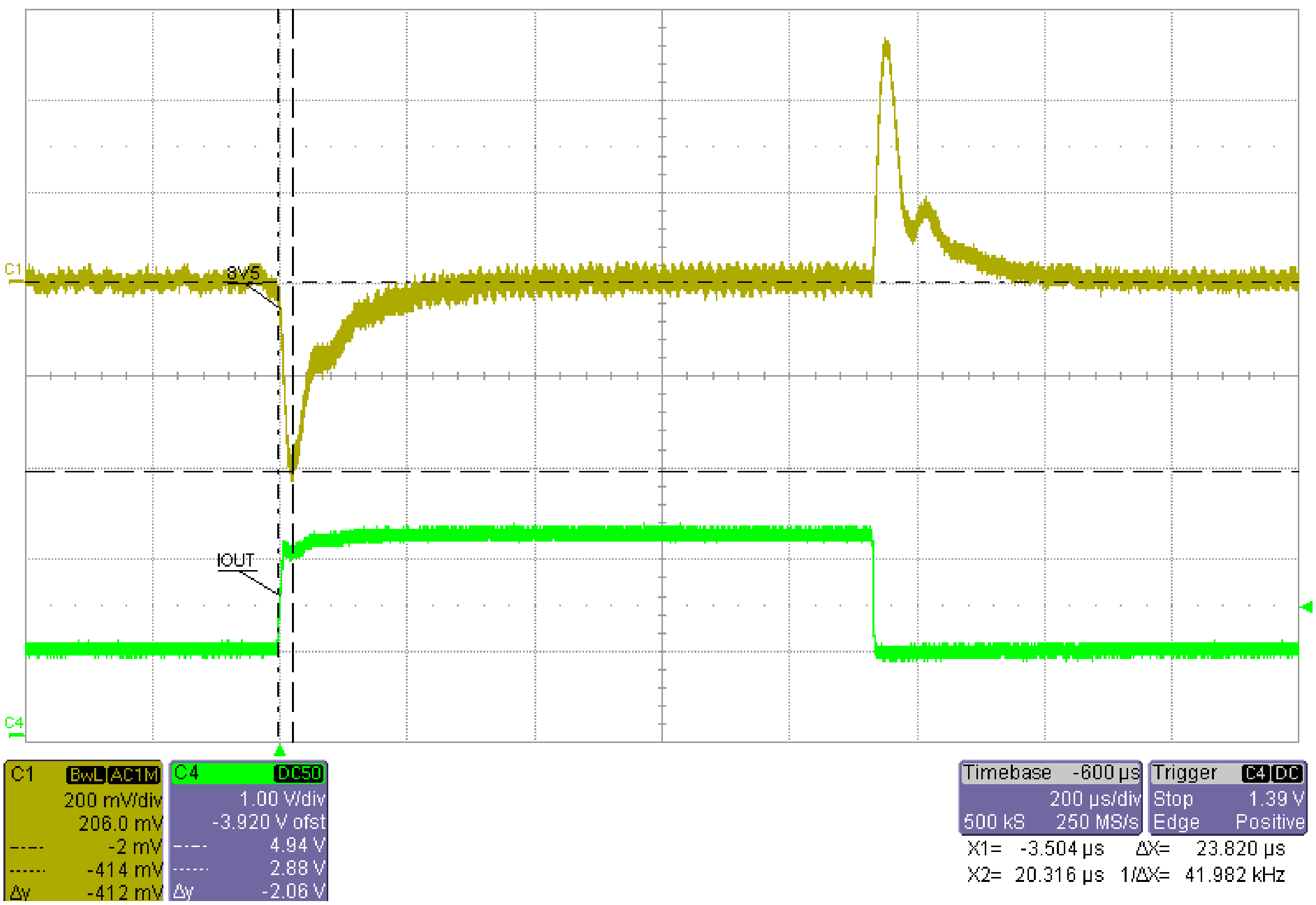

Figure 14: Load Transient Response of 8.5 V Rail

3.5.2 LM53635N – 3V3 Load Transient Response

The response on a load step of 1.1 A to 2.3 A at an input voltage of 13.5 V is shown in Figure 15. The primary buck rail 5V0 is fully loaded.

Channel C1: Output Voltage Ripple 5V0 (AC coupled, 50 mV/DIV), **fully loaded**
Channel C2: Output Voltage Ripple 3V3 (AC coupled, 100 mV/DIV),
50 mV undershoot (1.5%), 60 mV overshoot (1.8%)
Channel C4: Output Current 3V3 (1 A/DIV)
Time Scale: 200 us/div

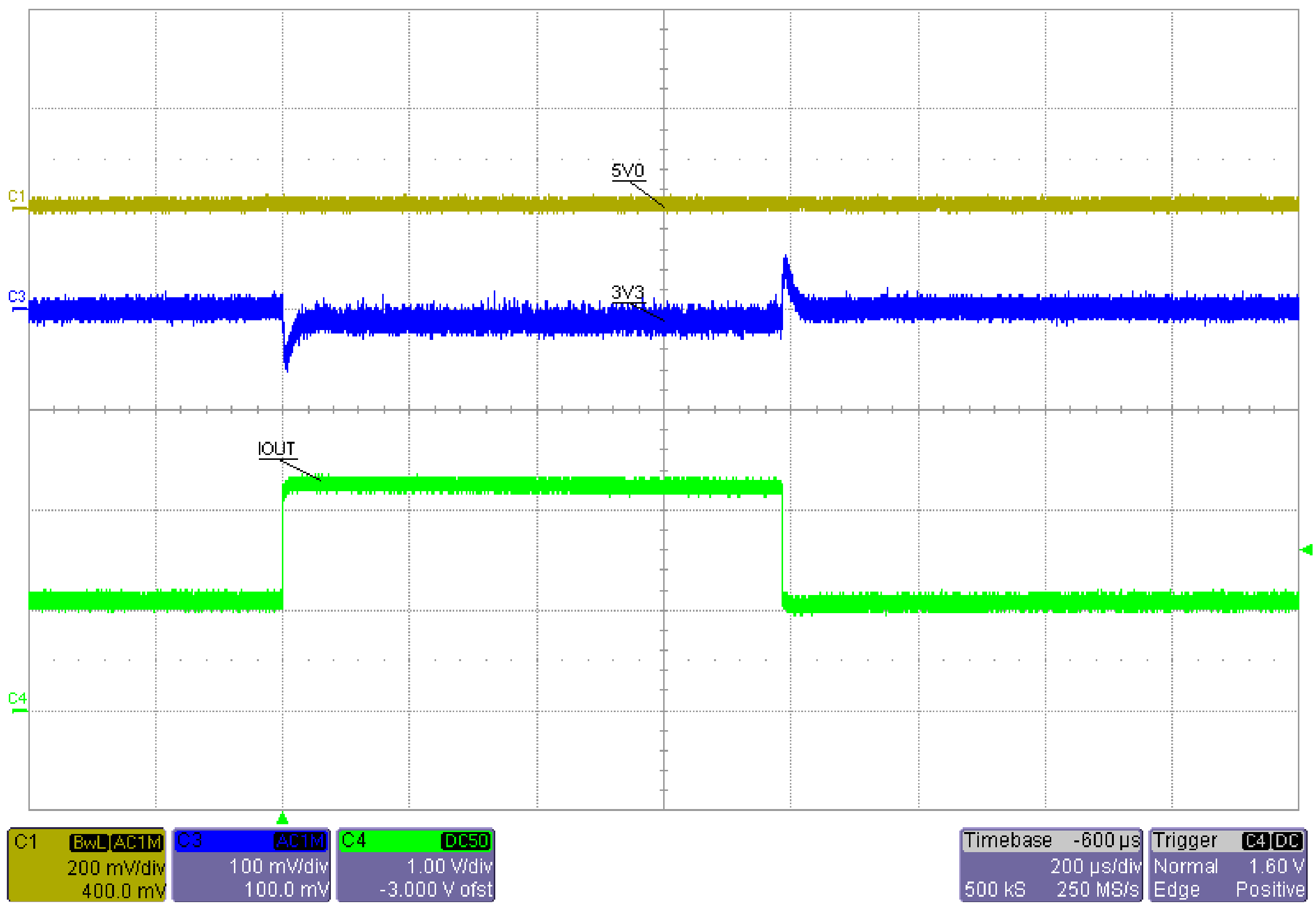

Figure 15: Load Transient Response of 3V3 Rail

3.5.3 LM53635L – 5V0 Load Transient Response

The response on a load step of 0.8 A to 1.6 A at an input voltage of 13.5 V is shown in Figure 16. The primary buck rail 3V3 is fully loaded.

Channel C3: Output Voltage Ripple 3V3 (AC coupled, 50 mV/DIV), **fully loaded**
Channel C1: Output Voltage Ripple 5V0 (AC coupled, 200 mV/DIV),
50 mV undershoot (1%), 50 mV overshoot (1%)
Channel C4: Output Current 5V0 (1 A/DIV)
Time Scale: 200 us/div

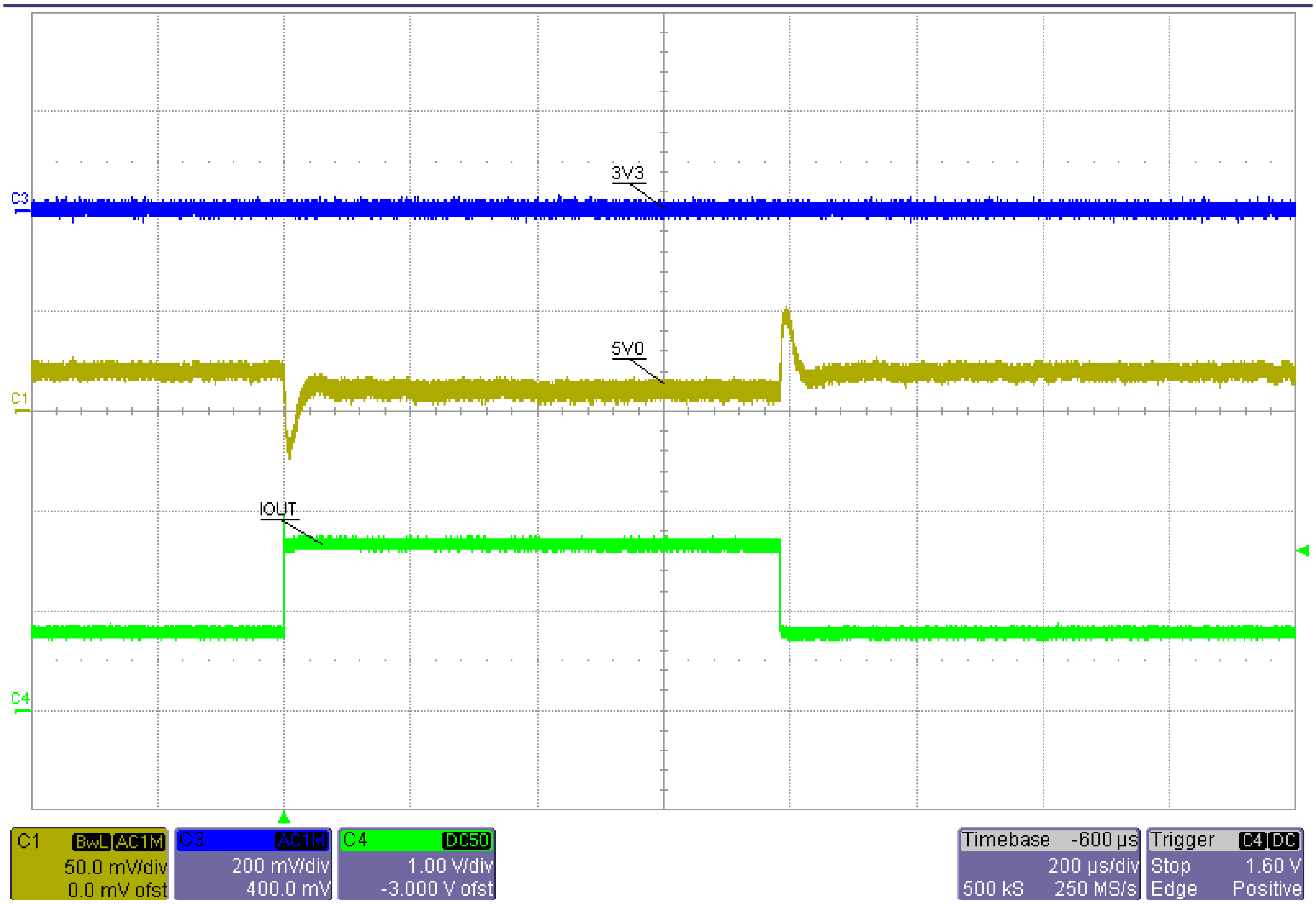

Figure 16: Load Transient Response of 5V0 Rail

3.6 *Start-up/Shut-down Sequence*

Figure 17 and Figure 18 shows the start-up and the shut-down sequence of the circuit.

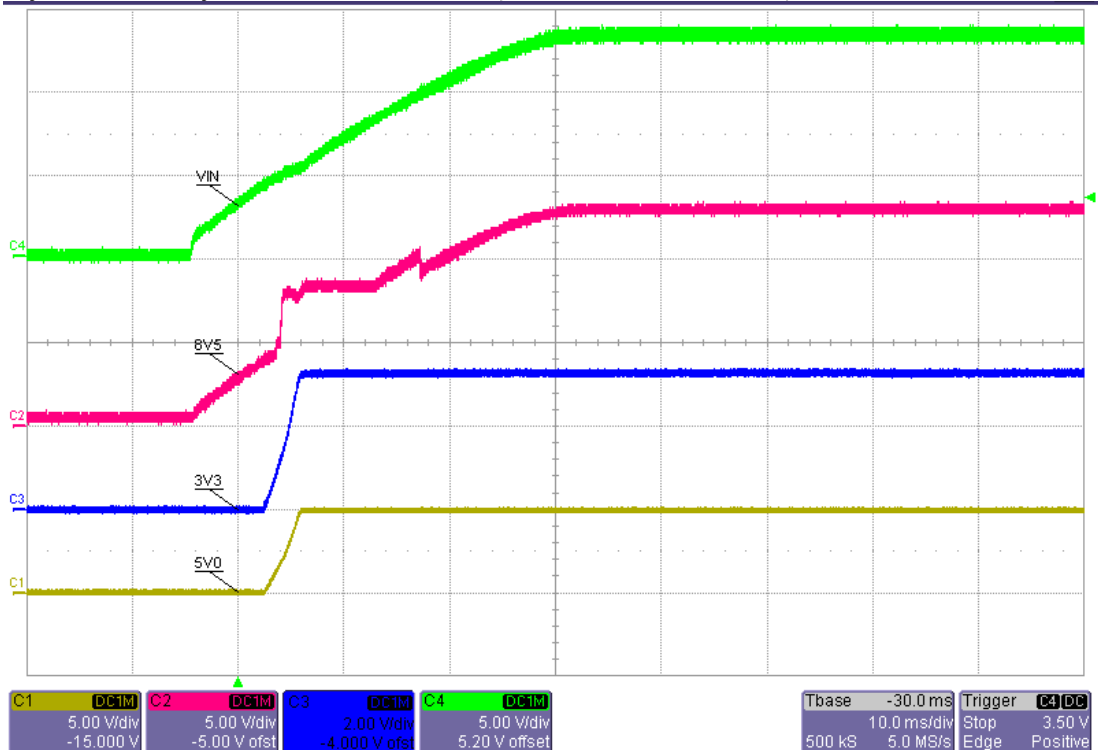

Figure 17: Start-Up Sequence

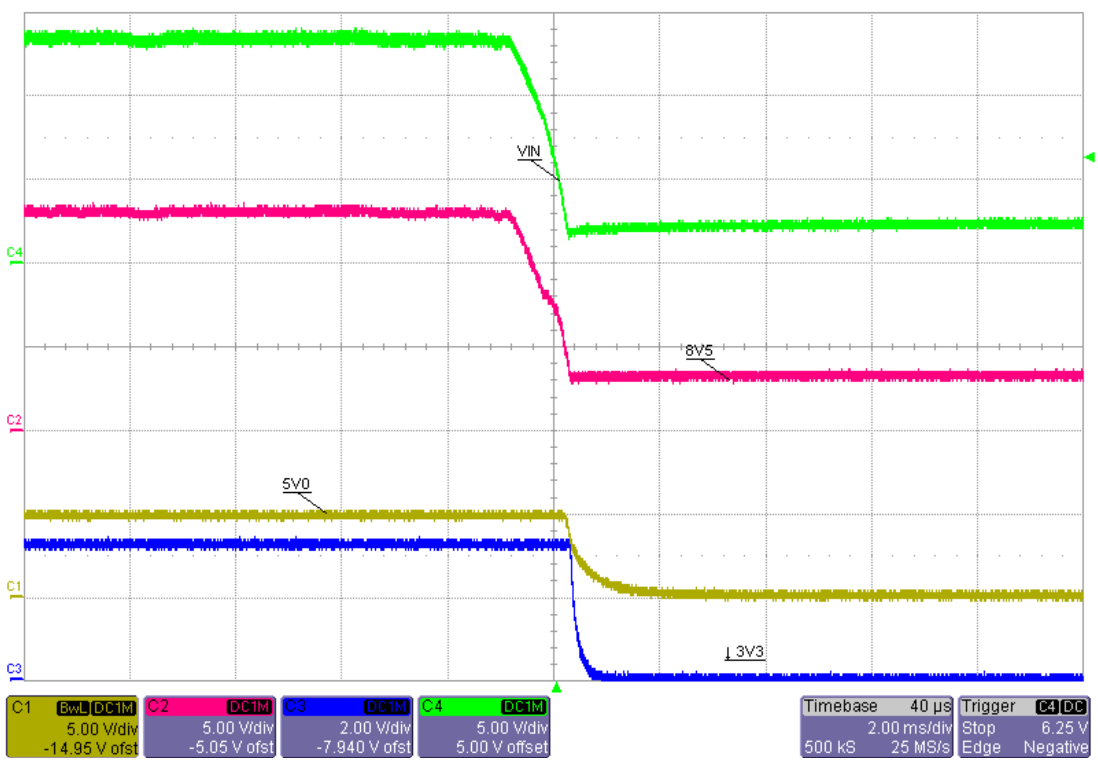

Figure 18: Shut-Down Sequence

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