CC3220R、CC3220S 和 CC3220SF SimpleLink™ Wi-Fi® 单芯片无线 MCU 解决方案

1 器件概述

1.1 特性

- 双核架构：
  - 用户专用的应用 MCU 子系统
  - 高度集成的 Wi-Fi 网络处理器
- 丰富的物联网安全功能 特性：
  - 增强的物联网网络安全性
  - 非对称密钥和唯一器件身份
  - 软件知识产权保护和安全存储 (CC3220S/CC3220SF)
- 高级低功耗模式，适用于电池供电 应用
- 内置电源管理子系统
- 工业温度范围：-40°C 至 85°C
- 芯片级 Wi-Fi Alliance® Wi-Fi CERTIFIED™

扩展 特性 列表：

- 应用 微控制器子系统：
  - Arm® Cortex®-M4 内核，运行频率 80MHz
  - 嵌入式存储器：
    - 256KB RAM
    - 可选的 1MB 可执行文件闪存
    - 外部串行闪存
  - 外设：
    - McASP 支持两个 I2S 通道
    - SD、SPI、I²C、UART
    - 8 位同步成像仪接口
    - 4 通道 12 位 ADC
    - 4 个具有 16 位 PWM 模式的通用计时器 (GPT)
    - 看门狗计时器
    - 多达 27 个 GPIO 引脚
    - 调试接口：JTAG、cJTAG、SWD
- Wi-Fi 网络处理器 (NWP) 子系统：
  - Wi-Fi 模式：
    - 802.11b/g/n 基站
    - 802.11b/g 接入点 (AP) 支持多达 4 个基站
    - Wi-Fi Direct®客户端和组所有者
  - WPA2个人和企业安全性：WEP、 WPA™/ WPA2™PSK、WPA2 企业版 (802.1x)
  - IPv4 和 IPv6 TCP/IP 堆栈
  - 行业标准 BSD 套接字应用编程接口 (API)：
    - 16 个同步 TCP 或 UDP 套接字
    - 6 个同步 TLS 和 SSL 套接字
  - IP 寻址：具有重复地址检测 (DAD) 功能的静态 IP、LLA、DHCPv4、DHCPv6
  - 适用于自主和快速 Wi-Fi 连接的 SimpleLink 连接管理器
  - 借助以下特性，实现灵活的 Wi-Fi 配置：SmartConfig™技术、AP 模式和 WPS2 选项
  - RESTful API 允许使用内部 HTTP 服务器
  - 广泛的安全 特性：
    - 硬件 特性：
      - 独立执行环境
      - 器件标识
      - 可实现高级快速安全性的硬件加密引擎（包括 AES、DES、3DES、SHA2、MD5、CRC 和校验和）
      - 初始安全编程：
        - 调试安全性
        - JTAG 和调试端口处于锁定状态
      - 个人和企业 Wi-Fi 安全性
      - 安全套接字（SSLv3、TLS1.0、TLS1.1、TLS1.2）
    - 网络安全性：
      - 个人和企业 Wi-Fi 安全性
      - 安全套接字（SSLv3、TLS1.0、TLS1.1、TLS1.2）
      - HTTPS 服务器
      - 受信任的根证书目录
      - TI 信任根公钥
    - 软件知识产权保护：
      - 安全密钥存储
      - 文件系统安全
      - 软件篡改检测
      - 克隆保护
      - 安全启动：启动期间验证运行时二进制的完整性和真实性

  - 在专用处理器上运行的嵌入式 网络 应用：
    - 具有动态用户回调的 HTTP/HTTPS Web 服务器
    - mDNS、DNS-SD、DHCP 服务器
    - Ping
  - 恢复机制 — 可恢复为出厂默认设置或恢复为完整出厂映像
  - Wi-Fi TX 功率：
    - 1 DSSS 时为 18.0dBm
    - 54 OFDM 时为 14.5dBm
  - Wi-Fi RX 灵敏度：
    - 1 DSSS 时为 -96dBm
    - 54 OFDM 时为 -74.5dBm
  - 应用吞吐量：
    - UDP：16Mbps
    - TCP：13Mbps
    - 峰值：72Mbps
- 电源管理子系统：
  - 集成式直流/直流转换器支持宽电源电压范围：
    - VBAT 宽电压模式：2.1V 至 3.6V
    - VIO 始终与 VBAT 关联
    - 预稳压 1.85V 模式
  - 高级低功耗模式:
    - 关断：1µA
    - 休眠：4.5µA
    - 低功耗深度睡眠 (LPDS)：135µA（测试对象为具有 256KB RAM 保持的 CC3220R、CC3220S 和 CC3220SF）
    - RX 流量（MCU 处于活动模式）：54 OFDM 时为 59mA（测试对象为 CC3220R 和 CC3220S；CC3220SF 会额外消耗 10mA）
    - TX 流量（MCU 处于活动模式）：在 54 OFDM、最大功耗时为 223mA（测量对象为 CC3220R 和 CC3220S；CC3220SF 会额外消耗 15 mA）
    - 空闲连接（MCU 处于 LPDS 模式）：DTIM = 1 时为 710µA（测量对象为具有 256KB RAM 保持的 CC3220R 和 CC3220S）
- 时钟源：
  - 具有内部振荡器的 40.0MHz 晶体
  - 32.768kHz 晶体或外部 RTC
- RGK 封装
  - 64 引脚 9mm × 9mm 极薄四方扁平无引线 (VQFN) 封装，0.5mm 间距
- 工作温度
  - 环境温度范围：–40°C 至 +85°C
- 器件支持 SimpleLink™ MCU 平台开发人员生态系统

1.2 应用

- 适用于物联网 应用，例如：
  - 楼宇和住宅自动化：
    - HVAC 系统和恒温器
    - 视频监控、可视门铃和低功耗摄像头
    - 楼宇安全系统和电子锁
  - 电器
  - 资产跟踪
  - 工厂自动化
  - 医疗和保健
  - 电网基础设施

1.3 说明

SoC 无线 MCU CC3220x 器件提供三种变体：CC3220R、CC3220S 和 C3220SF。

- CC3220R 特性 256KB RAM、物联网网络安全性和器件身份/密钥。
- CC3220S 基于 CC3220R 和 MCU 级安全性（例如文件系统加密、用户 IP [MCU 图像] 加密、安全启动和调试安全性）而构建。
- CC3220SF 基于 CC3220S 而构建，除了 256KB RAM 以外，还集成了一个用户专用的 1MB 可执行文件闪存。

使用 Wi-Fi CERTIFIED™ 无线微控制器开始您的物联网 (IoT) 设计。 SimpleLink™ Wi-Fi® CC3220x 器件系列是一个片上系统 (SoC) 解决方案，将两个处理器集成在一个芯片上：

- 应用处理器是一个 Arm® Cortex®-M4 MCU，具有用户专用的 256KB RAM 和可选的 1MB 串行闪存。
- 网络处理器 MCU 可运行所有 Wi-Fi® 和互联网逻辑层。这个基于 ROM 的子系统包含 802.11b/g/n 无线电、基带和具有强大加密引擎的 MAC。

这些器件引入了全新 特性 和功能，可进一步简化物联网连接。主要的新 特性 包括：

- 优化的低功耗管理
- 增强的网络安全性
- 器件身份和非对称密钥
- 增强的文件系统安全性（只有 CC3220S 和 CC3220SF 变体提供此支持）
- IPv6 TCP/IP 堆栈
- 支持 4 个基站的接入点模式
- 可同时打开多达 16 个 BSD 套接字，其中 6 个支持安全型
- HTTPS）
- 支持 RESTful API

CC3220x 器件系列是 SimpleLink™ MCU 平台的一部分，该平台是一个通用、简单易用的开发环境，基于一个单核软件开发套件 (SDK)、丰富的工具集、参考设计和 E2E™ 社区而构建，支持 Wi-Fi®、低功耗 Bluetooth®、低于 1GHz 和主机 MCU。有关更多信息，请访问 SimpleLink™ MCU 平台。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
CC3220RM2ARGKR/T	VQFN (64)	9.00mm x 9.00mm
CC3220SM2ARGKR/T	VQFN (64)	9.00mm x 9.00mm
CC3220SF12ARGKR/T	VQFN (64)	9.00mm x 9.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

1.4 功能方框图

图 1-1 显示了 CC3220x SimpleLink Wi-Fi 解决方案的功能方框图。

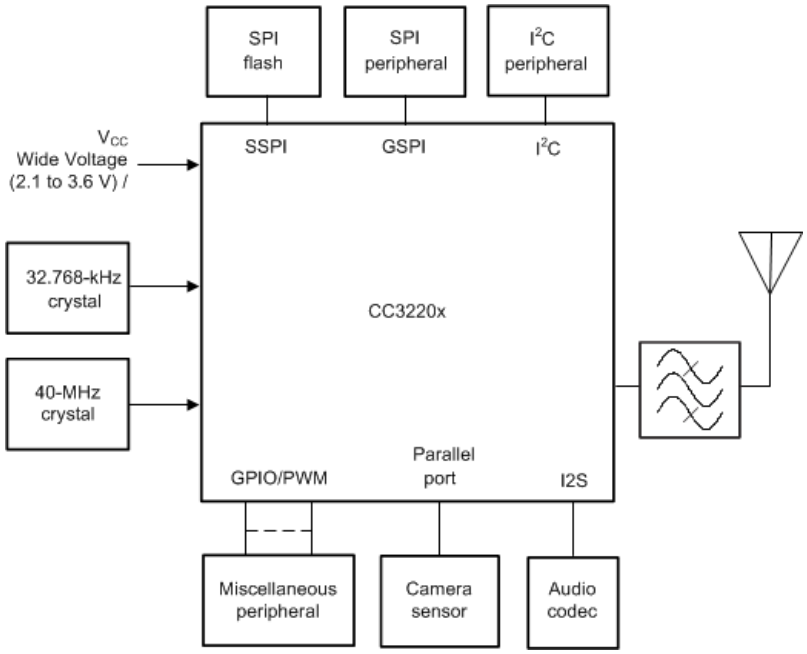


图 **1-1.** 功能框图

图 1-2 概要显示了 CC3220x 的硬件。

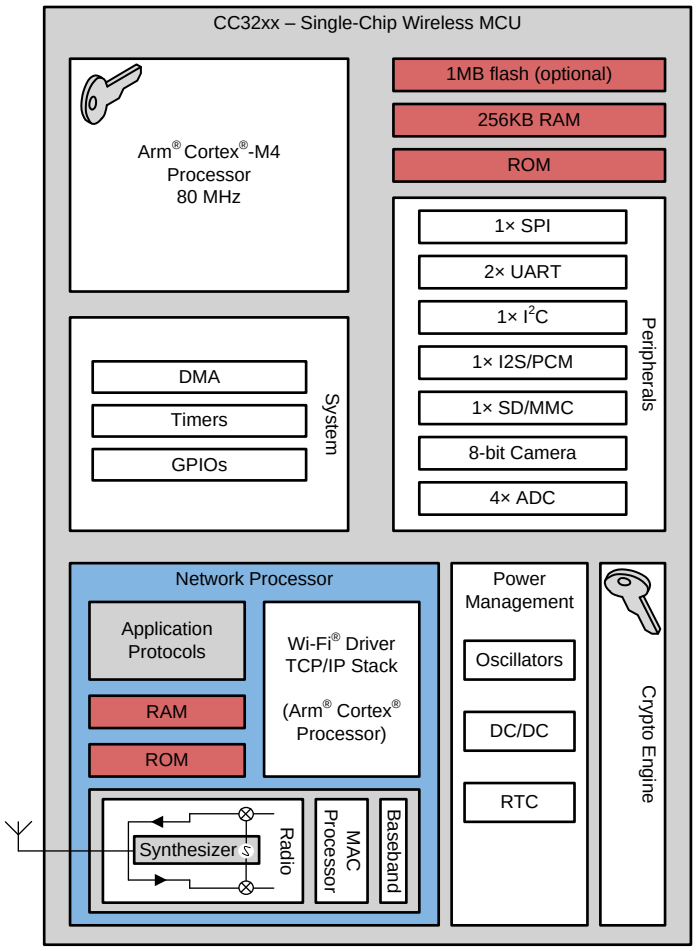


图 1-2. CC3220x 硬件概述

图 1-3 概要显示了 CC3220x 的嵌入式软件。

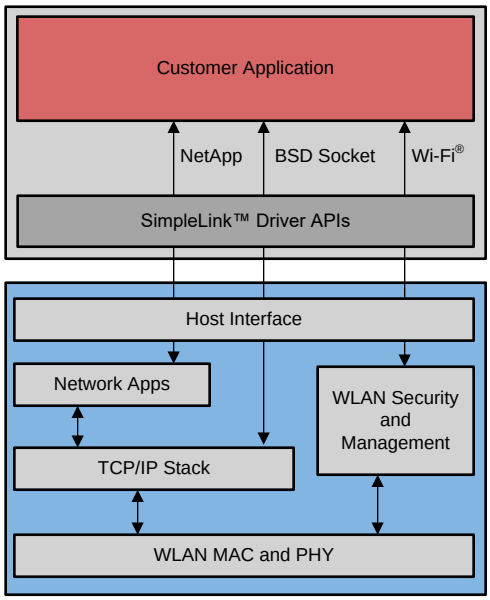


图 **1-3. CC3220x** 嵌入式软件概述

内容

2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from February 7, 2017 to November 29, 2018 **Page**

- 已更改 *特性* 部分 1
- 已更改 将出现的所有“XIP 闪存”更改为“串行闪存” 1
- 为 *功能方框图* 部分添加了 *功能方框图* 4
- Added *Device Comparison* section 9
- Changed *Device Features Comparison* table 9
- Added *NC = No internal connection* note to the pinout diagram 10
- Added *By default, all I/Os float in the Hibernate state. However, the default state can be changed by SW* in the *Pin Attributes and Pin Multiplexing* section 11
- Changed "mode 0" to "high impedance" in the note in the *Pin Attributes and Pin Multiplexing* section 11
- Added "2.4-GHz TX, RX" to the description of pin 31 12
- Added "+ve" to the description of pin 40 13
- Added "–ve" to the description of pin 40 13
- Deleted the pin number for GND_TAB 14
- Changed the condition statement in the *Absolute Maximum Ratings* table 28
- Deleted "VBAT present and nReset pin pulled low" from the "MCU SHUTDOWN" row in the *Current Consumption Summary (CC3220R, CC3220S)* table 30

- Added "MCU HIBERNATE" row to the *Current Consumption Summary (CC3220R, CC3220S)* table 30
- Deleted "VBAT present and nReset pin pulled low" from the "MCU SHUTDOWN" row in the *Current Consumption Summary (CC3200SF)* table 31
- Added the "MCU HIBERNATE" row to the *Current Consumption Summary (CC3200SF)* table 31
- Deleted the + sign from the typical values in the *WLAN Transmitter Characteristics* table 37
- Added the table note "Power of 802.11b rates are reduced to meet ETSI requirements" to the *WLAN Transmitter Characteristics* table 37
- Changed from "200-mS" to 200-ms" in the *Device Reset* section 39
- Changed from "pin 32" to "pin 52" in the second list item of the *Device Reset* section 39
- Changed *SPI Master Timing Diagram* 45
- Changed the parameter numbers in the *SPI Master Timing Parameters* table 45
- Changed *SPI Slave Timing Diagram* 46
- Changed the parameter numbers in the *SPI Slave Timing Parameters* table 46
- Changed *I2S Transmit Mode Timing Diagram* 47
- Changed the parameter numbers in the *I2S Transmit Mode Timing Parameters* table 47
- Changed I2S Receive Mode Timing Diagram 47
- Changed the parameter numbers in the *I2S Receive Mode Timing Parameters* table 48
- Changed *I^2C Timing Diagram* 50
- Changed the parameter names in the *I^2C Timing Parameters* table 50
- Changed *JTAG Timing Diagram* 51
- Changed the parameter names in the *JTAG Timing Parameters* table 51
- Changed *Camera Parallel Port Timing Diagram* 53
- Changed the parameter numbers in the *Camera Parallel Port Timing Parameters* table 53
- Deleted the *Functional Block Diagram* subsection in the *Detailed Description* section. Subsequent subsections renumbered 56
- Changed from "0x4401 EFFF" to "0x4401 DFFF" in the *Memory Map* table 67
- Changed from "0x4402 0FFF" to "0x4402 1FFF" in the *Memory Map* table 67
- Changed *CC3220x Wide-Voltage Mode Application Circuit* diagram 70
- Added footnote to L5 in the *Bill of Materials for CC3220x in Wide-Voltage Mode* table 71
- Added R7 information to the *Bill of Materials for CC3220x in Wide-Voltage Mode* table 71
- Added R8 information to the *Bill of Materials for CC3220x in Wide-Voltage Mode* table 71
- Changed *CC3220x Preregulated 1.85-V Mode Application Circuit* diagram 72
- Added footnote to L3 in the *Bill of Materials for CC3220x Preregulated, 1.85-V Mode* table 73
- Added R7 information to the *Bill of Materials for CC3220x in Preregulated, 1.85-V Mode* table 73
- Changed from "XTALM" to "XTAL_N" in the *Clock Interfaces* section 75
- 已更改 *工具和软件* 部分 77
- 已更改 *CC3220x 器件命名规则* 图片 78
- 已更改 *文档支持* 部分 79
- 已添加 *相关链接*小节 81

3 Device Comparison

Table 3-1 shows the features supported across different CC3220 devices.

Table 3-1. Device Features Comparison

FEATURE	DEVICE		
	CC3220R	CC3220S	CC3220SF
	On-Chip Application Memory		
RAM	256KB	256KB	256KB
Flash	–	–	1MB
	Security Features		
Enhanced Application Level Security	–	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming
Hardware Acceleration	Hardware Crypto Engines	Hardware Crypto Engines	Hardware Crypto Engines
Additional Networking Security	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key
Secure Boot	No	Yes	Yes
	Additional Features		
Standard	802.11 b/g/n		
TCP/IP Stack	IPv4, IPv6		
Package	9 mm × 9 mm VQFN		
Sockets	16		

3.1 Related Products

For information about other devices in this family of products or related products, see the following links:

SimpleLink™ MCU Portfolio This portfolio offers a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. With 100 percent code reuse across host MCUs, Wi-Fi™, Bluetooth® low energy, Sub-1 GHz devices and more, choose the MCU or connectivity standard that fits your design. A one-time investment with the SimpleLink software development kit (SDK) allows you to reuse often, opening the door to create unlimited applications.

SimpleLink™ Wi-Fi® Family This device platform offers several Internet-on-a chip™ solutions, which address the need of battery operated, security enabled products. Texas instruments offers a single chip wireless microcontroller and a wireless network processor which can be paired with any MCU, to allow developers to design new wi-fi products, or upgrade existing products with wi-fi capabilities.

BoosterPack™ Plug-In Modules The BoosterPack Plug-in modules extend the functionality of TI LaunchPad Development Kit. Application-specific BoosterPack Plug-in modules allow you to explore a broad range of applications, including capacitive touch, wireless sensing, LED Lighting control, and more. Stack multiple BoosterPack modules onto a single LaunchPad kit to further enhance the functionality of your design.

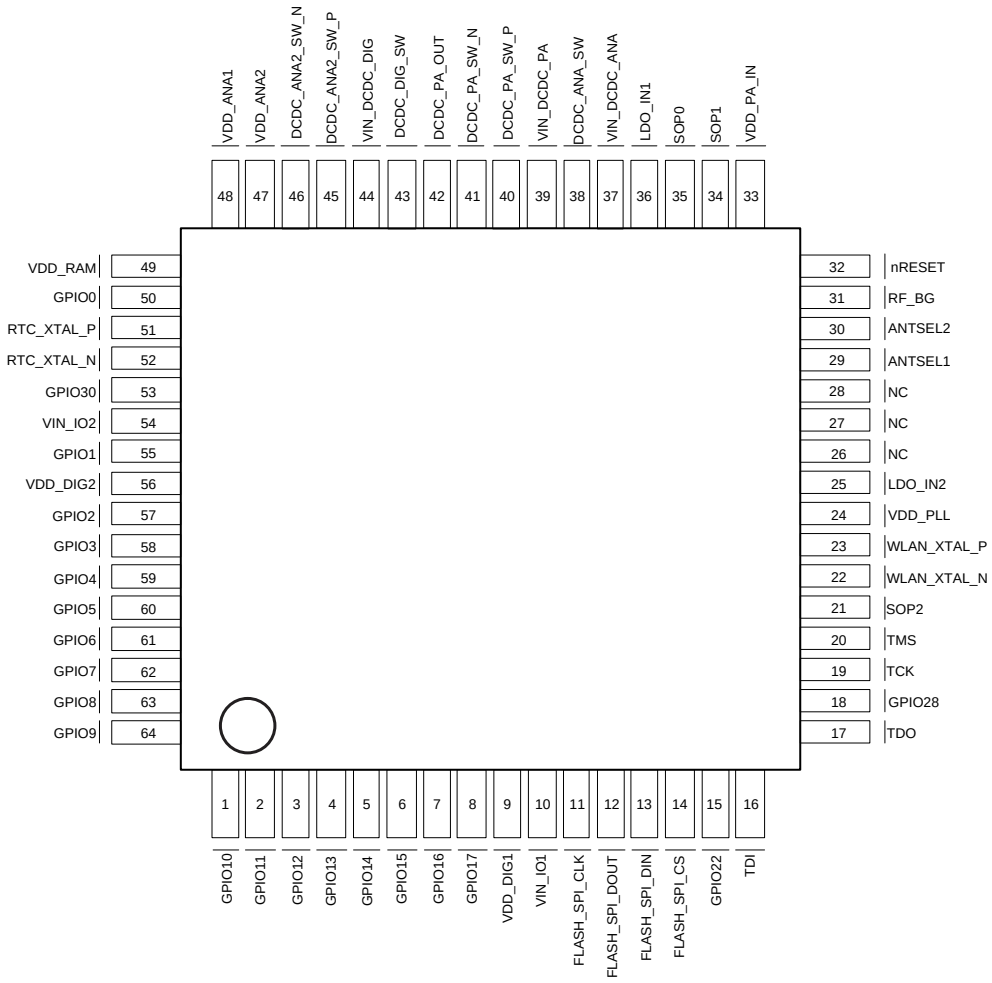
Reference Designs for CC3200 and CC3220 Devices TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

SimpleLink™ Wi-Fi® CC3220 SDK This SDK contains drivers for the CC3220 programmable MCU, sample applications, and documentation required to start development with CC3220 solutions.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows pin assignments for the 64-pin VQFN package.



NC = No internal connection

Figure 4-1. VQFN 64-Pin Assignments
Top View

4.2 Pin Attributes and Pin Multiplexing

The device makes extensive use of pin multiplexing to accommodate the large number of peripheral functions in the smallest possible package. To achieve this configuration, pin multiplexing is controlled using a combination of hardware configuration (at device reset) and register control.

NOTE

TI highly recommends using *Pin Mux Tool* to obtain the desired pinout.

The board and software designers are responsible for the proper pin multiplexing configuration. Hardware does not ensure that the proper pin multiplexing options are selected for the peripherals or interface mode used.

Table 4-1 and Table 4-2 list the pin descriptions and attributes. Table 4-3 lists the signal descriptions. Table 4-4 presents an overall view of pin multiplexing. All pin multiplexing options are configurable using the pin mux registers.

The following special considerations apply:

- All I/Os support drive strengths of 2, 4, and 6 mA. The drive strength is individually configurable for each pin.
- All I/Os support 10-µA pullup and pulldown resistors.
- The V_{IO} and V_{BAT} supply must be tied together at all times.
- By default, all I/Os float in the Hibernate state. However, the default state can be changed by SW.
- All digital I/Os are nonfail-safe.

NOTE

If an external device drives a positive voltage to the signal pads and the CC3220x device is not powered, DC is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the CC3220x device can occur. To prevent current draw, TI recommends any one of the following conditions:

- All devices interfaced to the CC3220x device must be powered from the same power rail as the chip.
- Use level shifters between the device and any external devices fed from other independent rails.
- The nRESET pin of the CC3220x device must be held low until the V_{BAT} supply to the device is driven and stable.
- All GPIO pins default to high impedance unless programmed by the MCU. The bootloader sets the TDI, TDO, TCK, TMS, and Flash_SPI pins to mode 1. All the other pins are left in the Hi-Z state.

Table 4-1. Pin Descriptions

PINS		TYPE	DESCRIPTION	SELECT AS WAKEUP SOURCE	CONFIGURE ADDITIONAL ANALOG MUX	MUXED WITH JTAG
NO.	NAME					
1	GPIO10	I/O	General-purpose input or output	No	No	No
2	GPIO11	I/O	General-purpose input or output	Yes	No	No
3	GPIO12	I/O	General-purpose input or output	No	No	No
4	GPIO13	I/O	General-purpose input or output	Yes	No	No
5	GPIO14	I/O	General-purpose input or output	No	No	No
6	GPIO15	I/O	General-purpose input or output	No	No	No
7	GPIO16	I/O	General-purpose input or output	No	No	No
8	GPIO17	I/O	General-purpose input or output	Yes	No	No
9	VDD_DIG1	Power	Internal digital core voltage	N/A	N/A	N/A

Table 4-1. Pin Descriptions (continued)

PINS		TYPE	DESCRIPTION	SELECT AS WAKEUP SOURCE	CONFIGURE ADDITIONAL ANALOG MUX	MUXED WITH JTAG
NO.	NAME					
10	VIN_IO1	Power	I/O power supply (same as battery voltage)	N/A	N/A	N/A
11	FLASH_SPI_CLK	O	Serial flash interface: SPI clock	N/A	N/A	N/A
12	FLASH_SPI_DOUT	O	Serial flash interface: SPI data out	N/A	N/A	N/A
13	FLASH_SPI_DIN	I	Serial flash interface: SPI data in	N/A	N/A	N/A
14	FLASH_SPI_CS	O	Serial flash interface: SPI chip select	N/A	N/A	N/A
15	GPIO22	I/O	General-purpose input or output	No	No	No
16	TDI	I/O	JTAG interface: data input	No	No	Muxed with JTAG TDI
17	TDO	I/O	JTAG interface: data output	Yes	No	Muxed with JTAG TDO
18	GPIO28	I/O	General-purpose input or output	No	No	No
19	TCK	I/O	JTAG/SWD interface: clock	No	No	Muxed with JTAG/ SWD-TCK
20	TMS	I/O	JTAG/SWD interface: mode select or SWDIO	No	No	Muxed with JTAG/ SWD-TMSC
21 (1)	SOP2	I	Configuration sense-on-power 2	No	No	No
22	WLAN_XTAL_N	Analog	40-MHz crystal. Pulldown if external TCXO is used.	N/A	N/A	N/A
23	WLAN_XTAL_P	Analog	40-MHz crystal or TCXO clock input	N/A	N/A	N/A
24	VDD_PLL	Power	Internal analog voltage	N/A	N/A	N/A
25	LDO_IN2	Power	Internal analog RF supply from analog DC/DC output	N/A	N/A	N/A
26	NC	—	No connect	N/A	N/A	N/A
27	NC	—	Reserved	N/A	N/A	N/A
28	NC	—	Reserved	N/A	N/A	N/A
29 (2)	ANTSEL1	O	Antenna selection control	No	User configuration not required (3)	No
30 (2)	ANTSEL2	O	Antenna selection control	No	User configuration not required (3)	No
31	RF_BG	RF	RF BG band: 2.4-GHz TX, RX	N/A	N/A	N/A
32	nRESET	I	Master chip reset input. Active low input.	N/A	N/A	N/A
33	VDD_PA_IN	Power	Internal RF power amplifier (PA) input from PA DC/DC output	N/A	N/A	N/A
34	SOP1	I	Configuration sense-on-power 1	N/A	N/A	N/A
35	SOP0	I	Configuration sense-on-power 0	N/A	N/A	N/A
36	LDO_IN1	Power	Internal Analog RF supply from analog DC/DC output	N/A	N/A	N/A
37	VIN_DCDC_ANA		Analog DC/DC supply input (same as battery voltage [V_{BAT}])	N/A	N/A	N/A
38	DCDC_ANA_SW	Power	Internal Analog DC/DC converter switching node	N/A	N/A	N/A

(1) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.
(2) This pin is reserved for WLAN antenna selection, controlling an external RF switch that multiplexes the RF pin of the CC3220x device between two antennas. These pins must not be used for other functionalities.
(3) Device firmware automatically enables the digital path during ROM boot.

Table 4-1. Pin Descriptions (continued)

PINS		TYPE	DESCRIPTION	SELECT AS WAKEUP SOURCE	CONFIGURE ADDITIONAL ANALOG MUX	MUXED WITH JTAG
NO.	NAME					
39	VIN_DCDC_PA	Power	PA DC/DC converter input supply (same as battery voltage [V_{BAT}])	N/A	N/A	N/A
40	DCDC_PA_SW_P	Power	Internal PA DC/DC converter +ve switching node	N/A	N/A	N/A
41	DCDC_PA_SW_N	Power	Internal PA DC/DC converter –ve switching node	N/A	N/A	N/A
42	DCDC_PA_OUT	Power	Internal PA buck DC/DC converter output	N/A	N/A	N/A
43	DCDC_DIG_SW	Power	Internal Digital DC/DC converter switching node	N/A	N/A	N/A
44	VIN_DCDC_DIG	Power	Digital DC/DC converter supply input (same as battery voltage [V_{BAT}])	N/A	N/A	N/A
45 (4)	DCDC_ANA2_SW_P	I/O	Analog2 DC/DC converter +ve switching node	No	User configuration not required (3)	No
46	DCDC_ANA2_SW_N	Power	Internal Analog2 DC/DC converter –ve switching node	N/A	N/A	N/A
47	VDD_ANA2	Power	Internal Analog2 DC/DC output	N/A	N/A	N/A
48	VDD_ANA1	Power	Internal Analog1 power supply fed by analog2 DC/DC converter output	N/A	N/A	N/A
49	VDD_RAM	Power	Internal SRAM LDO output	N/A	N/A	N/A
50	GPIO0	I/O	General-purpose input or output	No	User configuration not required (3)	No
51	RTC_XTAL_P	Analog	32.768-kHz XTAL_P or external CMOS level clock input	N/A	N/A	N/A
52 (5)	RTC_XTAL_N	Analog	32.768-kHz XTAL_N	N/A	User configuration not required (3)(6)	No
53	GPIO30	I/O	General-purpose input or output	No	User configuration not required (3)	No
54	VIN_IO2	Power	device supply voltage (V_{BAT})	N/A	N/A	N/A
55	GPIO1	I/O	General-purpose input or output	No	No	No
56	VDD_DIG2	Power	internal digital core voltage	N/A	N/A	N/A
57 (7)	GPIO2	I/O	Analog input (up to 1.5-V) or general-purpose input or output	Yes	See (8)	No
58 (7)	GPIO3	I/O	Analog input (up to 1.5-V) or general-purpose input or output	No	See (8)	No
59 (7)	GPIO4	I/O	Analog input (up to 1.5-V) or general-purpose input or output	Yes	See (8)	No
60 (7)	GPIO5	I/O	Analog input (up to 1.5 V) or general-purpose input or output	No	See (8)	No
61	GPIO6	I/O	General-purpose input or output	No	No	No
62	GPIO7	I/O	General-purpose input or output	No	No	No
63	GPIO8	I/O	General-purpose input or output	No	No	No

(4) Pin 45 is used by an internal DC/DC converter (ANA2_DCDC). This pin will be available automatically if the serial flash is forced in the CC3220SF device. For the CC3220R and CC3220S devices, pin 45 can be used as GPIO_31 if a supply is provided on pin 47.
(5) Pin 52 is used by the RTC crystal oscillator. These devices use automatic configuration sensing. Therefore, some board-level configuration is required to use pin 52 as a digital pad. Pin 52 is used for the RTC crystal in most applications. However, in some applications a 32.768-kHz square-wave clock might always be available onboard. When a 32.768-kHz square-wave clock is available, the crystal can be removed to free pin 52 for digital functions. The external clock must then be applied at pin 51. For the device to automatically detect this configuration, a 100-kΩ pullup resistor must be connected between pin 52 and the supply line. To prevent false detection, TI recommends using pin 52 for output-only functions.
(6) To use the digital functions, RTC_XTAL_N must be pulled high to the supply voltage using a 100-kΩ resistor.
(7) This pin is shared by the ADC inputs and digital I/O pad cells.
(8) Requires user configuration to enable the analog switch of the ADC channel (the switch is off by default.) The digital I/O is always connected and must be made Hi-Z before enabling the ADC switch.

Table 4-1. Pin Descriptions (continued)

PINS		TYPE	DESCRIPTION	SELECT AS WAKEUP SOURCE	CONFIGURE ADDITIONAL ANALOG MUX	MUXED WITH JTAG
NO.	NAME					
64	GPIO9	I/O	General-purpose input or output	No	No	No
GND_TAB		—	Thermal pad and electrical ground	N/A	N/A	N/A

Table 4-2. Pin Attributes

PIN NO.	SIGNAL NAME(1)	SIGNAL TYPE(2)	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS(3)	Hib(4)	nRESET = 0
1	GPIO10 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SCL		1	I/O (open drain)	Hi-Z, Pull, Drive		
	GT_PWM06		3	O	Hi-Z, Pull, Drive		
	UART1_TX		7	O	1		
	SDCARD_CLK		6	O	0		
	GT_CCP01		12	I	Hi-Z, Pull, Drive		
2	GPIO11 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SDA		1	I/O (open drain)	Hi-Z, Pull, Drive		
	GT_PWM07		3	O	Hi-Z, Pull, Drive		
	pXCLK (XVCLK)		4	O	0		
	SDCARD_CMD		6	I/O (open drain)	Hi-Z, Pull, Drive		
	UART1_RX		7	I	Hi-Z, Pull, Drive		
	GT_CCP02		12	I	Hi-Z, Pull, Drive		
	McAFSX		13	O	Hi-Z, Pull, Drive		
3	GPIO12 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	McACLK		3	O	Hi-Z, Pull, Drive		
	pVS (VSYNC)		4	I	Hi-Z, Pull, Drive		
	I2C_SCL		5	I/O (open drain)	Hi-Z, Pull, Drive		
	UART0_TX		7	O	1		
	GT_CCP03		12	I	Hi-Z, Pull, Drive		
4	GPIO13 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SDA		5	I/O (open drain)			
	pHS (HSYNC)		4	I			
	UART0_RX		7	I			
	GT_CCP04		12	I			
5	GPIO14 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SCL		5	I/O (open drain)			
	GSPI_CLK		7	I/O			
	pDATA8 (CAM_D4)		4	I			
	GT_CCP05		12	I			

(1) Signals names with (PN) denote the default pin name.
(2) Signal Types: I = Input, O = Output, I/O = Input or Output.
(3) LPDS state: Unused I/Os are in a Hi-Z state. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.
(4) Hibernate mode: The I/Os are in a Hi-Z state. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.

Table 4-2. Pin Attributes (continued)

PIN NO.	SIGNAL NAME(1)	SIGNAL TYPE(2)	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS(3)	Hib(4)	nRESET = 0
6	GPIO15 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SDA		5	I/O (open drain)			
	GSPI_MISO		7	I/O			
	pDATA9 (CAM_D5)		4	I			
	GT_CCP06		13	I			
	SDCARD_DATA0		8	I/O			
7	GPIO16 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GSPI_MOSI		7	I/O	Hi-Z, Pull, Drive		
	pDATA10 (CAM_D6)		4	I	Hi-Z, Pull, Drive		
	UART1_TX		5	O	1		
	GT_CCP07		13	I	Hi-Z, Pull, Drive		
	SDCARD_CLK		8	O	0		
8	GPIO17 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART1_RX		5	I			
	GSPI_CS		7	I/O			
	pDATA11 (CAM_D7)		4	I			
	SDCARD_CMD		8	I/O			
9	VDD_DIG1 (PN)	—	N/A	N/A	N/A	N/A	N/A
10	VIN_IO1	—	N/A	N/A	N/A	N/A	N/A
11	FLASH_SPI_CLK	O	N/A	O	Hi-Z, Pull, Drive(5)	Hi-Z, Pull, Drive	Hi-Z
12	FLASH_SPI_DOUT	O	N/A	O	Hi-Z, Pull, Drive(5)	Hi-Z, Pull, Drive	Hi-Z
13	FLASH_SPI_DIN	I	N/A	I	Hi-Z, Pull, Drive(5)	Hi-Z	Hi-Z
14	FLASH_SPI_CS	O	N/A	O	1	Hi-Z, Pull, Drive	Hi-Z
15	GPIO22 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	McAFSX	O	7	O			
	GT_CCP04	I	5	I			
16	TDI (PN)	I/O	1	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO23		0	I/O			
	UART1_TX		2	O	1		
	I2C_SCL		9	I/O (open drain)	Hi-Z, Pull, Drive		
17	TDO (PN)	I/O	1	O	Hi-Z, Pull, Drive	Driven high in SWD; driven low in 4-wire JTAG	Hi-Z
	GPIO24		0	I/O			
	PWM0		5	O			
	UART1_RX		2	I			
	I2C_SDA		9	I/O (open drain)			
	GT_CCP06		4	I			
	McAFSX		6	O			
18	GPIO28	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
19	TCK (PN)	I/O	1	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GT_PWM03		8	O			

(5) To minimize leakage in some serial flash vendors during LPDS, TI recommends that the user application always enables internal weak pulldown resistors on the FLASH_SPI_DIN, FLASH_SPI_DOUT, and FLASH_SPI_CLK pins.

Table 4-2. Pin Attributes (continued)

PIN NO.	SIGNAL NAME[1]	SIGNAL TYPE[2]	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS[3]	Hib[4]	nRESET = 0
20	TMS (PN)	I/O	1	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO29		0				
21[6]	GPIO25	O	0	O	Hi-Z, Pull, Drive	Driven low	Hi-Z
	GT_PWM02		9	O	Hi-Z, Pull, Drive		
	McAFSX		2	O	Hi-Z, Pull, Drive		
	TCXO_EN		N/A (see [7])	O	0		
	SOP2 (PN)		N/A (see [8])	I	Hi-Z, Pull, Drive		
22	WLAN_XTAL_N	—	N/A (see [7])	N/A	N/A	N/A	N/A
23	WLAN_XTAL_P	—	N/A	N/A	N/A	N/A	N/A
24	VDD_PLL	—	N/A	N/A	N/A	N/A	N/A
25	LDO_IN2	—	N/A	N/A	N/A	N/A	N/A
26	NC	—	N/A	N/A	N/A	N/A	N/A
27	NC	—	N/A	N/A	N/A	N/A	N/A
28	NC	—	N/A	N/A	N/A	N/A	N/A
29[9]	ANTSEL1	O	0	O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
30[9]	ANTSEL2	O	0	O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
31	RF_BG	—	N/A	N/A	N/A	N/A	N/A
32	nRESET	—	N/A	N/A	N/A	N/A	N/A
33	VDD_PA_IN	—	N/A	N/A	N/A	N/A	N/A
34	SOP1	—	N/A	N/A	N/A	N/A	N/A
35	SOP0	—	N/A	N/A	N/A	N/A	N/A
36	LDO_IN1	—	N/A	N/A	N/A	N/A	N/A
37	VIN_DCDC_ANA	—	N/A	N/A	N/A	N/A	N/A
38	DCDC_ANA_SW	—	N/A	N/A	N/A	N/A	N/A
39	VIN_DCDC_PA	—	N/A	N/A	N/A	N/A	N/A
40	DCDC_PA_SW_P	—	N/A	N/A	N/A	N/A	N/A
41	DCDC_PA_SW_N	—	N/A	N/A	N/A	N/A	N/A
42	DCDC_PA_OUT	—	N/A	N/A	N/A	N/A	N/A
43	DCDC_DIG_SW	—	N/A	N/A	N/A	N/A	N/A
44	VIN_DCDC_DIG	—	N/A	N/A	N/A	N/A	N/A

(6) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.
(7) For details on proper use, see Section 4.5.
(8) This pin is one of three that must have a passive pullup or pulldown resistor onboard to configure the device hardware power-up mode. For this reason, the pin must be output only when used for digital functions.
(9) This pin is reserved for WLAN antenna selection, controlling an external RF switch that multiplexes the RF pin of the CC3220x device between two antennas. These pins must not be used for other functionalities.

Table 4-2. Pin Attributes (continued)

PIN NO.	SIGNAL NAME(1)	SIGNAL TYPE(2)	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS(3)	Hib(4)	nRESET = 0
45(10)	GPIO31	I/O	0	I/O	Hi-Z	Hi-Z	Hi-Z
	UART0_RX		9	I			
	McAFSX		12	O			
	UART1_RX		2	I			
	McAXR0		6	I/O			
	GSPI_CLK		7	I/O			
	DCDC_ANA2_SW_P (PN)	—	N/A (see (7))	N/A	N/A	N/A	N/A
46	DCDC_ANA2_SW_N	—	N/A	N/A	N/A	N/A	N/A
47	VDD_ANA2	—	N/A	N/A	N/A	N/A	N/A
48	VDD_ANA1	—	N/A	N/A	N/A	N/A	N/A
49	VDD_RAM	—	N/A	N/A	N/A	N/A	N/A
50	GPIO0 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART0_CTS		12	I	Hi-Z, Pull, Drive		
	McAXR1		6	I/O	Hi-Z, Pull, Drive		
	GT_CCP00		7	I	Hi-Z, Pull, Drive		
	GSPI_CS		9	I/O	Hi-Z, Pull, Drive		
	UART1_RTS		10	O	1		
	UART0_RTS		3	O	1		
	McAXR0		4	I/O	Hi-Z, Pull, Drive		
51	RTC_XTAL_P	—	N/A	N/A	N/A	N/A	N/A
52(11)	RTC_XTAL_N (PN)	O	N/A	N/A	N/A	Hi-Z, Pull, Drive	Hi-Z
	GPIO32		0	O	Hi-Z, Pull, Drive		
	McACLK		2	O			
	McAXR0		4	O			
	UART0_RTS		6	O	1		
	GSPI_MOSI		8	O	Hi-Z, Pull, Drive		
53	GPIO30 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART0_TX		9	O	1		
	McACLK		2	O	Hi-Z, Pull, Drive		
	McAFSX		3	O			
	GT_CCP05		4	I			
	GSPI_MISO		7	I/O			
54	VIN_IO2	—	N/A	N/A	N/A	N/A	N/A
55	GPIO1 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART0_TX		3	O	1		
	pCLK (PIXCLK)		4	I	Hi-Z, Pull, Drive		
	UART1_TX		6	O	1		
	GT_CCP01		7	I	Hi-Z, Pull, Drive		
56	VDD_DIG2	—	N/A	N/A	N/A	N/A	N/A

(10) Pin 45 is used by an internal DC/DC (ANA2_DCDC). This pin will be available automatically if serial flash is forced in the CC3220SF device. For the CC3220R and CC3220S devices, pin 45 can be used as GPIO_31 if a supply is provided on pin 47.

(11) Pin 52 is used by the RTC crystal oscillator. These devices use automatic configuration sensing. Therefore, some board-level configuration is required to use pin 52 as a digital pad. Pin 52 is used for RTC crystal in most applications. However, in some applications a 32.768-kHz square-wave clock might always be available onboard. When a 32.768-kHz square-wave clock is available, the crystal can be removed to free pin 52 for digital functions. The external clock must then be applied at pin 51. For the chip to automatically detect this configuration, a 100-kΩ pullup resistor must be connected between pin 52 and the supply line. To prevent false detection, TI recommends using pin 52 for output-only functions.

Table 4-2. Pin Attributes (continued)

PIN NO.	SIGNAL NAME[1]	SIGNAL TYPE[2]	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS[3]	Hib[4]	nRESET = 0
57[12]	ADC_CH0	Analog input (up to 1.5 V) or digital I/O	N/A (see [7])	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO2 (PN)		0	I/O			
	UART0_RX		3	I			
	UART1_RX		6	I			
	GT_CCP02		7	I			
58[12]	ADC_CH1	Analog input (up to 1.5 V) or digital I/O	N/A (see [7])	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO3 (PN)		0	I/O			
	UART1_TX		6	O	1		
	pDATA7 (CAM_D3)		4	I	Hi-Z, Pull, Drive		
59[12]	ADC_CH2	Analog input (up to 1.5 V) or digital I/O	N/A (see [7])	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO4 (PN)		0	I/O			
	UART1_RX		6	I			
	pDATA6 (CAM_D2)		4	I			
60[12]	ADC_CH3	Analog input (up to 1.5 V) or digital I/O	N/A (see [7])	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO5 (PN)		0	I/O			
	pDATA5 (CAM_D1)		4	I			
	McAXR1		6	I/O			
	GT_CCP05		7	I			
61	GPIO6 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART0_RTS		5	O	1		
	pDATA4 (CAM_D0)		4	I	Hi-Z, Pull, Drive		
	UART1_CTS		3	I			
	UART0_CTS		6	I			
	GT_CCP06		7	I			
62	GPIO7 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	McACLKX		13	O			
	UART1_RTS		3	O	1		
	UART0_RTS		10	O			
	UART0_TX		11	O			
63	GPIO8 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	SDCARD_IRQ		6	I			
	McAFSX		7	O			
	GT_CCP06		12	I			
64	GPIO9 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GT_PWM05		3	O			
	SDCARD_DATA0		6	I/O			
	McAXR0		7	I/O			
	GT_CCP00		12	I			
GND_TAB		—	N/A	N/A	N/A	N/A	N/A

(12) This pin is shared by the ADC inputs and digital I/O pad cells.

NOTE

The ADC inputs are tolerant up to 1.8 V (see Table 5-18 for more details about the usable range of the ADC). On the other hand, the digital pads can tolerate up to 3.6 V. Hence, take care to prevent accidental damage to the ADC inputs. TI recommends first disabling the output buffers of the digital I/Os corresponding to the desired ADC channel (that is, converted to Hi-Z state), and thereafter disabling the respective pass switches (S7 [Pin 57], S8 [Pin 58], S9 [Pin 59], and S10 [Pin 60]). For more information about drive strength and reset states for analog-digital multiplexed pins, see Section 4.5.

4.3 Signal Descriptions

Table 4-3. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
ADC	ADC_CH0	57	I/O	I	ADC channel 0 input (maximum of 1.5 V)
	ADC_CH1	58	I/O	I	ADC channel 1 input (maximum of 1.5 V)
	ADC_CH2	59	I/O	I	ADC channel 2 input (maximum of 1.5 V)
	ADC_CH3	60	I/O	I	ADC channel 3 input (maximum of 1.5 V)
Antenna selection	ANTSEL1	29	O	O	Antenna selection control 1
	ANTSEL2	30	O	O	Antenna selection control 2
Clock	TCX0_EN	21	O	O	Enable to optional external 40-MHz TCXO
	WLAN_XTAL_N	22	—	—	40-MHz crystal; pull down if external TCXO is used
	WLAN_XTAL_P	23	—	—	40-MHz crystal or TCXO clock input
	RTC_XTAL_P	51	—	—	Connect 32.768-kHz crystal or force external CMOS level clock
	RTC_XTAL_N	52	—	—	Connect 32.768-kHz crystal or connect 100-kΩ resistor to supply voltage
JTAG / SWD	TDI	16	I/O	I	JTAG TDI. Reset default pinout.
	TDO	17	I/O	O	JTAG TDO. Reset default pinout.
	TCK	19	I/O	I	JTAG/SWD TCK. Reset default pinout.
	TMS	20	I/O	I/O	JTAG/SWD TMS. Reset default pinout.
I^2C	I2C_SCL	1	I/O	I/O (open drain)	I^2C clock data
		3			
		5			
		16			
	I2C_SDA	2	I/O	I/O (open drain)	I^2C data
		4			
		6			
		17			

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Timers	GT_PWM06	1	I/O	O	Pulse-width modulated O/P
	GT_CCP01	1	I/O	I	Timer capture port
	GT_PWM07	2	I/O	O	Pulse-width modulated O/P
	GT_CCP02	2	I/O	I	Timer capture port
	GT_CCP03	3	I/O	I	
	GT_CCP04	4	I/O	I	
		15	I/O	I	
	GT_CCP05	5	I/O	I	
	GT_CCP06	6	I/O	I	
		17	I/O	I	
		61	I/O	I	
		63	I/O	I	
	GT_CCP07	7	I/O	I	
	PWM0	17	I/O	O	Pulse-width modulated output
	GT_PWM03	19	I/O	O	
	GT_PWM02	21	O	O	
	GT_CCP00	50	I/O	I	Timer capture port
		64	I/O	I	
	GT_CCP05	53	I/O	I	
	GT_CCP01	55	I/O	I	
	GT_CCP02	57	I/O	I	
	GT_CCP05	60	I	I	
	GT_PWM05	64	I/O	O	Pulse-width modulated output

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
GPIO	GPIO10	1	I/O	I/O	General-purpose input or output
	GPIO11	2	I/O	I/O	
	GPIO12	3	I/O	I/O	
	GPIO13	4	I/O	I/O	
	GPIO14	5	I/O	I/O	
	GPIO15	6	I/O	I/O	
	GPIO16	7	I/O	I/O	
	GPIO17	8	I/O	I/O	
	GPIO22	15	I/O	I/O	
	GPIO23	16	I/O	I/O	
	GPIO24	17	I/O	I/O	
	GPIO28	18	I/O	I/O	
	GPIO29	20	I/O	I/O	
	GPIO25	21	O	O	General-purpose output only
	GPIO31	45	I/O	I/O	General-purpose input or output
	GPIO0	50	I/O	I/O	
	GPIO32	52	I/O	O	General-purpose output only
	GPIO30	53	I/O	I/O	General-purpose input or output
	GPIO1	55	I/O	I/O	
	GPIO2	57	I/O	I/O	
	GPIO3	58	I/O	I/O	
	GPIO4	59	I/O	I/O	
	GPIO5	60	I/O	I/O	
	GPIO6	61	I/O	I/O	
	GPIO7	62	I/O	I/O	
	GPIO8	63	I/O	I/O	
	GPIO9	64	I/O	I/O	
McASP I^2S or PCM	McAFSX	2	I/O	O	I^2S audio port frame sync
		15			
		17			
		21			
		45			
		53			
		63			
	McACLK	3	I/O	O	I^2S audio port clock output
		52	O	O	
		53	I/O	O	
	McAXR1	50	I/O	I/O	I^2S audio port data 1 (RX and TX)
		60	I	I/O	
	McAXR0	45	I/O	I/O	I^2S audio port data 0 (RX and TX)
		50	I/O	I/O	
		52	O	O	I^2S audio port data (only output mode is supported on pin 52)
		64	I/O	I/O	I^2S audio port data (RX and TX)
	McACLKX	62	I/O	O	I^2S audio port clock

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Multimedia card (MMC or SD)	SDCARD_CLK	1	I/O	O	SD card clock data
		7			
	SDCARD_CMD	2	I/O	I/O (open drain)	SD card command line
		8	I/O	I/O	
	SDCARD_DATA0	6	I/O	I/O	SD card data
		64			
	SDCARD_IRQ	63	I/O	I	Interrupt from SD card (future support)
Parallel interface (8-bit π)	pXCLK (XVCLK)	2	I/O	O	Free clock to parallel camera
	pVS (VSYNC)	3	I/O	I	Parallel camera vertical sync
	pHS (HSYNC)	4	I/O	I	Parallel camera horizontal sync
	pDATA8 (CAM_D4)	5	I/O	I	Parallel camera data bit 4
	pDATA9 (CAM_D5)	6	I/O	I	Parallel camera data bit 5
	pDATA10 (CAM_D6)	7	I/O	I	Parallel camera data bit 6
	pDATA11 (CAM_D7)	8	I/O	I	Parallel camera data bit 7
	pCLK (PIXCLK)	55	I/O	I	Pixel clock from parallel camera sensor
	pDATA7 (CAM_D3)	58	I/O	I	Parallel camera data bit 3
	pDATA6 (CAM_D2)	59	I/O	I	Parallel camera data bit 2
	pDATA5 (CAM_D1)	60	I	I	Parallel camera data bit 1
	pDATA4 (CAM_D0)	61	I/O	I	Parallel camera data bit 0
Power	VDD_DIG1	9	—	—	Internal digital core voltage
	VIN_IO1	10	—	—	Device supply voltage (V_{BAT})
	VDD_PLL	24	—	—	Internal analog voltage
	LDO_IN2	25	—	—	Internal analog RF supply from analog DC/DC output
	VDD_PA_IN	33	—	—	Internal PA supply voltage from PA DC/DC output
	LDO_IN1	36	—	—	Internal analog RF supply from analog DC/DC output
	VIN_DCDC_ANA	37	—	—	Analog DC/DC input (connected to device input supply [V_{BAT}])
	DCDC_ANA_SW	38	—	—	Internal analog DC/DC switching node
	VIN_DCDC_PA	39	—	—	PA DC/DC input (connected to device input supply [V_{BAT}])
	DCDC_PA_SW_P	40	—	—	Internal PA DC/DC switching node
	DCDC_PA_SW_N	41	—	—	
	DCDC_PA_OUT	42	—	—	Internal PA buck converter output
	DCDC_DIG_SW	43	—	—	Internal digital DC/DC switching node
	VIN_DCDC_DIG	44	—	—	Digital DC/DC input (connected to device input supply [V_{BAT}])
	DCDC_ANA2_SW_P	45	—	—	Analog to DC/DC converter +ve switching node
	DCDC_ANA2_SW_N	46	—	—	Internal analog to DC/DC converter –ve switching node
	VDD_ANA2	47	—	—	Internal analog to DC/DC output
	VDD_ANA1	48	—	—	Internal analog supply fed by ANA2 DC/DC output
	VDD_RAM	49	—	—	Internal SRAM LDO output
	VIN_IO2	54	—	—	Device supply voltage (V_{BAT})
	VDD_DIG2	56	—	—	Internal digital core voltage

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
SPI	GSPI_CLK	5	I/O	I/O	General SPI clock
		45	I/O	I/O	
	GSPI_MISO	6	I/O	I/O	General SPI MISO
		53	I/O	I/O	
	GSPI_CS	8	I/O	I/O	General SPI chip select
		50	I/O	I/O	
	GSPI_MOSI	7	I/O	I/O	General SPI MOSI
		52	O	O	
FLASH SPI	FLASH_SPI_CLK	11	O	O	Clock to SPI serial flash (fixed default)
	FLASH_SPI_DOUT	12	O	O	Data to SPI serial flash (fixed default)
	FLASH_SPI_DIN	13	I	I	Data from SPI serial flash (fixed default)
	FLASH_SPI_CS	14	O	O	Device select to SPI serial flash (fixed default)
UART	UART1_TX	1	I/O	O	UART1 TX data
		7	I/O	O	
		16	I/O	O	
		55	I/O	O	
		58	I/O	O	
	UART1_RX	2	I/O	I	UART1 RX data
		8	I/O	I	
		17	I/O	I	
		45	I/O	I	
		57	I/O	I	
		59	I/O	I	
	UART1_RTS	50	I/O	O	UART1 request-to-send (active low)
		62	I/O	O	
	UART1_CTS	61	I/O	I	UART1 clear-to-send (active low)
	UART0_TX	3	I/O	O	UART0 TX data
		53	I/O	O	
		55	I/O	O	
		62	I/O	O	
	UART0_RX	4	I/O	I	UART0 RX data
		45	I/O	I	
		57	I/O	I	
	UART0_CTS	50	I/O	I	UART0 clear-to-send input (active low)
		61	I/O	I	
	UART0_RTS	50	I/O	O	UART0 request-to-send (active low)
		52	O	O	
		61	I/O	O	
		62	I/O	O	
Sense-on-Power	SOP2	21 (1)	O	I	Sense-on-power 2
	SOP1	34	—	—	Configuration sense-on-power 1
	SOP0	35	—	—	Configuration sense-on-power 0
Reset	nRESET	32	—	—	Global master device reset (active low)
RF	RF_BG	31	—	—	WLAN analog RF 802.11 b/g bands

(1) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.

4.4 Pin Multiplexing

Table 4-4. Pin Multiplexing

REGISTER ADDRESS	REGISTER NAME	PIN	ANALOG OR SPECIAL FUNCTION	DIGITAL FUNCTION (XXX FIELD ENCODING)(1)													
			JTAG	0	1	2	3	4	5	6	7	8	9	10	11	12	13
0x4402 E0C8	GPIO_PAD_CONFIG_10	1	—	GPIO10	I2C_SCL	—	GT_PWM06	—	—	SDCARD_ CLK	UART1_TX	—	—	—	—	GT_CCP01	—
0x4402 E0CC	GPIO_PAD_CONFIG_11	2	—	GPIO11	I2C_SDA	—	GT_PWM07	pXCLK (XVCLK)	—	SDCARD_ CMD	UART1_RX	—	—	—	—	GT_CCP02	MCAFSX
0x4402 E0D0	GPIO_PAD_CONFIG_12	3	—	GPIO12	—	—	McACLK	pVS (VSYNC)	I2C_SCL	—	UART0_TX	—	—	—	—	GT_CCP03	—
0x4402 E0D4	GPIO_PAD_CONFIG_13	4	—	GPIO13	—	—	—	pHS (HSYNC)	I2C_SDA	—	UART0_RX	—	—	—	—	GT_CCP04	—
0x4402 E0D8	GPIO_PAD_CONFIG_14	5	—	GPIO14	—	—	—	pDATA8 (CAM_D4)	I2C_SCL	—	GSPI_CLK	—	—	—	—	GT_CCP05	—
0x4402 E0DC	GPIO_PAD_CONFIG_15	6	—	GPIO15	—	—	—	pDATA9 (CAM_D5)	I2C_SDA	—	GSPI_ MISO	SDCARD_ DATA0	—	—	—	—	GT_CCP06
0x4402 E0E0	GPIO_PAD_CONFIG_16	7	—	GPIO16	—	—	—	pDATA10 (CAM_D6)	UART1_TX	—	GSPI_ MOSI	SDCARD_ CLK	—	—	—	—	GT_CCP07
0x4402 E0E4	GPIO_PAD_CONFIG_17	8	—	GPIO17	—	—	—	pDATA11 (CAM_D7)	UART1_RX	—	GSPI_CS	SDCARD_ CMD	—	—	—	—	—
0x4402 E0F8	GPIO_PAD_CONFIG_22	15	—	GPIO22	—	—	—	—	GT_CCP04	—	McAFSX	—	—	—	—	—	—
0x4402 E0FC	GPIO_PAD_CONFIG_23	16	Muxed with JTAG	GPIO23	TDI	UART1_TX	—	—	—	—	—	—	I2C_SCL	—	—	—	—
0x4402 E100	GPIO_PAD_CONFIG_24	17	Muxed with JTAG TDO	GPIO24	TDO	UART1_RX	—	GT_CCP06	PWM0	McAFSX	—	—	I2C_SDA	—	—	—	—
0x4402 E140	GPIO_PAD_CONFIG_40	18	—	GPIO28	—	—	—	—	—	—	—	—	—	—	—	—	—
0x4402 E110	GPIO_PAD_CONFIG_28	19	Muxed with JTAG or SWD and TCK	—	TCK	—	—	—	—	—	—	GT_ PWM03	—	—	—	—	—
0x4402 E114	GPIO_PAD_CONFIG_29	20	Muxed with JTAG or SWD and TMSC	GPIO29	TMS	—	—	—	—	—	—	—	—	—	—	—	—
0x4402 E104	GPIO_PAD_CONFIG_25	21(2)	—	GPIO25	—	McAFSX	—	—	—	—	—	—	GT_ PWM02	—	—	—	—
0x4402 E108	GPIO_PAD_CONFIG_26	29	—	ANTSEL1(3)	—	—	—	—	—	—	—	—	—	—	—	—	—
0x4402 E10C	GPIO_PAD_CONFIG_27	30	—	ANTSEL2(3)	—	—	—	—	—	—	—	—	—	—	—	—	—

(1) Pin mux encodings with (RD) denote the default encoding after reset release.
(2) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.
(3) LPDS state: Unused I/Os are in a Hi-Z state. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.

Table 4-4. Pin Multiplexing (continued)

REGISTER ADDRESS	REGISTER NAME	PIN	ANALOG OR SPECIAL FUNCTION	DIGITAL FUNCTION (XXX FIELD ENCODING)(1)													
			JTAG	0	1	2	3	4	5	6	7	8	9	10	11	12	13
0x4402 E11C	GPIO_PAD_CONFIG_31	45	—	GPIO31	—	UART1_RX	—	—	—	McAXR0	GSPI_CLK	—	UART0_RX	—	—	McAFSX	—
0x4402 E0A0	GPIO_PAD_CONFIG_0	50	—	GPIO0	—	—	UART0_ RTS	McAXR0	—	McAXR1	GT_CCP00	—	GSPI_CS	UART1_ RTS	—	UART0_ CTS	—
0x4402 E120	GPIO_PAD_CONFIG_32	52	—	GPIO32	—	McACLK	—	McAXR0	—	UART0 _ RTS	—	GSPI_ MOSI	—	—	—	—	—
0x4402 E118	GPIO_PAD_CONFIG_30	53	—	GPIO30	—	McACLK	McAFSX	GT_CCP05	—	—	GSPI_ MISO	—	UART0_TX	—	—	—	—
0x4402 E0A4	GPIO_PAD_CONFIG_1	55	—	GPIO1	—	—	UART0_TX	pCLK (PIXCLK)	—	UART1_TX	GT_CCP01	—	—	—	—	—	—
0x4402 E0A8	GPIO_PAD_CONFIG_2	57	—	GPIO2	—	—	UART0_RX	—	—	UART1_RX	GT_CCP02	—	—	—	—	—	—
0x4402 E0AC	GPIO_PAD_CONFIG_3	58	—	GPIO3	—	—	—	pDATA7 (CAM_D3)	—	UART1_TX	—	—	—	—	—	—	—
0x4402 E0B0	GPIO_PAD_CONFIG_4	59	—	GPIO4	—	—	—	pDATA6 (CAM_D2)	—	UART1_RX	—	—	—	—	—	—	—
0x4402 E0B4	GPIO_PAD_CONFIG_5	60	—	GPIO5	—	—	—	pDATA5 (CAM_D1)	—	McAXR1	GT_CCP05	—	—	—	—	—	—
0x4402 E0B8	GPIO_PAD_CONFIG_6	61	—	GPIO6	—	—	UART1_ CTS	pDATA4 (CAM_D0)	UART0_ RTS	UART0_ CTS	GT_CCP06	—	—	—	—	—	—
0x4402 E0BC	GPIO_PAD_CONFIG_7	62	—	GPIO7	—	—	UART1_ RTS	—	—	—	—	—	—	UART0_ RTS	UART0_TX	—	McACLKX
0x4402 E0C0	GPIO_PAD_CONFIG_8	63	—	GPIO8	—	—	—	—	—	SDCARD_ IRQ	McAFSX	—	—	—	—	GT_CCP06	—
0x4402 E0C4	GPIO_PAD_CONFIG_9	64	—	GPIO9	—	—	GT_PWM05	—	—	SDCARD_ DATA0	McAXR0	—	—	—	—	GT_CCP00	—

4.5 Drive Strength and Reset States for Analog and Digital Multiplexed Pins

Table 4-5 describes the use, drive strength, and default state of analog and digital multiplexed pins at first-time power up and reset (nRESET pulled low).

Table 4-5. Drive Strength and Reset States for Analog and Digital Multiplexed Pins

Pin	BOARD-LEVEL CONFIGURATION AND USE	DEFAULT STATE AT FIRST POWER UP OR FORCED RESET	STATE AFTER CONFIGURATION OF ANALOG SWITCHES (ACTIVE, LPDS, AND HIB POWER MODES)	MAXIMUM EFFECTIVE DRIVE STRENGTH (mA)
29	Connected to the enable pin of the RF switch (ANTSEL1). Other use is not recommended.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
30	Connected to the enable pin of the RF switch (ANTSEL2). Other use is not recommended.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
45	VDD_ANA2 (pin 47) must be shorted to the input supply rail. Otherwise, the pin is driven by the ANA2 DC/DC.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
50	Generic I/O	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
52	The pin must have an external pullup of 100 kΩ to the supply rail and must be used in output signals only.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
53	Generic I/O	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
57	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
58	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
59	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
60	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4

4.6 Pad State After Application of Power to Chip But Before Reset Release

When a stable power is applied to the CC3220x chip for the first time or when supply voltage is restored to the proper value following a period with supply voltage less than 1.5 V, the level of each digital pad is undefined in the period starting from the release of nRESET and until DIG_DCDC powers up. This period is less than approximately 10 ms. During this period, pads can be internally pulled weakly in either direction. If a certain set of pins is required to have a definite value during this prereset period, an appropriate pullup or pulldown resistor must be used at the board level. The recommended value of this external pull is 2.7 kΩ.

4.7 Connections for Unused Pins

All unused pins must be left as no connect (NC) pins. Table 4-6 provides a list of NC pins.

Table 4-6. Connections for Unused Pins

PIN	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE	DESCRIPTION
26	NC	WLAN analog	—	Unused; leave unconnected.
27	NC	WLAN analog	—	Unused; leave unconnected.
28	NC	WLAN analog	—	Unused; leave unconnected.

5 Specifications

All measurements are referenced at the device pins, unless otherwise indicated. All specifications are over process and voltage, unless otherwise indicated.

5.1 Absolute Maximum Ratings

All measurements are referenced at the device pins unless otherwise indicated. All specifications are over process, voltage, and operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{BAT} and V_{IO}	Pins: 37, 39, 44	–0.5	3.8	V
V_{IO} – V_{BAT} (differential)	Pins: 10, 54		V_{BAT} and V_{IO} should be tied together	V
Digital inputs		–0.5	V_{IO} + 0.5	V
RF pins		–0.5	2.1	V
Analog pins, crystal	Pins: 22, 23, 51, 52	–0.5	2.1	V
Operating temperature, T_A		–40	85	°C
Storage temperature, T_{stg}		–55	125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Power-On Hours (POH)

This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

OPERATING CONDITION	POWER-ON HOURS [POH] (hours)
T_A up to 85°C(1)	87,600

(1) The TX duty cycle (power amplifier ON time) is assumed to be 10% of the device POH. Of the remaining 90% of the time, the device can be in any other state.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	TYP	MAX	UNIT
V_{BAT}, V_{IO} (shorted to V_{BAT})	Pins: 10, 37, 39, 44, 54	Direct battery connection(3)	2.1(4)	3.3	3.6	V
		Preregulated 1.85 V(5)(6)				
Ambient thermal slew			–20		20	°C/minute

(1) Operating temperature is limited by crystal frequency variation.
(2) When operating at an ambient temperature of over 75°C, the transmit duty cycle must remain below 50% to avoid the auto-protect feature of the power amplifier. If the auto-protect feature triggers, the device takes a maximum of 60 seconds to restart the transmission.
(3) To ensure WLAN performance, ripple on the supply must be less than ±300 mV.
(4) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. The brownout condition is also 2.1 V, and care must be taken when operating at the minimum specified voltage.
(5) To ensure WLAN performance, ripple on the 1.85-V supply must be less than 2% (±40 mV).
(6) TI recommends keeping V_{BAT} above 1.85 V. For lower voltages, use a boost converter.

5.5 Current Consumption Summary (CC3220R, CC3220S)

T_A = 25°C, V_{BAT} = 3.6 V

PARAMETER		TEST CONDITIONS(1) (2)			MIN	TYP	MAX	UNIT
MCU ACTIVE	NWP ACTIVE	TX	1 DSSS	TX power level = 0		272		mA
				TX power level = 4		190		
			6 OFDM	TX power level = 0		248		
				TX power level = 4		182		
			54 OFDM	TX power level = 0		223		
				TX power level = 4		160		
		RX	1 DSSS			59		
			54 OFDM			59		
	NWP idle connected(3)					15.3		
MCU SLEEP	NWP ACTIVE	TX	1 DSSS	TX power level = 0		269		mA
				TX power level = 4		187		
			6 OFDM	TX power level = 0		245		
				TX power level = 4		179		
			54 OFDM	TX power level = 0		220		
				TX power level = 4		157		
		RX	1 DSSS			56		
			54 OFDM			56		
	NWP idle connected(3)					12.2		

(1) TX power level = 0 implies maximum power (see Figure 5-1, Figure 5-2, and Figure 5-3). TX power level = 4 implies output power backed off approximately 4 dB.
(2) The CC3220x system is a constant power-source system. The active current numbers scale based on the V_{BAT} voltage supplied.
(3) DTIM = 1

Current Consumption Summary (CC3220R, CC3220S) *(continued)*

T_A = 25°C, V_{BAT} = 3.6 V

PARAMETER		TEST CONDITIONS (1) (2)			MIN	TYP	MAX	UNIT
MCU LPDS	NWP ACTIVE	TX	1 DSSS	TX power level = 0		266		mA
				TX power level = 4		184		
			6 OFDM	TX power level = 0		242		
				TX power level = 4		176		
			54 OFDM	TX power level = 0		217		
				TX power level = 4		154		
		RX	1 DSSS			53		
			54 OFDM			53		
	NWP LPDS (4)		120 µA at 64KB 135 µA at 256KB			135		µA
	NWP idle connected (3)					710		µA
MCU SHUTDOWN	MCU shutdown					1		µA
MCU HIBERNATE	MCU hibernate					4.5		µA
Peak calibration current (5)		V_{BAT} = 3.6 V				420		mA
		V_{BAT} = 3.3 V				450		
		V_{BAT} = 2.1 V				670		
		V_{BAT} = 1.85 V				700		

(4) LPDS current does not include the external serial Flash. The LPDS number of reported is with retention of 256KB of MCU SRAM. The CC3220x device can be configured to retain 0KB, 64KB, 128KB, 192KB, or 256KB of SRAM in LPDS. Each 64-KB block of MCU retained SRAM increases LPDS current by 4 µA.

(5) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. In default mode, calibration is performed sparingly, and typically occurs when re-enabling the NWP and when the temperature has changed by more than 20°C. There are two additional calibration modes that may be used to reduced or completely eliminate the calibration event. For further details, see *CC3120, CC3220 SimpleLink™ Wi-Fi® and IoT Network Processor Programmer's Guide*.

5.6 Current Consumption Summary (CC3220SF)

T_A = 25°C, V_{BAT} = 3.6 V

PARAMETER		TEST CONDITIONS(1) (2)			MIN	TYP	MAX	UNIT
MCU ACTIVE	NWP ACTIVE	TX	1 DSSS	TX power level = maximum		286		mA
				TX power level = maximum – 4		202		
			6 OFDM	TX power level = maximum		255		
				TX power level = maximum – 4		192		
			54 OFDM	TX power level = maximum		232		
				TX power level = maximum – 4		174		
		RX	1 DSSS			74		
			54 OFDM			74		
	NWP idle connected(3)					25.2		
MCU SLEEP	NWP ACTIVE	TX	1 DSSS	TX power level = maximum		282		mA
				TX power level = maximum – 4		198		
			6 OFDM	TX power level = maximum		251		
				TX power level = maximum – 4		188		
			54 OFDM	TX power level = maximum		228		
				TX power level = maximum – 4		170		
		RX	1 DSSS			70		
			54 OFDM			70		
	NWP idle connected(3)					21.2		
MCU LPDS	NWP active	TX	1 DSSS	TX power level = 0		266		mA
				TX power level = 4		184		
			6 OFDM	TX power level = 0		242		
				TX power level = 4		176		
			54 OFDM	TX power level = 0		217		
				TX power level = 4		154		
		RX	1 DSSS			53		
			54 OFDM			53		
	NWP LPDS(4)		120 µA at 64KB 135 µA at 256KB			135		µA
	NWP idle connected(3)					710		
MCU SHUTDOWN	MCU shutdown					1		
MCU HIBERNATE	MCU hibernate					4.5		
Peak calibration current(5)		V_{BAT} = 3.6 V				420		mA
		V_{BAT} = 3.3 V				450		
		V_{BAT} = 2.1 V				670		
		V_{BAT} = 1.85 V				700		

(1) TX power level = 0 implies maximum power (see Figure 5-1, Figure 5-2, and Figure 5-3). TX power level = 4 implies output power backed off approximately 4 dB.
(2) The CC3220x system is a constant power-source system. The active current numbers scale based on the V_{BAT} voltage supplied.
(3) DTIM = 1
(4) LPDS current does not include the external serial flash. The LPDS number of reported is with retention of 256KB of MCU SRAM. The CC3220x device can be configured to retain 0KB, 64KB, 128KB, 192KB, or 256KB of SRAM in LPDS. Each 64-KB block of MCU retained SRAM increases LPDS current by 4 µA.
(5) The complete calibration can take up to 17 mJ of energy from the battery over a period of 24 ms. Calibration is performed sparingly, typically when coming out of HIBERNATE and only if temperature has changed by more than 20°C. The calibration event can be controlled by a configuration file in the serial Flash..

5.7 TX Power and IBAT versus TX Power Level Settings

Figure 5-1, Figure 5-2, and Figure 5-3 show TX Power and IBAT versus TX power level settings for the CC3220R and CC3220S devices at modulations of 1 DSSS, 6 OFDM, and 54 OFDM, respectively. For the CC3220SF device, the IBAT current has an increase of approximately 10 mA to 15 mA depending on the transmitted rate. The TX power level will remain the same.

In Figure 5-1, the area enclosed in the circle represents a significant reduction in current during transition from TX power level 3 to level 4. In the case of lower range requirements (14-dBm output power), TI recommends using TX power level 4 to reduce the current.

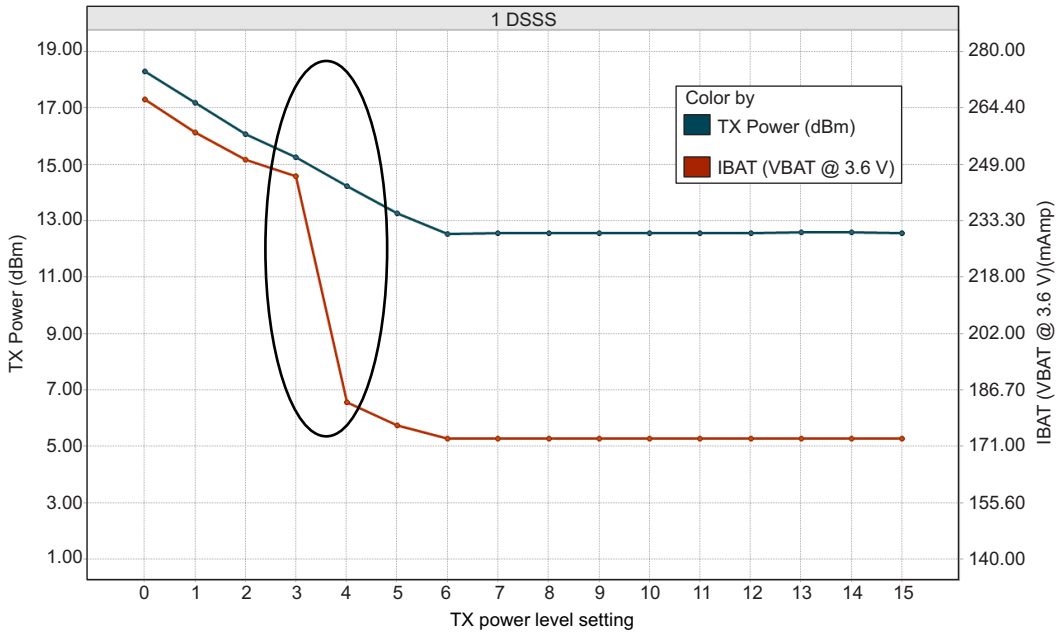


Figure 5-1. TX Power and IBAT vs TX Power Level Settings (1 DSSS)

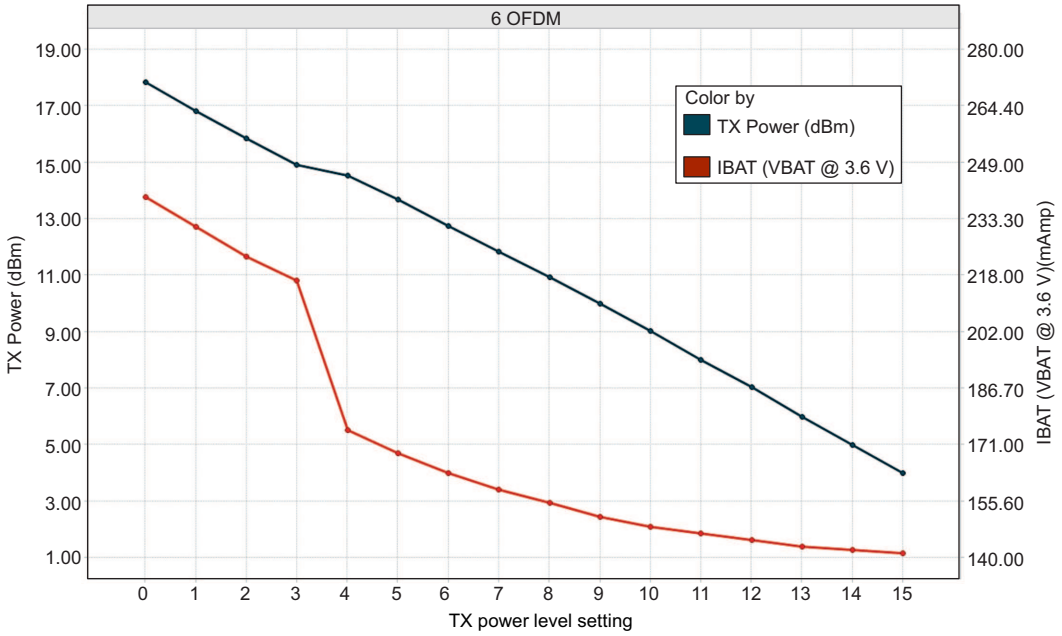


Figure 5-2. TX Power and IBAT vs TX Power Level Settings (6 OFDM)

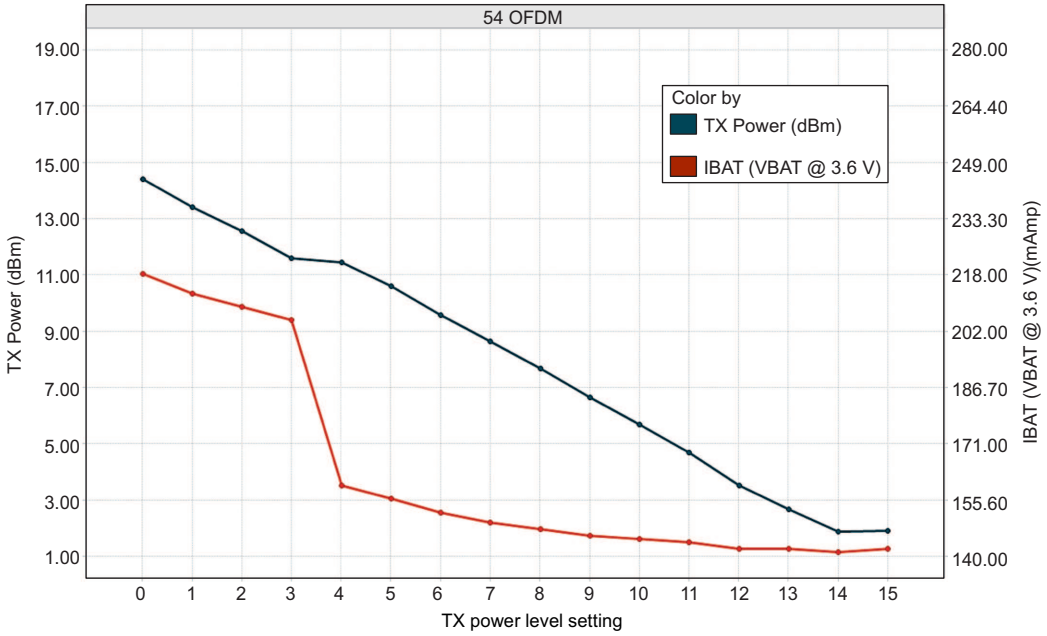


Figure 5-3. TX Power and IBAT vs TX Power Level Settings (54 OFDM)

5.8 Brownout and Blackout Conditions

The device enters a brownout condition when the input voltage drops below $V_{brownout}$ (see Figure 5-4 and Figure 5-5). This condition must be considered during design of the power supply routing, especially when operating from a battery. High-current operations, such as a TX packet or any external activity (not necessarily related directly to networking) can cause a drop in the supply voltage, potentially triggering a brownout condition. The resistance includes the internal resistance of the battery, the contact resistance of the battery holder (four contacts for 2× AA batteries), and the wiring and PCB routing resistance.

NOTE

When the device is in HIBERNATE state, brownout is not detected. Only blackout is in effect during HIBERNATE state.

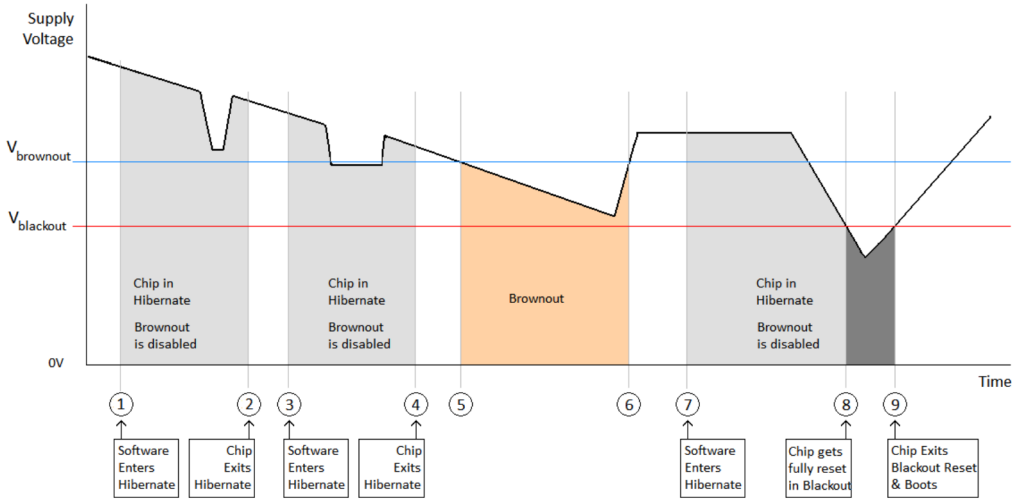


Figure 5-4. Brownout and Blackout Levels (1 of 2)

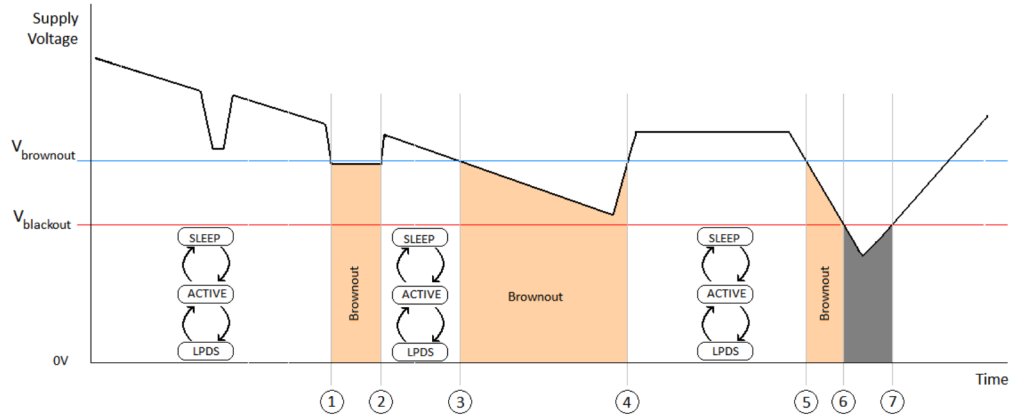


Figure 5-5. Brownout and Blackout Levels (2 of 2)

In the brownout condition, all sections of the device (including the 32-kHz RTC) shut down except for the Hibernate module, which remains on. The current in this state can reach approximately 400 µA. The blackout condition is equivalent to a hardware reset event in which all states within the device are lost.

Table 5-1 lists the brownout and blackout voltage levels.

Table 5-1. Brownout and Blackout Voltage Levels

CONDITION	VOLTAGE LEVEL	UNIT
$V_{brownout}$	2.1	V
$V_{blackout}$	1.67	V

5.9 Electrical Characteristics (3.3 V, 25°C)

GPIO Pins Except 29, 30, 50, 52, and 53 (25°C)(1)							
PARAMETER			TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{IN}	Pin capacitance				4		pF
V_{IH}	High-level input voltage			0.65 × V_{DD}		V_{DD} + 0.5 V	V
V_{IL}	Low-level input voltage			–0.5		0.35 × V_{DD}	V
I_{IH}	High-level input current				5		nA
I_{IL}	Low-level input current				5		nA
V_{OH}	High-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.8	V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V_{DD} < 2.4 V			V_{DD} × 0.75	
			IL = 2 mA; configured I/O drive strength = 2 mA; V_{DD} = 1.85 V			V_{DD} × 0.7	
V_{OL}	Low-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V_{DD} < 2.4 V	V_{DD} × 0.25			
			IL = 2 mA; configured I/O drive strength = 2 mA; V_{DD} = 1.85 V	V_{DD} × 0.35			
I_{OH}	High-level source current	2-mA drive		2			mA
		4-mA drive		4			
		6-mA drive		6			

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and reduces any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.

Electrical Characteristics (3.3 V, 25°C) *(continued)*

PARAMETER			TEST CONDITIONS	MIN	NOM	MAX	UNIT
GPIO Pins Except 29, 30, 50, 52, and 53 (25°C)(1)							
I_{OL}	Low-level sink current	2-mA drive		2			mA
		4-mA drive		4			
		6-mA drive		6			
GPIO Pins 29, 30, 50, 52, and 53 (25°C)(1)							
C_{IN}	Pin capacitance				7		pF
V_{IH}	High-level input voltage			0.65 × V_{DD}		V_{DD} + 0.5 V	V
V_{IL}	Low-level input voltage			–0.5		0.35 × V_{DD}	V
I_{IH}	High-level input current				50		nA
I_{IL}	Low-level input current				50		nA
V_{OH}	High-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.8	V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V_{DD} < 2.4 V			V_{DD} × 0.75	
			IL = 2 mA; configured I/O drive strength = 2 mA; V_{DD} = 1.85 V			V_{DD} × 0.7	
V_{OL}	Low-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V_{DD} < 2.4 V	V_{DD} × 0.25			
			IL = 2 mA; configured I/O drive strength = 2 mA; V_{DD} = 1.85 V	V_{DD} × 0.35			
I_{OH}	High-level source current, V_{OH} = 2.4	2-mA drive		1.5			mA
		4-mA drive		2.5			
		6-mA drive		3.5			
I_{OL}	Low-level sink current	2-mA drive		1.5			mA
		4-mA drive		2.5			
		6-mA drive		3.5			
V_{IL}	nRESET(2)				0.6		V
Pin Internal Pullup and Pulldown (25°C)(1)							
I_{OH}	Pullup current, V_{OH} = 2.4 (V_{DD} = 3.0 V)			5		10	µA
I_{OL}	Pulldown current, V_{OL} = 0.4 (V_{DD} = 3.0 V)			5			µA

(2) The nRESET pin must be held below 0.6 V for the device to register a reset.

5.10 WLAN Receiver Characteristics

T_A = 25°C, V_{BAT} = 2.1 V to 3.6 V. Parameters are measured at the SoC pin on channel 6 (2437 MHz).

PARAMETER	TEST CONDITIONS (Mbps)	MIN	TYP(1)	MAX	UNIT
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates) (10% PER)(2)	1 DSSS		–96.0		dBm
	2 DSSS		–94.0		
	11 CCK		–88.0		
	6 OFDM		–90.5		
	9 OFDM		–90.0		
	18 OFDM		–86.5		
	36 OFDM		–80.5		
	54 OFDM		–74.5		
	MCS7 (GF)(3)		–71.5		
	MCS7 (MM)(3)		–70.5		
Maximum input level (10% PER)	802.11b		–4.0		dBm
	802.11g		–10.0		

(1) In preregulated 1.85-V mode, RX sensitivity is 0.25- to 1-dB lower.
(2) Sensitivity is 1-dB worse on channel 13 (2472 MHz).
(3) Sensitivity for mixed mode is 1-dB worse.

5.11 WLAN Transmitter Characteristics

T_A = 25°C, V_{BAT} = 2.1 V to 3.6 V. Parameters measured at SoC pin on channel 6 (2437 MHz).(1)(2)(3)

PARAMETER	TEST CONDITIONS(3)	MIN	TYP	MAX	UNIT
Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM	1 DSSS		18.0		dBm
	2 DSSS		18.0		
	11 CCK		18.3		
	6 OFDM		17.3		
	9 OFDM		17.3		
	18 OFDM		17.0		
	36 OFDM		16.0		
	54 OFDM		14.5		
	MCS7 (MM)		13.0		
Transmit center frequency accuracy		–25		25	ppm

(1) The edge channels (2412 and 2472 MHz) have reduced TX power to meet FCC emission limits.
(2) Power of 802.11b rates are reduced to meet ETSI requirements.
(3) In preregulated 1.85-V mode, maximum TX power is 0.25- to 0.75-dB lower for modulations higher than 18 OFDM.

5.12 WLAN Filter Requirements

The device requires an external band-pass filter to meet the various emission standards, including FCC. Table 5-2 presents the attenuation requirements for the band-pass filter. TI recommends using the same filter used in the reference design to ease the process of certification.

Table 5-2. WLAN Filter Requirements

PARAMETER	FREQUENCY (MHz)	MIN	TYP	MAX	UNIT
Return loss	2412 to 2484	10			dB
Insertion loss(1)	2412 to 2484		1	1.5	dB
Attenuation	800 to 830	30	45		dB
	1600 to 1670	20	25		
	3200 to 3300	30	48		
	4000 to 4150	45	50		
	4800 to 5000	20	25		
	5600 to 5800	20	25		
	6400 to 6600	20	35		
	7200 to 7500	35	45		
	7500 to 10000	20	25		
Reference impendence	2412 to 2484		50		Ω
Filter type	Bandpass				

(1) Insertion loss directly impacts output power and sensitivity. At customer discretion, insertion loss can be relaxed to meet attenuation requirements.

5.13 Thermal Resistance Characteristics

5.14 Thermal Resistance Characteristics for RGK Package

AIR FLOW				
PARAMETER	0 lfm (C/W)	150 lfm (C/W)	250 lfm (C/W)	500 lfm (C/W)
θ_{ja}	23	14.6	12.4	10.8
Ψ_{jt}	0.2	0.2	0.3	0.1
Ψ_{jb}	2.3	2.3	2.2	2.4
θ_{jc}	6.3			
θ_{jb}	2.4			

5.15 Timing and Switching Characteristics

5.15.1 Power Supply Sequencing

For proper operation of the CC3220x device, perform the recommended power-up sequencing as follows:

1. Tie V_{BAT} (pins 37, 39, 44) and V_{IO} (pins 54 and 10) together on the board.
2. Hold the RESET pin low while the supplies are ramping up. TI recommends using a simple RC circuit (100 K ||, 1 µF, RC = 100 ms).
3. For an external RTC, ensure that the clock is stable before RESET is deasserted (high).

For timing diagrams, see Section 5.15.3.

5.15.2 Device Reset

When a device restart is required, the user may issue a negative pulse to the nRESET pin. The user must follow one of the two alternatives to ensure the reset is properly applied:

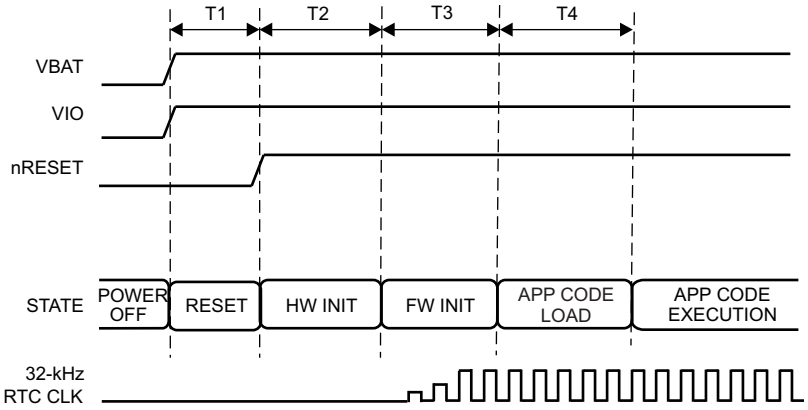
- A negative reset pulse (on pin 32) of at least 200-ms duration
- If the above cannot be guaranteed, a pull-down resistor of 2 MΩ should be connected to pin 52 (RTC_XTAL_N). If implemented, a shorter pulse of at least 100 µs can be used.

To ensure a proper reset sequence, the user has to call the sl_stop function prior to toggling the reset. It is preferable to use software reset instead of an external trigger when a reset is required.

5.15.3 Reset Timing

5.15.3.1 nRESET (32-kHz Crystal)

Figure 5-6 shows the reset timing diagram for the 32-kHz crystal first-time power-up and reset removal.



NOTE: T1 should be ≥200 ms without a pulldown resistor on the XTAL_N pin or T1 should be ≥100 µs if there is 2-MΩ pulldown resistor on the XTAL_N pin.

Figure 5-6. First-Time Power-Up and Reset Removal Timing Diagram (32-kHz Crystal)

Table 5-3 describes the timing requirements for the 32-kHz clock crystal first-time power-up and reset removal.

Table 5-3. First-Time Power-Up and Reset Removal Timing Requirements (32-kHz Crystal)

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T1	Supply settling time	Depends on application board power supply, decoupling capacitor, and so on		3		ms
T2	Hardware wake-up time			25		ms
T3	Time taken by ROM firmware to initialize hardware	Includes 32.768-kHz XOSC settling time		1.1		s
T4	App code load time for CC3220R and CC3220S	CC3220R		Image size (KB) × 0.75 ms		
		CC3220S		Image size (KB) × 1.7 ms		
	App code integrity check time for CC3220SF	CC3220SF		Image size (KB) × 0.06 ms		

5.15.3.2 nRESET (External 32-kHz)

Figure 5-7 shows the reset timing diagram for the external 32-kHz first-time power-up and reset removal.

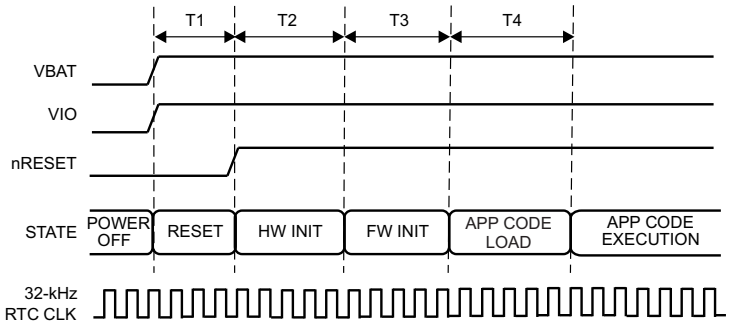


Figure 5-7. First-Time Power-Up and Reset Removal Timing Diagram (External 32-kHz)

Table 5-4 describes the timing requirements for the external 32-kHz clock first-time power-up and reset removal.

Table 5-4. First-Time Power-Up and Reset Removal Timing Requirements (External 32-kHz)

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T1	Supply settling time	Depends on application board power supply, decoupling capacitor, and so on		3		ms
T2	Hardware wake-up time			25		ms
T3	Time taken by ROM firmware to initialize hardware	CC3220R		5		ms
		CC3220S		10.3		
		CC3220SF		17.3		
T4	App code load time for CC3220R and CC3220S	CC3220R		Image size (KB) × 0.75 ms		
		CC3220S		Image size (KB) × 1.7 ms		
	App code integrity check time for CC3220SF	CC3220SF		Image size (KB) × 0.06 ms		

5.15.4 Wakeup From HIBERNATE Mode

Figure 5-8 shows the timing diagram for wakeup from HIBERNATE mode.

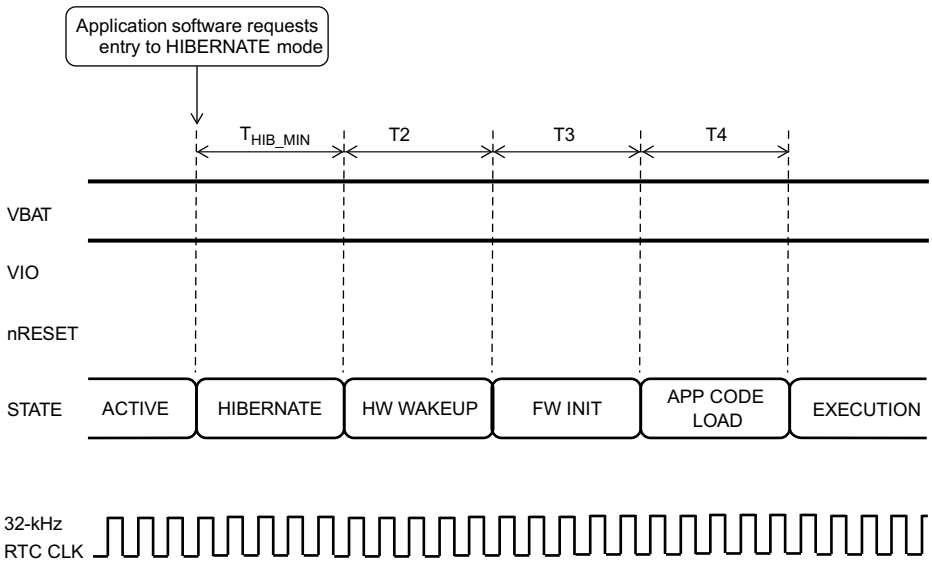


Figure 5-8. Wakeup From HIBERNATE Timing Diagram

NOTE

The 32.768-kHz crystal is kept enabled by default when the chip goes into HIBERNATE mode.

5.15.5 Clock Specifications

The CC3220x device requires two separate clocks for its operation:

- A slow clock running at 32.768 kHz is used for the RTC.
- A fast clock running at 40 MHz is used by the device for the internal processor and the WLAN subsystem.

The device features internal oscillators that enable the use of less-expensive crystals rather than dedicated TCXOs for these clocks. The RTC can also be fed externally to provide reuse of an existing clock on the system and to reduce overall cost.

5.15.5.1 Slow Clock Using Internal Oscillator

The RTC crystal connected on the device supplies the free-running slow clock. The accuracy of the slow clock frequency must be 32.768 kHz ±150 ppm. In this mode of operation, the crystal is tied between RTC_XTAL_P (pin 51) and RTC_XTAL_N (pin 52) with a suitable load capacitance to meet the ppm requirement.

Figure 5-9 shows the crystal connections for the slow clock.

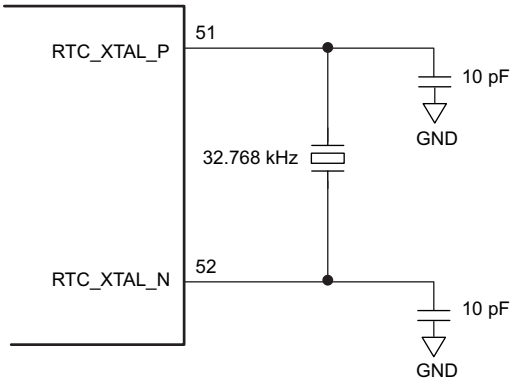


Figure 5-9. RTC Crystal Connections

Table 5-5 lists the RTC crystal requirements.

Table 5-5. RTC Crystal Requirements

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			32.768		kHz
Frequency accuracy	Initial plus temperature plus aging			±150	ppm
Crystal ESR	32.768 kHz			70	kΩ

5.15.5.2 Slow Clock Using an External Clock

When an RTC oscillator is present in the system, the CC3220x device can accept this clock directly as an input. The clock is fed on the RTC_XTAL_P line, and the RTC_XTAL_N line is held to V_{IO}. The clock must be a CMOS-level clock compatible with V_{IO} fed to the device.

Figure 5-10 shows the external RTC input connection.

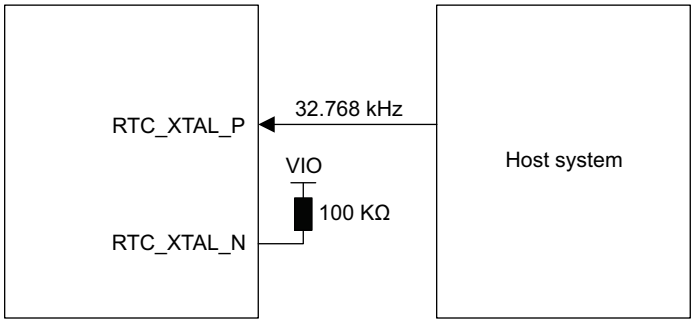


Figure 5-10. External RTC Input

Table 5-6 lists the external RTC digital clock requirements.

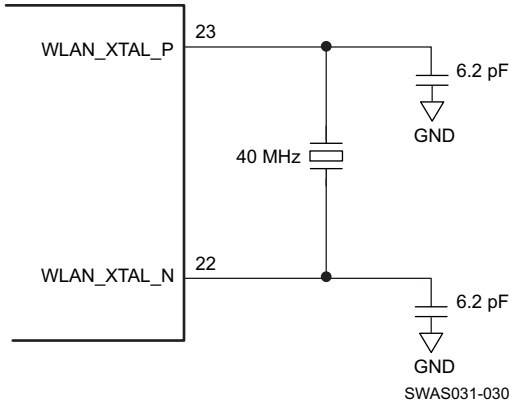
Table 5-6. External RTC Digital Clock Requirements

CHARACTERISTICS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency			32768		Hz
	Frequency accuracy (Initial plus temperature plus aging)			±150		ppm
t_r, t_f	Input transition time t_r, t_f (10% to 90%)				100	ns
	Frequency input duty cycle		20%	50%	80%	
V_{ih}	Slow clock input voltage limits	Square wave, DC coupled	0.65 × V_{IO}		V_{IO}	V
V_{il}			0		0.35 × V_{IO}	V_{peak}
	Input impedance		1			MΩ
					5	pF

5.15.5.3 Fast Clock (F_{ref}) Using an External Crystal

The CC3220x device also incorporates an internal crystal oscillator to support a crystal-based fast clock. The crystal is fed directly between WLAN_XTAL_P (pin 23) and WLAN_XTAL_N (pin 22) with suitable loading capacitors.

Figure 5-11 shows the crystal connections for the fast clock.



NOTE: The crystal capacitance must be tuned to ensure that the PPM requirement is met. See *CC31xx & CC32xx Frequency Tuning* for information on frequency tuning.

Figure 5-11. Fast Clock Crystal Connections

Table 5-7 lists the WLAN fast-clock crystal requirements.

Table 5-7. WLAN Fast-Clock Crystal Requirements

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			40		MHz
Frequency accuracy	Initial plus temperature plus aging			±25	ppm
Crystal ESR	40 MHz			60	Ω

5.15.5.4 Fast Clock (F_{ref}) Using an External Oscillator

The CC3220x device can accept an external TCXO/XO for the 40-MHz clock. In this mode of operation, the clock is connected to WLAN_XTAL_P (pin 23). WLAN_XTAL_N (pin 22) is connected to GND. The external TCXO/XO can be enabled by TCXO_EN (pin 21) from the device to optimize the power consumption of the system.

If the TCXO does not have an enable input, an external LDO with an enable function can be used. Using the LDO improves noise on the TCXO power supply.

Figure 5-12 shows the connection.

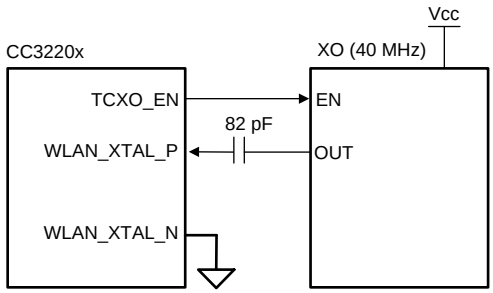


Figure 5-12. External TCXO Input

Table 5-8 lists the external F_{ref} clock requirements.

Table 5-8. External F_{ref} Clock Requirements (–40°C to +85°C)

CHARACTERISTICS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency				40.00		MHz
	Frequency accuracy (Initial plus temperature plus aging)					±25	ppm
	Frequency input duty cycle			45%	50%	55%	
V_{pp}	Clock voltage limits		Sine or clipped sine wave, AC coupled	0.7		1.2	V_{pp}
	Phase noise at 40 MHz		at 1 kHz			–125	dBc/Hz
			at 10 kHz			–138.5	
			at 100 kHz			–143	
	Input impedance	Resistance		12			kΩ
		Capacitance				7	pF

5.15.6 Peripherals Timing

This section describes the peripherals that are supported by the CC3220x device:

- SPI
- I2S
- GPIOs
- I^2C
- IEEE 1149.1 JTAG
- ADC
- Camera parallel port
- UART
- SD Host
- Timers

5.15.6.1 SPI

5.15.6.1.1 SPI Master

The CC3220x microcontroller includes one SPI module, which can be configured as a master or slave device. The SPI includes a serial clock with programmable frequency, polarity, and phase; a programmable timing control between chip select and external clock generation; and a programmable delay before the first SPI word is transmitted. Slave mode does not include a dead cycle between two successive words.

Figure 5-13 shows the timing diagram for the SPI master.

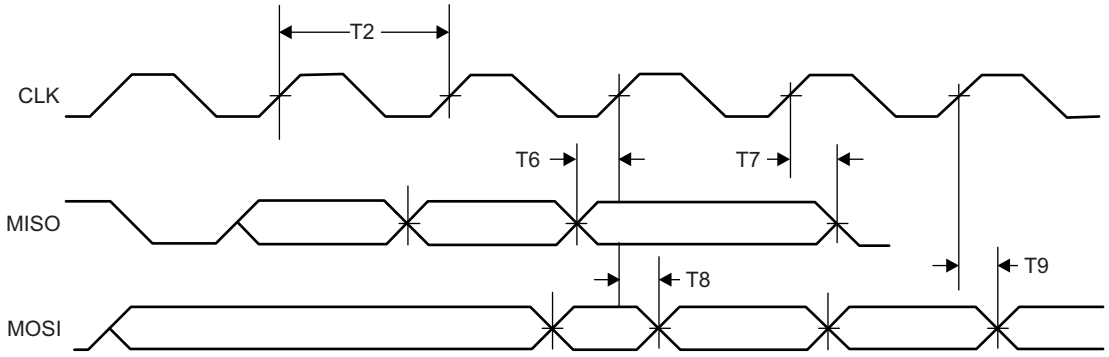


Figure 5-13. SPI Master Timing Diagram

Table 5-9 lists the timing parameters for the SPI master.

Table 5-9. SPI Master Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
	$F^{(1)}$	Clock frequency		20	MHz
T2	$T_{clk}^{(1)}$	Clock period	50		ns
	$D^{(1)}$	Duty cycle	45%	55%	
T6	$t_{IS}^{(1)}$	RX data setup time	1		ns
T7	$t_{IH}^{(1)}$	RX data hold time	2		ns
T8	$t_{OD}^{(1)}$	TX data output delay		8.5	ns
T9	$t_{OH}^{(1)}$	TX data hold time		8	ns

(1) Timing parameter assumes a maximum load of 20 pF.

5.15.6.1.2 SPI Slave

Figure 5-14 shows the timing diagram for the SPI slave.

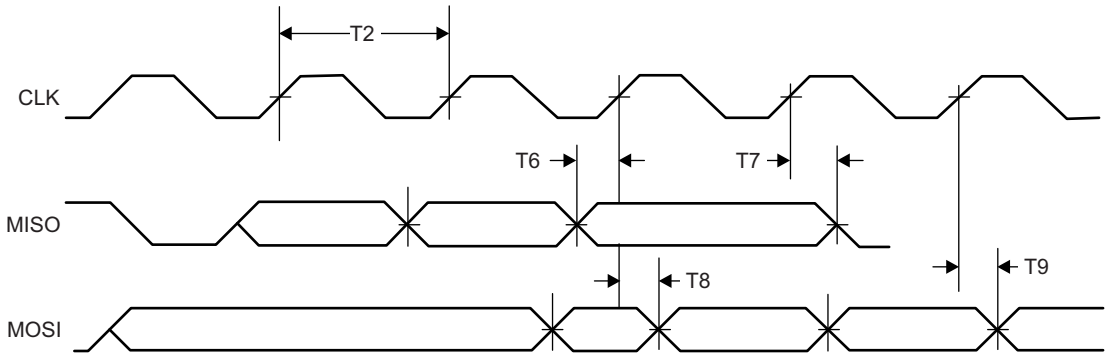


Figure 5-14. SPI Slave Timing Diagram

Table 5-10 lists the timing parameters for the SPI slave.

Table 5-10. SPI Slave Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
	F(1)	Clock frequency at V_{BAT} = 3.3 V		20	MHz
		Clock frequency at V_{BAT} ≤ 2.1 V		12	
T2	T_{clk}(1)	Clock period	50		ns
	D(1)	Duty cycle	45%	55%	
T6	t_{IS}(1)	RX data setup time	4		ns
T7	t_{IH}(1)	RX data hold time	4		ns
T8	t_{OD}(1)	TX data output delay		20	ns
T9	t_{OH}(1)	TX data hold time		24	ns

(1) Timing parameter assumes a maximum load of 20 pF at 3.3 V.

5.15.6.2 I2S

The McASP interface functions as a general-purpose audio serial port optimized for multichannel audio applications and supports transfer of two stereo channels over two data pins. The McASP consists of transmit and receive sections that operate synchronously and have programmable clock and frame-sync polarity. A fractional divider is available for bit-clock generation.

5.15.6.2.1 I2S Transmit Mode

Figure 5-15 shows the timing diagram for the I2S transmit mode.

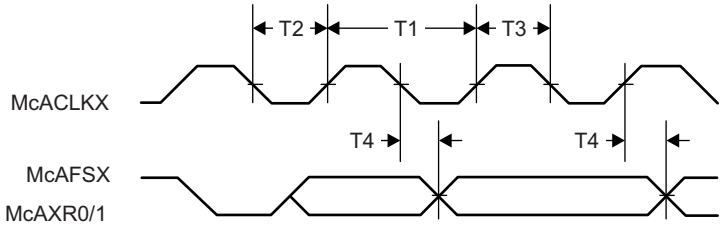


Figure 5-15. I2S Transmit Mode Timing Diagram

Table 5-11 lists the timing parameters for the I2S transmit mode.

Table 5-11. I2S Transmit Mode Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
T1	f_{clk} (1)	Clock frequency		9.216	MHz
T2	t^{LP} (1)	Clock low period		1/2 fclk	ns
T3	t_{HT} (1)	Clock high period		1/2 fclk	ns
T4	t_{OH} (1)	TX data hold time		22	ns

(1) Timing parameter assumes a maximum load of 20 pF.

5.15.6.2.2 I2S Receive Mode

Figure 5-16 shows the timing diagram for the I2S receive mode.

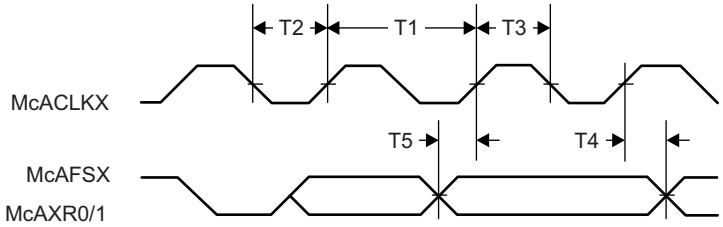


Figure 5-16. I2S Receive Mode Timing Diagram

Table 5-12 lists the timing parameters for the I2S receive mode.

Table 5-12. I2S Receive Mode Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
T1	f_{clk} (1)	Clock frequency		9.216	MHz
T2	t^{LP} (1)	Clock low period		1/2 f_{clk}	ns
T3	t_{HT} (1)	Clock high period		1/2 f_{clk}	ns
T4	t_{OH} (1)	RX data hold time		0	ns
T5	t_{OS} (1)	RX data setup time		15	ns

(1) Timing parameter assumes a maximum load of 20 pF.

5.15.6.3 GPIOs

All digital pins of the device can be used as general-purpose input/output (GPIO) pins. The GPIO module consists of four GPIO blocks, each of which provides eight GPIOs. The GPIO module supports 24 programmable GPIO pins, depending on the peripheral used. Each GPIO has configurable pullup and pulldown strength (weak 10 µA), configurable drive strength (2, 4, and 6 mA), and open-drain enable.

Figure 5-17 shows the GPIO timing diagram.

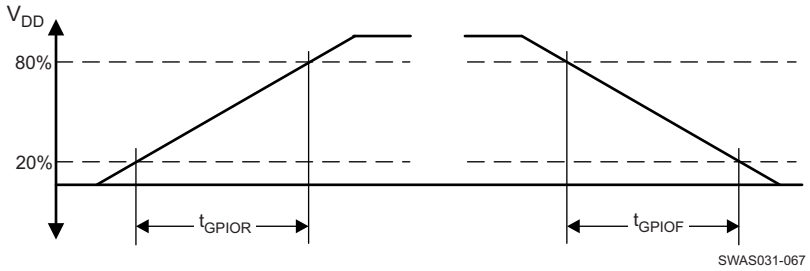


Figure 5-17. GPIO Timing Diagram

5.15.6.3.1 GPIO Output Transition Time Parameters (V_{supply} = 3.3 V)

Table 5-13 lists the GPIO output transition times for V_{supply} = 3.3 V.

Table 5-13. GPIO Output Transition Times (V_{supply} = 3.3 V) (1) (2)

DRIVE STRENGTH (mA)	DRIVE STRENGTH CONTROL BITS	t_r			t_f			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
2	2MA_EN=1 4MA_EN=0	8.0	9.3	10.7	8.2	9.5	11.0	ns
4	2MA_EN=0 4MA_EN=1	6.6	7.1	7.6	4.7	5.2	5.8	ns
6	2MA_EN=1 4MA_EN=1	3.2	3.5	3.7	2.3	2.6	2.9	ns

(1) V_{supply} = 3.3 V, T = 25°C, total pin load = 30 pF
(2) The transition data applies to the pins except the multiplexed analog-digital pins 29, 30, 45, 50, 52, and 53.

5.15.6.3.2 GPIO Output Transition Time Parameters (V_{supply} = 1.85 V)

Table 5-14 lists the GPIO output transition times for V_{supply} = 1.8 V.

Table 5-14. GPIO Output Transition Times (V_{supply} = 1.85 V)(1)(2)

DRIVE STRENGTH (mA)	DRIVE STRENGTH CONTROL BITS	t_r			t_f			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
2	2MA_EN=1	11.7	13.9	16.3	11.5	13.9	16.7	ns
	4MA_EN=0							
4	2MA_EN=0	13.7	15.6	18.0	9.9	11.6	13.6	ns
	4MA_EN=1							
6	2MA_EN=1	5.5	6.4	7.4	3.8	4.7	5.8	ns
	4MA_EN=1							

(1) V_{supply} = 1.8 V, T = 25°C, total pin load = 30 pF
(2) The transition data applies to the pins other than the multiplexed analog-digital pins 29, 30, 45, 50, 52, and 53.

5.15.6.3.3 GPIO Input Transition Time Parameters

Table 5-15 lists the input transition time parameters.

Table 5-15. GPIO Input Transition Time Parameters'

		MIN	MAX	UNIT
t_r	Input transition time (t_r, t_f), 10% to 90%	1	3	ns
t_f		1	3	ns

5.15.6.4 I²C

The CC3220x microcontroller includes one I2C module operating with standard (100 kbps) or fast (400 kbps) transmission speeds.

Figure 5-18 shows the I²C timing diagram.

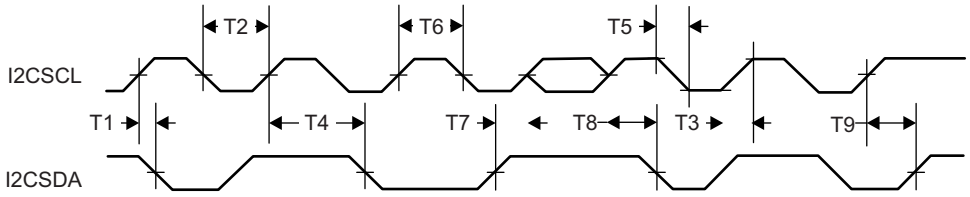


Figure 5-18. I²C Timing Diagram

Table 5-16 lists the I²C timing parameters.

Table 5-16. I²C Timing Parameters(1)

PARAMETER NUMBER			MIN	MAX	UNIT
T2	t_{LP}	Clock low period	See (2)		System clock
T3	t_{SRT}	SCL/SDA rise time		See (3)	ns
T4	t_{DH}	Data hold time	NA		
T5	t_{SFT}	SCL/SDA fall time	3		ns
T6	t_{HT}	Clock high time	See (2)		System clock
T7	t_{DS}	Data setup time	tLP/2		System clock
T8	t_{SCSR}	Start condition setup time	36		System clock
T9	t_{SCS}	Stop condition setup time	24		System clock

(1) All timing is with 6-mA drive and 20-pF load.
(2) This value depends on the value programmed in the clock period register of I²C. Maximum output frequency is the result of the minimal value programmed in this register.
(3) Because I²C is an open-drain interface, the controller can drive logic 0 only. Logic is the result of external pullup. Rise time depends on the value of the external signal capacitance and external pullup register.

5.15.6.5 IEEE 1149.1 JTAG

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. For detailed information on the operation of the JTAG port and TAP controller, see the IEEE Standard 1149.1,*Test Access Port and Boundary-Scan Architecture*.

Figure 5-19 shows the JTAG timing diagram.

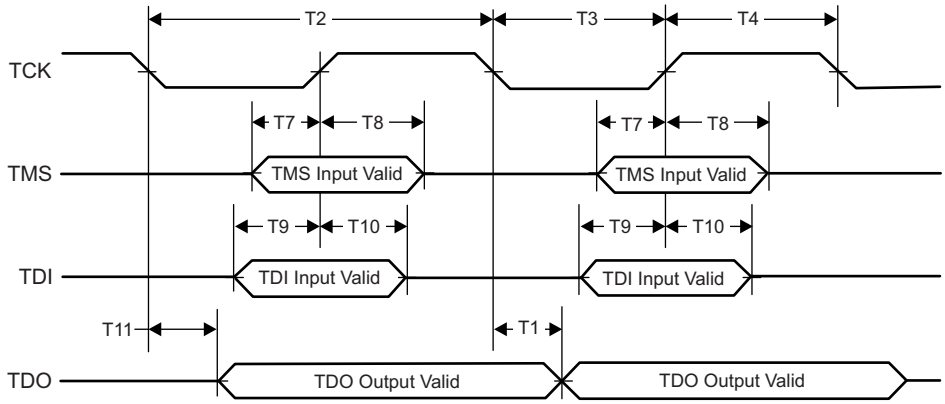


Figure 5-19. JTAG Timing Diagram

Table 5-17 lists the JTAG timing parameters.

Table 5-17. JTAG Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
T1	f_{TCK}	Clock frequency		15	MHz
T2	t_{TCK}	Clock period		$1 / f_{TCK}$	ns
T3	t_{CL}	Clock low period		$t_{TCK} / 2$	ns
T4	t_{CH}	Clock high period		$t_{TCK} / 2$	ns
T7	t_{TMS_SU}	TMS setup time	1		ns
T8	t_{TMS_HO}	TMS hold time	16		ns
T9	t_{TDI_SU}	TDI setup time	1		ns
T10	t_{TDI_HO}	TDI hold time	16		ns
T11	t_{TDO_HO}	TDO hold time		15	ns

5.15.6.6 ADC

Figure 5-20 shows the ADC clock timing diagram.

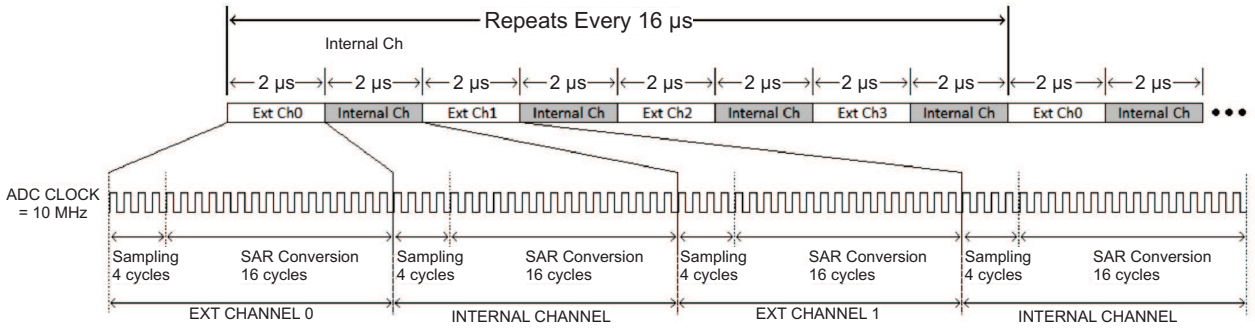


Figure 5-20. ADC Clock Timing Diagram

Table 5-18 lists the ADC electrical specifications. See *CC32xx ADC Appnote* for further information on using the ADC and for application-specific examples.

Table 5-18. ADC Electrical Specifications

PARAMETER	DESCRIPTION	TEST CONDITIONS AND ASSUMPTIONS	MIN	TYP	MAX	UNIT
Nbits	Number of bits			12		Bits
INL	Integral nonlinearity	Worst-case deviation from histogram method over full scale (not including first and last three LSB levels)	–2.5		2.5	LSB
DNL	Differential nonlinearity	Worst-case deviation of any step from ideal	–1		4	LSB
Input range			0		1.4	V
Driving source impedance					100	Ω
FCLK	Clock rate	Successive approximation input clock rate		10		MHz
Input capacitance				12		pF
Input impedance		ADC Pin 57		2.15		kΩ
		ADC Pin 58		0.7		
		ADC Pin 59		2.12		
		ADC Pin 60		1.17		
Number of channels				4		
F_{sample}	Sampling rate of each pin			62.5		KSPS
F_input_max	Maximum input signal frequency				31	kHz
SINAD	Signal-to-noise and distortion	Input frequency DC to 300 Hz and 1.4 V_{pp} sine wave input	55	60		dB
I_active	Active supply current	Average for analog-to-digital during conversion without reference current		1.5		mA
I_PD	Power-down supply current for core supply	Total for analog-to-digital when not active (this must be the SoC level test)		1		µA
Absolute offset error		FCLK = 10 MHz		±2		mV
Gain error				±2%		
V_{ref}	ADC reference voltage			1.467		V

5.15.6.7 Camera Parallel Port

The fast camera parallel port interfaces with a variety of external image sensors, stores the image data in a FIFO, and generates DMA requests. The camera parallel port supports 8 bits.

Figure 5-21 shows the timing diagram for the camera parallel port.

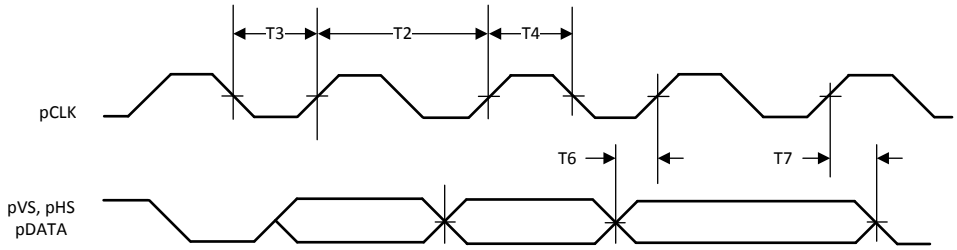


Figure 5-21. Camera Parallel Port Timing Diagram

Table 5-19 lists the timing parameters for the camera parallel port.

Table 5-19. Camera Parallel Port Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
	pCLK	Clock frequency		2	MHz
T2	T_{clk}	Clock period		1/pCLK	ns
T3	t_{LP}	Clock low period		$T_{clk}/2$	ns
T4	t_{HT}	Clock high period		$T_{clk}/2$	ns
T6	t_{IS}	RX data setup time		2	ns
T7	t_{IH}	RX data hold time		2	ns
	D	Duty cycle	45%	55%	

5.15.6.8 UART

The CC3220x device includes two UARTs with the following features:

- Programmable baud-rate generator allowing speeds up to 3 Mbps
- Separate 16-bit × 8-bit TX and RX FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including a 1-byte-deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- Generation and detection of line-breaks
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 data bits
  - Generation and detection of even, odd, stick, or no-parity bits
  - Generation of 1 or 2 stop-bits
- RTS and CTS hardware flow support
- Standard FIFO-level and end-of-transmission interrupts
- Efficient transfers using µDMA:
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level
- System clock is used to generate the baud clock.

5.15.6.9 SD Host

CC3220x provides an interface between a local host (LH), such as an MCU and an SD memory card, and handles SD transactions with minimal LH intervention.

The SD host does the following:

- Provides SD card access in 1-bit mode
- Deals with SD protocol at the transmission level
- Handles data packing
- Adds cyclic redundancy checks (CRC)
- Start and end bit
- Checks for syntactical correctness

The application interface sends every SD command and either polls for the status of the adapter or waits for an interrupt request. The result is then sent back to the application interface in case of exceptions or to warn of end-of-operation. The controller can be configured to generate DMA requests and work with minimum CPU intervention. Given the nature of integration of this peripheral on the CC3220x platform, TI recommends that developers use peripheral library APIs to control and operate the block. This section emphasizes understanding the SD host APIs provided in the peripheral library of the CC3220x Software Development Kit (SDK).

The SD Host features are as follows:

- Full compliance with SD command and response sets, as defined in the SD memory card
  - Specifications, v2.0
  - Includes high-capacity (size >2 GB) cards HC SD
- Flexible architecture, allowing support for new command structure.
- 1-bit transfer mode specifications for SD cards

- Built-in 1024-byte buffer for read or write
  - 512-byte buffer for both transmit and receive
  - Each buffer is 32-bits wide by 128-words deep
- 32-bit-wide access bus to maximize bus throughput
- Single interrupt line for multiple interrupt source events
- Two slave DMA channels (1 for TX, 1 for RX)
- Programmable clock generation
- Integrates an internal transceiver that allows a direct connection to the SD card without external transceiver
- Supports configurable busy and response timeout
- Support for a wide range of card clock frequency with odd and even clock ratio
- Maximum frequency supported is 24 MHz

5.15.6.10 Timers

Programmable timers can be used to count or time external events that drive the timer input pins. The CC3220x general-purpose timer module (GPTM) contains 16- or 32-bit GPTM blocks. Each 16- or 32-bit GPTM block provides two 16-bit timers or counters (referred to as Timer A and Timer B) that can be configured to operate independently as timers or event counters, or they can be concatenated to operate as one 32-bit timer. Timers can also be used to trigger µDMA transfers.

The GPTM contains four 16- or 32-bit GPTM blocks with the following functional options:

- Operating modes:
  - 16- or 32-bit programmable one-shot timer
  - 16- or 32-bit programmable periodic timer
  - 16-bit general-purpose timer with an 8-bit prescaler
  - 16-bit input-edge count- or time-capture modes with an 8-bit prescaler
  - 16-bit PWM mode with an 8-bit prescaler and software-programmable output inversion of the PWM signal
- Counts up or counts down
- Sixteen 16- or 32-bit capture compare pins (CCP)
- User-enabled stalling when the microcontroller asserts CPU Halt flag during debug
- Ability to determine the elapsed time between the assertion of the timer interrupt and entry into the interrupt service routine
- Efficient transfers using micro direct memory access controller (µDMA):
  - Dedicated channel for each timer
  - Burst request generated on timer interrupt
- Runs from system clock (80 MHz)

6 Detailed Description

The CC3220x wireless MCU family has a rich set of peripherals for diverse application requirements. This section briefly highlights the internal details of the CC3220x devices and offers suggestions for application configurations.

6.1 Arm® Cortex®-M4 Processor Core Subsystem

The high-performance Cortex-M4 processor provides a low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

- The Cortex-M4 core has low-latency interrupt processing with the following features:
  - A 32-bit Arm® Thumb® instruction set optimized for embedded applications
  - Handler and thread modes
  - Low-latency interrupt handling by automatic processor state saving and restoration during entry and exit
  - Support for ARMv6 unaligned accesses
- Nested vectored interrupt controller (NVIC) closely integrated with the processor core to achieve low-latency interrupt processing. The NVIC includes the following features:
  - Bits of priority configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping that enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tail-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
  - Processor state automatically saved on interrupt entry and restored on interrupt exit with no instruction overhead
  - Wake-up interrupt controller (WIC) providing ultra-low-power sleep mode support
- Bus interfaces:
  - Advanced high-performance bus (AHB-Lite) interfaces: system bus interfaces
  - Bit-band support for memory and select peripheral that includes atomic bit-band write and read operations
- Low-cost debug solution featuring:
  - Debug access to all memory and registers in the system, including access to memory-mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted
  - Serial wire debug port (SW-DP) or serial wire JTAG debug port (SWJ-DP) debug access
  - Flash patch and breakpoint (FPB) unit to implement breakpoints and code patches

6.2 Wi-Fi Network Processor Subsystem

The Wi-Fi network processor subsystem includes a dedicated Arm MCU to completely offload the host MCU along with an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast, secure WLAN and Internet connections with 256-bit encryption. The CC3220x devices support station, AP, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security and WPS 2.0. The Wi-Fi network processor includes an embedded IPv6, IPv4 TCP/IP stack.

6.2.1 WLAN

The WLAN features are as follows:

- 802.11b/g/n integrated radio, modem, and MAC supporting WLAN communication as a BSS station, AP, Wi-Fi Direct client and group owner with CCK and OFDM rates in the 2.4-GHz ISM band, channels 1 to 13.

NOTE

802.11n is supported only in Wi-Fi station, Wi-Fi direct, and P2P client modes.

- Autocalibrated radio with a single-ended 50-Ω interface enables easy connection to the antenna without requiring expertise in radio circuit design.
- Advanced connection manager with multiple user-configurable profiles stored in serial Flash allows automatic fast connection to an access point without user or host intervention.
- Supports all common Wi-Fi security modes for personal and enterprise networks with on-chip security accelerators, including: WEP, WPA/WPA2 PSK, WPA2 Enterprise (802.1x).
- Smart provisioning options deeply integrated within the device providing a comprehensive end-to-end solution. With elaborate events notification to the host, enabling the application to control the provisioning decision flow. The wide variety of Wi-Fi provisioning methods include:
  - Access Point using HTTPS
  - SmartConfig Technology: a 1-step, 1-time process to connect a CC3220-enabled device to the home wireless network, removing dependency on the I/O capabilities of the host MCU; thus, it is usable by deeply embedded applications
- 802.11 transceiver mode allows transmitting and receiving of proprietary data through a socket without adding MAC or PHY headers. The 802.11 transceiver mode provides the option to select the working channel, rate, and transmitted power. The receiver mode works with the filtering options.

6.2.2 Network Stack

The Network Stack features are as follows:

- Integrated IPv4, IPv6 TCP/IP stack with BSD (BSD adjacent) socket APIs for simple Internet connectivity with any MCU, microprocessor, or ASIC

NOTE

Not all APIs are 100% BSD compliant. Not all BSD APIs are supported.

- Support of 16 simultaneous TCP, UDP, or RAW sockets
- Support of 6 simultaneous SSL\TLS sockets
- Built-in network protocols:
  - Static IP, LLA, DHCPv4, DHCPv6 with DAD and stateless autoconfiguration
  - ARP, ICMPv4, IGMP, ICMPv6, MLD, ND
  - DNS client for easy connection to the local network and the Internet

- Built-in network application and utilities:
  - HTTP/HTTPS
    - Web page content stored on serial Flash
    - RESTful APIs for setting and configuring application content
    - Dynamic user callbacks
  - Service discovery: Multicast DNS service discovery lets a client advertise its service without a centralized server. After connecting to the access point, the CC3220x device provides critical information, such as device name, IP, vendor, and port number.
  - DHCP server
  - Ping

Table 6-1 describes the NWP features.

Table 6-1. NWP Features

Feature	Description
Wi-Fi standards	802.11b/g/n station 802.11b/g AP supporting up to four stations Wi-Fi Direct client and group owner
Wi-Fi channels	1 to 13
Wi-Fi security	WEP, WPA/WPA2 PSK, WPA2 enterprise (802.1x)
Wi-Fi provisioning	SmartConfig technology, Wi-Fi protected setup (WPS2), AP mode with internal HTTP web server
IP protocols	IPv4/IPv6
IP addressing	Static IP, LLA, DHCPv4, DHCPv6 with DAD
Cross layer	ARP, ICMPv4, IGMP, ICMPv6, MLD, NDP
Transport	UDP, TCP SSLv3.0/TLSv1.0/TLSv1.1/TLSv1.2 RAW
Network applications and utilities	Ping HTTP/HTTPS web server mDNS DNS-SD DHCP server
Host interface	UART/SPI
Security	Device identity Trusted root-certificate catalog TI root-of-trust public key The CC3220S and CC3220SF variants also support: • Secure key storage • File system security • Software tamper detection • Cloning protection • Secure boot • Validate the integrity and authenticity of the run-time binary during boot • Initial secure programming • Debug security • JTAG and debug
Power management	Enhanced power policy management uses 802.11 power save and deep-sleep power modes
Other	Transceiver Programmable RX filters with event-trigger mechanism

6.3 Security

The SimpleLink™ Wi-Fi® CC3220x Internet-on-a-Chip device enhances the security capabilities available for development of IoT devices, while completely offloading these activities from the MCU to the networking subsystem. The security capabilities include the following key features:

Wi-Fi and Internet Security:

- Personal and enterprise Wi-Fi security
  - Personal standards
    - AES (WPA2-PSK)
    - TKIP (WPA-PSK)
    - WEP
  - Enterprise standards
    - EAP Fast
    - EAP PEAPv0/1
    - EAP PEAPv0 TLS
    - EAP PEAPv1 TLS EAP LS
    - EAP TLS
    - EAP TTLS TLS
    - EAP TTLS MSCHAPv2

- Secure sockets
  - Protocol versions: SSL v3, TLS 1.0, TLS 1.1, TLS 1.2
  - Powerful crypto engine for fast, secure Wi-Fi and internet connections with 256-bit AES encryption for TLS and SSL connections
  - Ciphers suites
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_MD5
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_CHACHA20_POLY1305_SHA256
  - Server authentication
  - Client authentication
  - Domain name verification
  - Runtime socket upgrade to secure socket – STARTTLS
- Secure HTTP server (HTTPS)
- Trusted root-certificate catalog—Verifies that the CA used by the application is trusted and known secure content delivery
- TI root-of-trust public key—Hardware-based mechanism that allows authenticating TI as the genuine origin of a given content using asymmetric keys
- Secure content delivery—Allows encrypted file transfer to the system using asymmetric keys created by the device

Code and Data Security:

- Network passwords and certificates are encrypted and signed.
- Cloning protection—Application and data files are encrypted by a unique key per device.
- Access control—Access to application and data files only by using a token provided in file creation time. If an unauthorized access is detected, a tamper protection lockdown mechanism takes effect.
- Encrypted and Authenticated file system (not supported in CC3220R)
- Secured boot—Authentication of the application image on every boot
- Code and data encryption (not supported in CC3220R)—User application and data files are encrypted in serial flash.

- Code and data authentication (not supported in CC3220R)—User Application and data files are authenticated with a public key certificate.
- Offloaded crypto library for asymmetric keys, including the ability to create key-pair, sign and verify data buffer.
- Recovery mechanism

Device Security:

- Separate execution environments—Application processor and network processor run on separate Arm cores
- Initial secure programming (not supported in CC3220R)—Allows for keeping the content confidential on the production line
- Debug security (not supported in CC3220R)
  - JTAG lock
  - Debug ports lock
- True random number generator

Figure 6-1 shows the high-level structure of the CC3220R device. The network information files (passwords and certificates) are encrypted using a device-specific key.

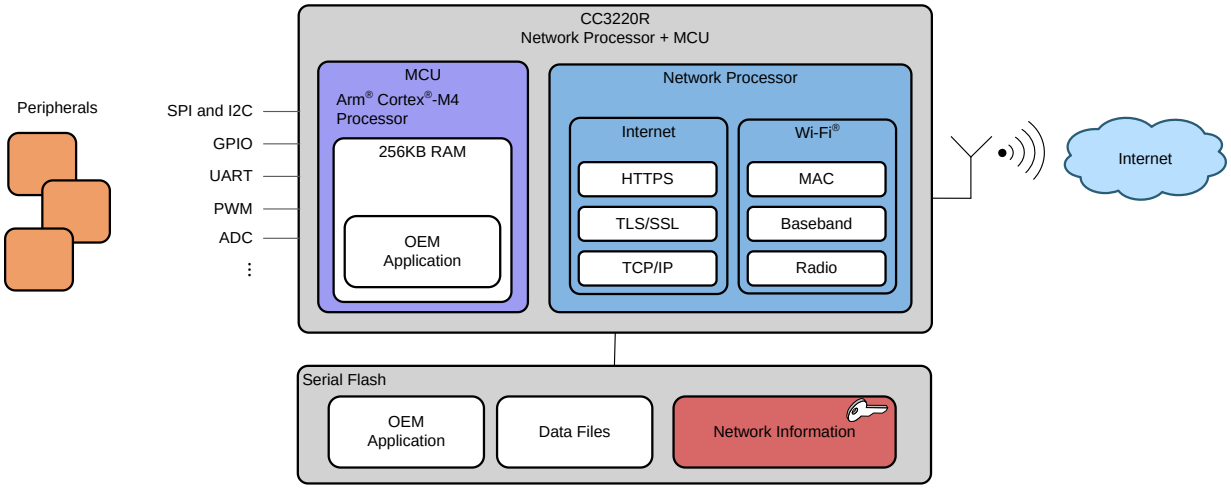


Figure 6-1. CC3220R High-Level Structure

Figure 6-2 shows the high-level structure of the CC3220S and CC3220SF devices. The application image, user data, and network information files (passwords, certificates) are encrypted using a device-specific key.

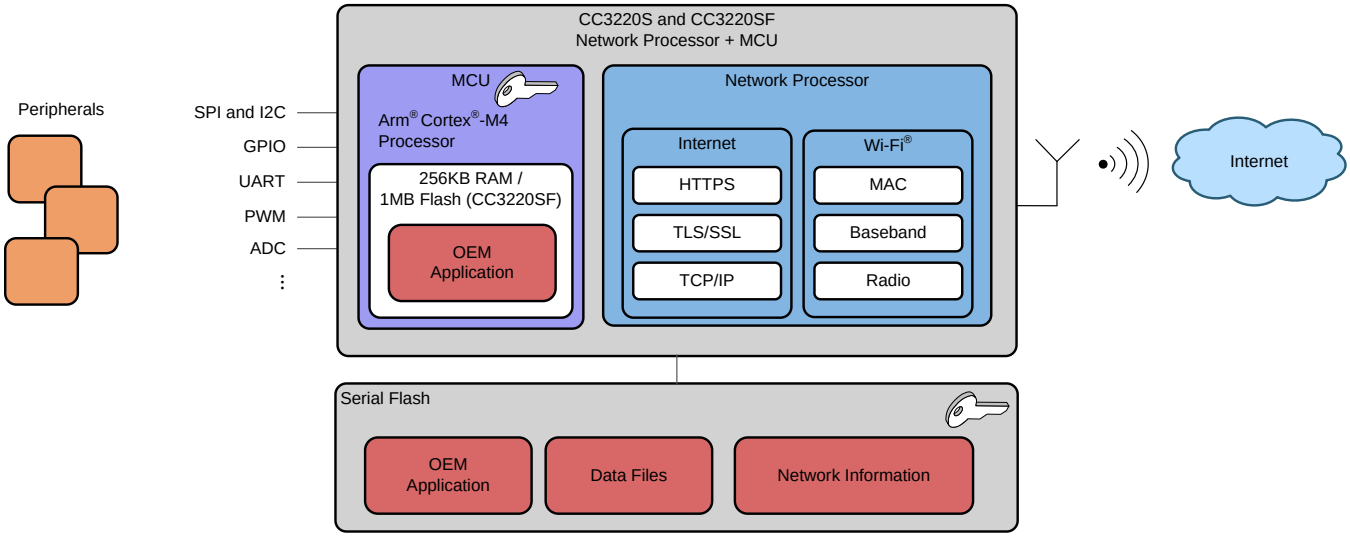


Figure 6-2. CC3220S and CC3220SF High-Level Structure

6.4 Power-Management Subsystem

The CC3220x power-management subsystem contains DC/DC converters to accommodate the different voltage or current requirements of the system.

- Digital DC/DC (Pin 44)
  - Input: V_{BAT} wide voltage (2.1 to 3.6 V) or preregulated 1.85 V
- ANA1 DC/DC (Pin 37)
  - Input: V_{BAT} wide voltage (2.1 to 3.6 V)
  - In preregulated 1.85-V mode, the ANA1 DC/DC converter is bypassed.
- PA DC/DC (Pin 39)
  - Input: V_{BAT} wide voltage (2.1 to 3.6 V)
  - In preregulated 1.85-V mode, the PA DC/DC converter is bypassed.
- ANA2 DC/DC (Pin 47)
  - Input: V_{BAT} wide voltage (2.1 to 3.6 V) or preregulated 1.85 V

The CC3220x device is a single-chip WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC/DC converters and LDOs, generates all of the voltages required for the device to operate from a wide variety of input sources. For maximum flexibility, the device can operate in the modes described in Section 6.4.1 and Section 6.4.2.

6.4.1 V_{BAT} Wide-Voltage Connection

In the wide-voltage battery connection, the device is powered directly by the battery or preregulated 3.3-V supply. All other voltages required to operate the device are generated internally by the DC/DC converters. This scheme supports wide-voltage operation from 2.1 to 3.6 V and is thus the most common mode for the device.

6.4.2 Preregulated 1.85-V Connection

The preregulated 1.85-V mode of operation applies an external regulated 1.85 V directly at pins 10, 25, 33, 36, 37, 39, 44, 48, and 54 of the device. The V_{BAT} and the V_{IO} are also connected to the 1.85-V supply. This mode provides the lowest BOM count version in which inductors used for PA DC/DC and ANA1 DC/DC (2.2 and 1 µH) and a capacitor (22 µF) can be avoided.

In the preregulated 1.85-V mode, the regulator providing the 1.85 V must have the following characteristics:

- Load current capacity ≥900 mA
- Line and load regulation with <2% ripple with 500-mA step current and settling time of < 4 µs with the load step

NOTE

The regulator must be placed as close as possible to the device so that the IR drop to the device is very low.

6.5 Low-Power Operating Mode

From a power-management perspective, the CC3220x device comprises the following two independent subsystems:

- Arm Cortex-M4 application processor subsystem
- Networking subsystem

Each subsystem operates in one of several power states.

The Cortex-M4 application processor runs the user application loaded from an external serial Flash, or internal Flash (in CC3220SF). The networking subsystem runs preprogrammed TCP/IP and Wi-Fi data link layer functions.

The user program controls the power state of the application processor subsystem and can be in one of the five modes described in Table 6-2.

Table 6-2. User Program Modes

APPLICATION PROCESSOR (MCU) MODE(1)	DESCRIPTION
MCU active mode	MCU executing code at 80-MHz state rate
MCU sleep mode	The MCU clocks are gated off in sleep mode and the entire state of the device is retained. Sleep mode offers instant wakeup. The MCU can be configured to wake up by an internal fast timer or by activity from any GPIO line or peripheral.
MCU LPDS mode	State information is lost and only certain MCU-specific register configurations are retained. The MCU can wake up from external events or by using an internal timer. (The wake-up time is less than 3 ms.) Certain parts of memory can be retained while the MCU is in LPDS mode. The amount of memory retained is configurable. Users can choose to preserve code and the MCU-specific setting. The MCU can be configured to wake up using the RTC timer or by an external event on specific GPIOs as the wake-up source.
MCU hibernate mode	The lowest power mode in which all digital logic is power-gated. Only a small section of the logic directly powered by the input supply is retained. The RTC keeps running and the MCU supports wakeup from an external event or from an RTC timer expiry. Wake-up time is longer than LPDS mode at about 15 ms plus the time to load the application from serial Flash, which varies according to code size. In this mode, the MCU can be configured to wake up using the RTC timer or external event on a GPIO.
MCU shutdown mode	The lowest power mode system-wise. All device logics are off, including the RTC. The wake-up time in this mode is longer than hibernate at about 1.1 s. To enter or exit the shutdown mode, the state of the nRESET line is changed (low to shut down, high to turn on).

(1) Modes are listed in order of power consumption, with highest power modes listed first.

The NWP can be active or in LPDS mode and takes care of its own mode transitions. When there is no network activity, the NWP sleeps most of the time and wakes up only for beacon reception (see Table 6-3).

Table 6-3. Networking Subsystem Modes

NETWORK PROCESSOR MODE	DESCRIPTION
Network active mode (processing layer 3, 2, and 1)	Transmitting or receiving IP protocol packets
Network active mode (processing layer 2 and 1)	Transmitting or receiving MAC management frames; IP processing not required.
Network active listen mode	Special power optimized active mode for receiving beacon frames (no other frames supported)
Network connected Idle	A composite mode that implements 802.11 infrastructure power save operation. The CC3220x NWP automatically goes into LPDS mode between beacons and then wakes to active listen mode to receive a beacon and determine if there is pending traffic at the AP. If not, the NWP returns to LPDS mode and the cycle repeats.
Network LPDS mode	Low-power state between beacons in which the state is retained by the NWP, allowing for a rapid wake up.
Network disabled	The network is disabled

The operation of the application and network processor ensures that the device remains in the lowest power mode most of the time to preserve battery life.

The following examples show the use of the power modes in applications:

- A product that is continuously connected to the network in the 802.11 infrastructure power-save mode but sends and receives little data spends most of the time in connected idle, which is a composite of receiving a beacon frame and waiting for the next beacon.
- A product that is not continuously connected to the network but instead wakes up periodically (for example, every 10 minutes) to send data, spends most of the time in hibernate mode, jumping briefly to active mode to transmit data.

6.6 Memory

6.6.1 External Memory Requirements

The CC3220x device maintains a proprietary file system on the serial flash. The CC3220x file system stores the MCU binary, service pack file, system files, configuration files, certificate files, web page files, and user files. By using a format command through the API, users can provide the total size allocated for the file system. The starting address of the file system cannot be set and is always at the beginning of the serial flash. The applications microcontroller must access the serial flash memory area allocated to the file system directly through the CC3220x file system. The applications microcontroller must not access the serial flash memory area directly.

The file system manages the allocation of serial flash blocks for stored files according to download order, which means that the location of a specific file is not fixed in all systems. Files are stored on serial flash using human-readable filenames rather than file IDs. The file system API works using plain text, and file encryption and decryption is invisible to the user. Encrypted files can be accessed only through the file system.

All file types can have a maximum of 100 supported files in the file system. All files are stored in 4-KB blocks and thus use a minimum of 4KB of Flash space. Fail-safe files require twice the original size and use a minimum of 8KB. Encrypted files are counted as fail-safe in terms of space. The maximum file size is 1MB.

Table 6-4 lists the minimum required memory consumption under the following assumptions:

- System files in use consume 64 blocks (256KB).
- Vendor files are not taken into account.
- MCU code is taken as the maximal possible size for the CC3220 with fail-safe enabled to account for future updates, such as through OTA.
- Gang image:
  - Storage for the gang image is rounded up to 32 blocks (meaning 128KB resolution).
  - Gang image size depends on the actual content size of all components. Additionally, the image should be 128KB aligned so unaligned memory is considered lost. Service pack, system files, and the 128KB aligned memory are assumed to occupy 256KB.
- All calculations consider that the restore-to-default is enabled.

Table 6-4. Recommended Flash Size

ITEM	CC3220R and CC3220S [KB]	CC3220SF [KB]
File system allocation table	20	20
System and configuration files (1)	256	256
Service Pack (1)	264	264
MCU Code (1)	512	2048
Gang image size	256 + MCU	256 + MCU
Total	1308 + MCU	2844 + MCU
Minimal Flash size (2)	16MBit	32MBit
Recommended Flash size (2)	16MBit	32MBit

(1) Including fail-safe.
(2) For maximum MCU size.

NOTE

The maximum supported serial flash size is 32MB (256Mb). See the *Using Serial Flash on CC3120/CC3220 SimpleLink™ Wi-Fi® and Internet-of-Things Devices* application report.

6.6.2 Internal Memory

The CC3220x device includes on-chip SRAM to which application programs are downloaded and executed. The application developer must share the SRAM for code and data. The micro direct memory access (µDMA) controller can transfer data to and from SRAM and various peripherals. The CC3220x ROM holds the rich set of peripheral drivers, which saves SRAM space. For more information on drivers, see the CC3220x API list.

6.6.2.1 SRAM

The CC3220x family provides 256KB of on-chip SRAM. Internal RAM is capable of selective retention during LPDS mode. This internal SRAM is at offset 0x2000 0000 of the device memory map.

Use the µDMA controller to transfer data to and from the SRAM.

When the device enters low-power mode, the application developer can choose to retain a section of memory based on need. Retaining the memory during low-power mode provides a faster wakeup. The application developer can choose the amount of memory to retain in multiples of 64KB. For more information, see the API guide.

6.6.2.2 ROM

The internal zero-wait-state ROM of the CC3220x device is at address 0x0000 0000 of the device memory and is programmed with the following components:

- Bootloader
- Peripheral driver library (DriverLib) release for product-specific peripherals and interfaces

The bootloader is used as an initial program loader (when the serial Flash memory is empty). The CC3220x DriverLib software library controls on-chip peripherals with a bootloader capability. The library performs peripheral initialization and control functions, with a choice of polled or interrupt-driven peripheral support. The DriverLib APIs in ROM can be called by applications to reduce Flash memory requirements and free the Flash memory for other purposes.

6.6.2.3 Flash Memory

The CC3220SF device comes with an on-chip Flash memory of 1MB that allows application code to execute in place while freeing SRAM exclusively for read-write data. The Flash memory is used for code and constant data sections and is directly attached to the ICODE/DCODE bus of the Cortex-M4 core. A 128-bit-wide instruction prefetch buffer allows maintenance of maximum performance for linear code or loops that fit inside the buffer.

The Flash memory is organized as 2-KB sectors that can be independently erased. Reads and writes can be performed at word (32-bit) level.

6.6.2.4 Memory Map

Table 6-5 describes the various MCU peripherals and how they are mapped to the processor memory. For more information on peripherals, see the API document.

Table 6-5. Memory Map

START ADDRESS	END ADDRESS	DESCRIPTION	COMMENT
0x0000 0000	0x0007 FFFF	On-chip ROM (bootloader + DriverLib)	
0x0100 0000	0x010F FFFF	On-chip Flash (for user application code)	CC3220SF device only
0x2000 0000	0x2003 FFFF	Bit-banded on-chip SRAM	
0x2200 0000	0x23FF FFFF	Bit-band alias of 0x2000 0000 to 0x200F FFFF	
0x4000 0000	0x4000 0FFF	Watchdog timer A0	
0x4000 4000	0x4000 4FFF	GPIO port A0	
0x4000 5000	0x4000 5FFF	GPIO port A1	
0x4000 6000	0x4000 6FFF	GPIO port A2	
0x4000 7000	0x4000 7FFF	GPIO port A3	
0x4000 C000	0x4000 CFFF	UART A0	
0x4000 D000	0x4000 DFFF	UART A1	
0x4002 0000	0x4000 07FF	I^2C A0 (master)	
0x4002 4000	0x4002 4FFF	GPIO group 4	
0x4002 0800	0x4002 0FFF	I^2C A0 (slave)	
0x4003 0000	0x4003 0FFF	General-purpose timer A0	
0x4003 1000	0x4003 1FFF	General-purpose timer A1	
0x4003 2000	0x4003 2FFF	General-purpose timer A2	
0x4003 3000	0x4003 3FFF	General-purpose timer A3	
0x400F7000	0x400F 7FFF	Configuration registers	
0x400F E000	0x400F EFFF	System control	
0x400F F000	0x400F FFFF	µDMA	
0x4200 0000	0x43FF FFFF	Bit band alias of 0x4000 0000 to 0x400F FFFF	
0x4401 0000	0x4401 0FFF	SDIO master	
0x4401 8000	0x4401 8FFF	Camera Interface	
0x4401 C000	0x4401 DFFF	McASP	
0x4402 0000	0x4402 1FFF	SSPI	Used for external serial Flash
0x4402 1000	0x4402 2FFF	GSPI	Used by application processor
0x4402 5000	0x4402 5FFF	MCU reset clock manager	
0x4402 6000	0x4402 6FFF	MCU configuration space	
0x4402 D000	0x4402 DFFF	Global power, reset, and clock manager (GPRCM)	
0x4402 E000	0x4402 EFFF	MCU shared configuration	
0x4402 F000	0x4402 FFFF	Hibernate configuration	
0x4403 0000	0x4403 FFFF	Crypto range (includes apertures for all crypto-related blocks as follows)	
0x4403 0000	0x4403 0FFF	DTHE registers and TCP checksum	
0x4403 5000	0x4403 5FFF	MD5/SHA	
0x4403 7000	0x4403 7FFF	AES	
0x4403 9000	0x4403 9FFF	DES	
0xE000 0000	0xE000 0FFF	Instrumentation trace Macrocell™	
0xE000 1000	0xE000 1FFF	Data watchpoint and trace (DWT)	
0xE000 2000	0xE000 2FFF	Flash patch and breakpoint (FPB)	
0xE000 E000	0xE000 EFFF	NVIC	
0xE004 0000	0xE004 0FFF	Trace port interface unit (TPIU)	
0xE004 1000	0xE004 1FFF	Reserved for embedded trace macrocell (ETM)	
0xE004 2000	0xE00F FFFF	Reserved	

6.7 Restoring Factory Default Configuration

The device has an internal recovery mechanism that allows rolling back the file system to its predefined factory image or restoring the factory default parameters of the device. The factory image is kept in a separate sector on the serial flash in a secure manner and cannot be accessed from the host processor. The following restore modes are supported:

- None—no factory restore settings
- Enable restore of factory default parameters
- Enable restore of factory image and factory default parameters

The restore process is performed by calling SW APIs, or by pulling or forcing SOP[2:0] = 110 pins and toggling the nRESET pin from low to high.

The process is fail-safe and resumes operation if a power failure occurs before the restore is finished. The restore process typically takes about 8 seconds, depending on the attributes of the serial Flash vendor.

6.8 Boot Modes

6.8.1 Boot Mode List

The CC3220x device implements a sense-on-power (SoP) scheme to determine the device operation mode.

SoP values are sensed from the device pin during power up. This encoding determines the boot flow. Before the device is taken out of reset, the SoP values are copied to a register and used to determine the device operation mode while powering up. These values determine the boot flow as well as the default mapping for some of the pins (JTAG, SWD, UART0). Table 6-6 lists the pull configurations.

Table 6-6. CC3220x Functional Configurations

NAME	SOP[2]	SOP[1]	SOP[0]	SoP MODE	COMMENT
UARTLOAD	Pullup	Pulldown	Pulldown	LDfrUART	Factory, lab Flash, and SRAM loads through the UART. The device waits indefinitely for the UART to load code. The SOP bits then must be toggled to configure the device in functional mode. Also puts JTAG in 4-wire mode.
FUNCTIONAL_2WJ	Pulldown	Pulldown	Pullup	Fn2WJ	Functional development mode. In this mode, 2-pin SWD is available to the developer. TMS and TCK are available for debugger connection.
FUNCTIONAL_4WJ	Pulldown	Pulldown	Pulldown	Fn4WJ	Functional development mode. In this mode, 4-pin JTAG is available to the developer. TDI, TMS, TCK, and TDO are available for debugger connection.
UARTLOAD_FUNCTIONAL_4WJ	Pulldown	Pullup	Pulldown	LDfrUART_Fn4WJ	Supports Flash and SRAM load through UART and functional mode. The MCU bootloader tries to detect a UART break on UART receive line. If the break signal is present, the device enters the UARTLOAD mode, otherwise, the device enters the functional mode. TDI, TMS, TCK, and TDO are available for debugger connection.
RET_FACTORY_IMAGE	Pulldown	Pullup	Pullup	RetFactDef	When device reset is toggled, the MCU bootloader kickstarts the procedure to restore factory default images.

The recommended values of pull resistors are 100 kΩ for SOP0 and SOP1 and 2.7 kΩ for SOP2. The application can use SOP2 for other functions after chip has powered up. However, to avoid spurious SOP values from being sensed at power up, TI strongly recommends using the SOP2 pin only for output signals. The SOP0 and SOP1 pins are multiplexed with the WLAN analog test pins and are not available for other functions.

7 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Typical Application—CC3220x Wide-Voltage Mode

Figure 7-1 shows the schematic for an application using the CC3220x device in the wide-voltage mode of operation. For a full operation reference design, refer to *CC3220 SimpleLink™ and Internet of Things Hardware Design Files*.

NOTE

For complete reference schematics and BOM, see the CC3220x product page.

Table 7-1 lists the bill of materials for an application using the CC3220x device in wide-voltage mode.

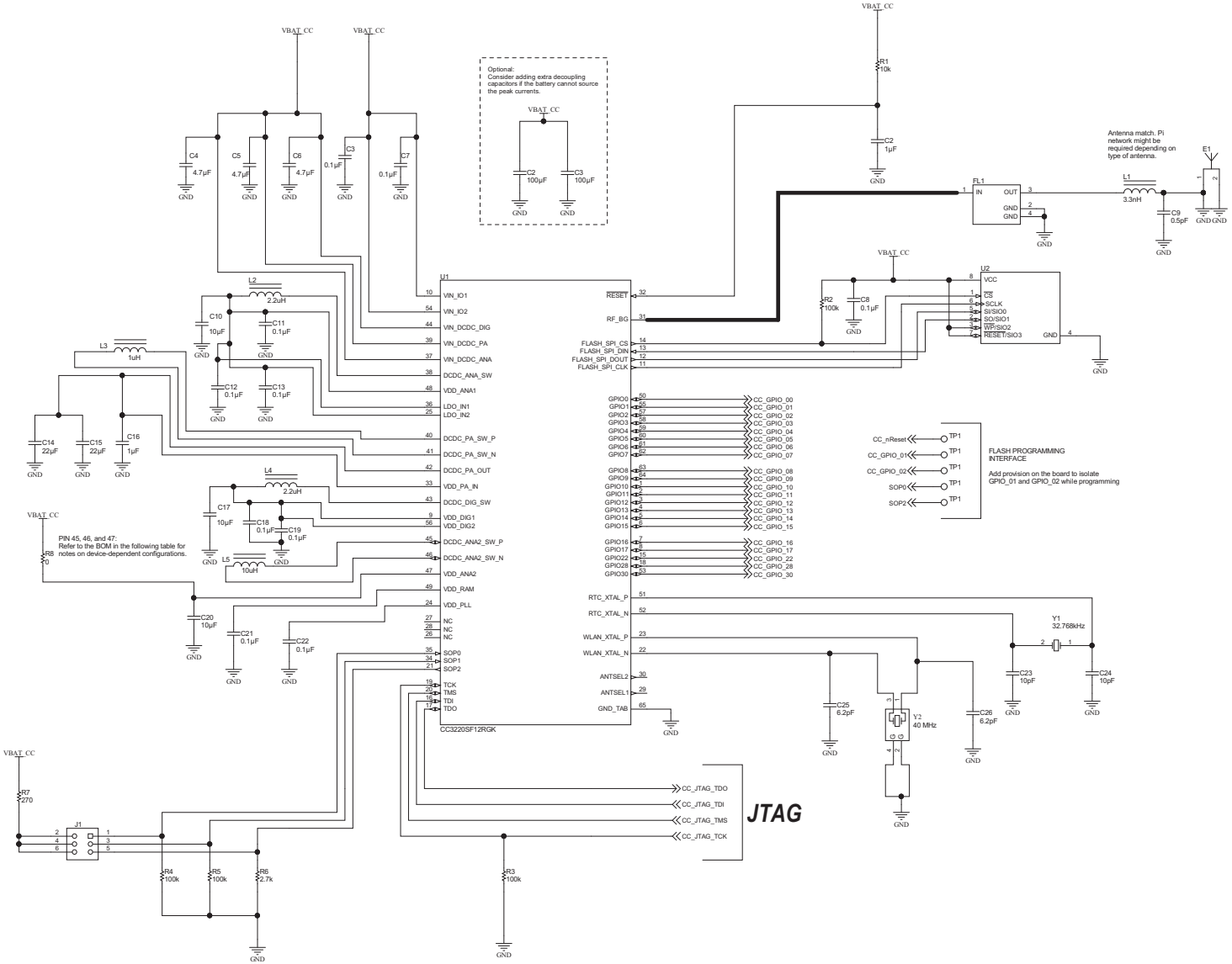


Figure 7-1. CC3220x Wide-Voltage Mode Application Circuit

Table 7-1. Bill of Materials for CC3220x in Wide-Voltage Mode

QUANTITY	DESIGNATOR	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
1	C1	1 µF	MuRata	GRM155R61A105KE15D	Capacitor, Ceramic, 1 µF, 10 V, ±10%, X5R, 0402
10	C2, C6, C10, C12, C13, C14, C19, C20, C22, C23	0.1 µF	TDK	C1005X5R1A104K050BA	Capacitor, Ceramic, 0.1 µF, 10 V, ±10%, X5R, 0402
3	C3, C4, C5	4.7 µF	TDK	C1005X5R0J475M050BC	Capacitor, Ceramic, 4.7 µF, 6.3 V, ±20%, X5R, 0402
2	C7, C8	100 µF	Taiyo Yuden	LMK325ABJ107MMHT	Capacitor, Ceramic, 100 µF, 10 V, ±20%, X5R, AEC-Q200 Grade 3, 1210
1	C9	0.5 pF	MuRata	GRM1555C1HR50BA01D	Capacitor, Ceramic, 0.5 pF, 50 V, ±20%, C0G/NP0, 0402
3	C11, C18, C21	10 µF	MuRata	GRM188R60J106ME47D	Capacitor, Ceramic, 10 µF, 6.3 V, ±20%, X5R, 0603
1	C15	1 µF	TDK	C1005X5R1A105K050BB	Capacitor, Ceramic, 1 µF, 10 V, ±10%, X5R, 0402
2	C16, C17	22 µF	TDK	C1608X5R0G226M080AA	Capacitor, Ceramic, 22 µF, 4 V, ±20%, X5R, 0603
2	C24, C25	10 pF	MuRata	GRM1555C1H100JA01D	Capacitor, Ceramic, 10 pF, 50 V, ±5%, C0G/NP0, 0402
2	C26, C27	6.2 pF	MuRata	GRM1555C1H6R2CA01D	Capacitor, Ceramic, 6.2 pF, 50 V, ±5%, C0G/NP0, 0402
1	E1	2.45-GHz Antenna	Taiyo Yuden	AH316M245001-T	ANT Bluetooth W-LAN Zigbee® WiMAX™, SMD
1	FL1	1.02 dB	TDK	DEA202450BT-1294C1-H	Multilayer Chip Band Pass Filter For 2.4 GHz W-LAN/Bluetooth, SMD
1	L1	3.3 nH	MuRata	LQG15HS3N3S02D	Inductor, Multilayer, Air Core, 3.3 nH, 0.3 A, 0.17 ohm, SMD
2	L2, L4	2.2 µH	MuRata	LQM2HPN2R2MG0L	Inductor, Multilayer, Ferrite, 2.2 µH, 1.3 A, 0.08 ohm, SMD
1	L3	1 µH	MuRata	LQM2HPN1R0MG0L	Inductor, Multilayer, Ferrite, 1 µH, 1.6 A, 0.055 ohm, SMD
1	L5(1)	10 µH	Taiyo Yuden	CBC2518T100M	Inductor, Wirewound, Ceramic, 10 µH, 0.48 A, 0.36 ohm, SMD
1	R1	10 k	Vishay-Dale	CRCW040210K0JNED	Resistor, 10 k, 5%, 0.063 W, 0402
4	R2, R3, R4, R5	100 k	Vishay-Dale	CRCW0402100KJNED	Resistor, 100 k, 5%, 0.063 W, 0402
1	R6	2.7 k	Vishay-Dale	CRCW04022K70JNED	Resistor, 2.7 k, 5%, 0.063 W, 0402
1	R7	270	Vishay-Dale	CRCW0402270RJNED	Resistor, 270, 5%, 0.063 W, 0402
1	R8(2)	0	Panasonic	ERJ-2GE0R00X	Resistor, 0, 5% 0.063W, 0402
1	U1	MX25R	Macronix International Co., LTD	MX25R3235FM1IL0	Ultra-Low Power, 32-Mbit [x 1/x 2/x 4] CMOS MXSMIO (Serial Multi I/O) Flash Memory, SOP-8
1	U2	CC3220	Texas Instruments	CC3220SF12RGK	SimpleLink™ Wi-Fi® and internet-of-things Solution, a Single-Chip Wireless MCU, RGK0064B
1	Y1	Crystal	Abracon Corportation	ABS07-32.768KHZ-9-T	Crystal, 32.768 KHz, 9PF, SMD
1	Y2	Crystal	Epson	Q24FA20H0039600	Crystal, 40 MHz, 8pF, SMD

(1) For CC3220SF device, L5 is populated. For CC3220R and CC3220S devices, L5 is not populated.
(2) For CC3220SF device, R8 is not populated. For CC3220R and CC3220S devices if R8 is populated, Pin 47 can be used as GPIO_31.

7.1.2 Typical Application Schematic—CC3220x Preregulated, 1.85-V Mode

Figure 7-2 shows the typical application schematic using the CC3220x in preregulated, 1.85-V mode of operation. For addition information on this mode of operation please contact your TI representative.

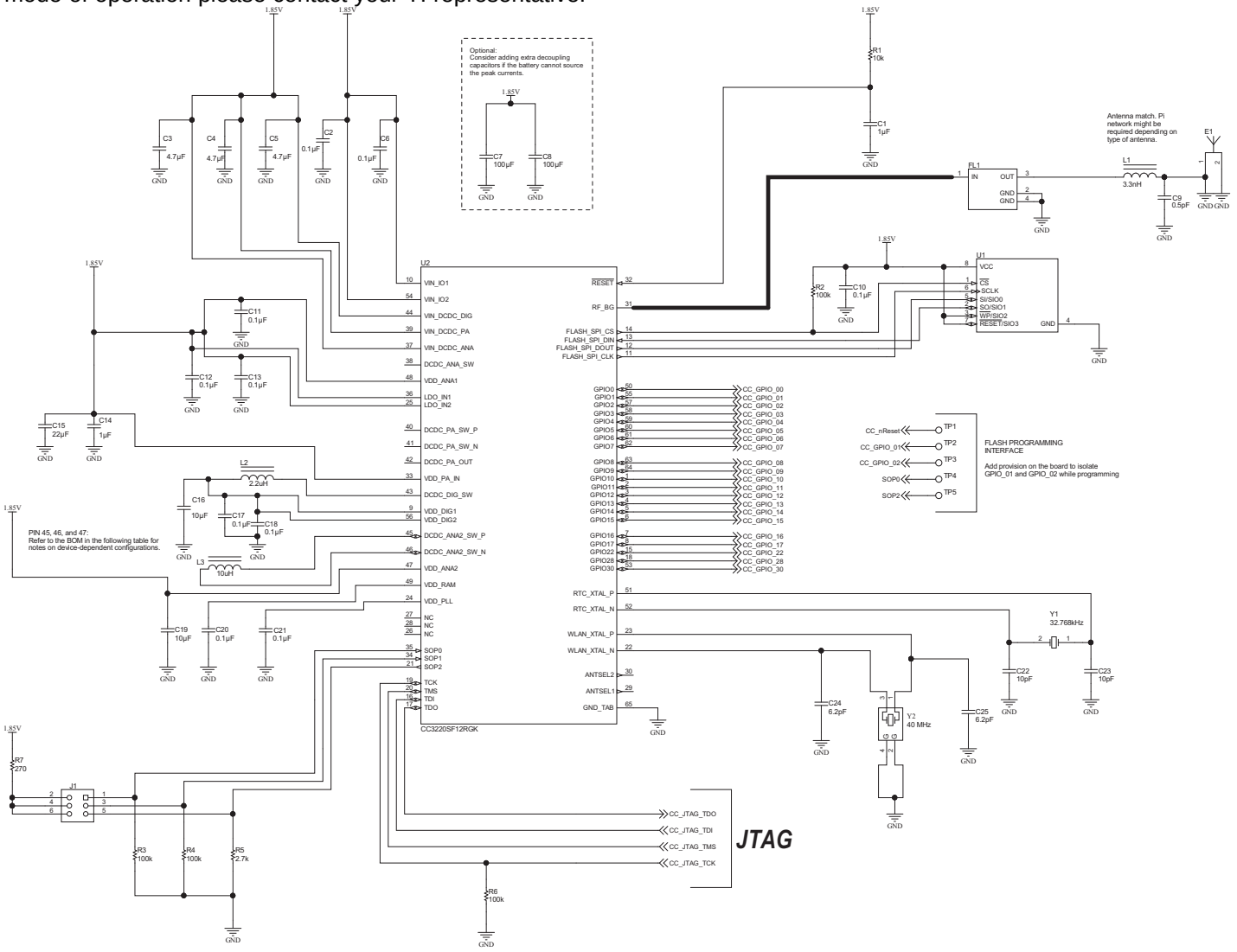


Figure 7-2. CC3220x Preregulated 1.85-V Mode Application Circuit

Table 7-2 lists the bill of materials for an application using the CC3120R device in preregulated 1.85-V mode.

Table 7-2. Bill of Materials for CC3220x Preregulated, 1.85-V Mode

QUANTITY	DESIGNATOR	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
1	C1	1 µF	MuRata	GRM155R61A105KE15D	Capacitor, Ceramic, 1 µF, 10 V, ±10%, X5R, 0402
10	C2, C6, C10, C11, C12, C13, C17, C18, C20, C21	0.1 µF	TDK	C1005X5R1A104K050BA	Capacitor, Ceramic, 0.1 µF, 10 V, ±10%, X5R, 0402
3	C3, C4, C5	4.7 µF	TDK	C1005X5R0J475M050BC	Capacitor, Ceramic, 4.7 µF, 6.3 V, ±20%, X5R, 0402
2	C7, C8	100 µF	Taiyo Yuden	LMK325ABJ107MMHT	Capacitor, Ceramic, 100 µF, 10 V, ± 20%, X5R, AEC-Q200 Grade 3, 1210
1	C9	0.5 pF	MuRata	GRM1555C1HR50BA01D	Capacitor, Ceramic, 0.5 pF, 50 V, ±20%, C0G/NP0, 0402
1	C14	1 µF	TDK	C1005X5R1A105K050BB	Capacitor, Ceramic, 1 µF, 10 V, ±10%, X5R, 0402
1	C15	22 µF	TDK	C1608X5R0G226M080AA	Capacitor, Ceramic, 22 µF, 4 V, ±20%, X5R, 0603
2	C16, C19	10 µF	MuRata	GRM188R60J106ME47D	Capacitor, Ceramic, 10 µF, 6.3 V, ±20%, X5R, 0603
2	C22, C23	10 pF	MuRata	GRM1555C1H100JA01D	Capacitor, Ceramic, 10 pF, 50 V, ±5%, C0G/NP0, 0402
2	C24, C25	6.2 pF	MuRata	GRM1555C1H6R2CA01D	Capacitor, Ceramic, 6.2 pF, 50 V, ±5%, C0G/NP0, 0402
1	U1	MX25R	Macronix International Co. LTD	MX25R3235FM1IL0	Ultra-low power, 32-Mbit [x 1/x 2/x 4] CMOS MXSMIO (Serial Multi I/O) Flash Memory, SOP-8
1	E1	2.45-GHz Antenna	Taiyo Yuden	AH316M245001-T	ANT Bluetooth W-LAN Zigbee® WiMAX™, SMD
1	FL1	1.02 dB	TDK	DEA202450BT-1294C1-H	Multilayer Chip Band Pass Filter For 2.4GHz W-LAN/Bluetooth, SMD
1	L1	3.3 nH	MuRata	LQG15HS3N3S02D	Inductor, Multilayer, Air Core, 3.3 nH, 0.3 A, 0.17 ohm, SMD
1	L2	2.2 µH	MuRata	LQM2HPN2R2MG0L	Inductor, Multilayer, Ferrite, 2.2 µH, 1.3 A, 0.08 ohm, SMD
1	L3(1)	10 µH	Taiyo Yuden	CBC2518T100M	Inductor, Wirewound, Ceramic, 10 µH, 0.48 A, 0.36 ohm, SMD
1	R1	10 k	Vishay-Dale	CRCW040210K0JNED	Resistor, 10 k, 5%, 0.063 W, 0402
4	R2, R3, R4, R6	100 k	Vishay-Dale	CRCW0402100KJNED	Resistor, 100 k, 5%, 0.063 W, 0402
1	R5	2.7 k	Vishay-Dale	CRCW04022K70JNED	Resistor, 2.7 k, 5%, 0.063 W, 0402
1	R7	270	Vishay-Dale	CRCW0402270RJNED	Resistor, 270, 5%, 0.063 W, 0402
1	U2	CC3220	Texas Instruments	CC3220SF12RGK	SimpleLink™ Wi-Fi® and internet-of-things solution, a Single-Chip Wireless MCU, RGK0064B
1	Y1	Crystal	Abracon Corporation	ABS07-32.768KHZ-9-T	Crystal, 32.768 kHZ, 9PF, SMD
1	Y2	Crystal	Epson	Q24FA20H0039600	Crystal, 40 MHz, 8pF, SMD

(1) For CC3220SF device, L3 is populated. For CC3220R and CC3220S devices, L3 is not populated and Pin 47 can be used as GPIO_31.

7.2 PCB Layout Guidelines

This section details the PCB guidelines to speed up the PCB design using the CC3220x VQFN device. Follow these guidelines ensures that the design will minimize the risk with regulatory certifications including FCC, ETSI, and CE. For more information, see *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines*.

7.2.1 General PCB Guidelines

Use the following PCB guidelines:

- Verify the recommended PCB stackup in the PCB design guidelines, as well as the recommended layers for signals and ground.
- Ensure that the PCB footprint of the VQFN follows the information in 节 9.
- Ensure that the GND and solder paste of the VQFN PCB follow the recommendations provided in *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines*.
- Decoupling capacitors must be as close as possible to the VQFN device.

7.2.2 Power Layout and Routing

Three critical DC/DC converters must be considered for the CC3220x device.

- Analog DC/DC converter
- PA DC/DC converter
- Digital DC/DC converter

Each converter requires an external inductor and capacitor that must be laid out with care. DC current loops are formed when laying out the power components.

7.2.2.1 Design Considerations

The following design guidelines must be followed when laying out the CC3220x device:

- Route all of the input decoupling capacitors (C11, C13, and C18) on L2 using thick traces, to isolate the RF ground from the noisy supply ground. This step is also required to meet the IEEE spectral mask specifications.
- Maintain the thickness of power traces to be greater than 12 mils. Take special consideration for power amplifier supply lines (pins 33, 40, 41, and 42), and all input supply pins (pins 37, 39, and 44).
- Ensure the shortest grounding loop for the PLL supply decoupling capacitor (pin 24).
- Place all decoupling capacitors as close to the respective pins as possible.
- Power budget: The CC3220x device can consume up to 450 mA for 3.3 V, 670 mA for 2.1 V, and 700 mA for 1.85 V, for 24 ms during the calibration cycle.
- Ensure the power supply is designed to source this current without any issues. The complete calibration (TX and RX) can take up to 17 mJ of energy from the battery over a time of 24 ms.
- The CC3220x device contains many high-current input pins. Ensure the trace feeding these pins is capable of handling the following currents:
  - VIN_DCDC_PA input (pin 39) maximum is 1 A
  - VIN_DCDC_ANA input (pin 37) maximum is 600 mA
  - VIN_DCDC_DIG input (pin 44) maximum is 500 mA
  - DCDC_PA_SW_P (pin 40) and DCDC_PA_SW_N (pin 41) switching nodes maximum is 1 A
  - DCDC_PA_OUT output node (pin 42) maximum 1 A
  - DCDC_ANA_SW switching node (pin 38) maximum is 600 mA
  - DCDC_DIG_SW switching node (pin 43) maximum is 500 mA
  - VDD_PA_IN supply (pin 33) maximum is 500 mA

Figure 7-3 shows the ground routing for the input decoupling capacitors.

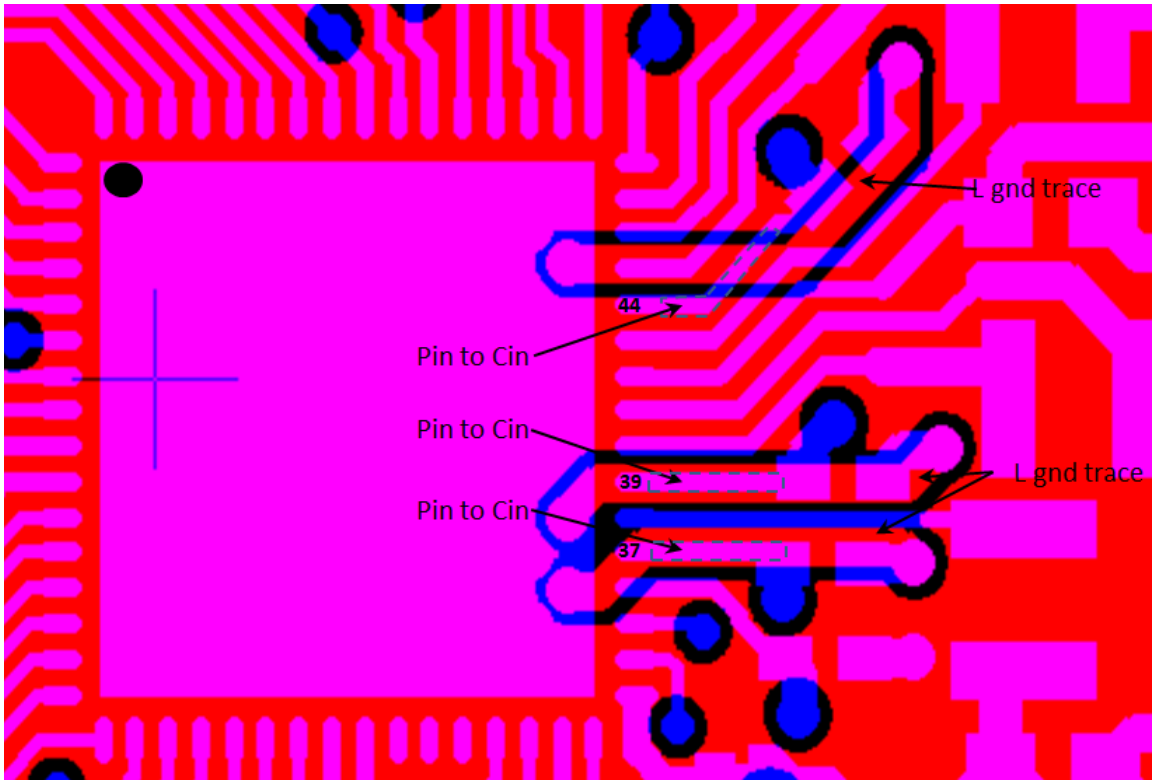


Figure 7-3. Ground Routing for the Input Decoupling Capacitors

The ground return for the input capacitors are routed on L2 to reduce the EMI and improve the spectral mask. This routing must be strictly followed because it is critical for the overall performance of the device.

7.2.3 Clock Interfaces

The following guidelines are for the slow clock.

- The 32.768-kHz crystal must be placed close to the VQFN package.
- Ensure that the load capacitance is tuned according to the board parasitics to the frequency tolerance is within ±150 ppm.
- The ground plane on layer two is solid below the trace lanes and there is ground around these traces on the top layer.

The following guidelines are for the fast clock.

- The 40-MHz crystal must be placed close to the VQFN package.
- Ensure that he load capacitance is tuned according to the board parasitics to the frequency tolerance is within ±100 ppm at room temperature. The total frequency across parts, temperature, and with aging, must be ±25 ppm to meet the WLAN specification.
- Ensure that no high-frequency lines are routed close to the crystal routing to avoid noise degradation.
- Ensure that crystal tuning capacitors are close to the crystal pads.
- Make both traces (XTAL_N and XTAL_P) as close to parallel as possible and approximately the same length.
- The ground plane on layer two is solid below the trace lines and that there is ground around these traces on the top layer.
- See *CC31xx & CC32xx Frequency Tuning* for frequency tuning.

7.2.4 Digital Input and Output

The following guidelines are for the digital I/O.

- Route SPI and UART lines away from any RF traces.
- Keep the length of the high-speed lines as short as possible to avoid transmission line effects.
- Keep the line lower than 1/10 of the rise time of the signal to ignore transmission line effects. This is required if the traces cannot be kept short. Place the resistor at the source end, closer to the device that is driving the signal.
- Add a series-terminating resistor for each high-speed line (such as SPI_CLK or SPI_DATA) to match the driver impedance to the line. Typical terminating-resistor values range from 27 to 36 Ω for a 50-Ω line impedance.
- Route high-speed lines with a ground reference plane continuously below it to offer good impedance throughout. This routing also helps shield the trace against EMI.
- Avoid stubs on high-speed lines to minimize the reflections. If the line must be routed to multiple locations, use a separate line driver for each line.
- If the lines are longer compared to the rise time, add series-terminating resistors near the driver for each high-speed line to match the driver impedance to the line. Typical terminating-resistor values range from 27 to 36 Ω for a 50-Ω line impedance.

7.2.5 RF Interface

The following guidelines are for the RF interface. Follow guidelines specified in the vendor-specific antenna design guides (including placement of the antenna). Also see *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines* for general antenna guidelines.

- Ensure that the antenna is matched for 50-Ω. TI recommends using a Pi-matching network.
- Ensure that the area underneath the BPF pads is grounded on layer one and layer two, and ensure that the minimum filter requirements are met.
- Verify that the Wi-Fi RF trace is a 50-Ω, impedance-controlled trace with a reference to solid ground.
- The RF trace bends must be made with gradual curves. Avoid using 90-degree bends.
- The RF traces must not have sharp corners.
- Do not place traces or ground under the antenna section.
- The RF traces must have via stitching on the ground plane beside the RF trace on both sides.

8 器件和文档支持

TI 提供大量的开发工具。此部分列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

8.1 开发工具和软件

有关开发工具和软件的最新列表，请参阅 *CC3220 工具和软件*产品页面。用户也可以单击 *CC3220 工具和软件*页面右上角的“通知我”按钮，随时获取有关 CC3220MOD 器件的最新消息。

开发工具

引脚复用工具 支持的器件包括：CC3200 和 CC3220x。

Pin Mux 工具是一款软件工具，可提供图形用户界面 (GUI) 用于配置引脚多路复用设置、解决冲突以及指定 TI MPU 的 I/O 单元特性。结果采用 C 头文件/代码文件的形式输出，可导入到软件开发套件 (SDK) 中或用于配置客户的定制软件。Pin Mux 工具版本 3 增加了一个功能，可自动选择多路复用器配置以满足输入要求。

SimpleLink™ Wi-Fi® Starter Pro 支持的器件包括：CC3100、CC3200、CC3120R 和 CC3220x。

SimpleLink™ Wi-Fi® Starter Pro 移动应用是一款用于配置 SimpleLink 的新型移动应用。该应用与嵌入式配置库和在器件端运行的示例一同提供（请参阅 *SimpleLink™ Wi-Fi® CC3120 SDK 插件*和 *TI SimpleLink™ Wi-Fi® CC3220 软件开发套件 (SDK)*）。如需使用 SimpleLink Wi-Fi 产品进行 Wi-Fi 配置，TI 建议使用新配置版本。此配置版本实施了高级接入点模式以及 SmartConfig™技术配置、反馈和备用选项，可确保成功完成处理。客户可以使用嵌入式库和移动库来集成其最终产品。

SimpleLink™ Wi-Fi® 无线电测试工具 支持的器件包括：CC3100、CC3200 和 CC3220x。

SimpleLink™ Wi-Fi® 无线电测试工具是一款基于 Windows 系统的软件工具，用于在开发和认证过程中对 SimpleLink Wi-Fi CC3120 和 CC3220 设计进行射频评估和测试。通过手动将无线电设置为传输或接收模式，该工具可提供低级无线电测试功能。使用此工具需要熟悉并了解无线电电路理论和无线电测试方法的知识。

专为物联网 (IoT) 打造的 SimpleLink Wi-Fi CC31xx 和 CC32xx 系列器件包含片上 Wi-Fi、互联网和稳固的安全协议，您无需具备 Wi-Fi 经验就可以以更快的速度进行开发。有关这些器件的更多信息，请访问 SimpleLink™ Wi-Fi® 系列 Internet-on-a-chip™ 解决方案。

CC3220 软件开发套件 (SDK) 支持 CC3220x 器件。

CC3220 SDK 包含驱动程序、 针对 Wi-Fi 功能 和互联网的很多示例应用以及使用 CC3220 Internet-on-a-chip 解决方案所需的文档。此 SDK 可与 TI 的 MSP432P401R LaunchPad™开发套件或 SimpleLink Studio（一款允许使用 CC3220 进行 MCU 开发的 PC 工具）配合使用。您也可以将此 SDK 用作任何平台的示例代码。此 SDK 中的 所有示例应用 均支持在 TI 的 MSP432P401R 超低功耗 MCU 上运行（借助 Code Composer Studio™IDE 和 TI-RTOS。此外，许多 应用 都支持 IAR。

*适用于 **TI** 微控制器 **(MCU)**、**Sitara** 处理器和 **SimpleLink** 器件的 **Uniflash** 独立闪存工具* CCS Uniflash 是一个独立工具，用于编程 TI MCU 的片上闪存内存和 Sitara 处理器的板载闪存内存。Uniflash 具有 GUI、命令行和脚本界面。CCS UniFlash 免费提供。

TI 设计和参考设计

TI Designs 参考设计库是一个涵盖模拟、嵌入式处理器和连接的强大参考设计资源库。所有 TI 设计由 TI 专家构建，旨在帮助您快速开始系统设计，其中包括原理图或方框图、BOM 和设计文件，助您加速产品上市时间。

8.2 固件更新

即使未发布 相关计划， TI 也会不时更新此模块相应服务包中的功能。由于更改不断发生，TI 建议用户在其用于生产的模块中使用最新服务包。

要随时获取最新信息，请单击产品页面右上角的 SDK“通知我”按钮，或者访问 *SimpleLink™ Wi-Fi® CC3120 SDK 插件*。

8.3 器件命名规则

为了标示产品开发周期所处的阶段，TI 为 CC3220x 器件和支持工具的部件号分配了前缀（请参阅图 8-1）。

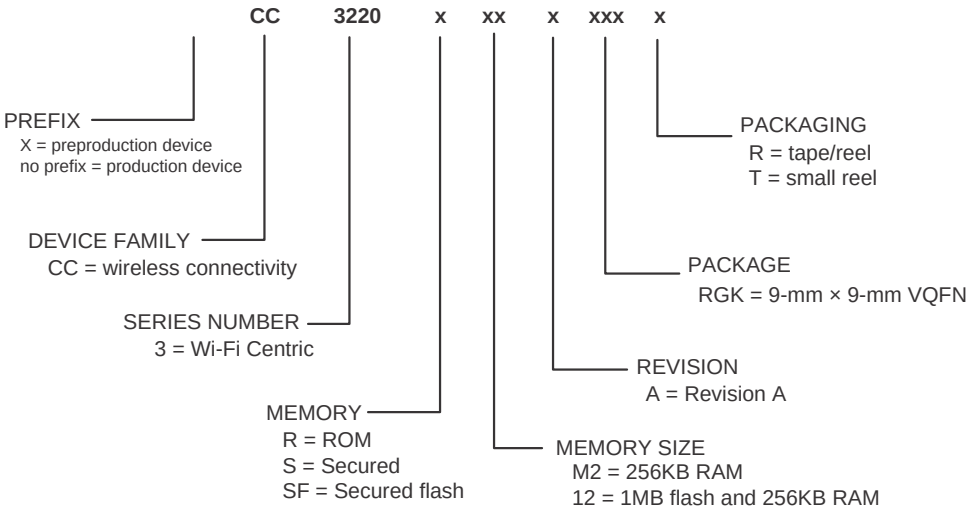


图 **8-1. CC3220x** 器件命名规则

8.4 文档支持

要接收文档更新通知（包括器件勘误表），请转至 ti.com 上相关器件的产品文件夹 (CC3220)。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。下面列出了介绍处理器、相关外设以及其他配套技术资料的最新文档。

以下文档为 CC3220 器件提供支持。

勘误表

CC3220R、CC3220S 器件勘误表 本文档介绍了 CC3220R 和 CC3220S SimpleLink™ Wi-Fi® 无线和物联网解决方案（一种单芯片无线 MCU 解决方案）功能规格的已知例外情况。

CC3220SF 器件勘误表 本文档介绍了 CC3220SF SimpleLink™ Wi-Fi® 无线和物联网解决方案（一种单芯片无线 MCU 解决方案）功能规格的已知例外情况。

应用报告

CC3120 和 CC3220 SimpleLink™ Wi-Fi® 嵌入式编程 CC3120 和 CC3220 SimpleLink™ Wi-Fi® 嵌入式编程

SimpleLink™ CC3120、CC3220 Wi-Fi® Internet-on-a-chip™ 网络子系统电源管理 该应用报告介绍了进行电源管理和延长电池寿命的最佳实践，适用于嵌入式低功耗 Wi-Fi 器件，例如德州仪器 (Texas Instruments™) 的 SimpleLink™ Wi-Fi® Internet-on-a-chip™ 解决方案。

SimpleLink™ CC3120、CC3220 Wi-Fi® Internet-on-a-chip™ 解决方案内置安全性 特性 德州仪器 (Texas Instruments™) 的 SimpleLink™ Wi-Fi® CC3120 和 CC3220 Internet-on-a-chip™ 系列器件具有多种内置的安全 功能 ，以便帮助开发人员解决各种安全需求，且不会对主微控制器 (MCU) 造成任何处理负担。本文档介绍这些安全相关的 特性 ，并提供有关在实际系统实现环境中利用每个特性的建议。

SimpleLink™ CC3120、CC3220 Wi-Fi® 和物联网无线更新 本文档介绍了德州仪器 (Texas Instruments™) SimpleLink™ Wi-Fi® CC3x20 系列器件的 OTA 库，并说明了如何准备新的云更新供 OTA 库下载。

SimpleLink™ CC3120、CC3220 Wi-Fi® Internet-on-a-chip™ 解决方案器件配置 本指南介绍了配置过程，为 SimpleLink™ Wi-Fi® 器件提供了连接到无线网络时所需的信息（网络名称、密码等等）。

将 ***TI 的 Wi-Fi® Alliance 认证转移到基于 SimpleLink™ 的产品*** 本文档说明了如何使用 Wi-Fi® Alliance (WFA) 衍生认证转移策略将德州仪器 (TI) 已获得的 WFA 认证转移到您开发的系统中。

在 SimpleLink™ CC3120 和 CC3220 Wi-Fi® 以及物联网设备上使用串行闪存 本应用手册分为两个部分。第一部分提供重要指南以及在选择和嵌入与 CC3120 和 CC3220 (CC3x20) 器件配对的串行闪存时应考虑的最佳实践设计技巧。第二部分介绍文件系统，同时为使用 CC3x20 器件的系统设计人员提供相关指南及注意事项。

用户指南

SimpleLink™ Wi-Fi® 以及物联网 CC3120 和 CC3220 网络处理器 本文档为软件 (SW) 程序员提供了使用 SimpleLink™ Wi-Fi® 器件网络子系统所需的全部知识。本指南提供了编写强大、优化型网络主机应用 的基本指南，并介绍了网络子系统的功能。本指南包含一些示例代码屏幕截图，以便使用户明白如何使用主机驱动程序。可在正式的软件开发套件 (SDK) 中找到更全面的代码示例。本指南未提供 有关 主机驱动程序 API 的详细说明。

SimpleLink™ Wi-Fi® CC3120 和 CC3220 以及物联网解决方案布局指南 本文档提供了用于德州仪器 (Texas Instruments™) CC3120 和 CC3220 SimpleLink™ Wi-Fi® 系列器件的 4 层 PCB 的设计指南。CC3120 和 CC3220 器件易于布置，采用四方扁平无引线 (QFNS) 封装。当设计电路板时，请遵循本文档中的建议，以优化电路板的性能。

SimpleLink™ Wi-Fi® 和物联网解决方案 CC3220（一种单芯片无线 MCU） 本指南旨在协助用户完成运行首个 CC3220、CC3220S、CC3220SF SimpleLink™ Wi-Fi® 和物联网解决方案（来自德州仪器 (Texas Instruments™) 的单芯片无线 MCU）示例应用的初始设置和演示。本指南介绍如何安装软件开发套件 (SDK) 以及开始创建首个应用所需的各种其他工具。

SimpleLink™ CC3220 Wi-Fi® LaunchPad™ 开发套件硬件 CC3220 SimpleLink LaunchPad™ 开发套件 (CC3220-LAUNCHXL) 是一个基于 Arm® Cortex®-M4 的 MCU 的低成本评估平台。LaunchPad 设计着重强调 CC3220 Internet-on-a chip™ 解决方案和 Wi-Fi 功能。CC3220 LaunchPad 还 具有 温度和加速计传感器、可编程用户按钮、用于自定义 应用的三个 LED 和用于调试的板载仿真。CC3220 LaunchPad XL 接口采用可堆栈接头，使其在与众多现有 BoosterPack™ 插件模块附加板上的其他外设对接时可轻松扩展 LaunchPad 的功能，例如图形显示、音频编解码、天线选择、环境传感等。

SimpleLink™ Wi-Fi® 和物联网 CC3220 本文档为用户介绍了 CC3220x 器件的环境设置以及软件开发套件 (SDK) 的一些参考示例。本文档介绍了可用于支持进一步应用开发的平台和框架。

SimpleLink™ Wi-Fi® CC3220 开箱即用应用 本指南展示了 CC3220 LaunchPad™ 开发套件的开箱即用体验，重点说明它可以使用 SimpleLink™ Wi-Fi® Starter Pro 应用轻松连接到 CC3220 LaunchPad，并介绍了无线更新。

SimpleLink™ Wi-Fi® 和 Internet-on-a-chip™ CC3120 和 CC3220 解决方案无线电工具 这款无线电工具作为直接接入无线电的控制面板，可用于射频 (RF) 评估及获取认证。本指南介绍如何使该工具在德州仪器 (Texas Instruments™) 评估平台（例如 CC3120 器件的 BoosterPack™ 和 FTDI 仿真板或 CC3220 器件的 LaunchPad™）上无缝运行。

SimpleLink™ Wi-Fi® CC3120 和 CC3220 面向移动应用的 配置 本指南介绍了 TI 的 SimpleLink™ Wi-Fi® 配置解决方案，适用于移动 应用，特别是介绍如何使用Android™ 和 iOS® 构建块来满足 UI 要求、进行联网以及配置构建移动应用所需的 API。

SimpleLink™ Wi-Fi® CC3220 开箱即用应用 本指南详细介绍了德州仪器 (Texas Instruments™) 的 CC3220 LaunchPad™ 开发套件所提供的开箱即用 (OOB) 体验。

UniFlash CC3120 和 CC3220 SimpleLink™ Wi-Fi®、Internet-on-a-chip™ 解决方案 ImageCreator 和编程工具
本文档介绍如何安装、操作和使用作为 UniFlash 一部分的 SimpleLink ImageCreator 工具。

更多文献

CC3220、CC3220S、CC3220SF SimpleLink™ Wi-Fi® 和物联网 本技术参考手册详细介绍了 SimpleLink™ CC32xx 无线 MCU 的模块和外设。每个 说明 均从一般意义上介绍模块或外设。可能并未对所有器件上的 所有 模块或外设的所有特性和功能都作出介绍。引脚功能、内部信号连接和操作参数都因器件不同而各异。有关这些细节，用户应查阅具体器件的产品说明书。

RemoTI 清单

CC3120、CC3220 SimpleLink™ Wi-Fi® 和物联网设计检查清单

CC3220 SimpleLink™ Wi-Fi® 和物联网 CC3220 硬件设计文件。

8.5 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **8-1.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
CC3220R	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
CC3220S	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
CC3220SF	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.7 商标

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

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8.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

9.1 封装信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC3220RM2ARGKR	ACTIVE	VQFN	RGK	64	2500	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3220R M2A	Samples
CC3220RM2ARGKT	ACTIVE	VQFN	RGK	64	250	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3220R M2A	Samples
CC3220SF12ARGKR	ACTIVE	VQFN	RGK	64	2500	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3220SF 12A	Samples
CC3220SF12ARGKT	ACTIVE	VQFN	RGK	64	250	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3220SF 12A	Samples
CC3220SM2ARGKR	ACTIVE	VQFN	RGK	64	2500	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3220S M2A	Samples
CC3220SM2ARGKT	ACTIVE	VQFN	RGK	64	250	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3220S M2A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

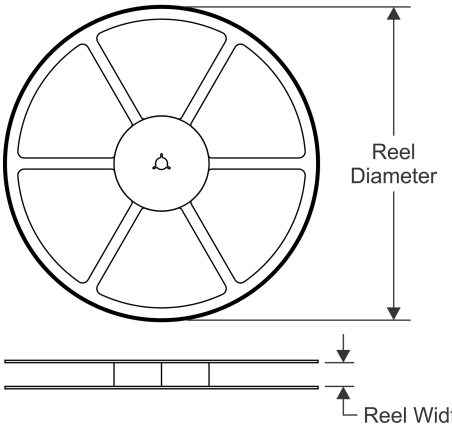
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

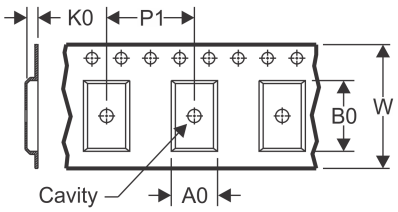
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

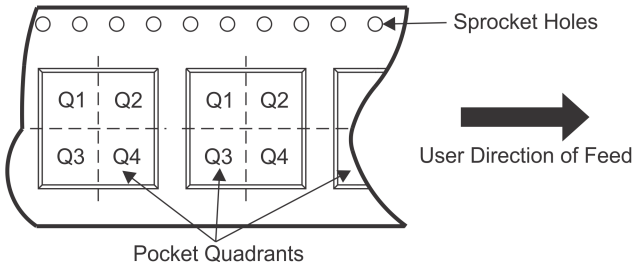


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

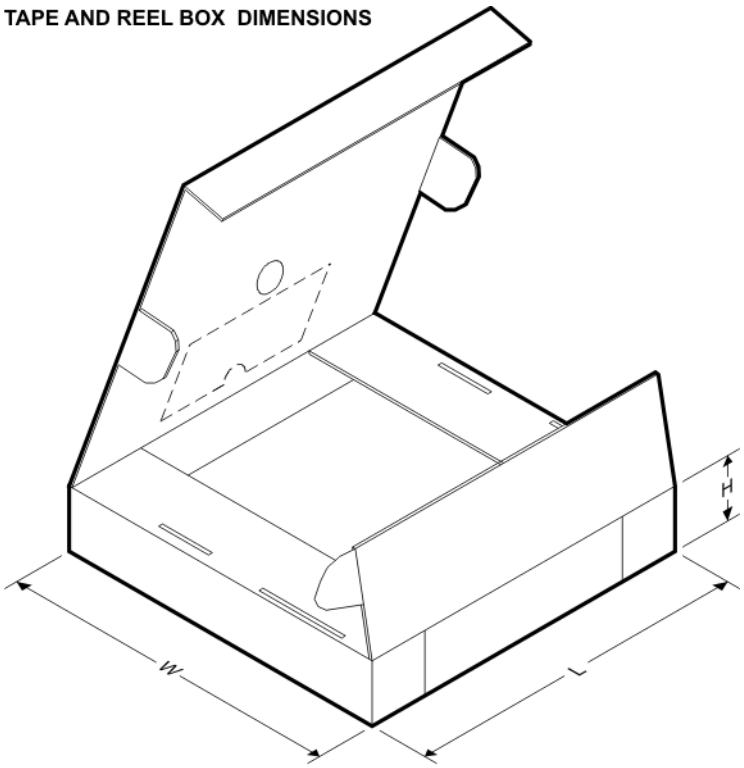
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC3220RM2ARGKR	VQFN	RGK	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3220RM2ARGKR	VQFN	RGK	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3220RM2ARGKT	VQFN	RGK	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3220RM2ARGKT	VQFN	RGK	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3220SF12ARGKR	VQFN	RGK	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3220SF12ARGKR	VQFN	RGK	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3220SF12ARGKT	VQFN	RGK	64	250	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3220SF12ARGKT	VQFN	RGK	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3220SM2ARGKR	VQFN	RGK	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3220SM2ARGKR	VQFN	RGK	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3220SM2ARGKT	VQFN	RGK	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3220SM2ARGKT	VQFN	RGK	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



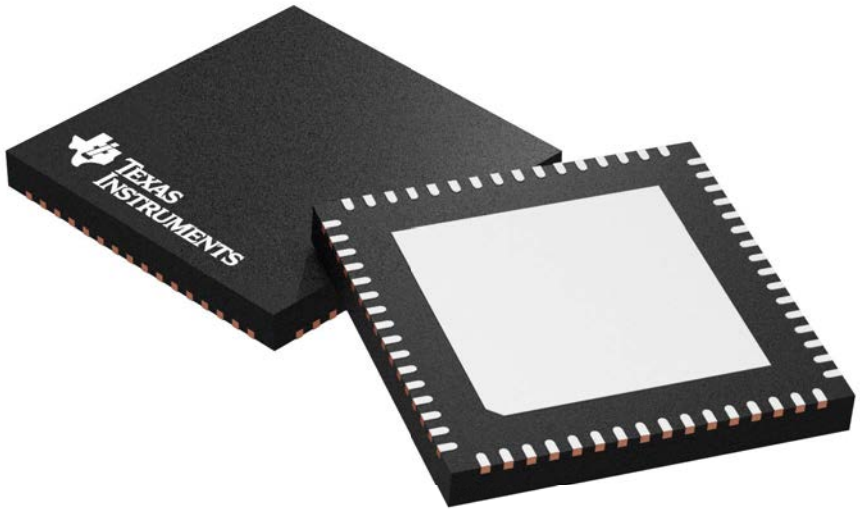
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC3220RM2ARGKR	VQFN	RGK	64	2500	336.6	336.6	31.8
CC3220RM2ARGKR	VQFN	RGK	64	2500	367.0	367.0	38.0
CC3220RM2ARGKT	VQFN	RGK	64	250	210.0	185.0	35.0
CC3220RM2ARGKT	VQFN	RGK	64	250	210.0	185.0	35.0
CC3220SF12ARGKR	VQFN	RGK	64	2500	367.0	367.0	38.0
CC3220SF12ARGKR	VQFN	RGK	64	2500	336.6	336.6	31.8
CC3220SF12ARGKT	VQFN	RGK	64	250	336.6	336.6	31.8
CC3220SF12ARGKT	VQFN	RGK	64	250	210.0	185.0	35.0
CC3220SM2ARGKR	VQFN	RGK	64	2500	336.6	336.6	31.8
CC3220SM2ARGKR	VQFN	RGK	64	2500	367.0	367.0	38.0
CC3220SM2ARGKT	VQFN	RGK	64	250	210.0	185.0	35.0
CC3220SM2ARGKT	VQFN	RGK	64	250	210.0	185.0	35.0

RGK 64

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



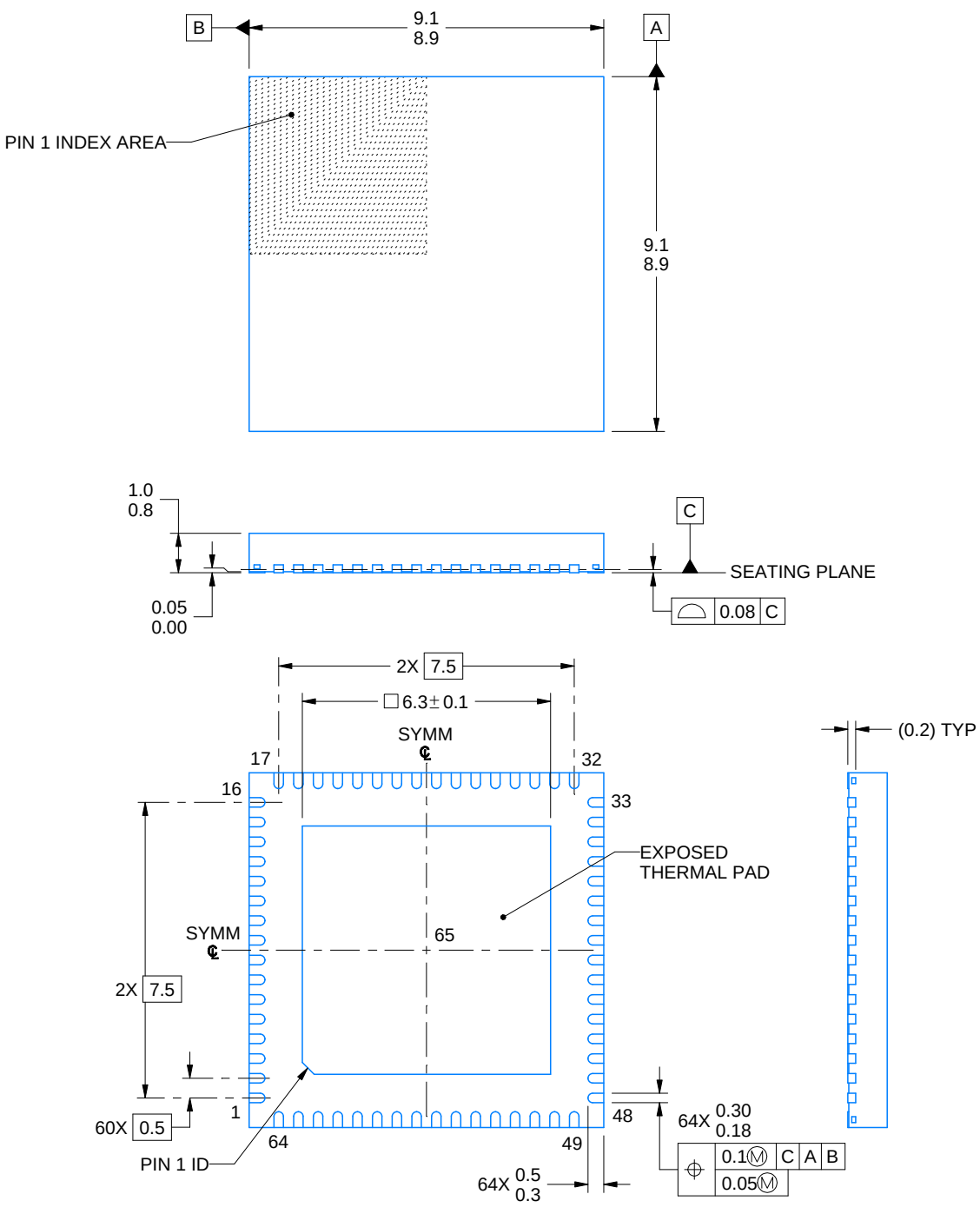
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGK0064B

PACKAGE OUTLINE

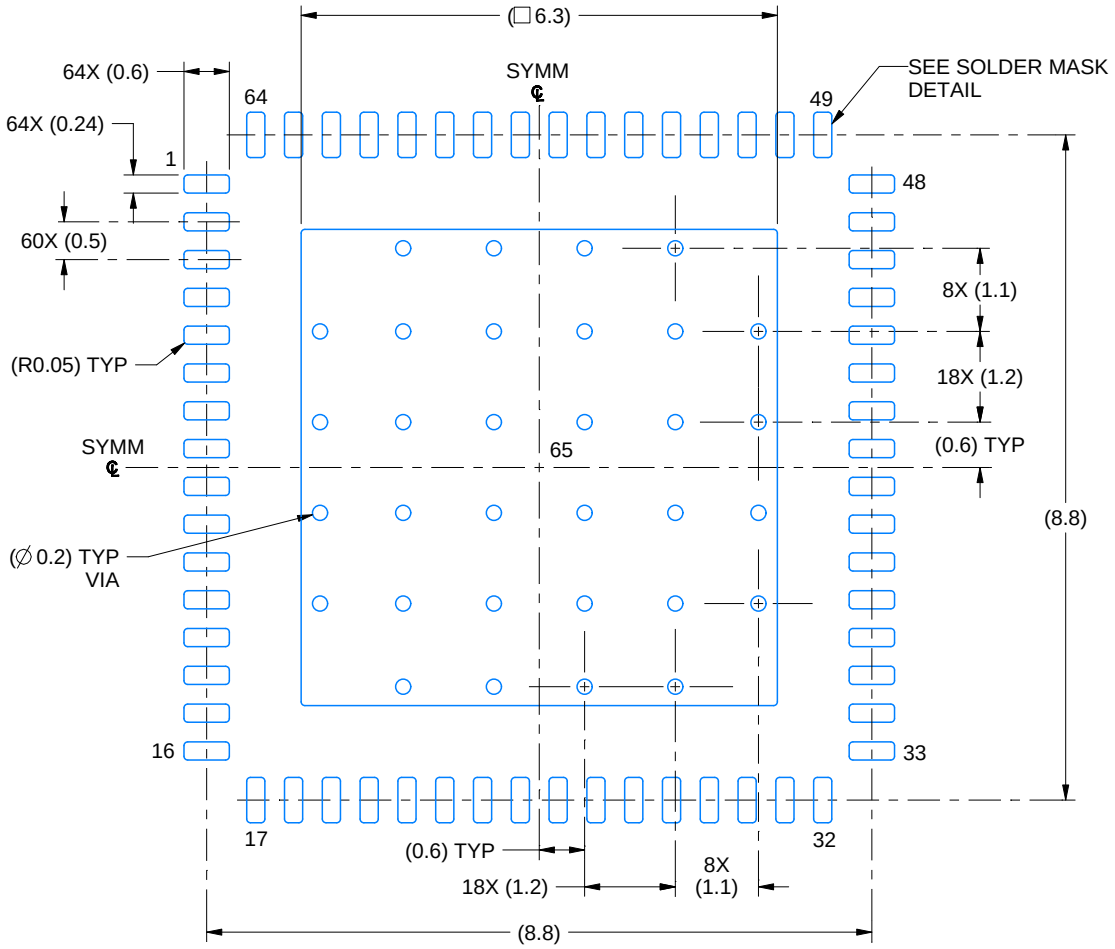
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

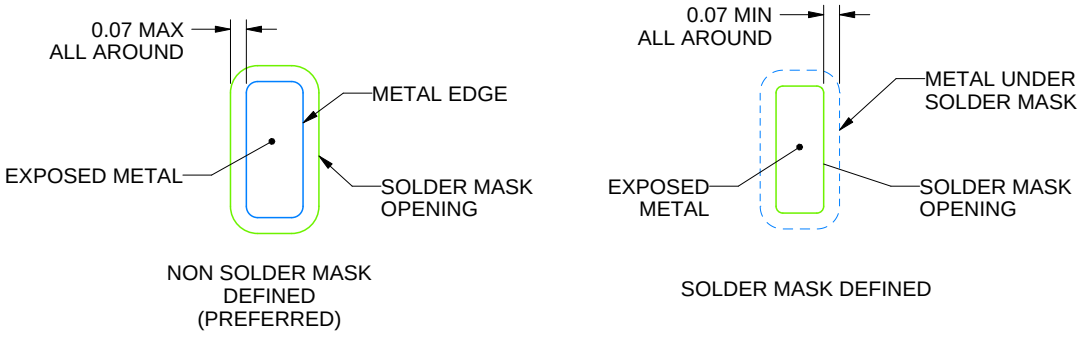


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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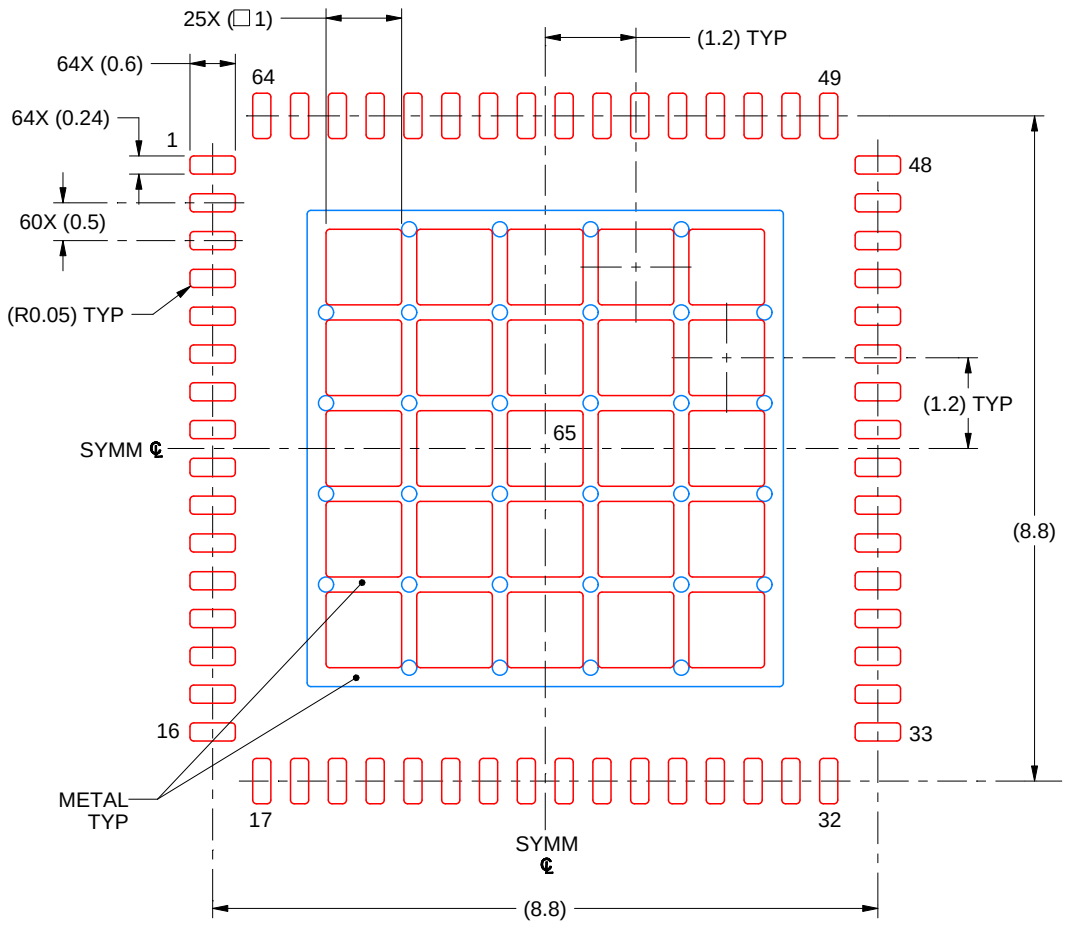
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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