Methods of output-voltage adjustment for DC/DC converters

By Chris Glaser
Member Group Technical Staff, Senior Applications Engineer

Introduction

Some systems benefit by adjusting the output voltage of one or more DC/DC converters while the converters are enabled and the system is operating. Solid-state drives, smartphones and optical modules adjust the core voltage (usually through I^{2}C communication) to the main processor to fine-tune performance and power consumption.

Other, simpler systems such as USB Type-C™ ports and lower-power microcontrollers (MCUs) use a single digital signal to adjust between two output voltages in order to adapt to power delivery demands or reduce power consumption in standby or sleep mode.

Modulators and drivers found in high-speed optical modules and optical line cards may require an adjustable supply voltage, such as a negative voltage for biasing optical circuits. Most LED drivers dim their light output through the same analog voltage or a filtered pulse-width modulation (PWM) signal technique. These types of output-voltage adjustment and their typical use cases are described with numerous applications across a variety of end equipments.

Digital-communication interface

A digital-communication interface, like I^{2}C, generally provides the most control when adjusting the output voltage. I^{2}C requires a system with a communication interface, which in turn requires a host MCU to run the interface as the master device.

The output voltage can typically be set to a large number of discrete values within a given range and with a specific step size. For example, the TPS62866 allows output voltages between 0.4 V and 1.675 V in 5-mV increments. The host processor fine-tunes the output voltage to optimize power consumption and performance on the main processor's core rail. This is known as adaptive voltage scaling (AVS).

In some systems, the host processor is the same as the main processor. This processor controls its own core voltage, which changes based on the operating conditions and tasks being executed. The converter's default or startup voltage is critical because it must be high enough to properly boot the processor before the processor can

Figure 1. Example of using the VSET pin to set a converter's default or startup voltage
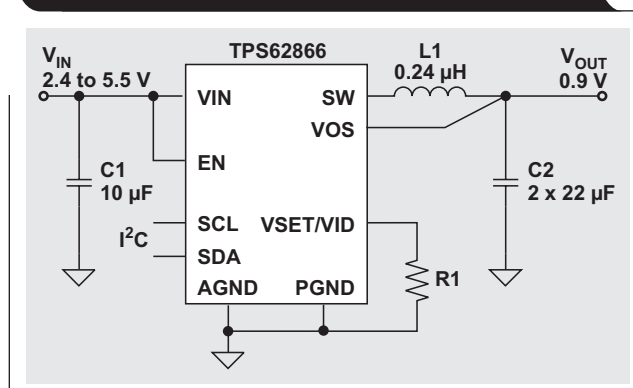
operate the I^{2}C bus and program the output voltage.

Figure 1 shows an application schematic of the TPS62866 and its voltage-setting (VSET) pin, which enables setting the startup voltage in hardware before the I^{2}C bus is active with resistor R1 based on the specific processor used.

The TPS62866 integrates a resistor-to-digital (R2D) converter on the VSET/VID pin, which reads this resistor value at startup and programs the device. Setting the output voltage with a VSET pin saves one feedback (FB) resistor (and its cost and size); increases output voltage accuracy by not including the inaccuracy of the two FB resistors; and provides lower leakage current because the resistor value is only measured at startup and consumes no current afterwards.

The main disadvantage of the VSET pin in devices without an I^{2}C bus is that the output voltage cannot be changed during operation because the resistor value is only measured at startup. The TPS62866 overcomes this limitation by combining the VSET pin with a function for voltage identification definition (VID). After startup, the pin functions as a digital input to change the output

voltage. Table 1 shows the different configurations of output voltages and I²C addresses possible with the R1 resistor and VSET pin.

A digital-communication interface also allows much more system control, interaction and fault reporting. The TPS62866's I²C registers contain other settings, including device enable, device reset, programmable slew rate when changing output voltages, mode selection for either light-load efficiency or lowest ripple, overtemperature warning, current-limit indication, and power-good indication.

A power-management bus (PMBus), another digital-communication interface based on the I²C physical layer, allows digital control of a power supply with a communications protocol and command language. The main difference between PMBus and I²C is that no I²C code is required; with PMBus, the programming, monitoring and fault commands can be selected from a preselected command set. PMBus is usually used in applications with output voltage adjustment when high flexibility and reconfigurability are required. Figure 2 shows a typical PMBus multiphase application using the TPS40428 dual-phase, dual-output buck controller.

Table 1. VSET pins set the startup output voltage with a single resistor within a predefined set of values

R1 Resistor (E96 Series) at VSET/VID pin	Default Output Voltage (V)	Device Address
249 k	1.15 V	1000 110
205 k	1.10 V	1000 101
162 k	1.05 V	1000 100
133 k	1.00 V	1000 011
105 k	0.95 V	1000 010
86.6 k	0.90 V	1000 001
68.1 k	0.85 V	1001 000
56.2 k	0.80 V	1001 001
44.2 k	0.75 V	1001 010
36.5 k	0.70 V	1001 011
28.7 k	0.65 V	1001 100
23.7 k	0.60 V	1001 101
18.7 k	0.55 V	1001 110
15.4 k	0.50 V	1001 111
12.1 k	0.45 V	1000 000
10 k	0.40 V	1000 111

Figure 2. TPS40428 dual buck controller with PMBus (PMBDATA, PMBCLK and SMBALERT pins)
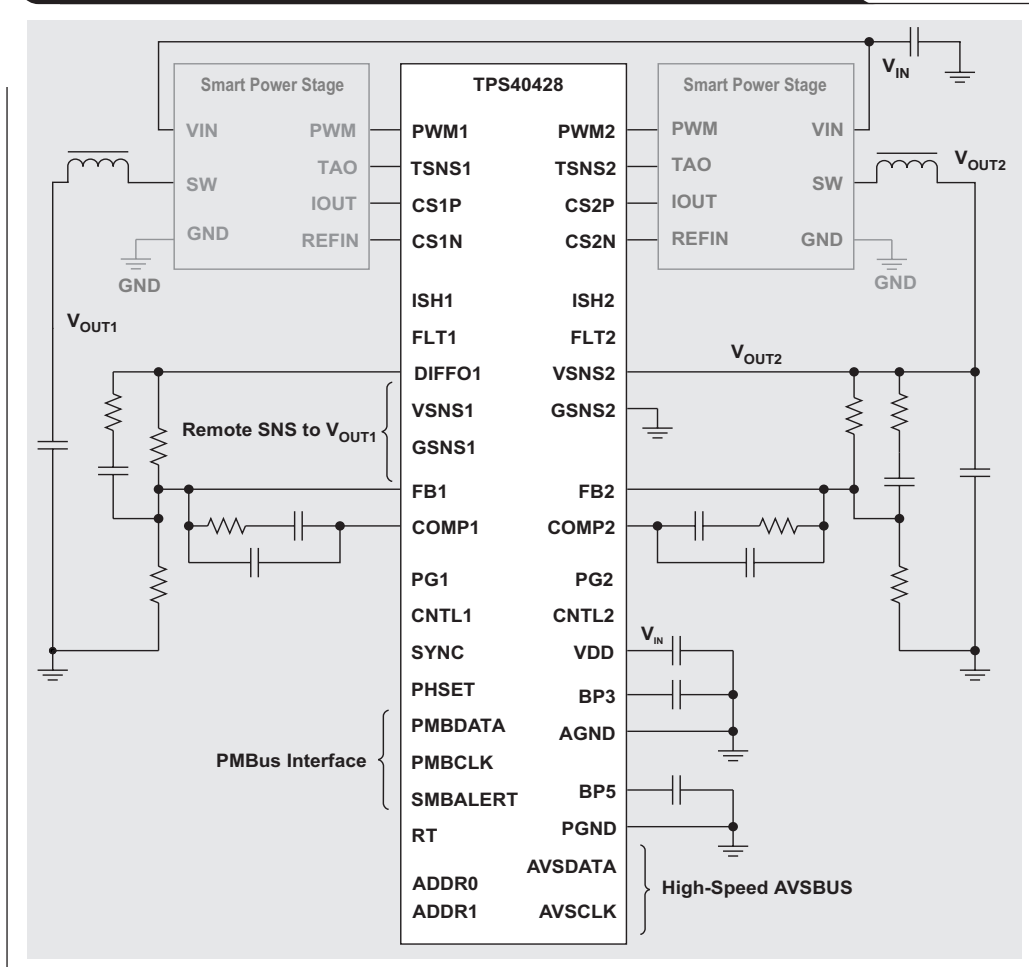
Digital input(s)

A single digital-input signal is the simplest way to adjust the output between two voltages. This method requires a general-purpose input/output (GPIO) pin of the host MCU (or any other digital signal). Changing the output voltage between two states during operation is useful for USB Type-C ports, which deliver more power at voltages higher than 5 V. Some MCUs also use dynamic voltage scaling (DVS) to reduce power consumption in operating modes such as standby or sleep, which operate with a lower supply voltage. This is called a voltage select (VSEL) function and is a dedicated pin on some devices, such as the TPSM82480 and TPS62136.

The VSEL technique described in Reference 1 changes the voltage of a USB Type-C port from the standard 5-V to a higher 9-V fast-charging level. Figure 3 shows the typical VSEL circuit and Figure 4 shows the resulting change in output voltage. Generally, the output-voltage slew rate is not controllable when using a VSEL pin. The circuit's control loop operates quickly to bring the output voltage to the new regulation point.

Some VSEL pins operate with a VID function for powering processor-core voltage rails, where the connection of the VSELx pins directly controls the output-voltage set point. The margining transistor and resistor are internal. The VSELx pins can connect to fixed logic levels, MCU pins or discrete logic.

The TPS62866 shown in Figure 1 combines its VSET pin with a VID pin so that the startup voltage is set, then the output voltage is changed after startup through the same pin. The TPS62802 contains a similar multifunction pin with its VSEL/MODE pin. The VSEL portion operates like a VSET pin, setting the output voltage with a single resistor. After startup, the MODE function changes the device from power-save mode to a lower-noise and less-efficient forced PWM mode.

In some ultra-low-power devices, the FB resistors and connections are completely internal and the output voltage is only changed via the VSELx pins. This internal configuration can achieve much higher impedance to achieve ultra-low power and still be immune to noise coupling. With external FB resistors, the FB net is larger and therefore has greater coupling to other nets, which requires a higher FB resistor current. Table 2 shows 16 possible output voltage settings for the TPS62745 and its four VSELx pins. The VSELx pins are changeable during operation but do not allow output-voltage adjustment outside the listed values.

Figure 3. A VSEL pin integrates the required transistor to achieve voltage margining through resistor R3
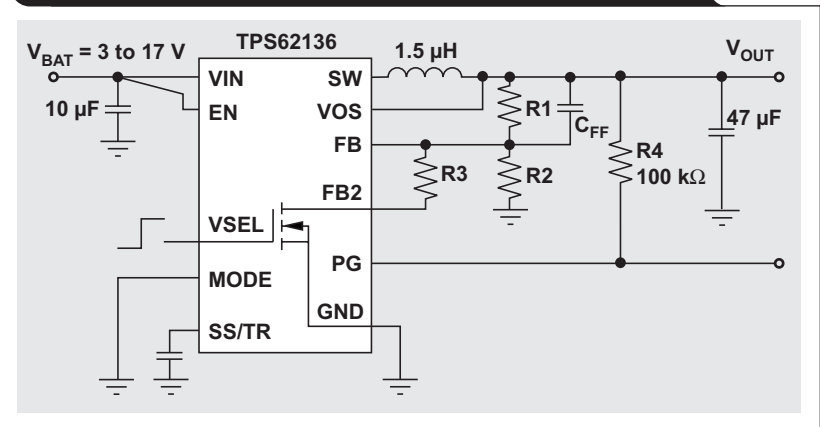
Figure 4. Voltage margining through the VSEL pin changes the output voltage
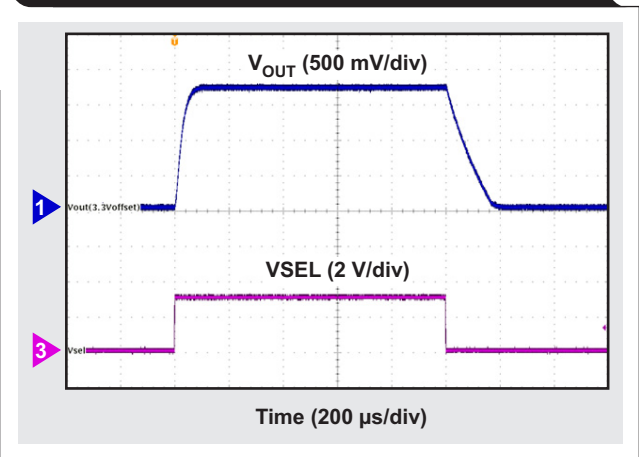
Table 2. Some VSEL pins set the output voltage within a pre-defined set of values

Device	V_{OUT} (V)	VSEL 4	VSEL 3	VSEL 2	VSEL 1
TPS62745	1.8	0	0	0	0
	1.9	0	0	0	1
	2	0	0	1	0
	2.1	0	0	1	1
	2.2	0	1	0	0
	2.3	0	1	0	1
	2.4	0	1	1	0
	2.5	0	1	1	1
	2.6	1	0	0	0
	2.7	1	0	0	1
	2.8	1	0	1	0
	2.9	1	0	1	1
	3	1	1	0	0
	3.1	1	1	0	1
	3.2	1	1	1	0
	3.3	1	1	1	1

Analog voltage input

The final type of output-voltage adjustment uses an analog signal to control the output voltage. This analog signal, fed into the FB pin through a resistor, is usually generated from a voltage reference, either a discrete voltage reference like the TLV431 or an analog output created from the voltage reference inside an MCU, the current or voltage output of a digital-to-analog converter (DAC), or a PWM signal filtered with a simple resistor-capacitor (RC) filter. With an analog voltage, any output voltage is attain-able, instead of just discrete settings as with the previ-ously discussed methods. This is critical for analog LED dimming, which requires a gradual change in light output instead of larger step changes. A fully adjustable output voltage also allows fine-tuning of analog-circuit biasing.

The filtered PWM-signal method requires just a single GPIO pin of an MCU, two resistors and one capacitor. Using a DAC instead of a PWM signal gives a cleaner output voltage, with no possibility of a PWM frequency appearing on the output rail. A DAC also eliminates issues arising from variation in the PWM signal's RC filter over temperature or component tolerance.

Reference 2 and Equations 1 through 3 show details of the necessary calculations for basic output-voltage adjust-ment from an analog voltage. Using the same calculations with the TPS62088 and DAC53608 generates an output voltage between 0.3 V and 1.8 V from a DAC output voltage between 0.3 V and 3 V. Figure 5 shows the tested schematic. Figure 6 shows measured data (with a 3.3-V input voltage and 1-A load) compared to the ideal curve, with nearly perfect matching. Equation 1 gives the transfer function of the analog voltage to the output voltage, while Equations 2 and 3 select the proper resistor values.

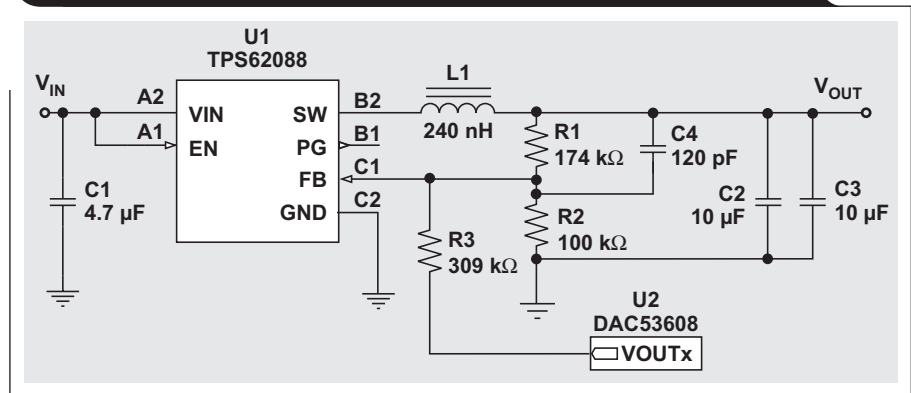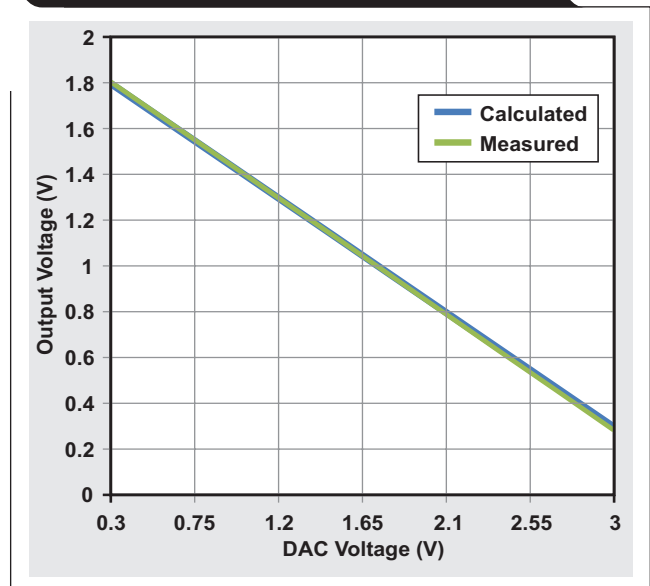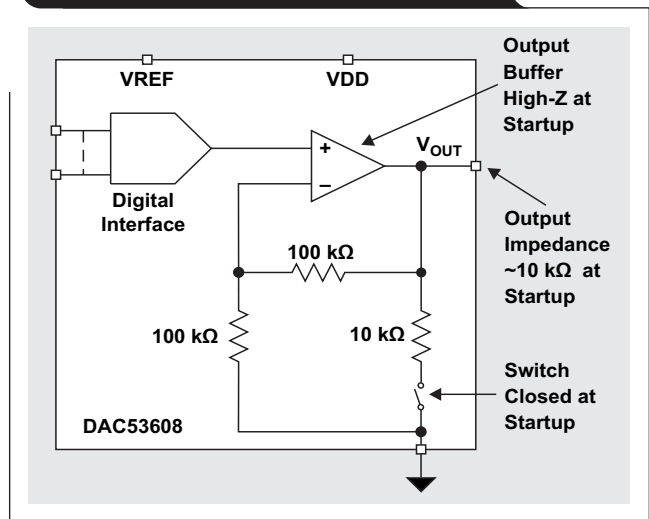**Figure 5. The DAC53608 adjusts the TPS62088's output voltage**

Figure 6. Comparison of measured output voltage adjustment to calculated

$$V_{OUT} = V_{FB}\left(1 + \frac{R1}{R2}\right) - \frac{R1}{R3}\left(V_{DAC} - V_{FB}\right) \tag{1}$$

$$R2 = -V_{FB} \times R1 \times \frac{V_{DACLOW} - V_{DACHI}}{\left(V_{OUTLOW} - V_{OUTHI} + V_{DACLOW} - V_{DACHI}\right) \times V_{FB} - \left(V_{DACLOW} \times V_{OUTLOW}\right) + \left(V_{DACHI} \times V_{OUTHI}\right)} \tag{2}$$

$$R3 = R2 \times R1 \times \frac{V_{DACHI} - V_{FB}}{\left(R2 \times V_{FB}\right) + \left(R1 \times V_{FB}\right) - \left(R2 \times V_{OUTLOW}\right)} \tag{3}$$

A further benefit of the DAC53608 is that its disabled outputs have a defined ~10-kΩ pulldown, as Figure 7 shows. This internal pulldown resistor eliminates the disabled-to-enabled power-on glitch from the DAC's output, which can cause transients on the output voltage during startup. Such glitches can potentially have a catastrophic impact on the load.

Figure 8 uses this same analog voltage-margining technique for a negative voltage, based on Reference 3. Using the TPS82130 power module in the inverting buck-boost configuration creates a variable negative-output voltage, useful for optical circuit biasing. Figure 9 shows very good matching until the lowest output voltages.

Equation 4 gives the transfer function from DAC voltage to output voltage.

$$V_{OUT} = \frac{\dfrac{-V_{FB}}{R2} - \dfrac{V_{FB}}{R1} - \dfrac{V_{FB}}{R3} + \dfrac{V_{DAC}}{R3}}{\dfrac{1}{R1} + \dfrac{1}{R3}} \qquad (4)$$

Figures 6 and 9 also show a hidden benefit of analog voltage margining: adding a voltage into the FB pin achieves output voltages below the converter's FB pin voltage. The margining circuit shown in Figure 5 achieves a 0.3-V output voltage even with the TPS62088's 0.6-V FB pin voltage, while Figure 8 achieves voltages below –0.5 V even with the TPS82130's 0.8-V FB pin voltage. Such circuits can also be used with a fixed analog voltage instead of an adjustable DAC. Reference 4 uses this method to increase LED driver efficiency.

If no available analog voltage exists, an RC filter can create one by filtering a PWM signal. The frequency is held constant, while the duty cycle varies to adjust the resulting analog voltage. Reference 5 explains such a circuit for LED dimming applications. For DC/DC converters, the PWM frequency should be above the control-loop bandwidth, to allow easier filtering and to prevent the control loop from gaining up the frequency of the PWM signal and appearing on the output voltage.

Figure 7. The DAC53608 has a ~10-kΩ resistance to ground at startup

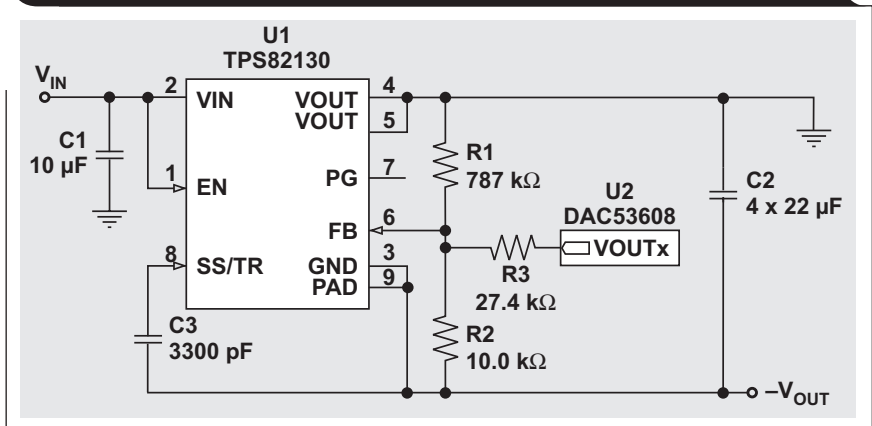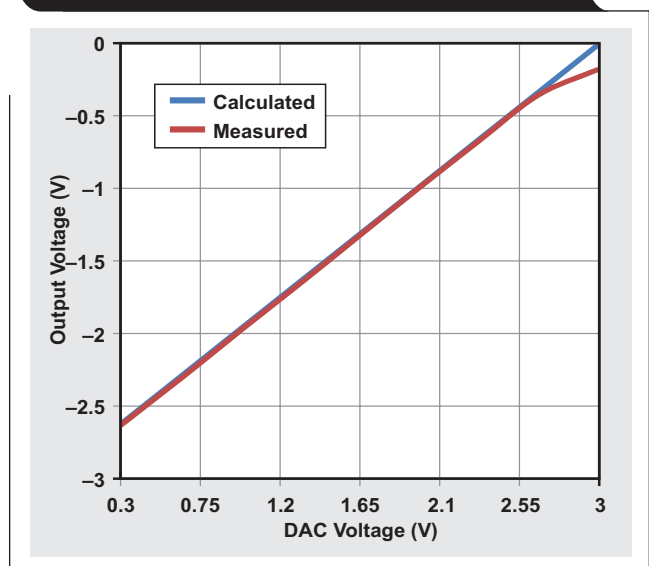Figure 8. DAC53608 adjusts the TPS82130's negative output voltage

Figure 9. Comparison of measured negative output voltage adjustment to calculated

A 1-MHz PWM signal replaces the DAC shown in Figure 5 to create Figure 10, which shows that the RC-filtered PWM signal creates an analog voltage to adjust the TPS62088's output voltage. Figure 11 shows the margining performance. As the PWM signal's duty cycle increases, the analog voltage created by the RC filter increases and the output voltage decreases. To adapt Equation 1 to use with a PWM signal, replace V_{DAC} with $[D \times V_{PWMHI} - (1 - D) \times V_{PWMLOW}]$ and R3 with $(R3 + R_{filter})$.

Any of these three methods—DAC output, analog voltage or filtered PWM signal—generate an analog output that adjusts the output voltage. Simple systems use a filtered PWM signal or spare MCU analog output to adjust the voltage on one rail. As the number of voltages needing adjustment increases, a multichannel DAC becomes a more cost- and space-effective solution, since it's possible to control more DAC outputs on the same interface bus without an increase in MCU pins or additional circuitry. With the filtered PWM-signal method, every extra rail requires an additional MCU pin and RC filter.

Reference 6 is a calculator spreadsheet which aids in the design and analysis of both the positive- and negative-output voltage circuits shown in Figures 5 and 8.

Conclusion

Changing the output voltage can optimize power delivery, reduce power consumption, or properly bias analog circuits such as LED drivers and optics. Three basic tech-niques—a digital communication interface, digital input and analog input—adjust the output voltage differently to match specific requirements. The examples shown in this article demonstrated common adjustment techniques that are transferable to your specific system and design challenges.

References

1. "Voltage-Margining Power Supply for USB Type-C Ports in Docking Stations," Texas Instruments reference design (TIDA-01567).

2. Will Hadden, "Dynamically Adjustable Output Using TPS63000," Texas Instruments application report (SLVA251), August 2006.

3. "3- to 11.5-VIN, –5-VOUT, 1.5-A Inverting Power Module Reference Design for Small, Low-Noise Systems," Texas Instruments reference design (TIDA-01457).

4. Jeurgen Neuhaeusler, "Different Methods to Drive LEDs Using TPS630xx Buck-Boost Converters," Texas Instruments application report (SLVA419B), January 2012.

5. Matt Guibord, "How to Use Analog Dimming with the TPS6116x," Texas Instruments application report (SLVA471), July 2011.

6. Design Tool for Output Voltage Adjustment using a DAC (SLVC780), Texas Instruments, 2019

Figure 10. RC-filtered PWM signal controls the output voltage

Figure 11. Output voltage margining by a PWM signal

Related Web sites

Product information:

TPS62866, TPS40428, TPSM82480, TPS62136, TPS62802, TPS62745, TLV431, TPS62088, DAC53608, TPS82130

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