MSP430FR413x 混合信号微控制器

1 器件概述

1.1 特性

- 嵌入式微控制器
  - 频率高达 16MHz 的 16 位精简指令集计算机 (RISC) 架构
  - 3.6V 至 1.8V 的宽电源电压范围（最低电源电压受限于 SVS 电平，请参阅 SVS 规格）
- 经优化的低功耗模式（3V 时）
  - 激活模式：126µA/MHz
  - 待机模式：<1µA，实时时钟 (RTC) 计数器和液晶显示器 (LCD) 处于工作状态
  - 关断 (LPM4.5)：15nA
- 高性能模拟
  - 10 通道 10 位模数转换器 (ADC)
    - 1.5V 的内部基准电压
    - 采样与保持 200ksps
  - 低功耗 LCD 驱动器
    - 支持高达 4×36 段或 8×32 段 LCD 配置
    - 片上电荷泵，在待机模式 (LPM3.5) 下可使 LCD 保持激活状态
    - 每个 LCD 引脚均可通过软件配置为 SEG 或 COM
    - 在 2.6V 至 3.5V 范围内提供对比度控制（阶跃为 0.06V）
- 低功耗铁电 RAM (FRAM)
  - 容量高达 15.5KB 的非易失性存储器
  - 内置错误修正码 (ECC)
  - 可配置的写保护
  - 对程序、常量和存储的统一存储
  - 耐写次数达 10^{15} 次
  - 抗辐射和非磁性
- 智能数字外设
  - 红外调制逻辑
  - 两个 16 位定时器，每个定时器有 3 个捕捉/比较寄存器 (Timer_A3)
  - 一个仅用作计数器的 16 位 RTC 计数器
  - 16 位循环冗余校验器 (CRC)
- 增强型串行通信
  - 增强型 USCI A (eUSCI_A) 支持 UART、IrDA 和 SPI
  - 增强型 USCI B (eUSCI_B) 支持 SPI 和 I^2C
- 时钟系统 (CS)
  - 片上 32kHz RC 振荡器 (REFO)
  - 带有锁频环 (FLL) 的片上 16MHz 数控振荡器 (DCO)
    - 室温下的精度为 ±1%（具有片上基准）
  - 片上超低频 10kHz 振荡器 (VLO)
  - 片上高频调制振荡器时钟 (MODCLK)
  - 外部 32kHz 晶振 (XT1)
  - 可编程 MCLK 预分频器（1 至 128）
  - 通过可编程预分频器（1、2、4 或 8）从 MCLK 获得的 SMCLK
- 通用输入/输出和引脚功能
  - 60 个 I/O（64 引脚封装）
  - 16 个中断引脚（P1 和 P2）可以将 MCU 从 LPM 唤醒
  - 所有 I/O 均为电容式触摸 I/O
- 开发工具和软件
  - 开发套件（MSP-EXP430FR4133 LaunchPad™ 开发套件和 MSP-TS430PM64D 目标开发板）
  - 免费软件（ MSP430Ware™ 软件）
- 系列成员（另请参阅 器件比较）
  - MSP430FR4133：15KB 程序 FRAM + 512B 信息 FRAM + 2KB RAM
  - MSP430FR4132：8KB 程序 FRAM + 512B 信息 FRAM + 1KB RAM
  - MSP430FR4131：4KB 程序 FRAM + 512B 信息 FRAM + 512B RAM
- 封装选项
  - 64 引脚：LQFP (PM)
  - 56 引脚：TSSOP (G56)
  - 48 引脚：TSSOP (G48)
- 有关完整的模块说明，请参阅 *《MSP430FR4xx 和 MSP430FR2xx 系列器件用户指南》*

1.2 应用

- 遥控
- 恒温器
- 水表
- 热量计
- 燃气表
- 一次性密码令牌
- 血糖监测仪
- 血压监护仪

1.3 说明

MSP430FR41xx 超低功耗 (ULP) 微控制器系列支持各种低成本 LCD 应用， 如远程控制、恒温器、智能仪表、血糖监测仪和血压监测仪等，该系列器件的集成 10 位 ADC 对这些应用的性能提升大有帮助。MCU 具有功能强大的 16 位 RISC CPU、16 位寄存器和常数发生器，有助于实现最大编码效率。数控振荡器 (DCO) 可使器件在不到 10µs 的时间内从低功耗模式唤醒至活动模式。该架构与多种低功耗模式配合使用，经过优化，可在便携式测量应用延长电池 寿命。

该 MSP430™FRAM 微控制器平台将独特的嵌入式铁电随机存取存储器 (FRAM) 和全面的超低功耗系统架构相结合，从而使系统设计人员能够在降低能耗的同时提升性能。FRAM 技术将 RAM 的低功耗快速写入、灵活性和耐用性与闪存的非易失性相结合。

MSP430FR41x MCU 由一个由各种软、硬件资源组成的生态系统提供支持，并配套提供有参考设计和代码示例，可帮助您快速开展设计。MSP430FR41xx 的开发套件包括 MSP-EXP430FR4133 LaunchPad™开发套件和 MSP-TS430PM64D 64 引脚目标开发板。TI 还提供免费的 MSP430Ware™ 软件，该软件作为 Code Composer Studio™IDE 桌面和云端版本组件的形式在 TI 资源管理器内部提供。MSP430 MCU 还通过 E2E™ 论坛提供广泛的在线配套资料、培训和在线支持。

器件信息(1)

器件型号	封装	封装尺寸(2)
MSP430FR4133IPM	LQFP (64)	10mm x 10mm
MSP430FR4133IG56	TSSOP (56)	14mm x 6.1mm
MSP430FR4133IG48	TSSOP (48)	12.5mm x 6.1mm

(1) 要获得最新的产品、封装和订购信息，请参见*封装选项附录*（节 9），或者访问德州仪器 (TI) 网站 www.ti.com.cn。
(2) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参见*机械数据*（节 9）。

1.4 功能框图

图 1-1 给出了功能框图。

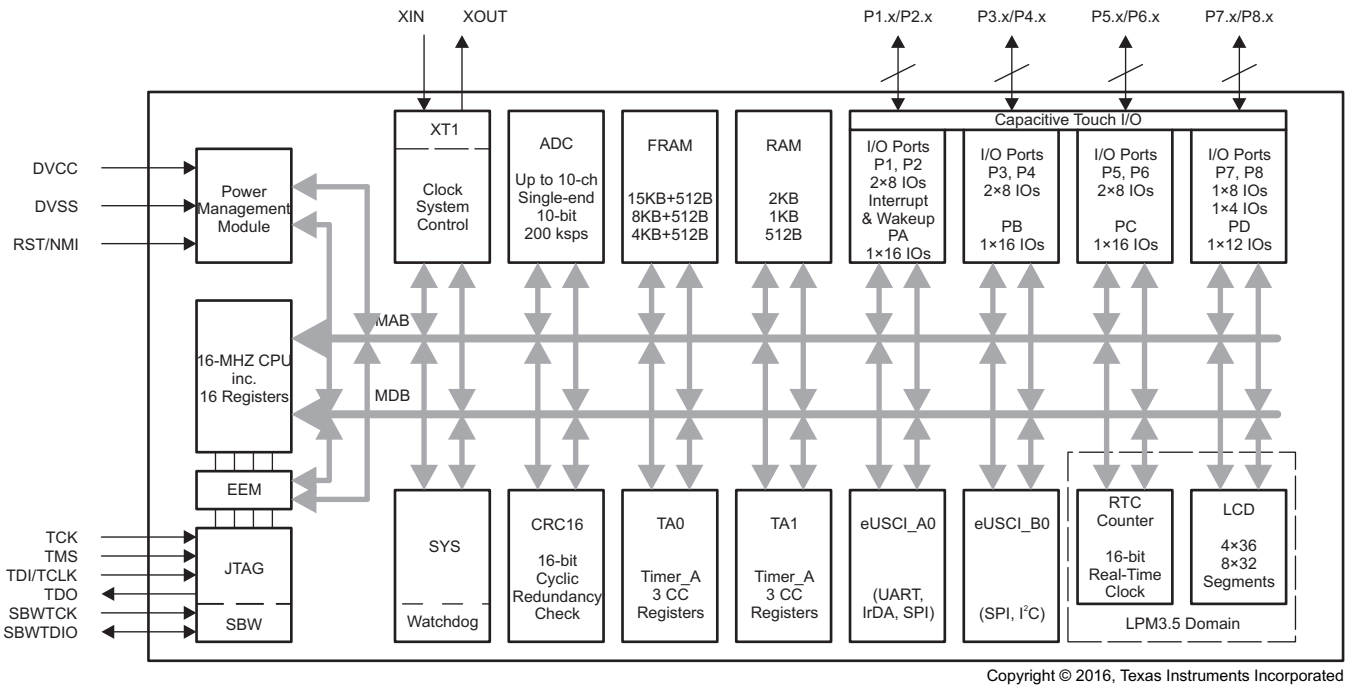

图 1-1. 功能框图

- 该器件具有一对主电源（DVCC 和 DVSS），分别为数字和模拟模块供电。推荐的旁路和去耦电容分别为 4.7µF 至 10µF 和 0.1µF，精度为 ±5%。
- P1 和 P2 特有引脚中断功能，可将 MCU 从 LPM3.5 模式唤醒。
- 每个 Timer_A3 均有 3 个 CC 寄存器，不过只有 CCR1 和 CCR2 从外部连接。CCR0 寄存器仅用于内部周期时序和产生中断。
- 在 LPM3.5 模式下，RTC 计数器与 LCD 可继续工作，而其余外设会停止工作。
- 所有 I/O 均可配置为电容式触摸 I/O。

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2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from August 29, 2018 to January 17, 2019 **Page**

- 已通篇将调制振荡器 (MODOSC) 更改为调制振荡器时钟 (MODCLK) 1
- Added "or memory corruption" in table that starts "Stresses beyond those listed..." of Section 5.1, *Absolute Maximum Ratings* 14
- Added note of VLO clock frequency shift in LPM3 and LPM4 mode in Table 5-6, *Internal Very-Low-Power Low-Frequency Oscillator (VLO)* 23
- Changed from R_I to $R_{I,MUX}$ in Table 5-17, *ADC, Power Supply and Input Range Conditions* 32
- Added $R_{I,Misc}$ TYP value 34kΩ in Table 5-17, *ADC, Power Supply and Input Range Conditions* 32
- Removed ADCDIV from the formula because ADCCLK is after division in Table 5-18, *ADC, 10-Bit Timing Parameters* 32
- Added formula for R_I calculation in Table 5-18, *ADC, 10-Bit Timing Parameters* 32
- Remove description of "±3°C" in table note that starts "The device descriptor structure ..." of Table 5-19, *ADC, 10-Bit Linearity Parameters* 33
- Add "10b" for ADCSSEL bit in Table 6-6, *Clock Distribution* 41
- Added "Clock Distribution Block Diagram" in Section 6.9.2, *Clock System (CS) and Clock Distribution* 41
- Corrected bitfield from IRDSEL to IRDSSEL in Section 6.9.8, *Timers (Timer0_A3, Timer1_A3)*, in the description that starts "The interconnection of Timer0_A3 and ..." 46
- Corrected the ADCINCHx column heading in Table 6-12, *ADC Channel Connections* 47
- Added word "Sensor" in Table 6-27, *Device Descriptors* 66
- Added word "Sensor" in Table 6-27, *Device Descriptors* 66

3 Device Comparison

Table 3-1 summarizes the features of the available family members.

Table 3-1. Device Comparison(1)(2)

DEVICE	PROGRAM FRAM + INFORMATION FRAM (BYTES)	SRAM (BYTES)	TA0, TA1	eUSCI_A	eUSCI_B	10-BIT ADC CHANNELS	LCD SEGMENTS	I/O	PACKAGE TYPE
MSP430FR4133IPM	15360 + 512	2048	3 × CCR(3)	1	1	10	4 × 36 8 × 32	60	64 PM (LQFP)
MSP430FR4132IPM	8192 + 512	1024	3 × CCR(3)	1	1	10	4 × 36 8 × 32	60	64 PM (LQFP)
MSP430FR4131IPM	4096 + 512	512	3 × CCR(3)	1	1	10	4 × 36 8 × 32	60	64 PM (LQFP)
MSP430FR4133IG56	15360 + 512	2048	3 × CCR(3)	1	1	8	4 × 30 8 × 26	52	56 DGG (TSSOP56)
MSP430FR4132IG56	8192 + 512	1024	3 × CCR(3)	1	1	8	4 × 30 8 × 26	52	56 DGG (TSSOP56)
MSP430FR4131IG56	4096 + 512	512	3 × CCR(3)	1	1	8	4 × 30 8 × 26	52	56 DGG (TSSOP56)
MSP430FR4133IG48	15360 + 512	2048	3 × CCR(3)	1	1	8	4 × 24 8 × 20	44	48 DGG (TSSOP48)
MSP430FR4132IG48	8192 + 512	1024	3 × CCR(3)	1	1	8	4 × 24 8 × 20	44	48 DGG (TSSOP48)
MSP430FR4131IG48	4096 + 512	512	3 × CCR(3)	1	1	8	4 × 24 8 × 20	44	48 DGG (TSSOP48)

(1) For the most current device, package, and ordering information, see the *Package Option Addendum* in 节 9, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit Microcontrollers High-performance, low-power solutions to enable the autonomous future

Products for MSP430 Ultra-Low-Power Sensing and Measurement Microcontrollers One platform. One ecosystem. Endless possibilities.

Products for MSP430 Value Line Microcontrollers Low-cost, ultra-low-power MCUs for simple sensing and measurement applications

Companion Products for MSP430FR4133 Review products that are frequently purchased or used with this product.

Reference Designs for MSP430FR4133 The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout of the 64-pin PM package.

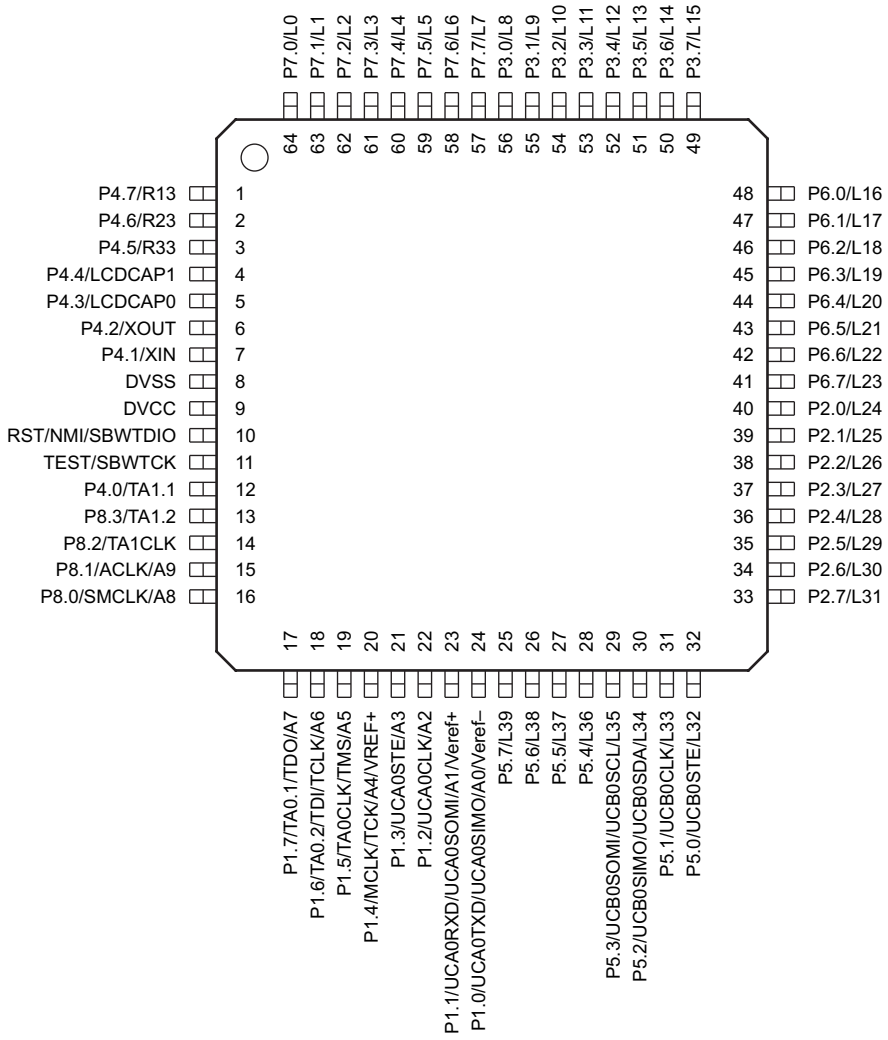


Figure 4-1. 64-Pin PM (LQFP) (Top View)

Figure 4-2 shows the pinout of the 56-pin DGG package.

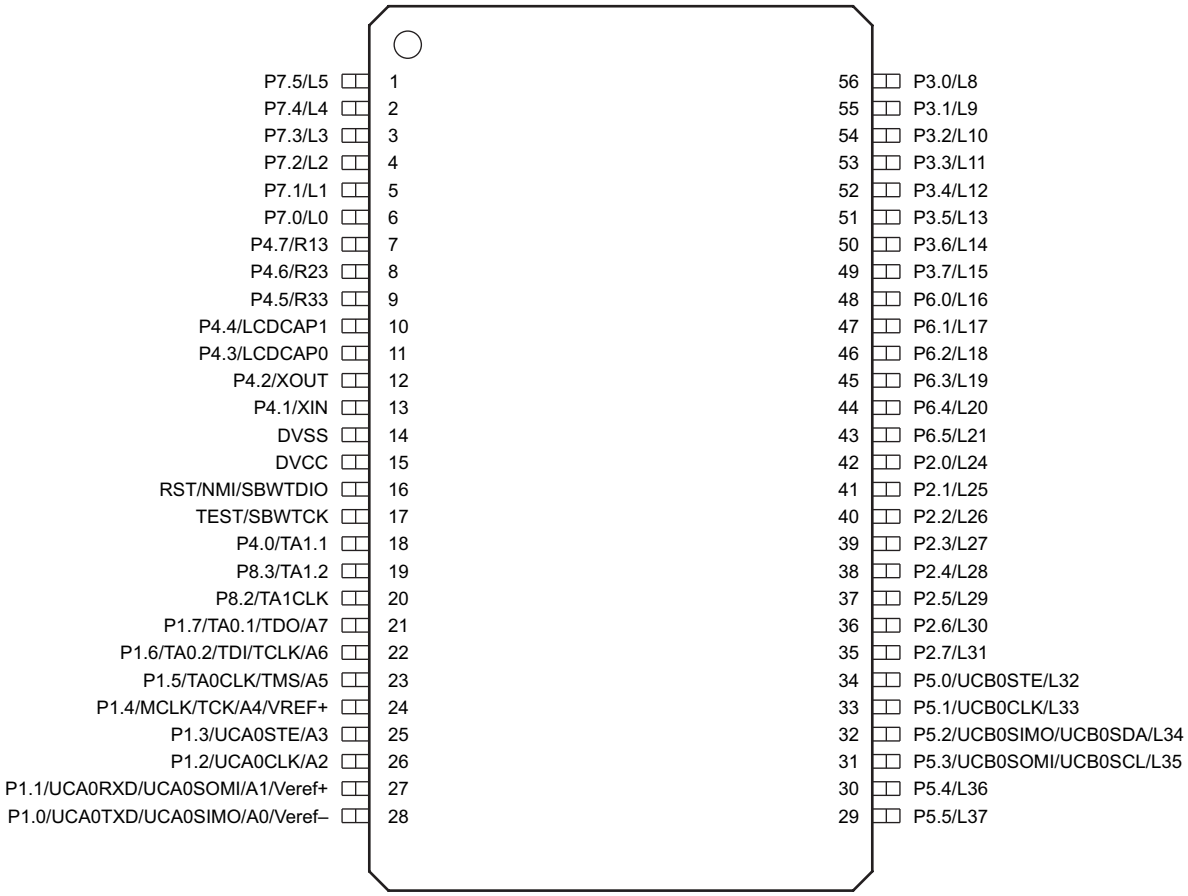


Figure 4-2. 56-Pin DGG (TSSOP) (Top View)

Figure 4-3 shows the pinout of the 48-pin DGG package.

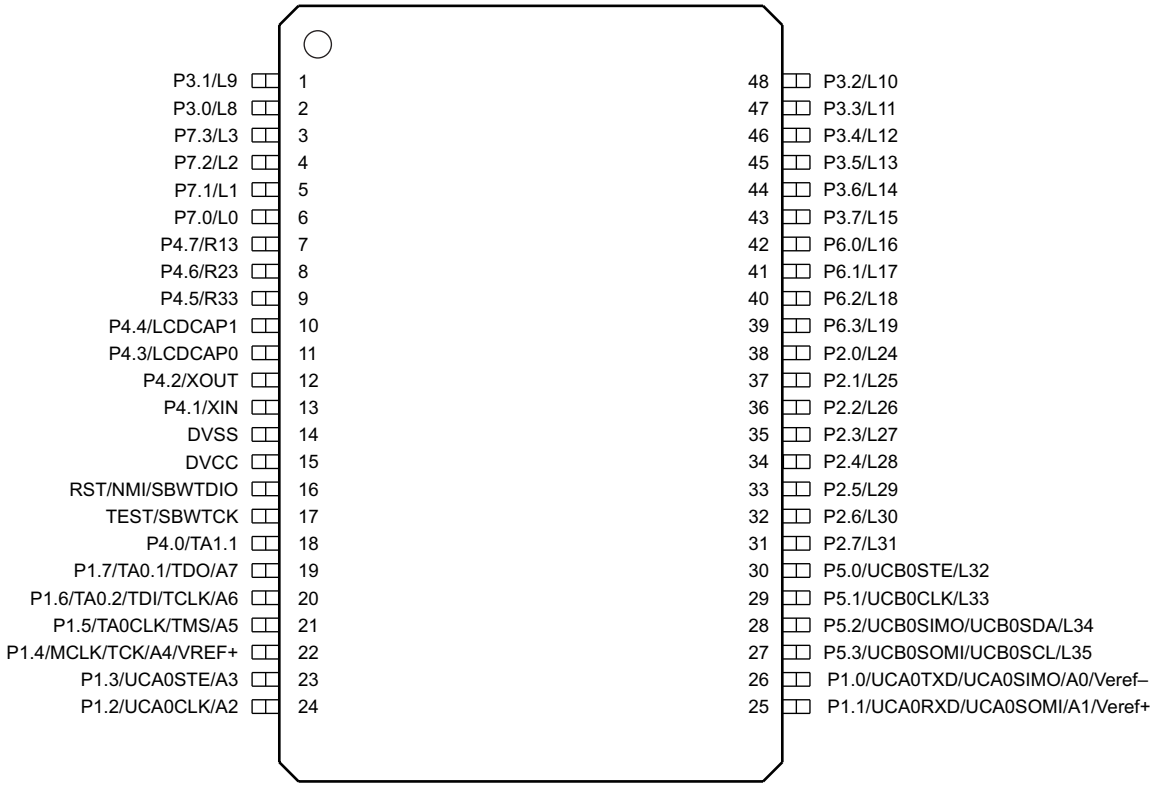


Figure 4-3. 48-Pin DGG (TSSOP) Designation

4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants and package options.

Table 4-1. Signal Descriptions

TERMINAL				I/O	DESCRIPTION
NAME	PACKAGE SUFFIX				
	PM	G56	G48		
P4.7/R13	1	7	7	I/O	General-purpose I/O Input/output port of third most positive analog LCD voltage V4
P4.6/R23	2	8	8	I/O	General-purpose I/O Input/output port of second most positive analog LCD voltage V2
P4.5/R33	3	9	9	I/O	General-purpose I/O Input/output port of first most positive analog LCD voltage V1
P4.4/LCDCAP1	4	10	10	I/O	General-purpose I/O LCD charge pump external port connecting to LCDCAP0 pin by 0.1-µF capacitor
P4.3/LCDCAP0	5	11	11	I/O	General-purpose I/O LCD charge pump external port connecting to LCDCAP1 pin by 0.1-µF capacitor
P4.2/XOUT	6	12	12	I/O	General-purpose I/O Output terminal for crystal oscillator
P4.1/XIN	7	13	13	I/O	General-purpose I/O Input terminal for crystal oscillator
DVSS	8	14	14		Power ground
DVCC	9	15	15		Power supply
$\overline{\text{RST}}$/NMI/SBWTDIO	10	16	16	I/O	Reset input active low Nonmaskable interrupt input Spy-Bi-Wire data input/output
TEST/SBWTCK	11	17	17	I	Test Mode pin – selected digital I/O on JTAG pins Spy-Bi-Wire input clock
P4.0/TA1.1	12	18	18	I/O	General-purpose I/O Timer TA1 CCR1 capture: CCI1A input, compare: Out1 outputs
P8.3/TA1.2 (1)	13	19	–	I/O	General-purpose I/O Timer TA1 CCR2 capture: CCI2A input, compare: Out2 outputs
P8.2/TA1CLK (1)	14	20	–	I/O	General-purpose I/O Timer clock input TACLK for TA1
P8.1/ACLK/A9 (1)	15	–	–	I/O	General-purpose I/O ACLK output Analog input A9
P8.0/SMCLK/A8 (1)	16	–	–	I/O	General-purpose I/O SMCLK output Analog input A8
P1.7/TA0.1/TDO/A7	17	21	19	I/O	General-purpose I/O (2) Timer TA0 CCR1 capture: CCI1A input, compare: Out1 outputs Test data output Analog input A7
P1.6/TA0.2/TDI/TCLK/A6	18	22	20	I/O	General-purpose I/O (2) Timer TA0 CCR2 capture: CCI2A input, compare: Out2 outputs Test data input or test clock input Analog input A6
P1.5/TA0CLK/TMS/A5	19	23	21	I/O	General-purpose I/O (2) Timer clock input TACLK for TA0 Test mode select Analog input A5

(1) Any pin that is not bonded out in a smaller package must be initialized by software after reset to achieve the lowest leakage current.
(2) Because this pin is multiplexed with the JTAG function, TI recommends disabling the pin interrupt function while in JTAG debug to prevent collisions.

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	PACKAGE SUFFIX				
	PM	G56	G48		
P1.4/MCLK/TCK/A4/VREF+	20	24	22	I/O	General-purpose I/O[2] MCLK output Test clock Analog input A4 Output of positive reference voltage with ground as reference
P1.3/UCA0STE/A3	21	25	23	I/O	General-purpose I/O eUSCI_A0 SPI slave transmit enable Analog input A3
P1.2/UCA0CLK/A2	22	26	24	I/O	General-purpose I/O eUSCI_A0 SPI clock input/output Analog input A2
P1.1/UCA0RXD/UCA0SOMI/ A1/Veref+	23	27	25	I/O	General-purpose I/O eUSCI_A0 UART receive data eUSCI_A0 SPI slave out/master in Analog input A1, and ADC positive reference
P1.0/UCA0TXD/UCA0SIMO/ A0/Veref-	24	28	26	I/O	General-purpose I/O eUSCI_A0 UART transmit data eUSCI_A0 SPI slave in/master out Analog input A0, and ADC negative reference
P5.7/L39[1]	25	–	–	I/O	General-purpose I/O LCD drive pin; either segment or common output
P5.6/L38[1]	26	–	–	I/O	General-purpose I/O LCD drive pin; either segment or common output
P5.5/L37[1]	27	29	–	I/O	General-purpose I/O LCD drive pin; either segment or common output
P5.4/L36[1]	28	30	–	I/O	General-purpose I/O LCD drive pin; either segment or common output
P5.3/UCB0SOMI/UCB0SCL/L35	29	31	27	I/O	General-purpose I/O eUSCI_B0 SPI slave out/master in; eUSCI_B0 I2C clock LCD drive pin; either segment or common output
P5.2/UCB0SIMO/UCB0SDA/L34	30	32	28	I/O	General-purpose I/O eUSCI_B0 SPI slave in/master out; eUSCI_B0 I2C data LCD drive pin; either segment or common output
P5.1/UCB0CLK/L33	31	33	29	I/O	General-purpose I/O eUSCI_B0 clock input/output LCD drive pin; either segment or common output
P5.0/UCB0STE/L32	32	34	30	I/O	General-purpose I/O eUSCI_B0 slave transmit enable LCD drive pin; either segment or common output
P2.7/L31	33	35	31	I/O	General-purpose I/O LCD drive pin; either segment or common output
P2.6/L30	34	36	32	I/O	General-purpose I/O LCD drive pin; either segment or common output
P2.5/L29	35	37	33	I/O	General-purpose I/O LCD drive pin; either segment or common output
P2.4/L28	36	38	34	I/O	General-purpose I/O LCD drive pin; either segment or common output
P2.3/L27	37	39	35	I/O	General-purpose I/O LCD drive pin; either segment or common output
P2.2/L26	38	40	36	I/O	General-purpose I/O LCD drive pin; either segment or common output
P2.1/L25	39	41	37	I/O	General-purpose I/O LCD drive pin; either segment or common output
P2.0/L24	40	42	38	I/O	General-purpose I/O LCD drive pin; either segment or common output

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	PACKAGE SUFFIX				
	PM	G56	G48		
P6.7/L23(1)	41	–	–	I/O	General-purpose I/O LCD drive pin; either segment or common output
P6.6/L22(1)	42	–	–	I/O	General-purpose I/O LCD drive pin; either segment or common output
P6.5/L21(1)	43	43	–	I/O	General-purpose I/O LCD drive pin; either segment or common output
P6.4/L20(1)	44	44	–	I/O	General-purpose I/O LCD drive pin; either segment or common output
P6.3/L19	45	45	39	I/O	General-purpose I/O LCD drive pin; either segment or common output
P6.2/L18	46	46	40	I/O	General-purpose I/O LCD drive pin; either segment or common output
P6.1/L17	47	47	41	I/O	General-purpose I/O LCD drive pin; either segment or common output
P6.0/L16	48	48	42	I/O	General-purpose I/O LCD drive pin; either segment or common output
P3.7/L15	49	49	43	I/O	General-purpose I/O LCD drive pin; either segment or common output
P3.6/L14	50	50	44	I/O	General-purpose I/O LCD drive pin; either segment or common output
P3.5/L13	51	51	45	I/O	General-purpose I/O LCD drive pin; either segment or common output
P3.4/L12	52	52	46	I/O	General-purpose I/O LCD drive pin; either segment or common output
P3.3/L11	53	53	47	I/O	General-purpose I/O LCD drive pin; either segment or common output
P3.2/L10	54	54	48	I/O	General-purpose I/O LCD drive pin; either segment or common output
P3.1/L9	55	55	1	I/O	General-purpose I/O LCD drive pin; either segment or common output
P3.0/L8	56	56	2	I/O	General-purpose I/O LCD drive pin; either segment or common output
P7.7/L7(1)	57	–	–	I/O	General-purpose I/O LCD drive pin; either segment or common output
P7.6/L6(1)	58	–	–	I/O	General-purpose I/O LCD drive pin; either segment or common output
P7.5/L5(1)	59	1	–	I/O	General-purpose I/O LCD drive pin; either segment or common output
P7.4/L4(1)	60	2	–	I/O	General-purpose I/O LCD drive pin; either segment or common output
P7.3/L3	61	3	3	I/O	General-purpose I/O LCD drive pin; either segment or common output
P7.2/L2	62	4	4	I/O	General-purpose I/O LCD drive pin; either segment or common output
P7.1/L1	63	5	5	I/O	General-purpose I/O LCD drive pin; either segment or common output
P7.0/L0	64	6	6	I/O	General-purpose I/O LCD drive pin; either segment or common output

4.3 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see Section 6.9.13.

4.4 Connection of Unused Pins

Table 4-2 shows the correct termination of unused pins.

Table 4-2. Connection of Unused Pins(1)

PIN	POTENTIAL	COMMENT
Px.0 to Px.7	Open	Switched to port function, output direction (PxDIR.n = 1)
$\overline{\text{RST}}$/NMI	DVCC	47-kΩ pullup or internal pullup selected with 10-nF (1.1-nF) pulldown(2)
TEST	Open	This pin always has an internal pulldown enabled.

(1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
(2) The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode with TI tools like FET interfaces or GANG programmers.

5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at DVCC pin to V_{SS}	–0.3	4.1	V
Voltage applied to any pin(2)	–0.3	V_{CC} + 0.3 (4.1 Max)	V
Diode current at any device pin		±2	mA
Maximum junction temperature, T_J		85	°C
Storage temperature, T_{stg}(3)	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage or memory corruption to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage applied at DVCC pin(1)(2)		1.8(3)		3.6	V
V_{SS}	Supply voltage applied at DVSS pin			0		V
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C
C_{DVCC}	Recommended capacitor at DVCC(4)		4.7	10		µF
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(3)(5)	No FRAM wait states (NWAITSx = 0)	0		8	MHz
		With FRAM wait states (NWAITSx = 1)(6)	0		16(7)	
f_{ACLK}	Maximum ACLK frequency				40	kHz
f_{SMCLK}	Maximum SMCLK frequency				16(7)	MHz

(1) Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset even within the recommended supply voltage range.
(2) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(3) The minimum supply voltage is defined by the SVS levels. See the SVS threshold parameters in Table 5-1.
(4) A capacitor tolerance of ±20% or better is required.
(5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(6) Wait states only occur on actual FRAM accesses (that is, on FRAM cache misses). RAM and peripheral accesses are always executed without wait states.
(7) If clock sources such as HF crystals or the DCO with frequencies >16 MHz are used, the clock must be divided in the clock system to comply with this operating condition.

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

See (1)

PARAMETER	EXECUTION MEMORY	TEST CONDITIONS	Frequency ($f_{MCLK} = f_{SMCLK}$)						UNIT
			1 MHz 0 WAIT STATES (NWAITSx = 0)		8 MHz 0 WAIT STATES (NWAITSx = 0)		16 MHz 1 WAIT STATE (NWAITSx = 1)		
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, FRAM}$(0%)	FRAM 0% cache hit ratio	3 V, 25°C	504		2874		3156	3700	µA
		3 V, 85°C	516		2919		3205		
$I_{AM, FRAM}$(100%)	FRAM 100% cache hit ratio	3 V, 25°C	209		633		1056	1298	µA
		3 V, 85°C	217		647		1074		
$I_{AM, RAM}$ (2)	RAM	3 V, 25°C	231		809		1450		µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. Characterized with program executing typical data processing.
f_{ACLK} = 32786 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ at specified frequency
Program and data entirely reside in FRAM. All execution is from FRAM.
(2) Program and data reside entirely in RAM. All execution is from RAM. No access to FRAM.

5.5 Active Mode Supply Current Per MHz

V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
$dI_{AM,FRAM}/df$	Active mode current consumption per MHz, execution from FRAM, no wait states (1)	(($I_{AM, 75\% \text{ cache hit rate}}$ at 8 MHz) – ($I_{AM, 75\% \text{ cache hit rate}}$ at 1 MHz)) / 7 MHz	126	µA/MHz

(1) All peripherals are turned on in default settings.

5.6 Low-Power Mode LPM0 Supply Currents Into V_{CC} Excluding External Current

V_{CC} = 3 V, T_A = 25°C (unless otherwise noted) (1) (2)

PARAMETER		V_{CC}	FREQUENCY (f_{SMCLK})						UNIT
			1 MHz		8 MHz		16 MHz		
			TYP	MAX	TYP	MAX	TYP	MAX	
I_{LPM0}	Low-power mode LPM0 supply current	2 V	158		307		415		µA
		3 V	169		318		427		

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Current for watchdog timer clocked by SMCLK included.
f_{ACLK} = 32786 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} at specified frequency.

5.7 Low-Power Mode LPM3, LPM4 Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		V_{CC}	–40°C		25°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3,XT1}$	Low-power mode 3, includes SVS (2)(3)(4)	3 V	1.13		1.31	1.99	3.00		µA
		2 V	1.06		1.21		2.94		
$I_{LPM3,VLO}$	Low-power mode 3, VLO, excludes SVS (5)	3 V	0.92		1.00	1.75	2.89		µA
		2 V	0.86		1.00		2.75		
$I_{LPM3,\ LCD,\ CP}$	Low-power mode 3, LCD, excludes SVS (6)	3 V	1.07		1.25		3.04		µA
$I_{LPM3,\ RTC}$	Low-power mode 3, RTC, excludes SVS (7)	3 V	1.08		1.25		3.04		µA
$I_{LPM4,\ SVS}$	Low-power mode 4, includes SVS	3 V	0.65		0.75		1.88		µA
		2 V	0.63		0.73		1.85		
I_{LPM4}	Low-power mode 4, excludes SVS	3 V	0.51		0.58		1.51		µA
		2 V	0.50		0.57		1.49		

(1) All inputs are tied to 0 V or to VCC. Outputs do not source or sink any current
(2) Not applicable for devices with HF crystal oscillator only.
(3) Characterized with a Golledge MS1V-TK/I_32.768KHZ crystal with a load capacitance chosen to closely match the required load.
(4) **Low-power mode 3, includes SVS** test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) **Low-power mode 3, VLO, excludes SVS** test conditions:
Current for watchdog timer clocked by VLO included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz
(6) LCD works in LPM3 if internal charge pump and V_{REF} switch mode are enabled. LCD driver pins are configured as 4 × 36 at 32-Hz frame frequency with external 32768-Hz clock source.
(7) RTC periodically wakes up every second with external 32768-Hz as source.

5.8 Low-Power Mode LPMx.5 Supply Currents (Into V_{CC}) Excluding External Current

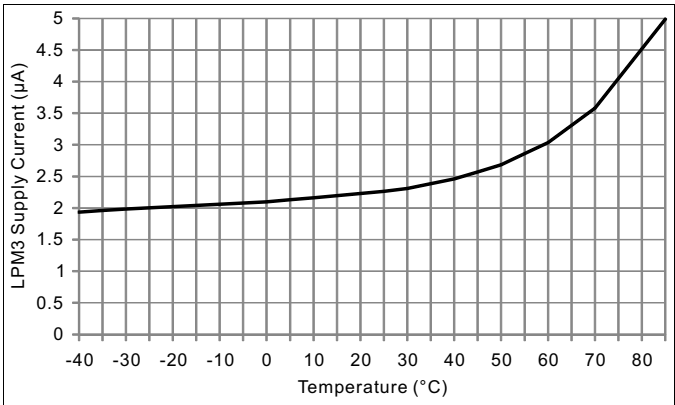
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	–40°C		25°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3.5, XT1}$	Low-power mode 3.5, includes SVS(1)(2) (3) (also see Figure 5-3)	3 V	0.71		0.77	1.25	1.06	2.06	µA
		2 V	0.66		0.70		0.95		
$I_{LPM3.5, LCD, CP}$	Low-power mode 3.5, excludes SVS(4)	3 V	0.90		0.94		1.27		µA
$I_{LPM4.5, SVS}$	Low-power mode 4.5, includes SVS(5)	3 V	0.23		0.25	0.375	0.32	0.43	µA
		2 V	0.20		0.20		0.24		
$I_{LPM4.5}$	Low-power mode 4.5, excludes SVS(6)	3 V	0.010		0.015	0.070	0.073	0.140	µA
		2 V	0.008		0.013		0.060		

(1) Not applicable for devices with HF crystal oscillator only.
(2) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance chosen to closely match the required load.
(3) **Low-power mode 3.5, includes SVS** test conditions:
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(4) LCD works in LPM3.5 if the internal charge pump and VREF switch mode are enabled. The LCD driver pins are configured as 4x36 at 32-Hz frame frequency with an external 32768-Hz clock source.
(5) **Low-power mode 4.5, includes SVS** test conditions:
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz
(6) **Low-power mode 4.5, excludes SVS** test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz

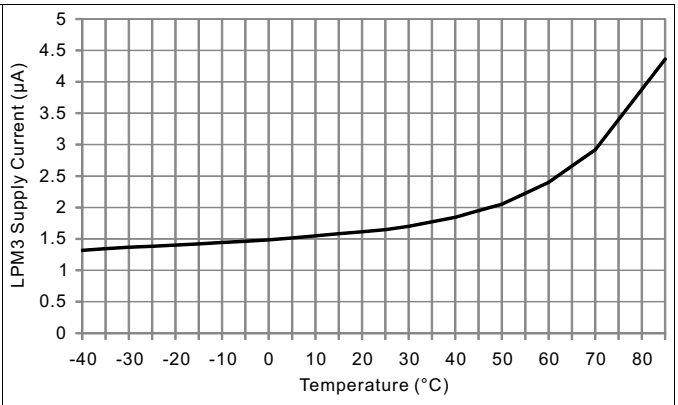
5.9 Typical Characteristics, Low-Power Mode Supply Currents

The graphs in this section show only board-level test result on a small number of samples. A MS1V-T1K crystal from Micro-Crystal was populated for 32-kHz clock generation. LCD is configured in 4xCOM mode without LCD panel populated.



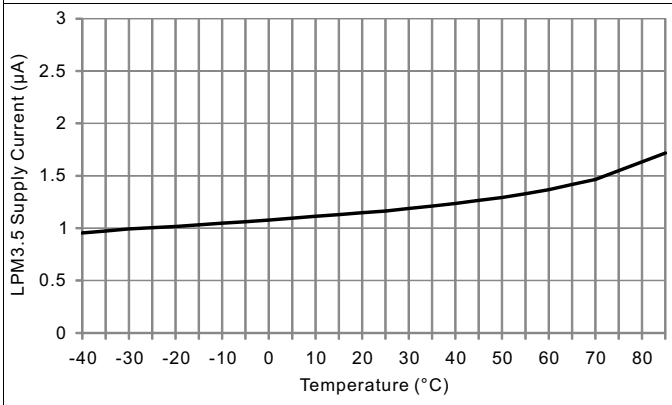
LPM3 DVCC = 3 V
LCD on SVS disabled

Figure 5-1. LPM3 Supply Current vs Temperature



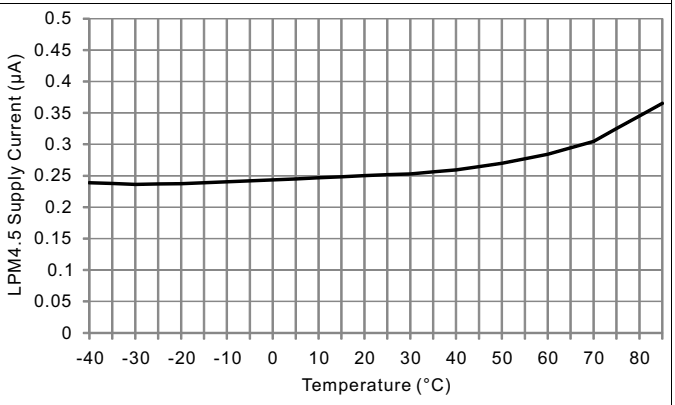
LPM3 DVCC = 3 V
RTC counter on SVS disabled

Figure 5-2. LPM3 Supply Current vs Temperature



LPM3.5 DVCC = 3 V
12.5-pF crystal on XT1 SVS enabled

Figure 5-3. LPM3.5 Supply Current vs Temperature



LPM4.5 DVCC = 3 V
SVS enabled

Figure 5-4. LPM4.5 Supply Current vs Temperature

5.10 Typical Characteristics, Current Consumption Per Module

MODULE	TEST CONDITIONS	REFERENCE CLOCK	TYP	UNIT
Timer_A		Module input clock	5	µA/MHz
eUSCI_A	UART mode	Module input clock	7	µA/MHz
eUSCI_A	SPI mode	Module input clock	5	µA/MHz
eUSCI_B	SPI mode	Module input clock	5	µA/MHz
eUSCI_B	I^2C mode, 100 kbaud	Module input clock	5	µA/MHz
RTC		32 kHz	85	nA
CRC	From start to end of operation	MCLK	8.5	µA/MHz

5.11 Thermal Characteristics

PARAMETER			VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air(1)	LQFP-64 (PM)	61.7	°C/W
$\theta_{JC, (TOP)}$	Junction-to-case (top) thermal resistance(2)		25.4	°C/W
θ_{JB}	Junction-to-board thermal resistance(3)		32.7	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		32.4	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		2.5	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air(1)	TSSOP-56 (DGG56)	62.4	°C/W
$\theta_{JC, (TOP)}$	Junction-to-case (top) thermal resistance(2)		18.7	°C/W
θ_{JB}	Junction-to-board thermal resistance(3)		31.4	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		31.1	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.8	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air(1)	TSSOP-48 (DGG48)	68.9	°C/W
$\theta_{JC, (TOP)}$	Junction-to-case (top) thermal resistance(2)		23	°C/W
θ_{JB}	Junction-to-board thermal resistance(3)		35.8	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		35.3	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		1.1	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold place test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold place fixture to control the PCB temperature, as described in JESD51-8.

5.12 Timing and Switching Characteristics

5.12.1 Power Supply Sequencing

Figure 5-5 shows the power cycle, SVS, and BOR reset conditions.

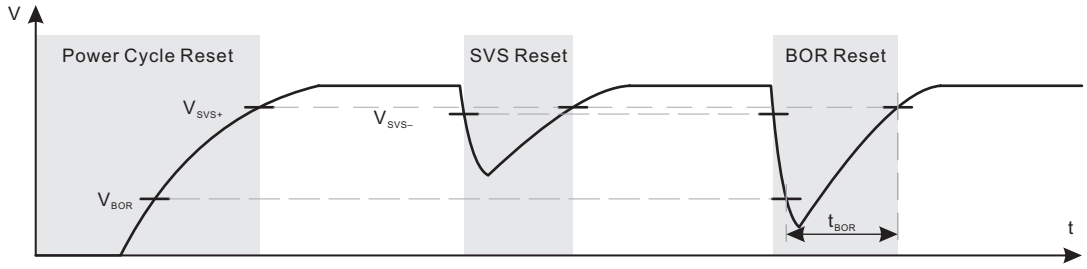


Figure 5-5. Power Cycle, SVS, and BOR Reset Conditions

Table 5-1 lists the characteristics of the SVS and BOR.

Table 5-1. PMM, SVS and BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BOR, safe}$	Safe BOR power-down level(1)		0.1			V
$t_{BOR, safe}$	Safe BOR reset delay(2)		10			ms
$I_{SVSH,AM}$	SVS_H current consumption, active mode	V_{CC} = 3.6 V			1.5	µA
$I_{SVSH,LPM}$	SVS_H current consumption, low-power modes	V_{CC} = 3.6 V		240		nA
V_{SVSH-}	SVS_H power-down level(3)		1.71	1.81	1.87	V
V_{SVSH+}	SVS_H power-up level(3)		1.76	1.88	1.99	V
V_{SVSH_hys}	SVS_H hysteresis			70		mV
$t_{PD,SVSH, AM}$	SVS_H propagation delay, active mode				10	µs
$t_{PD,SVSH, LPM}$	SVS_H propagation delay, low-power modes				100	µs
$V_{REF, 1.2V}$	1.2-V REF voltage(4)		1.158	1.20	1.242	V

(1) A safe BOR can be correctly generated only if DVCC drops below this voltage before it rises.
(2) When an BOR occurs, a safe BOR can be correctly generated only if DVCC is kept low longer than this period before it reaches V_{SVSH+}.
(3) For additional information, see the Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design.
(4) This is a characterized result with external 1-mA load to ground from –40°C to 85°C.

5.12.2 Reset Timing

Table 5-2 lists the device wake-up times.

Table 5-2. Wake-Up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{WAKE-UP\ FRAM}$	Additional wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from a LPM if immediate activation is selected for wake-up (1)		3 V		10		µs
$t_{WAKE-UP\ LPM0}$	Wake-up time from LPM0 to active mode (1)		3 V			200 ns + 2.5/f_{DCO}	
$t_{WAKE-UP\ LPM3}$	Wake-up time from LPM3 to active mode (2)		3 V		10		µs
$t_{WAKE-UP\ LPM4}$	Wake-up time from LPM4 to active mode		3 V		10		µs
$t_{WAKE-UP\ LPM3.5}$	Wake-up time from LPM3.5 to active mode (2)		3 V		350		µs
$t_{WAKE-UP\ LPM4.5}$	Wake-up time from LPM4.5 to active mode (2)	SVSHE = 1	3 V		350		µs
		SVSHE = 0	3 V		1		ms
$t_{WAKE-UP-RESET}$	Wake-up time from $\overline{RST}$ or BOR event to active mode (2)		3 V		1		ms
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI pin to accept a reset		3 V	2			µs

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge.
(2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

5.12.3 Clock Specifications

Table 5-3 lists the characteristics of XT1.

Table 5-3. XT1 Crystal Oscillator (Low Frequency)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{XT1,\ LF}$	XT1 oscillator crystal, low frequency	LFXTBYPASS = 0			32768		Hz
$DC_{XT1,\ LF}$	XT1 oscillator LF duty cycle	Measured at MCLK, f_{LFXT} = 32768 Hz		30%		70%	
$f_{XT1,SW}$	XT1 oscillator logic-level square-wave input frequency	LFXTBYPASS = 1(2)(3)			32768		Hz
$DC_{XT1,\ SW}$	LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1		40%		60%	
OA_{LFXT}	Oscillation allowance for LF crystals (4)	LFXTBYPASS = 0, LFXTDRIVE = {3}, f_{LFXT} = 32768 Hz, $C_{L,eff}$ = 12.5 pF			200		kΩ
$C_{L,eff}$	Integrated effective load capacitance (5)	See (6)			1		pF
$t_{START,LFXT}$	Start-up time (7)	f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12.5 pF			1000		ms
$f_{Fault,LFXT}$	Oscillator fault frequency (8)	XTS = 0(9)		0		3500	Hz

(1) To improve EMI on the LFXT oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger inputs section of this data sheet. Duty cycle requirements are defined by $DC_{LFXT,\ SW}$.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF.
- For LFXTDRIVE = {1}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF.
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 10 pF.
- For LFXTDRIVE = {3}, 6 pF ≤ $C_{L,eff}$ ≤ 12 pF.

(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).

(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(7) Includes startup counter of 1024 clock cycles.

(8) Frequencies above the MAX specification do not set the fault flag. Frequencies in between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition sets the flag.

(9) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-4 lists the frequency characteristics of the DCO FLL.

Table 5-4. DCO FLL, Frequency

Over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{DCO, FLL}$	FLL lock frequency, 16 MHz, 25°C	Measured at MCLK, Internal trimmed REFO as reference	3 V	–1.0%		1.0%	
	FLL lock frequency, 16 MHz, –40°C to 85°C		3 V	–2.0%		2.0%	
	FLL lock frequency, 16 MHz, –40°C to 85°C	Measured at MCLK, XT1 crystal as reference	3 V	–0.5%		0.5%	
f_{DUTY}	Duty cycle	Measured at MCLK, XT1 crystal as reference	3 V	40%	50%	60%	
$Jitter_{cc}$	Cycle-to-cycle jitter, 16 MHz		3 V		0.25%		
$Jitter_{long}$	Long-term jitter, 16 MHz		3 V		0.022 %		
$t_{FLL, lock}$	FLL lock time		3 V		120		ms

Table 5-5 lists the characteristics of the REFO.

Table 5-5. REFO

Over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	3 V		15		µA
f_{REFO}	REFO calibrated frequency	Measured at MCLK	3 V		32768		Hz
	REFO absolute calibrated tolerance	T_A = –40°C to 85°C	1.8 V to 3.6 V	–3.5%		+3.5%	
df_{REFO}/d_T	REFO frequency temperature drift	Measured at MCLK(1)	3 V		0.01		%/°C
df_{REFO}/d_{VCC}	REFO frequency supply voltage drift	Measured at MCLK at 25°C(2)	1.8 V to 3.6 V		1		%/V
f_{DC}	REFO duty cycle	Measured at MCLK	1.8 V to 3.6 V	40%	50%	60%	
t_{START}	REFO startup time	40% to 60% duty cycle			50		µs

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-6 lists the characteristics of the VLO.

Table 5-6. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at MCLK	3 V		10		kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at MCLK(1)	3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at MCLK(2)	1.8 V to 3.6 V		4		%/V
$f_{VLO,DC}$	Duty cycle	Measured at MCLK	3 V		50%		

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

NOTE

The VLO clock frequency is reduced by 15% (typical) when the device switches from active mode to LPM3 or LPM4, because the reference changes. This lower frequency is not a violation of the VLO specifications (see Table 5-6).

Table 5-7 lists the characteristics of the MODCLK.

Table 5-7. Module Oscillator Clock (MODCLK)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{MODCLK}	MODCLK frequency	3 V	3.8	4.8	5.8	MHz
f_{MODCLK}/dT	MODCLK frequency temperature drift	3 V		0.102		%/℃
f_{MODCLK}/dV_{CC}	MODCLK frequency supply voltage drift	1.8 V to 3.6 V		1.02		%/V
$f_{MODCLK,DC}$	Duty cycle	3 V	40%	50%	60%	

5.12.4 Digital I/Os

Table 5-8 lists the characteristics of the digital inputs.

Table 5-8. Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2 V	0.90		1.50	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		2 V	0.50		1.10	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		2 V	0.3		0.8	V
			3 V	0.4		1.2	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	$V_{IN} = V_{SS}$ or V_{CC}			3		pF
$C_{I,ana}$	Input capacitance, port pins with shared analog functions	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
$I_{lkg(Px.y)}$	High-impedance leakage current (also see (1) and (2))		2 V, 3 V	–20		+20	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Table 5-9 lists the characteristics of the digital outputs.

Table 5-9. Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –3 mA (1)	2 V	1.4		2.0	V
		$I_{(OHmax)}$ = –5 mA (1)	3 V	2.4		3.0	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA (1)	2 V	0.0		0.60	V
		$I_{(OHmax)}$ = 5 mA (1)	3 V	0.0		0.60	
f_{Port_CLK}	Clock output frequency	C_L = 20 pF (2)	2 V	16			MHz
			3 V	16			
$t_{rise,dig}$	Port output rise time, digital only port pins	C_L = 20 pF	2 V		10		ns
			3 V		7		
$t_{fall,dig}$	Port output fall time, digital only port pins	C_L = 20 pF	2 V		10		ns
			3 V		5		

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The port can output frequencies at least up to the specified limit and might support higher frequencies.

5.12.4.1 Digital I/O Typical Characteristics

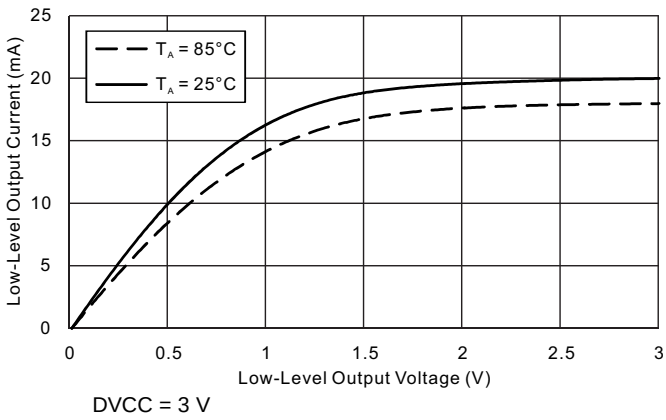


Figure 5-6. Typical Low-Level Output Current vs Low-Level Output Voltage

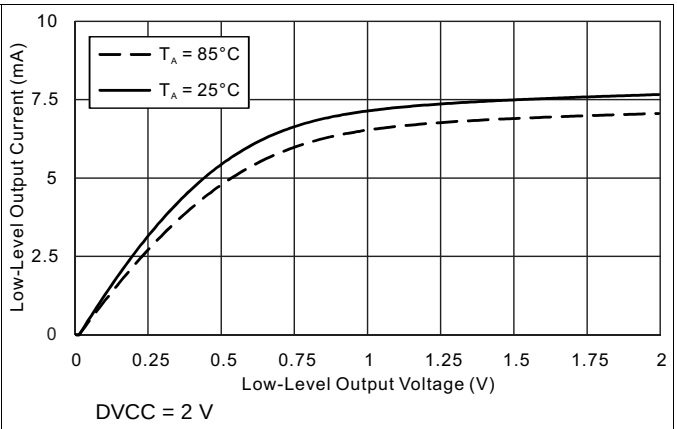


Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage

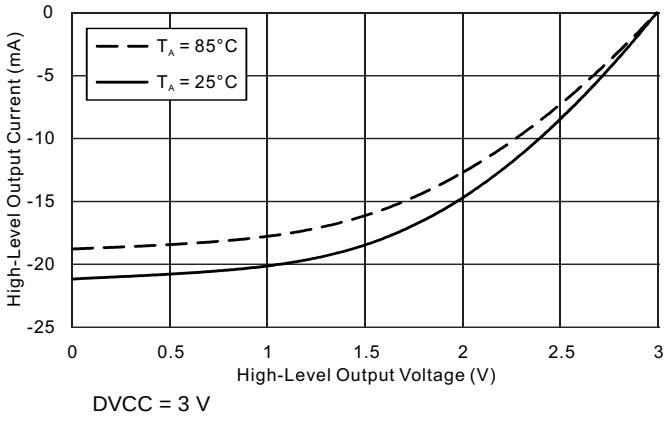


Figure 5-8. Typical High-Level Output Current vs High-Level Output Voltage

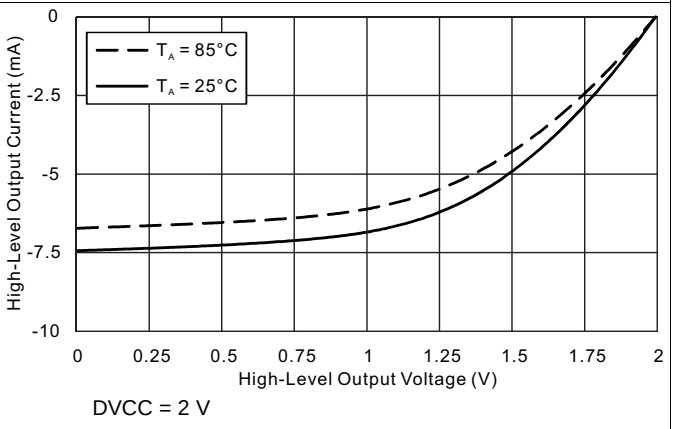


Figure 5-9. Typical High-Level Output Current vs High-Level Output Voltage

5.12.5 Timer_A

Table 5-10 lists the operating frequency of Timer_A.

Table 5-10. Timer_A Operating Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ±10%	2 V, 3 V		16	MHz

5.12.6 eUSCI

Table 5-11 lists the operating conditions of the eUSCI in UART mode.

Table 5-11. eUSCI (UART Mode) Operating Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, MODCLK External: UCLK Duty cycle = 50% ±10%	2 V, 3 V		16	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in Mbaud)		2 V, 3 V		5	MHz

Table 5-12 lists the switching characteristics of the eUSCI in UART mode.

Table 5-12. eUSCI (UART Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
t_t	UART receive deglitch time (1)	UCGLITx = 0	2 V, 3 V	12	ns
		UCGLITx = 1		40	
		UCGLITx = 2		68	
		UCGLITx = 3		110	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

Table 5-13 lists the operating conditions of the eUSCI in SPI master mode.

Table 5-13. eUSCI (SPI Master Mode) Operating Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, MODCLK Duty cycle = 50% ±10%		8	MHz

Table 5-14 lists the switching characteristics of the eUSCI in SPI master mode.

Table 5-14. eUSCI (SPI Master Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10		1		UCxCLK cycles
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10		1		UCxCLK cycles
$t_{SU,MI}$	SOMI input data setup time		2 V	45		ns
			3 V	35		
$t_{HD,MI}$	SOMI input data hold time		2 V	0		ns
			3 V	0		
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	2 V		20	ns
			3 V		20	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	2 V	0		ns
			3 V	0		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-10 and Figure 5-11.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-10 and Figure 5-11.

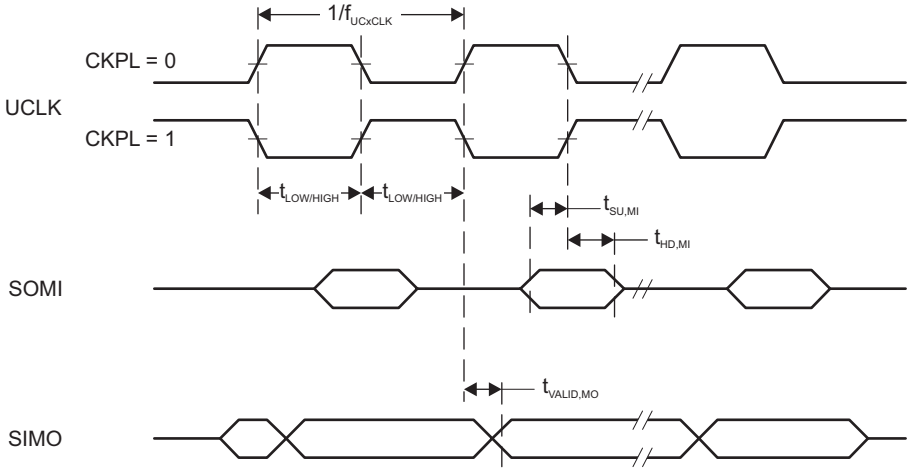


Figure 5-10. SPI Master Mode, CKPH = 0

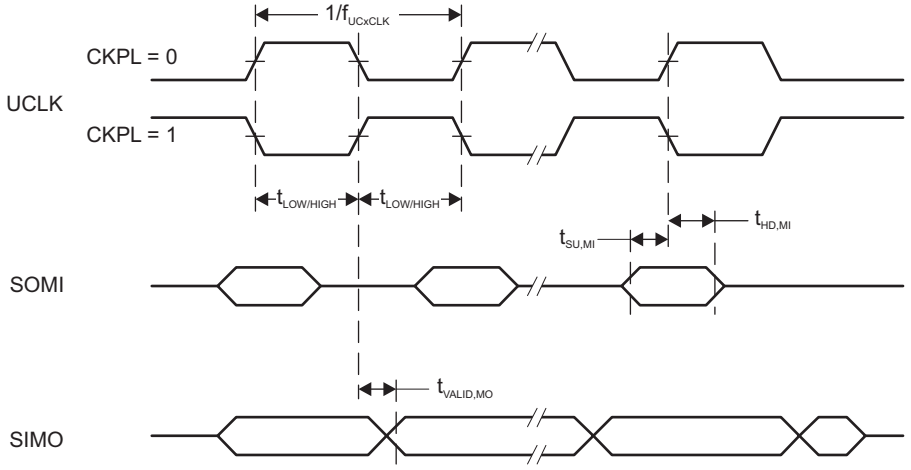


Figure 5-11. SPI Master Mode, CKPH = 1

Table 5-15 lists the switching characteristics of the eUSCI in SPI slave mode.

Table 5-15. eUSCI (SPI Slave Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		2 V	55		ns
			3 V	45		
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive		2 V	20		ns
			3 V	20		
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		2 V		65	ns
			3 V		40	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		2 V		40	ns
			3 V		35	
$t_{SU,SI}$	SIMO input data setup time		2 V	4		ns
			3 V	4		
$t_{HD,SI}$	SIMO input data hold time		2 V	12		ns
			3 V	12		
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF	2 V		65	ns
			3 V		40	
$t_{HD,SO}$	SOMI output data hold time (3)	C_L = 20 pF	2 V	5		ns
			3 V	5		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-12 and Figure 5-13.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-12 and Figure 5-13.

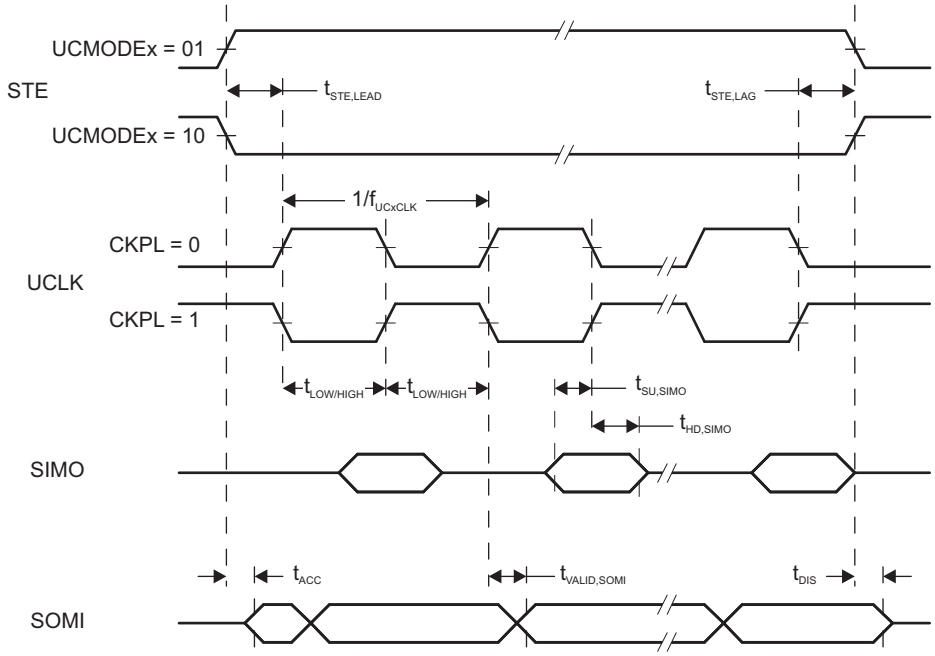


Figure 5-12. SPI Slave Mode, CKPH = 0

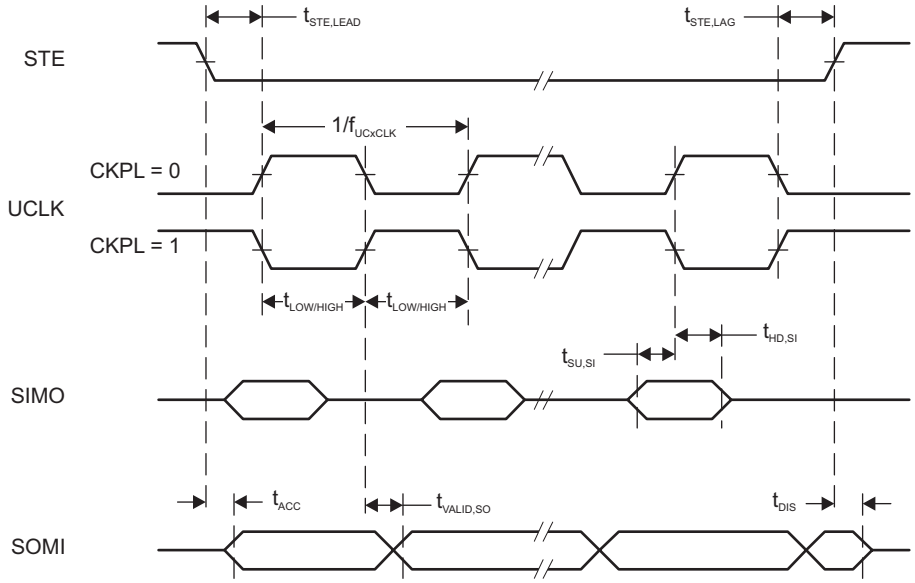


Figure 5-13. SPI Slave Mode, CKPH = 1

Table 5-16 lists the switching characteristics of the eUSCI in I²C mode.

Table 5-16. eUSCI (I²C Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-14)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, MODCLK External: UCLK Duty cycle = 50% ±10%				16	MHz
f_{SCL}	SCL clock frequency		2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	2 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	2 V, 3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		2 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		2 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	2 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	2 V, 3 V	50		600	ns
		UCGLITx = 1		25		300	
		UCGLITx = 2		12.5		150	
		UCGLITx = 3		6.3		75	
$t_{TIMEOUT}$	Clock low time-out	UCCLTOx = 1	2 V, 3 V		27		ms
		UCCLTOx = 2			30		
		UCCLTOx = 3			33		

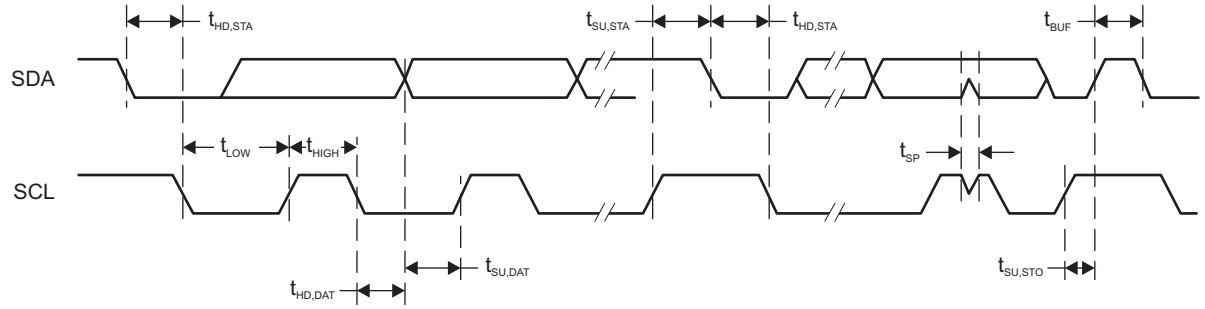


Figure 5-14. I²C Mode Timing

5.12.7 ADC

Table 5-17 lists the power supply and input conditions of the ADC.

Table 5-17. ADC, Power Supply and Input Range Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
DV_{CC}	ADC supply voltage			2.0		3.6	V
$V_{(Ax)}$	Analog input voltage range	All ADC pins		0		DV_{CC}	V
I_{ADC}	Operating supply current into DVCC terminal, reference current not included, repeat-single-channel mode	f_{ADCCLK} = 5 MHz, ADCON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADCDIV = 0, ADCCONSEQx = 10b	2 V		185		µA
			3 V		207		
C_I	Input capacitance	Only one terminal Ax can be selected at one time from the pad to the ADC capacitor array, including wiring and pad	2.2 V		1.6	2.0	pF
$R_{I,MUX}$	Input MUX ON resistance	DV_{CC} = 2 V, 0 V = V_{Ax} = DV_{CC}				2	kΩ
$R_{I,Misc}$	Input miscellaneous resistance				34		kΩ

Table 5-18 lists the timing parameters of the ADC.

Table 5-18. ADC, 10-Bit Timing Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{ADCCLK}		For specified performance of ADC linearity parameters	2 V to 3.6 V	0.45	5	5.5	MHz
f_{ADCOSC}	Internal ADC oscillator (MODCLK)	ADCDIV = 0, f_{ADCCLK} = f_{ADCOSC}	2 V to 3.6 V	4.5	5.0	5.5	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, 10 ADCCLK cycles, 10-bit mode, f_{ADCOSC} = 4.5 MHz to 5.5 MHz	2 V to 3.6 V	2.18		2.67	µs
		External f_{ADCCLK} from ACLK, MCLK, or SMCLK, ADCSSEL ≠ 0	2 V to 3.6 V		(1)		
t_{ADCON}	Turn on settling time of the ADC	The error in a conversion started after t_{ADCON} is less than ±0.5 LSB, Reference and input signal already settled				100	ns
t_{Sample}	Sampling time	R_S = 1000 Ω, R_I (2) = 36000 Ω, C_I = 3.5 pF, Approximately 8 Tau (t) are required for an error of less than ±0.5 LSB	2 V	1.5			µs
			3 V	2.0			

(1) 12 × 1/f_{ADCCLK}
(2) R_I = $R_{I,MUX}$ + $R_{I,Misc}$.

Table 5-19 lists the linearity parameters of the ADC.

Table 5-19. ADC, 10-Bit Linearity Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (10-bit mode)	V_{DVCC} as reference	2.4 V to 3.6 V	–2		2	LSB
	Integral linearity error (8-bit mode)		2 V to 3.6 V	–2		2	
E_D	Differential linearity error (10-bit mode)	V_{DVCC} as reference	2.4 V to 3.6 V	–1		1	LSB
	Differential linearity error (8-bit mode)		2 V to 3.6 V	–1		1	
E_O	Offset error (10-bit mode)	V_{DVCC} as reference	2.4 V to 3.6 V	–6.5		6.5	mV
	Offset error (8-bit mode)		2 V to 3.6 V	–6.5		6.5	
E_G	Gain error (10-bit mode)	V_{DVCC} as reference	2.4 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
	Gain error (8-bit mode)	V_{DVCC} as reference	2 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
E_T	Total unadjusted error (10-bit mode)	V_{DVCC} as reference	2.4 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
	Total unadjusted error (8-bit mode)	V_{DVCC} as reference	2 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
V_{SENSOR}	See (1)	ADCON = 1, INCH = 0Ch, T_A = 0°C	3 V		1.013		mV
TC_{SENSOR}	See (2)	ADCON = 1, INCH = 0Ch	3 V		3.35		mV/°C
t_{SENSOR} (sample)	Sample time required if channel 12 is selected(3)	ADCON = 1, INCH = 0Ch, Error of conversion result ≤ 1 LSB, AM and all LPM above LPM3	3 V	30			µs
		ADCON = 1, INCH = 0Ch, Error of conversion result ≤ 1 LSB, LPM3	3 V	100			

(1) The temperature sensor offset can vary significantly. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(2) The device descriptor structure contains calibration values for 30°C and 85°C for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature, °C}) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
(3) The typical equivalent impedance of the sensor is 700 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.

5.12.8 LCD Controller

Table 5-20 lists the operating conditions of the LCD controller.

Table 5-20. LCD Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{CC,LCD,CP\ en,3.6}$	Supply voltage range, charge pump enabled, $V_{LCD} \le 3.6$ V	LCDCPEN = 1, 0000 < VLCDx ≤ 1111, LCDREFEN = 1 (charge pump enabled, $V_{LCD} \le 3.6$ V)	1.8		3.6	V
$V_{CC,LCD,ext.\ bias}$	Supply voltage range, external biasing, charge pump enabled	LCDCPEN = 1, LCDREFEN = 0	1.8		3.6	V
$V_{CC,LCD,VLCDEXT}$	Supply voltage range, external LCD voltage, external biasing, charge pump disabled	LCDCPEN = 0, LCDSELVDD = 0	1.8		3.6	V
V_{R33}	External LCD voltage at LCDCAP/R33, external biasing, charge pump disabled	LCDCPEN = 0, LCDSELVDD = 0	2.4		3.6	V
C_{LCDCAP}				0.1		µF
C_{R33}				0.1		µF
C_{R23}				0.1		µF
C_{R13}				0.1		µF
f_{Frame}	LCD frame frequency range	$f_{LCD} = 2 \times mux \times f_{FRAME}$ with mux = 1 (static), 2, 3, 4	16	32	64	Hz
$f_{ACLK,in}$	ACLK input frequency range		30	32	40	kHz
C_{Panel}	Panel capacitance	32-Hz frame frequency			8000	pF
V_{R33}	Analog input voltage at R33	LCDCPEN = 0, LCDSELVDD = 0, LCDREFEN = 0	2.4		3.6	V
$V_{R23,1/3bias}$	Analog input voltage at R23	LCDCPEN = 0, LCDSELVDD = 0, LCDREFEN = 0	1.2		2.4	V
$V_{R13,1/3bias}$	Analog input voltage at R13 with 1/3 biasing		0.0		1.2	V
$V_{LCDREF/R13}$	External LCD reference voltage applied at LCDREF/R13	LCDCPEN = 1, LCDSELVDD = 0, LCDREFEN = 0	0.8	1.0	1.2	V

5.12.9 FRAM

Table 5-21 lists the characteristics of the FRAM.

Table 5-21. FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
	Read and write endurance		10^{15}		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100		years
		T_J = 70°C	40		
		T_J = 85°C	10		

5.12.10 Emulation and Debug

Table 5-22 lists the characteristics of the JTAG and SBW interface.

Table 5-22. JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2 V, 3 V	0		10	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2 V, 3 V	0.028		15	µs
$t_{SBW,\ En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1)	2 V, 3 V			110	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency, 4-wire JTAG (2)	2 V	0		16	MHz
		3 V	0		16	MHz
$R_{internal}$	Internal pulldown resistance on TEST	2 V, 3 V	20	35	50	kΩ

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter (PC), stack pointer (SP), status register (SR), and constant generator (CG), respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

6.2 Operating Modes

The devices have one active mode and several software-selectable low-power modes of operation. An interrupt event can wake up the device from low-power mode LPM0 or LPM3, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

Table 6-1. Operating Modes

MODE		AM	LPM0	LPM3	LPM4	LPM3.5	LPM4.5
		ACTIVE MODE	CPU OFF	STANDBY	OFF	ONLY RTC COUNTER AND LCD	SHUTDOWN
Maximum System Clock		16 MHz	16 MHz	40 kHz	0	40 kHz	0
Power Consumption at 25°C, 3 V		126 µA/MHz	20 µA/MHz	1.2 µA	0.6 µA without SVS	0.77 µA with RTC only	13 nA without SVS
Wake-up time		N/A	Instant	10 µs	10 µs	150 µs	150 µs
Wake-up events		N/A	All	All	I/O	RTC Counter I/O	I/O
Power	Regulator	Full Regulation	Full Regulation	Partial Power Down	Partial Power Down	Partial Power Down	Power Down
	SVS	On	On	Optional	Optional	Optional	Optional
	Brown Out	On	On	On	On	On	On
Clock	MCLK	Active	Off	Off	Off	Off	Off
	SMCLK	Optional	Optional	Off	Off	Off	Off
	FLL	Optional	Optional	Off	Off	Off	Off
	DCO	Optional	Optional	Off	Off	Off	Off
	MODCLK	Optional	Optional	Off	Off	Off	Off
	REFO	Optional	Optional	Optional	Off	Off	Off
	ACLK	Optional	Optional	Optional	Off	Off	Off
	XT1CLK	Optional	Optional	Optional	Off	Optional	Off
	VLOCLK	Optional	Optional	Optional	Off	Optional	Off
Core	CPU	On	Off	Off	Off	Off	Off
	FRAM	On	On	Off	Off	Off	Off
	RAM	On	On	On	On	Off	Off
	Backup Memory(1)	On	On	On	On	On	Off

(1) Backup memory contains one 32-byte register in the peripheral memory space. See Table 6-29 and Table 6-48 for its memory allocation.

Table 6-1. Operating Modes (continued)

MODE		AM	LPM0	LPM3	LPM4	LPM3.5	LPM4.5
		ACTIVE MODE	CPU OFF	STANDBY	OFF	ONLY RTC COUNTER AND LCD	SHUTDOWN
Peripherals	Timer0_A3	Optional	Optional	Optional	Off	Off	Off
	Timer1_A3	Optional	Optional	Optional	Off	Off	Off
	WDT	Optional	Optional	Optional	Off	Off	Off
	eUSCI_A0	Optional	Optional	Off	Off	Off	Off
	eUSCI_B0	Optional	Optional	Off	Off	Off	Off
	CRC	Optional	Optional	Off	Off	Off	Off
	ADC	Optional	Optional	Optional	Off	Off	Off
	LCD	Optional	Optional	Optional	Off	Optional	Off
	RTC Counter	Optional	Optional	Optional	Off	Optional	Off
I/O	General Digital Input/Output	On	Optional	State Held	State Held	State Held	State Held
	Capacitive Touch I/O	Optional	Optional	Optional	Off	Off	Off

6.3 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-2. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-up, Brownout, Supply Supervisor External Reset RST Watchdog Time-out, Key Violation FRAM uncorrectable bit error detection Software POR, FLL unlock error	SVSHIFG PMMRSTIFG WDTIFG PMMPORIFG, PMMBORIFG SYSRSTIV FLLUNLOCKIFG	Reset	FFFEh	63, Highest
System NMI Vacant Memory Access JTAG Mailbox FRAM bit error detection	VMAIFG JMBINIFG, JMBOUTIFG CBDIFG, UBDIFG	Nonmaskable	FFFCh	62
User NMI External NMI Oscillator Fault	NMIIFG OFIFG	Nonmaskable	FFFAh	61
Timer0_A3	TA0CCR0 CCIFG0	Maskable	FFF8h	60
Timer0_A3	TA0CCR1 CCIFG1, TA0CCR2 CCIFG2, TA0IFG (TA0IV)	Maskable	FFF6h	59
Timer1_A3	TA1CCR0 CCIFG0	Maskable	FFF4h	58
Timer1_A3	TA1CCR1 CCIFG1, TA1CCR2 CCIFG2, TA1IFG (TA1IV)	Maskable	FFF2h	57
RTC Counter	RTCIFG	Maskable	FFF0h	56
Watchdog Timer Interval mode	WDTIFG	Maskable	FFEEh	55
eUSCI_A0 Receive or Transmit	UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA0IV))	Maskable	FFECh	54

Table 6-2. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
eUSCI_B0 Receive or Transmit	UCB0RXIFG, UCB0TXIFG (SPI mode) UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I2C mode) (UCB0IV)	Maskable	FFEAh	53
ADC	ADCIFG0, ADCINIFG, ADCLOIFG, ADCHIIFG, ADCTOVIFG, ADCOVIFG (ADCIV)	Maskable	FFE8h	52
P1	P1IFG.0 to P1IFG.7 (P1IV)	Maskable	FFE6h	51
P2	P2IFG.0 to P2IFG.7 (P2IV)	Maskable	FFE4h	50
LCD	LCDBLKOFFIFG, LCDBLKONIFG, LCDFRMIFG (LCDEIV)	Maskable	FFE2h	49, Lowest
Reserved	Reserved	Maskable	FFE0h to FF88h	
Signatures	BSL Signature 2		0FF86h	
	BSL Signature 1		0FF84h	
	JTAG Signature 2		0FF82h	
	JTAG Signature 1		0FF80h	

6.4 Bootloader (BSL)

The BSL lets users program the FRAM or RAM using a UART serial interface. Access to the device memory through the BSL is protected by an user-defined password. Use of the BSL requires four pins as shown in Table 6-3. BSL entry requires a specific entry sequence on the $\overline{\text{RST}}$/NMI/SBWTDIO and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see the *MSP430 FRAM Device Bootloader (BSL) User's Guide*.

Table 6-3. BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.0	Data transmit
P1.1	Data receive
VCC	Power supply
VSS	Ground supply

6.5 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in Table 6-4. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming With the JTAG Interface*.

Table 6-4. JTAG Pin Requirements and Function

DEVICE SIGNAL	DIRECTION	JTAG FUNCTION
P1.4/MCLK/TCK/A4/VREF+	IN	JTAG clock input
P1.5/TA0CLK/TMS/A5	IN	JTAG state control
P1.6/TA0.2/TDI/TCLK/A6	IN	JTAG data input/TCLK input
P1.7/TA0.1/TDO/A7	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
RST/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

6.6 Spy-Bi-Wire Interface (SBW)

The MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. Table 6-5 shows the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*.

Table 6-5. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SBW FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
RST/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
VSS		Ground supply

6.7 FRAM

The FRAM can be programmed using the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Byte and word access capability
- Programmable wait state generation
- Error correction code (ECC) generation

6.8 Memory Protection

The device features memory protection that can restrict user access and enable write protection:

- Securing the whole memory map to prevent unauthorized access from JTAG port or BSL, by writing JTAG and BSL signatures using the JTAG port, SBW, the BSL, or in-system by the CPU.
- Write protection enabled to prevent unwanted write operation to FRAM contents by setting the control bits in System Configuration register 0. For more detailed information, see the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

NOTE

The FRAM is protected by default on PUC. To write to FRAM during code execution, the application must first clear the corresponding PFWP or DFWP bit in System Configuration Register 0 to unprotect the FRAM.

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be handled by using all instructions in the memory map. For complete module description, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

6.9.1 Power Management Module (PMM) and On-Chip Reference Voltages

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout reset circuit (BOR) is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary supply.

The device contains two on-chip reference: 1.5 V for internal reference and 1.2 V for external reference.

The 1.5-V reference is internally connected to ADC channel 13. DVCC is internally connected to ADC channel 15. When DVCC is set as the reference voltage for ADC conversion, the DVCC can be easily represent as Equation 1 by using ADC sampling 1.5-V reference without any external components support.

$$DVCC = (1023 \times 1.5\ V) \div 1.5\text{-V reference ADC result} \quad (1)$$

A 1.2-V reference voltage can be buffered and output to P1.4/MCLK/TCK/A4/VREF+, when the ADC channel 4 is selected as the function. For more detailed information, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

6.9.2 Clock System (CS) and Clock Distribution

The clock system includes a 32-kHz crystal oscillator (XT1), an internal very low-power low-frequency oscillator (VLO), an integrated 32-kHz RC oscillator (REFO), an integrated internal digitally controlled oscillator (DCO) that may use frequency-locked loop (FLL) locking with internal or external 32-kHz reference clock, and on-chip asynchronous high-speed clock (MODCLK). The clock system is designed to target cost-effective designs with minimal external components. A fail-safe mechanism is designed for XT1. The clock system module offers the following clock signals.

- Main Clock (MCLK): the system clock used by the CPU and all relevant peripherals accessed by the bus. All clock sources except MODCLK can be selected as the source with a predivider of 1, 2, 4, 8, 16, 32, 64, or 128.
- Sub-Main Clock (SMCLK): the subsystem clock used by the peripheral modules. SMCLK derives from the MCLK with a predivider of 1, 2, 4, or 8. This means SMCLK is always equal to or less than MCLK.
- Auxiliary Clock (ACLK): this clock is derived from the external XT1 clock or internal REFO clock up to 40 kHz.

All peripherals may have one or several clock sources depending on specific functionality. Table 6-6 shows the clock distribution used in this device.

Table 6-6. Clock Distribution

	CLOCK SOURCE SELECT BITS	MCLK	SMCLK	ACLK	MODCLK	XT1CLK(1)	VLOCLK	EXTERNAL PIN
Frequency Range		DC to 16 MHz	DC to 16 MHz	DC to 40 kHz	5 MHz ±10%	DC to 40 kHz	10 kHz ±50%	
CPU	N/A	Default						
FRAM	N/A	Default						
RAM	N/A	Default						
CRC	N/A	Default						
I/O	N/A	Default						
TA0	TASSEL		10b	01b				00b (TA0CLK pin)
TA1	TASSEL		10b	01b				00b (TA1CLK pin)
eUSCI_A0	UCSSELx		10b or 11b		01b			00b (UCA0CLK pin)
eUSCI_B0	UCSSELx		10b or 11b		01b			00b (UCB0CLK pin)
WDT	WDTSSEL		00b	01b			10b	
ADC	ADCSSEL		10b or 11b	01b	00b			
LCD	LCDSSEL			01b		00b	10b	
RTC	RTCSS		01b			10b	11b	

(1) To enable XT1 functionality, configure P4SEL0.1 (XIN) and P4SEL0.2 (XOUT) before configuring the Clock System registers.

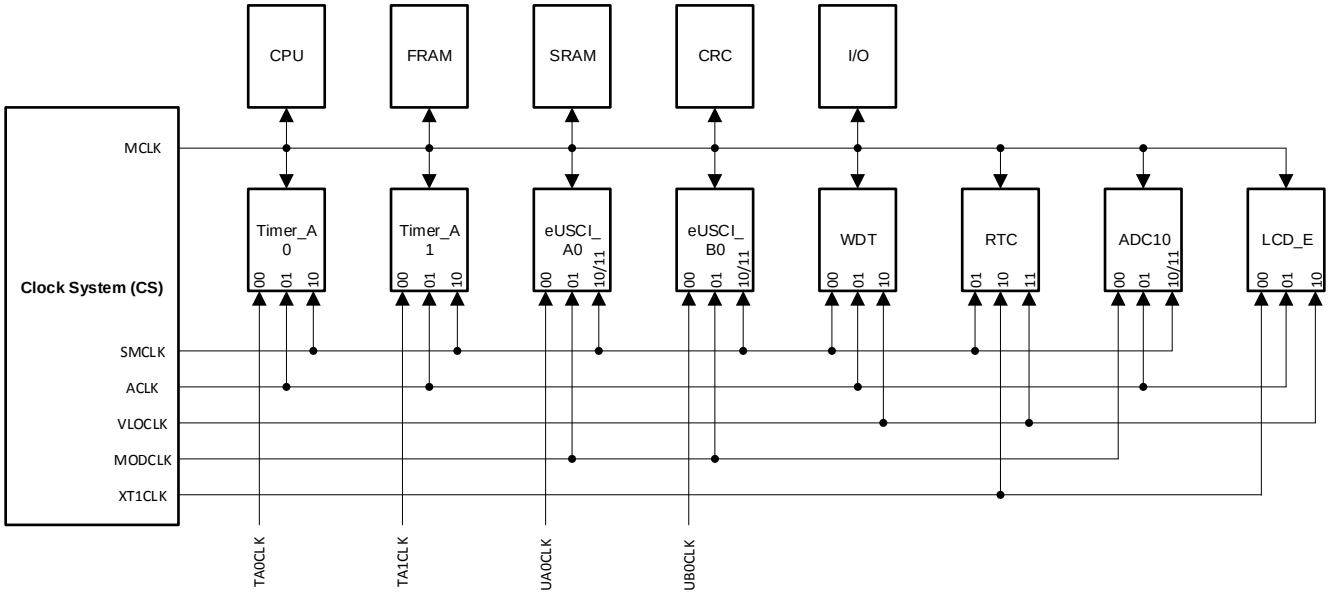


Figure 6-1. Clock Distribution Block Diagram

6.9.3 General-Purpose Input/Output Port (I/O)

Up to 60 I/O ports are implemented.

- P1, P2, P3, P4, P5, P6, and P7 are full 8-bit ports; P8 has 4 bits implemented.
- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for P1 and P2.
- Read and write access to port-control registers is supported by all instructions.

- Ports can be accessed byte-wise or word-wise in pairs.
- Capacitive Touch IO functionality is supported on all pins.

NOTE

Configuration of digital I/Os after BOR reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions disabled. To enable the I/O functions after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section in the Digital I/O chapter of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

6.9.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as interval timer and can generate interrupts at selected time intervals.

Table 6-7. WDT Clocks

WDTSSEL	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	VLOCLK

6.9.5 System Module (SYS)

The SYS module handles many of the system functions within the device. These include Power-On Reset (POR) and Power-Up Clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). SYS also includes a data exchange mechanism through SBW called a JTAG mailbox mail box that can be used in the application.

Table 6-8. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	015Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RSTIFG $\overline{\text{RST}}$/NMI (BOR)	04h	
		PMMSWBOR software BOR (BOR)	06h	
		LPMx.5 wakeup (BOR)	08h	
		Security violation (BOR)	0Ah	
		Reserved	0Ch	
		SVSHIFG SVSH event (BOR)	0Eh	
		Reserved	10h	
		Reserved	12h	
		PMMSWPOR software POR (POR)	14h	
		WDTIFG watchdog time-out (PUC)	16h	
		WDTPW password violation (PUC)	18h	
		FRCTLPW password violation (PUC)	1Ah	
		Uncorrectable FRAM bit error detection	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMMPW PMM password violation (PUC)	20h	
		Reserved	22h	
		FLL unlock (PUC)	24h	
		Reserved	26h to 3Eh	Lowest

Table 6-8. System Module Interrupt Vector Registers (continued)

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSSNIV, System NMI	015Ch	No interrupt pending	00h	
		SVS low-power reset entry	02h	Highest
		Uncorrectable FRAM bit error detection	04h	
		Reserved	06h	
		Reserved	08h	
		Reserved	0Ah	
		Reserved	0Ch	
		Reserved	0Eh	
		Reserved	10h	
		VMAIFG Vacant memory access	12h	
		JMBINIFG JTAG mailbox input	14h	
		JMBOUTIFG JTAG mailbox output	16h	
		Correctable FRAM bit error detection	18h	
		Reserved	1Ah to 1Eh	Lowest
SYSUNIV, User NMI	015Ah	No interrupt pending	00h	
		NMIIFG NMI pin or SVS_H event	02h	Highest
		OFIFG oscillator fault	04h	
		Reserved	06h to 1Eh	Lowest

6.9.6 Cyclic Redundancy Check (CRC)

The 16-bit cyclic redundancy check (CRC) module produces a signature based on a sequence of data values and can be used for data checking purposes. The CRC generation polynomial is compliant with CRC-16-CCITT standard of $x^{16} + x^{12} + x^5 + 1$.

6.9.7 Enhanced Universal Serial Communication Interface (eUSCI_A0, eUSCI_B0)

The eUSCI modules are used for serial data communications. The eUSCI_A module supports either UART or SPI communications. The eUSCI_B module supports either SPI or I^2C communications. Additionally, eUSCI_A supports automatic baud-rate detection and IrDA.

Table 6-9. eUSCI Pin Configurations

	PIN	UART	SPI
eUSCI_A0	P1.0	TXD	SIMO
	P1.1	RXD	SOMI
	P1.2		SCLK
	P1.3		STE
	PIN	**I^2C**	**SPI**
eUSCI_B0	P5.0		STE
	P5.1		SCLK
	P5.2	SDA	SIMO
	P5.3	SCL	SOMI

6.9.8 Timers (Timer0_A3, Timer1_A3)

The Timer0_A3 and Timer1_A3 modules are 16-bit timers and counters with three capture/compare registers each. Each can support multiple captures or compares, PWM outputs, and interval timing. Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. The CCR0 registers on both TA0 and TA1 are not externally connected and can only be used for hardware period timing and interrupt generation. In Up Mode, they can be used to set the overflow value of the counter.

Table 6-10. Timer0_A3 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P1.5	TA0CLK	TACLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	from Capacitive Touch IO (internal)	INCLK			
		CCI0A	CCR0	TA0	
		CCI0B			Timer1_A3 CCI0B input
	DVSS	GND			
	DVCC	VCC			
P1.7	TA0.1	CCI1A	CCR1	TA1	TA0.1
	from RTC (internal)	CCI1B			Timer1_A3 CCI1B input
	DVSS	GND			
	DVCC	VCC			
P1.6	TA0.2	CCI2A	CCR2	TA2	TA0.2
	from Capacitive Touch I/O (internal)	CCI2B			Timer1_A3 INCLK Timer1_A3 CCI2B input, IR Input
	DVSS	GND			
	DVCC	VCC			

Table 6-11. Timer1_A3 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P8.2	TA1CLK	TACLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	Timer0_A3 CCR2B output (internal)	INCLK			
		CCI0A	CCR0	TA0	
	Timer0_A3 CCR0B output (internal)	CCI0B			
	DVSS	GND			
	DVCC	VCC			
P4.0	TA1.1	CCI1A	CCR1	TA1	TA1.1
	Timer0_A3 CCR1B output (internal)	CCI1B			to ADC trigger
	DVSS	GND			
	DVCC	VCC			
P8.3	TA1.2	CCI2A	CCR2	TA2	TA1.2
	Timer0_A3 CCR2B output (internal)	CCI2B			IR Input
	DVSS	GND			
	DVCC	VCC			

The interconnection of Timer0_A3 and Timer1_A3 can be used to modulate the eUSCI_A pin of UCA0TXD/UCA0SIMO in either ASK or FSK mode, with which a user can easily acquire a modulated infrared command for directly driving an external IR diode. The IR functions are fully controlled by SYS configuration registers 1 including IREN (enable), IRPSEL (polarity select), IRMSEL (mode select), IRDSSEL (data select), and IRDATA (data) bits. For more information, see the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

6.9.9 Real-Time Clock (RTC) Counter

The RTC counter is a 16-bit modulo counter that is functional in AM, LPM0, LPM3, and LPM3.5. This module may periodically wake up the CPU from LPM0, LPM3, and LPM3.5 based on timing from a low-power clock source such as the XT1 and VLO clocks. In AM, RTC can be driven by SMCLK to generate high-frequency timing events and interrupts. The RTC overflow events trigger:

- Timer0_A3 CCR1B
- ADC conversion trigger when ADCSHSx bits are set as 01b

6.9.10 10-Bit Analog Digital Converter (ADC)

The 10-bit ADC module supports fast 10-bit analog-to-digital conversions with single-ended input. The module implements a 10-bit SAR core, sample select control, reference generator and a conversion result buffer. A window comparator with a lower and upper limit allows CPU independent result monitoring with three window comparator interrupt flags.

The ADC supports 10 external inputs and four internal inputs (see Table 6-12).

Table 6-12. ADC Channel Connections

ADCINCHx	ADC CHANNELS	EXTERNAL PIN OUT
0	A0/Veref–	P1.0
1	A1/Veref+	P1.1
2	A2	P1.2
3	A3	P1.3
4	A4 (1)	P1.4
5	A5	P1.5
6	A6	P1.6
7	A7	P1.7
8	A8	P8.0 (2)
9	A9	P8.1 (2)
10	Not Used	N/A
11	Not Used	N/A
12	On-chip Temperature Sensor	N/A
13	Reference Voltage (1.5 V)	N/A
14	DVSS	N/A
15	DVCC	N/A

(1) When A4 is used, the PMM 1.2-V reference voltage can be output to this pin by setting the PMM control register. The 1.2-V voltage can be directly measured by A4 channel.
(2) P8.0 and P8.1 are only available in the LQFP-64 package.

The AD conversion can be started by software or a hardware trigger. Table 6-13 shows the trigger sources that are available.

Table 6-13. ADC Trigger Signal Connections

ADCSHSx		TRIGGER SOURCE
Binary	Decimal	
00	0	ADCSC bit (software trigger)
01	1	RTC event
10	2	TA1.1B
11	3	TA1.2B

6.9.11 Liquid Crystal Display (LCD)

The LCD driver generates the segment and common signals to drive segment liquid crystal display (LCD) glass. The LCD controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, up to 8-mux LCDs are supported. The module can provide an LCD voltage independent from the main supply voltage with its integrated charge pump. The LCD display contrast can be trimmed by setting the LCD drive voltage. The LCD module can be fully functional in any power mode from AM to LPM3.5.

When supplied by the on-chip charge pump with on-chip regulator reference, the LCD driver needs five pins and four external 0.1-µF capacitors to achieve low-power consumption during operation. Figure 6-2 shows the recommended connections.

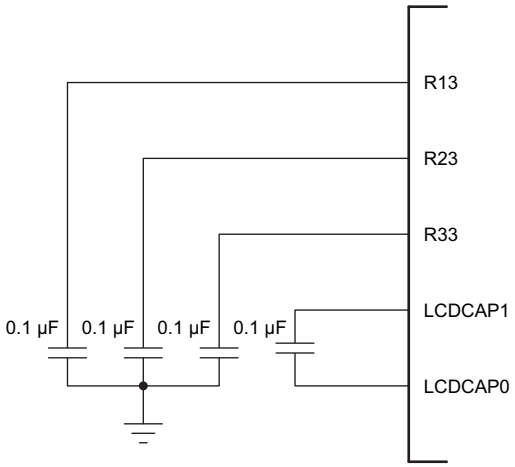


Figure 6-2. LCD Power Supply Configuration With On-Chip Charge Pump and Regulator Reference

The LCD contains 20 16-bit words (40 bytes) display memory. The use of memory is flexible, depending on the selected mode:

- 4-mux mode
  - LCDM0 to LCDM19 can be used for LCD display contents. If it is not used as LCD drive pin, the corresponding LCDMx can be used for user data (up to 20 bytes).
  - LCDBM0 to LCDBM19 can be used for LCD blinking contents. If it is not used as blinking, the corresponding LCDBMx can be used for user data (up to 20 bytes).
- 8-mux mode
  - LCDM0 to LCDM39 can be used for LCD display contents. If it is not used as LCD drive pin, the corresponding LCDMx can be used for user data (up to 40 bytes).

6.9.12 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The EEM on these devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.9.13 Input/Output Schematics

6.9.13.1 Port P1 Input/Output With Schmitt Trigger

Figure 6-3 shows the port schematic. Table 6-14 summarizes the selection of the pin functions.

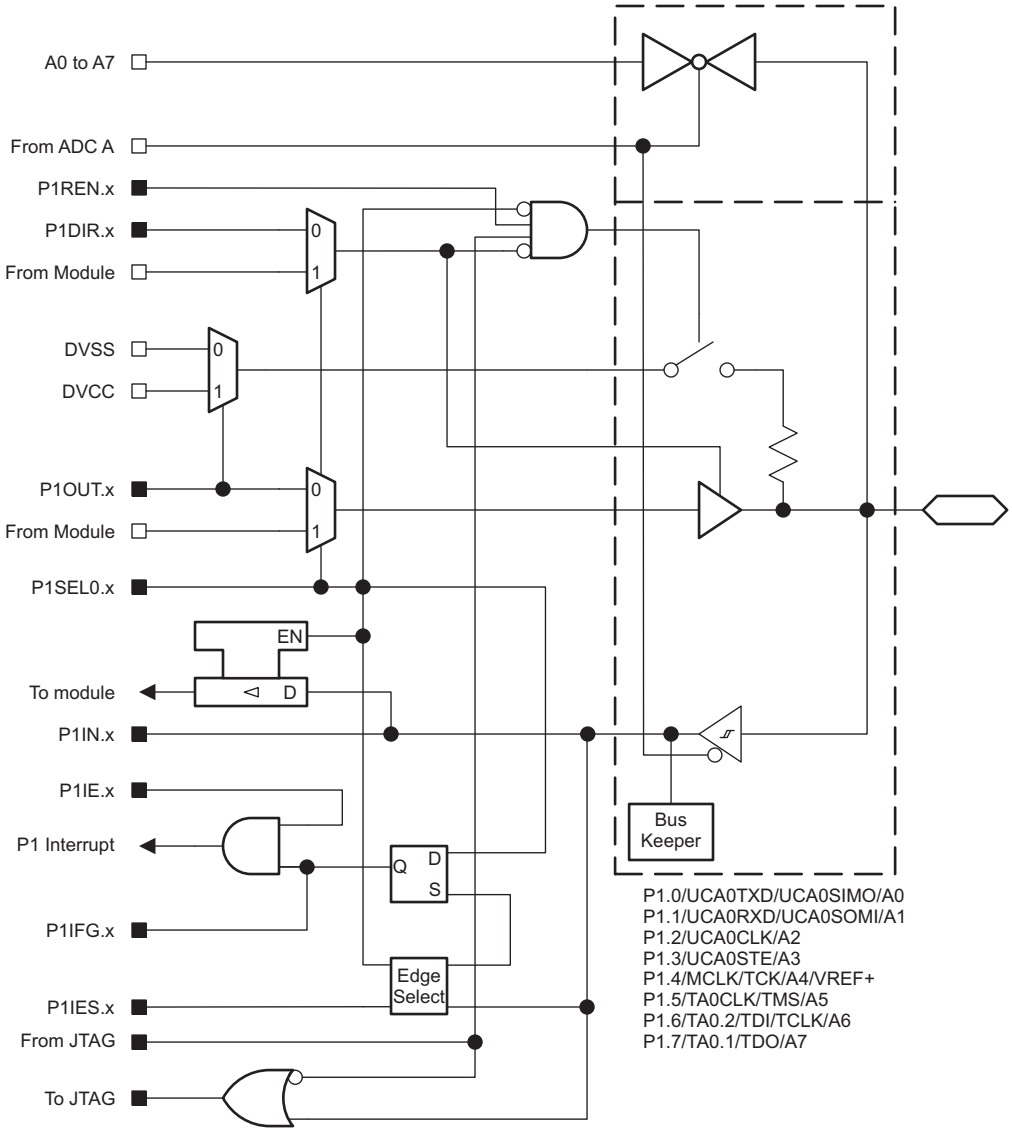


Figure 6-3. Port P1 Input/Output With Schmitt Trigger

Table 6-14. Port P1 Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)			
			P1DIR.x	P1SEL0.x	ADCPCTLx(2)	JTAG
P1.0/UCA0TXD/ UCA0SIMO/A0	0	P1.0 (I/O)	I: 0; O: 1	0	0	N/A
		UCA0TXD/UCA0SIMO	X	1	0	N/A
		A0	X	X	1 (x = 0)	N/A
P1.1/UCA0RXD/ UCA0SOMI/A1	1	P1.1 (I/O)	I: 0; O: 1	0	0	N/A
		UCA0RXD/UCA0SOMI	X	1	0	N/A
		A1	X	X	1 (x = 1)	N/A
P1.2/UCA0CLK/A2	2	P1.2 (I/O)	I: 0; O: 1	0	0	N/A
		UCA0CLK	X	1	0	N/A
		A2	X	X	1 (x = 2)	N/A
P1.3/UCA0STE/A3	3	P1.3 (I/O)	I: 0; O: 1	0	0	N/A
		UCA0STE	X	1	0	N/A
		A3	X	X	1 (x = 3)	N/A
P1.4/MCLK/TCK/A4/ VREF+	4	P1.4 (I/O)	I: 0; O: 1	0	0	Disabled
		VSS	0	1	0	Disabled
		MCLK	1			
		A4, VREF+	X	X	1 (x = 4)	Disabled
		JTAG TCK	X	X	X	TCK
P1.5/TA0CLK/TMS/A5	5	P1.5 (I/O)	I: 0; O: 1	0	0	Disabled
		TA0CLK	0	1	0	Disabled
		VSS	1			
		A5	X	X	1 (x = 5)	Disabled
		JTAG TMS	X	X	X	TMS
P1.6/TA0.2/TDI/TCLK/ A6	6	P1.6 (I/O)	I: 0; O: 1	0	0	Disabled
		TA0.CCI2A	0	1	0	Disabled
		TA0.2	1			
		A6	X	X	1 (x = 6)	Disabled
		JTAG TDI/TCLK	X	X	X	TDI/TCLK
P1.7/TA0.1/TDO/A7	7	P1.7 (I/O)	I: 0; O: 1	0	0	Disabled
		TA0.CCI1A	0	1	0	Disabled
		TA0.1	1			
		A7	X	X	1 (x = 7)	Disabled
		JTAG TDO	X	X	X	TDO

(1) X = don't care
(2) Setting the ADCPCTLx bit in SYSCFG2 register will disable both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

6.9.13.2 Port P2 Input/Output With Schmitt Trigger

Figure 6-4 shows the port schematic. Table 6-15 summarizes the selection of the pin functions.

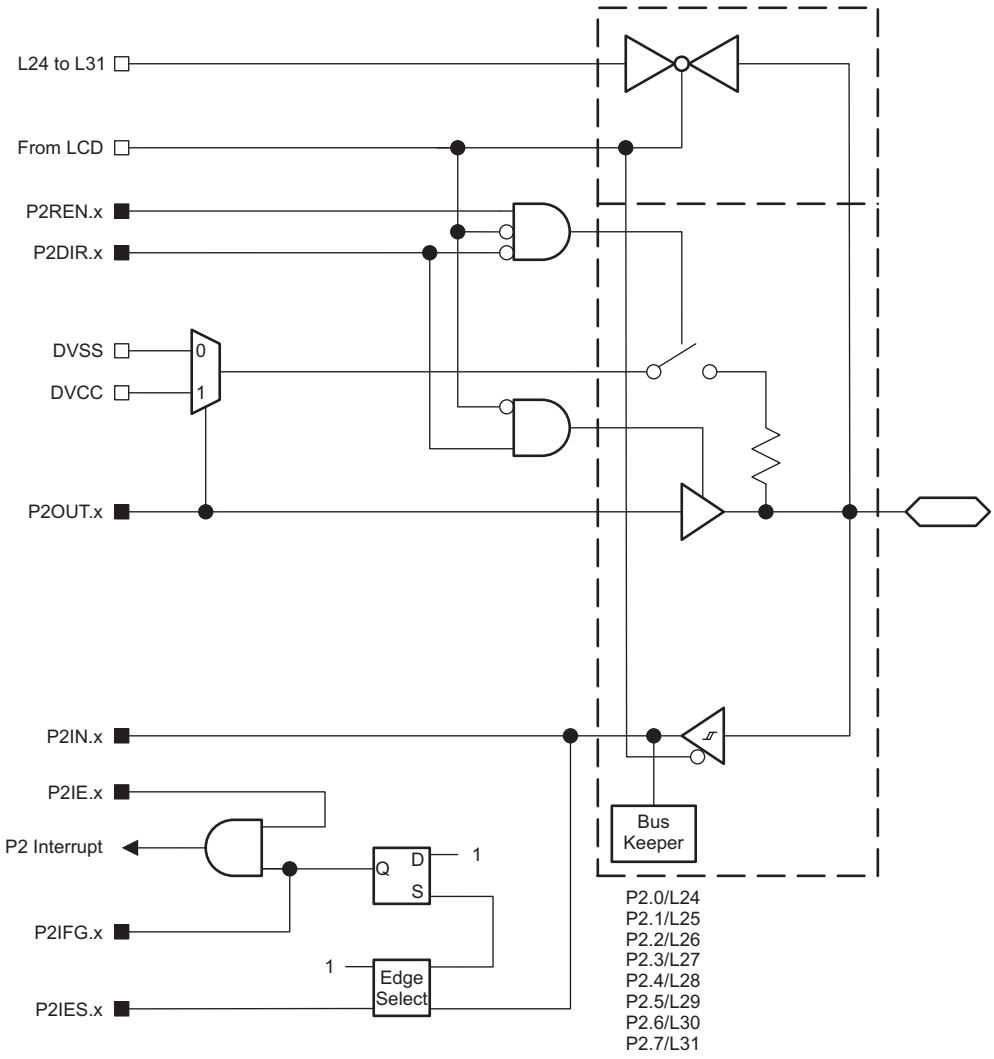


Figure 6-4. Port P2 Input/Output With Schmitt Trigger

Table 6-15. Port P2 Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P2DIR.x	LCDSy
P2.0/L24	0	P2.0 (I/O)	I: 0; O: 1	0
		L24	X	1 (y = 24)
P2.1/L25	1	P2.1 (I/O)	I: 0; O: 1	0
		L25	X	1 (y = 25)
P2.2/L26	2	P2.2 (I/O)	I: 0; O: 1	0
		L26	X	1 (y = 26)
P2.3/L27	3	P2.3 (I/O)	I: 0; O: 1	0
		L27	X	1 (y = 27)
P2.4/L28	4	P2.4 (I/O)	I: 0; O: 1	0
		L28	X	1 (y = 28)
P2.5/L29	5	P2.5 (I/O)	I: 0; O: 1	0
		L29	X	1 (y = 29)
P2.6/L30	6	P2.6 (I/O)	I: 0; O: 1	0
		L30	X	1 (y = 30)
P2.7/L31	7	P2.7 (I/O)	I: 0; O: 1	0
		L31	X	1 (y = 31)

(1) X = don't care

6.9.13.3 Port P3 Input/Output With Schmitt Trigger

Figure 6-5 shows the port schematic. Table 6-16 summarizes the selection of the pin functions.

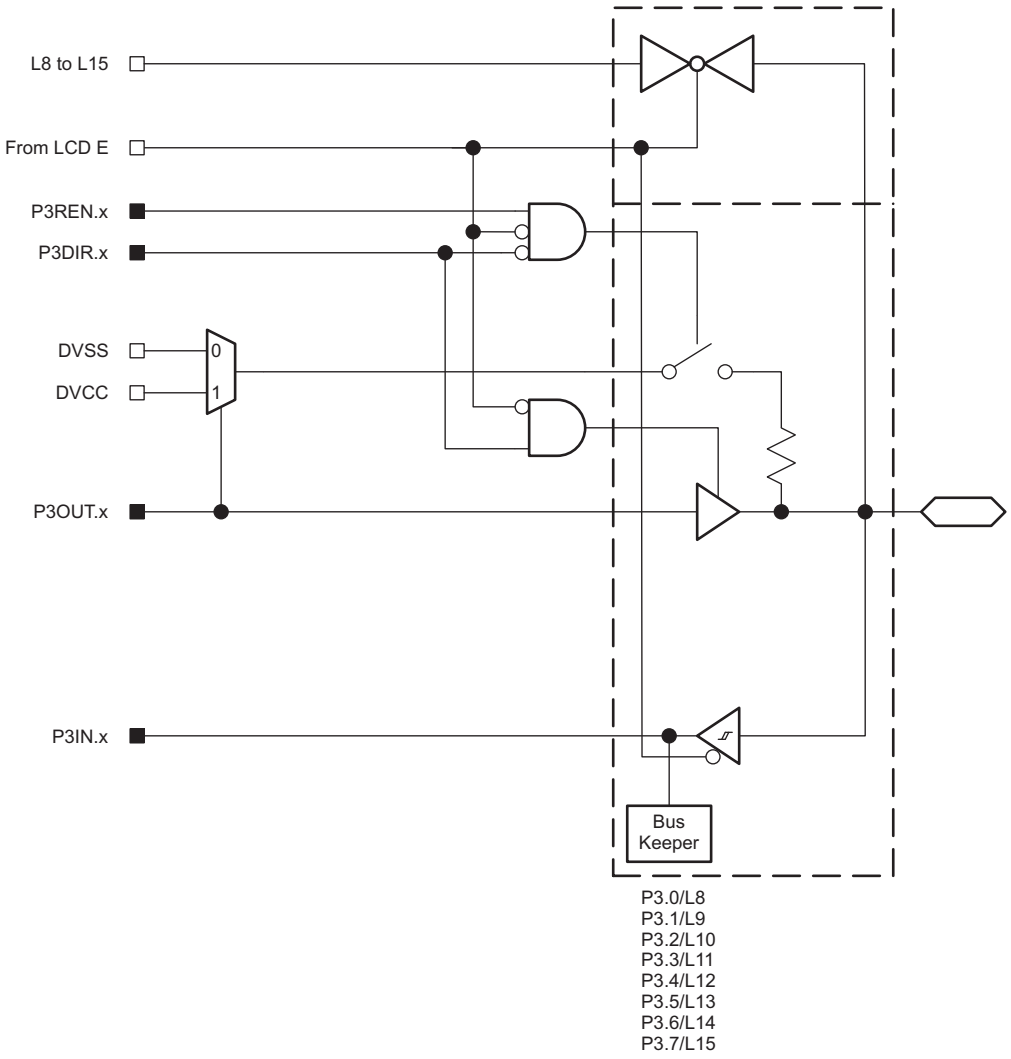


Figure 6-5. Port P3 Input/Output With Schmitt Trigger

Table 6-16. Port P3 Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P3DIR.x	LCDSy
P3.0/L8	0	P3.0 (I/O)	I: 0; O: 1	0
		L8	X	1 (y = 8)
P3.1/L9	1	P3.1 (I/O)	I: 0; O: 1	0
		L9	X	1 (y = 9)
P3.2/L10	2	P3.2 (I/O)	I: 0; O: 1	0
		L10	X	1 (y = 10)
P3.3/L11	3	P3.3 (I/O)	I: 0; O: 1	0
		L11	X	1 (y = 11)
P3.4/L12	4	P3.4 (I/O)	I: 0; O: 1	0
		L12	X	1 (y = 12)
P3.5/L13	5	P3.5 (I/O)	I: 0; O: 1	0
		L13	X	1 (y = 13)
P3.6/L14	6	P3.6 (I/O)	I: 0; O: 1	0
		L14	X	1 (y = 14)
P3.7/L15	7	P3.7 (I/O)	I: 0; O: 1	0
		L15	X	1 (y = 15)

(1) X = don't care

6.9.13.4 Port P4.0 Input/Output With Schmitt Trigger

Figure 6-6 shows the port schematic. Table 6-17 summarizes the selection of the pin functions.

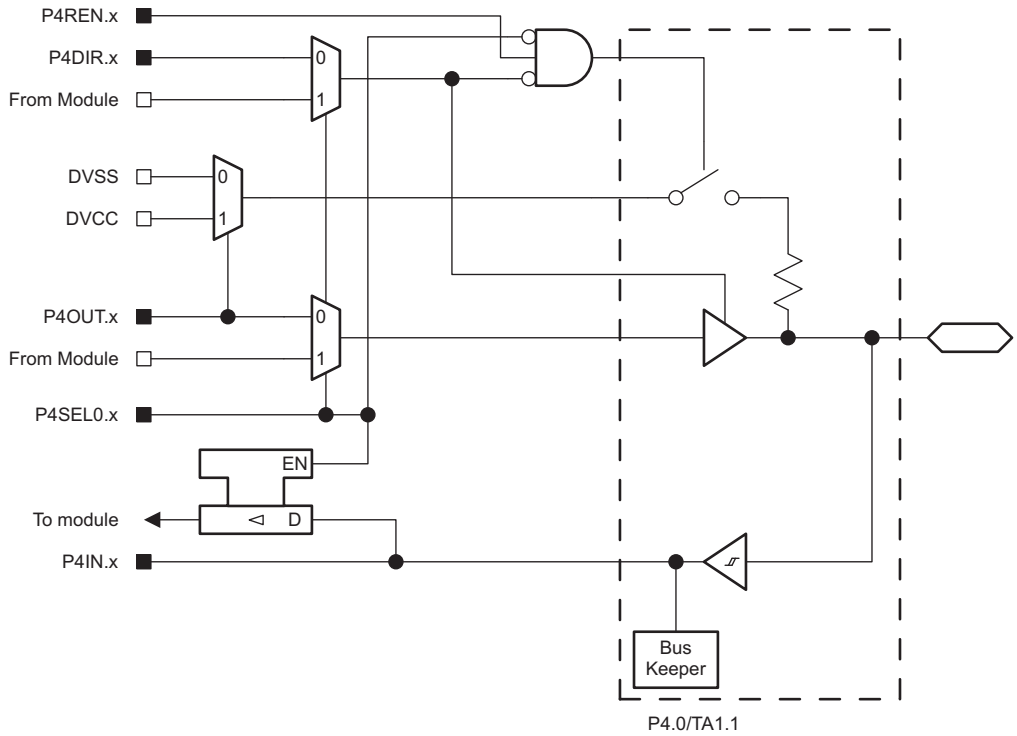


Figure 6-6. Port P4.0 Input/Output With Schmitt Trigger

Table 6-17. Port P4.0 Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS	
			P4DIR.x	P4SEL0.x
P4.0/TA1.1	0	P4.0 (I/O)	I: 0; O: 1	0
		TA1.CCI1A	0	1
		TA1.1	1	

6.9.13.5 Port P4.1 and P4.2 Input/Output With Schmitt Trigger

Figure 6-7 shows the port schematic. Table 6-18 summarizes the selection of the pin functions.

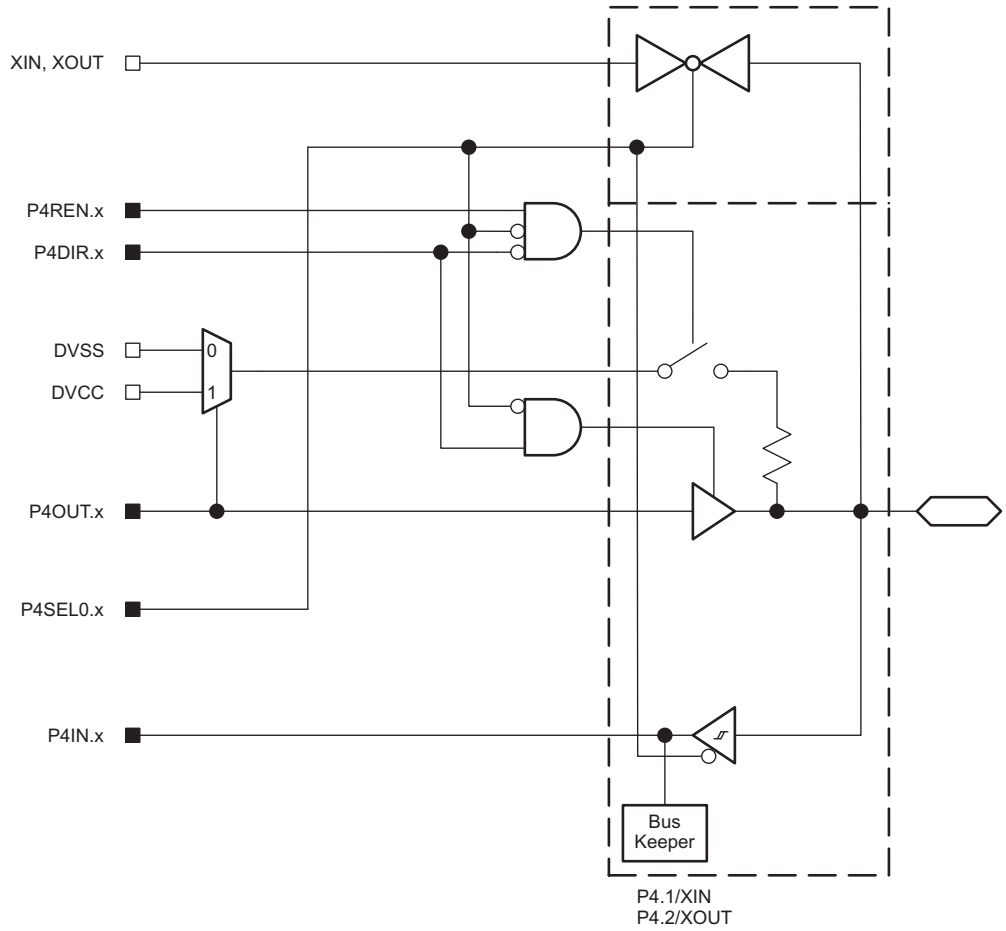


Figure 6-7. Port P4.1 and P4.2 Input/Output With Schmitt Trigger

Table 6-18. Port P4.1 and P4.2 Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P4DIR.x	P4SEL0.x
P4.1/XIN	1	P4.1 (I/O)	I: 0; O: 1	0
		XIN	X	1
P4.2/XOUT	2	P4.2 (I/O)	I: 0; O: 1	0
		XOUT	X	1

(1) X = don't care

6.9.13.6 Port 4.3, P4.4, P4.5, P4.6, and P4.7 Input/Output With Schmitt Trigger

Figure 6-8 shows the port schematic. Table 6-19 summarizes the selection of the pin functions.

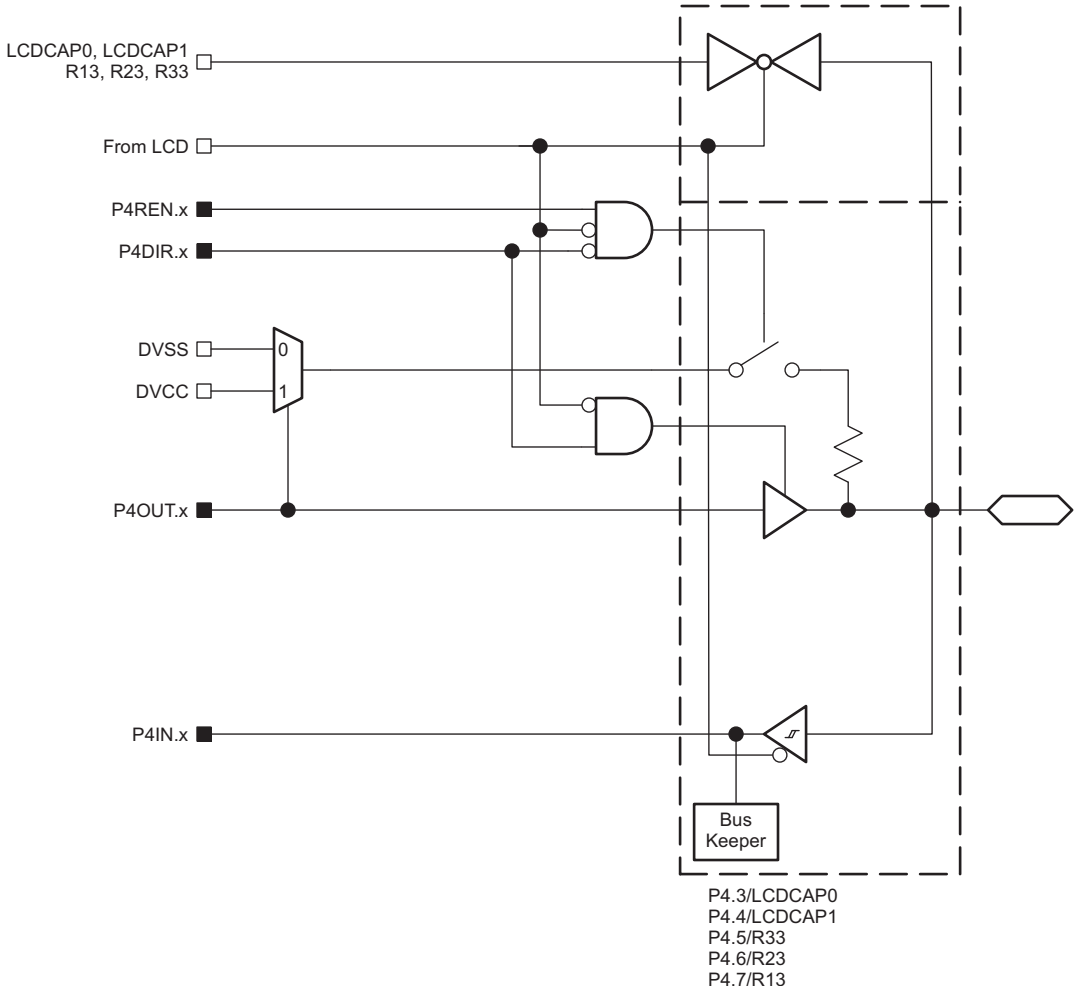


Figure 6-8. Port 4.3, P4.4, P4.5, P4.6, and P4.7 Input/Output With Schmitt Trigger

Table 6-19. Port P4.3, P4.4, P4.5, P4.6, and P4.7 Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P4DIR.x	LCDPCTL(2)
P4.3/LCDCAP0	3	P4.3 (I/O)	I: 0; O: 1	X
		LCDCAP0	X	1
P4.4/LCDCAP1	4	P4.4 (I/O)	I: 0; O: 1	0
		LCDCAP1	X	1
P4.5/R33	5	P4.5 (I/O)	I: 0; O: 1	0
		R33	X	1
P4.6/R23	6	P4.6 (I/O)	I: 0; O: 1	0
		R23	X	1
P4.7/R13	7	P4.7 (I/O)	I: 0; O: 1	0
		R13	X	1

(1) X = don't care
(2) Setting the LCDPCTL bit in SYSCFG2 register will disable both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

6.9.13.7 Port P5.0, P5.1, P5.2, and P5.3 Input/Output With Schmitt Trigger

Figure 6-9 shows the port schematic. Table 6-20 summarizes the selection of the pin functions.

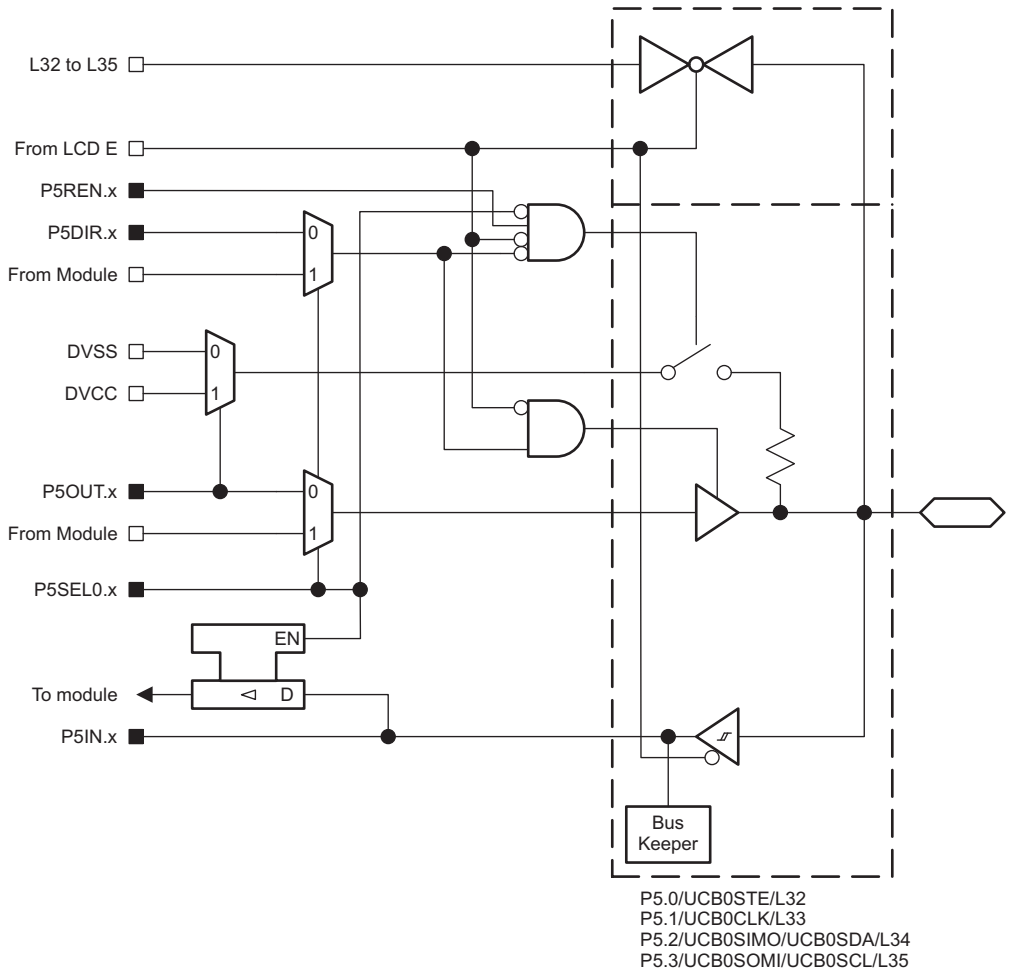


Figure 6-9. Port P5.0, P5.1, P5.2, and P5.3 Input/Output With Schmitt Trigger

Table 6-20. Port P5.0, P5.1, P5.2, and P5.3 Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P5DIR.x	P5SEL0.x	LCDSy
P5.0/UCB0STE/L32	0	P5.0 (I/O)	I: 0; O: 1	0	0
		UCB0STE	0	1	0
		L32	X	X	1 (y = 32)
P5.1/UCB0CLK/L33	1	P5.1 (I/O)	I: 0; O: 1	0	0
		UCB0CLK	0	1	0
		L33	X	X	1 (y = 33)
P5.2/UCB0SIMO/ UCB0SDA/L34	2	P5.2 (I/O)	I: 0; O: 1	0	0
		UCB0SIMO/UCB0SDA	0	1	0
		L34	X	X	1 (y = 34)
P5.3/UCB0SOMI/ UCB0SCL/L35	3	P5.3 (I/O)	I: 0; O: 1	0	0
		UCB0SOMI/UCB0SCL	0	1	0
		L35	X	X	1 (y = 35)

(1) X = don't care

6.9.13.8 Port P5.4, P5.5, P5.6, and P5.7 Input/Output With Schmitt Trigger

Figure 6-10 shows the port schematic. Table 6-21 summarizes the selection of the pin functions.

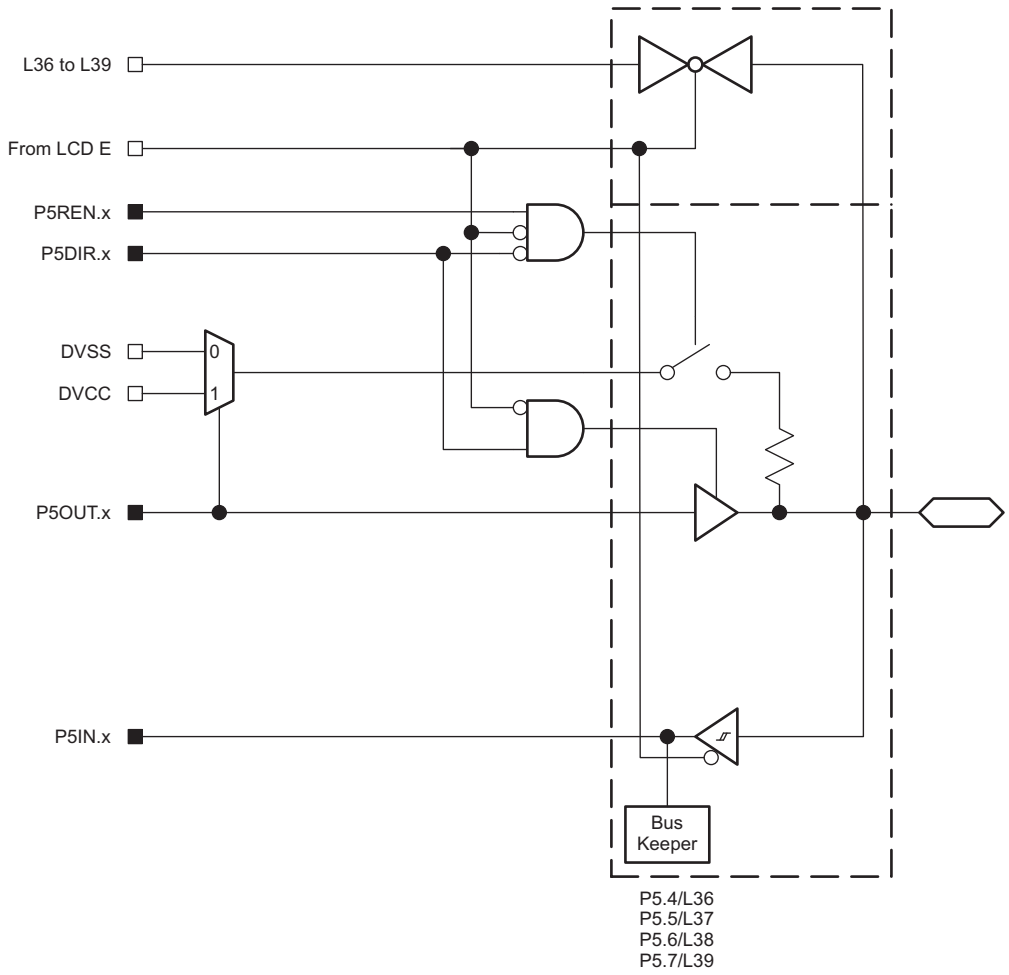


Figure 6-10. Port P5.4, P5.5, P5.6, and P5.7 Input/Output With Schmitt Trigger

Table 6-21. Port P5.4, P5.5, P5.6, and P5.7 Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P5DIR.x	LCDSy
P5.4/L36	4	P5.4 (I/O)	I: 0; O: 1	0
		L36	X	1 (y = 36)
P5.5/L37	5	P5.5 (I/O)	I: 0; O: 1	0
		L37	X	1 (y = 37)
P5.6/L38	6	P5.6 (I/O)	I: 0; O: 1	0
		L38	X	1 (y = 38)
P5.7/L39	7	P5.7 (I/O)	I: 0; O: 1	0
		L39	X	1 (y = 39)

(1) X = don't care

6.9.13.9 Port P6 Input/Output With Schmitt Trigger

Figure 6-11 shows the port schematic. Table 6-22 summarizes the selection of the pin functions.

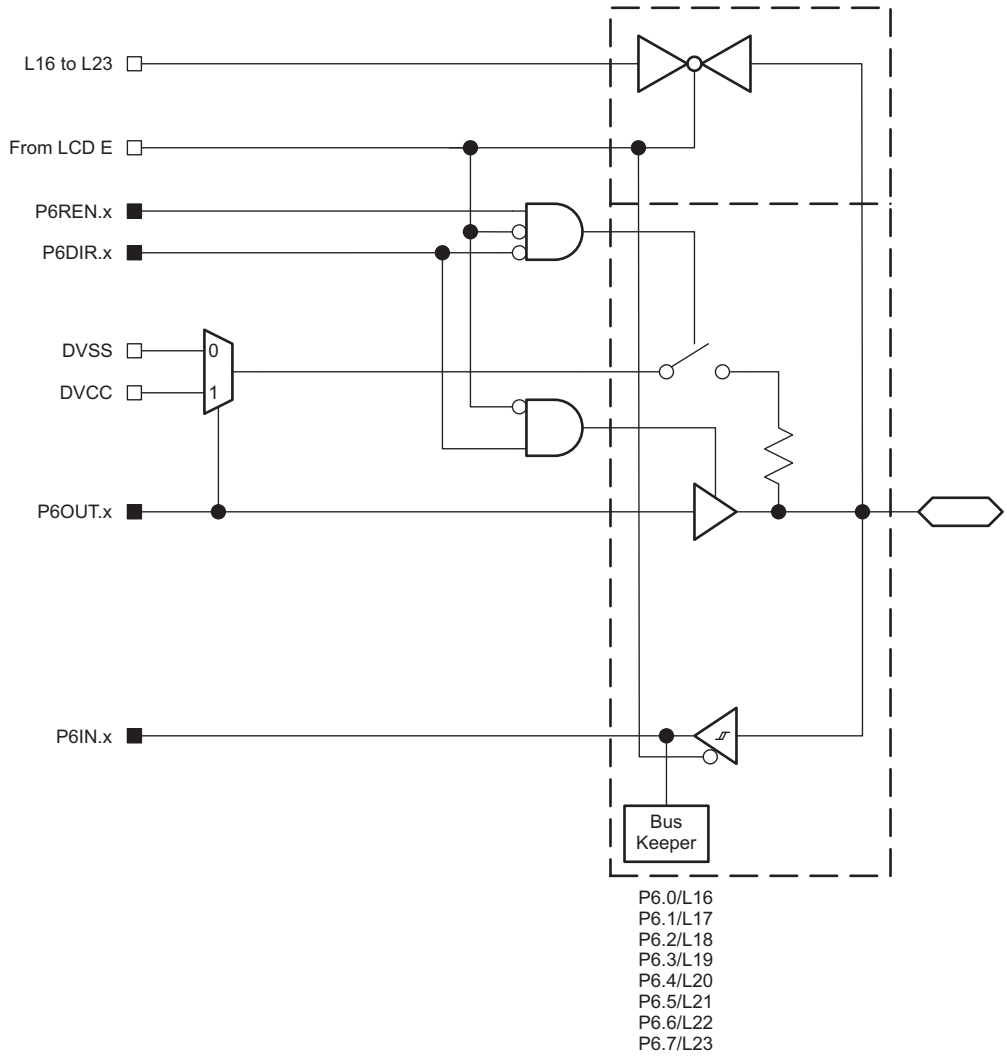


Figure 6-11. Port P6 Input/Output With Schmitt Trigger

Table 6-22. Port P6 Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P6DIR.x	LCDSy
P6.0/L16	0	P6.0 (I/O)	I: 0; O: 1	0
		L16	X	1 (y = 16)
P6.1/L17	1	P6.1 (I/O)	I: 0; O: 1	0
		L17	X	1 (y = 17)
P6.2/L18	2	P6.2 (I/O)	I: 0; O: 1	0
		L18	X	1 (y = 18)
P6.3/L19	3	P6.3 (I/O)	I: 0; O: 1	0
		L19	X	1 (y = 19)
P6.4/L20	4	P6.4 (I/O)	I: 0; O: 1	0
		L20	X	1 (y = 20)
P6.5/L21	5	P6.5 (I/O)	I: 0; O: 1	0
		L21	X	1 (y = 21)
P6.6/L22	6	P6.6 (I/O)	I: 0; O: 1	0
		L22	X	1 (y = 22)
P6.7/L23	7	P6.7 (I/O)	I: 0; O: 1	0
		L23	X	1 (y = 23)

(1) X = don't care

6.9.13.10 Port P7 Input/Output With Schmitt Trigger

Figure 6-12 shows the port schematic. Table 6-23 summarizes the selection of the pin functions.

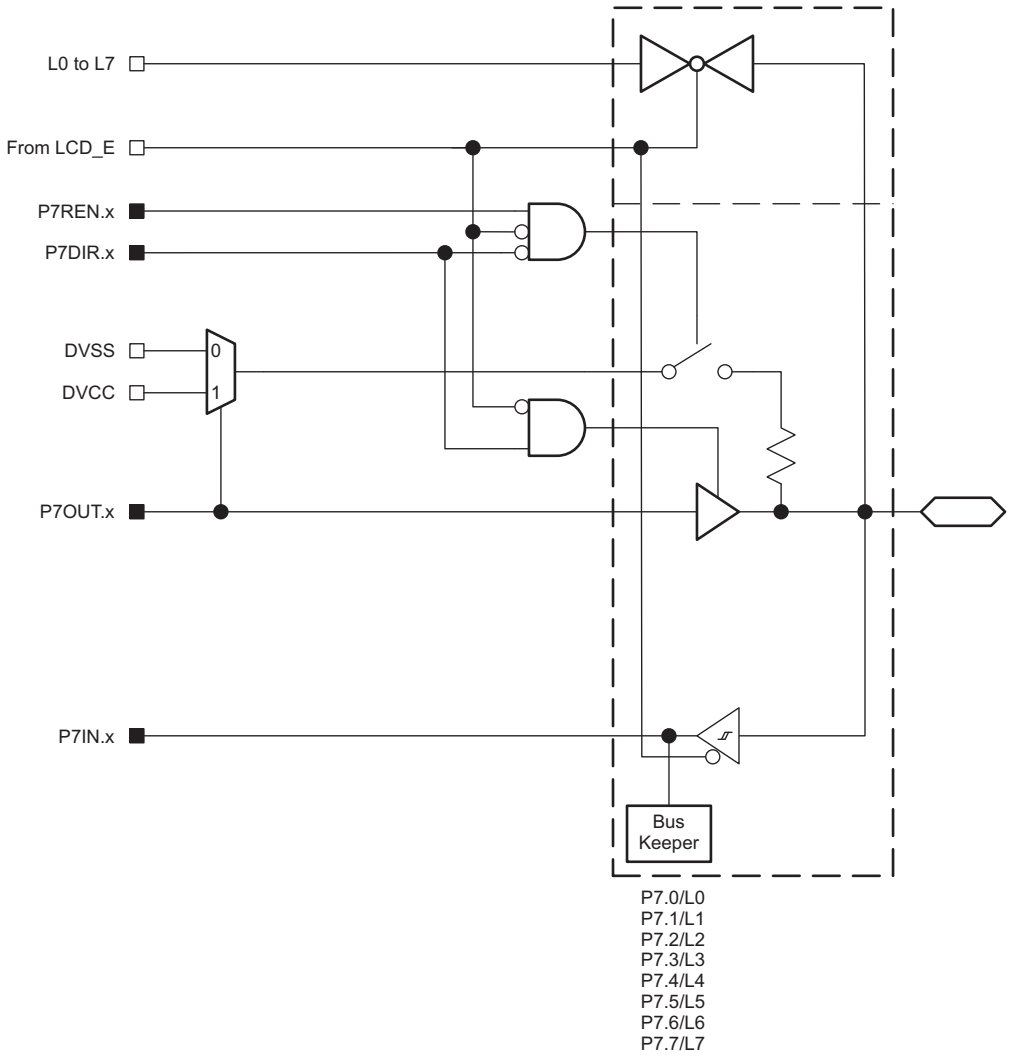


Figure 6-12. Port P7 Input/Output With Schmitt Trigger

Table 6-23. Port P7 Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)	
			P7DIR.x	LCDSy
P7.0/L0	0	P7.0 (I/O)	I: 0; O: 1	0
		L0	X	1 (y = 0)
P7.1/L1	1	P7.1 (I/O)	I: 0; O: 1	0
		L1	X	1 (y = 1)
P7.2/L2	2	P7.2 (I/O)	I: 0; O: 1	0
		L2	X	1 (y = 2)
P7.3/L3	3	P7.3 (I/O)	I: 0; O: 1	0
		L3	X	1 (y = 3)
P7.4/L4	4	P7.4 (I/O)	I: 0; O: 1	0
		L4	X	1 (y = 4)
P7.5/L5	5	P7.5 (I/O)	I: 0; O: 1	0
		L5	X	1 (y = 5)
P7.6/L6	6	P7.6 (I/O)	I: 0; O: 1	0
		L6	X	1 (y = 6)
P7.7/L7	7	P7.7 (I/O)	I: 0; O: 1	0
		L7	X	1 (y = 7)

(1) X = don't care

6.9.13.11 Port P8.0 and P8.1 Input/Output With Schmitt Trigger

Figure 6-13 shows the port schematic. Table 6-24 summarizes the selection of the pin functions.

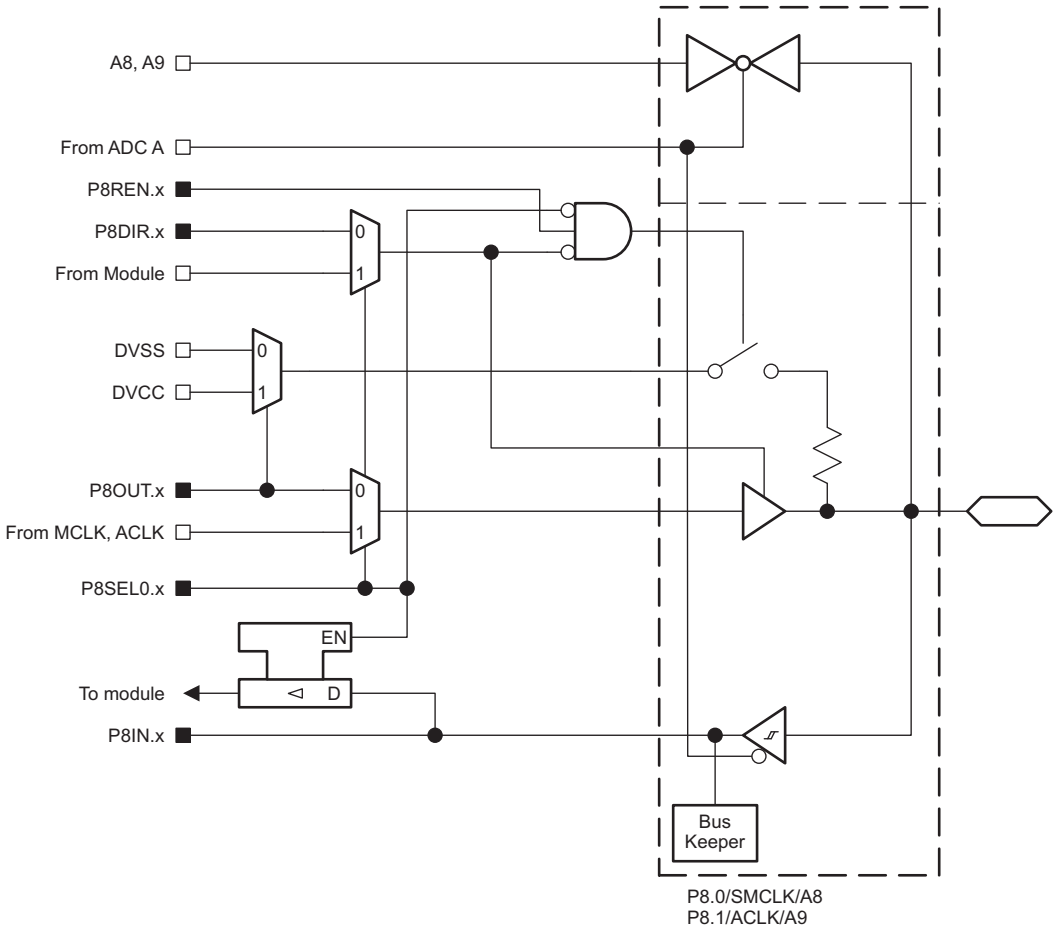


Figure 6-13. Port P8.0 and P8.1 Input/Output With Schmitt Trigger

Table 6-24. Port P8.0 and P8.1 Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P8DIR.x	P8SEL0.x	ADCPCTLx(2)
P8.0/SMCLK/A8	0	P8.0 (I/O)	I: 0; O: 1	0	0
		VSS	0	1	0
		SMCLK	1		
		A8	X	X	1 (x = 8)
P8.1/ACLK/A9	1	P8.1 (I/O)	I: 0; O: 1	0	0
		VSS	0	1	0
		ACLK	1		
		A9	X	X	1 (x = 9)

(1) X = don't care
(2) Setting the ADCPCTLx bit in SYSCFG2 register will disable both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

6.9.13.12 Port P8.2 and P8.3 Input/Output With Schmitt Trigger

Figure 6-14 shows the port schematic. Table 6-25 summarizes the selection of the pin functions.

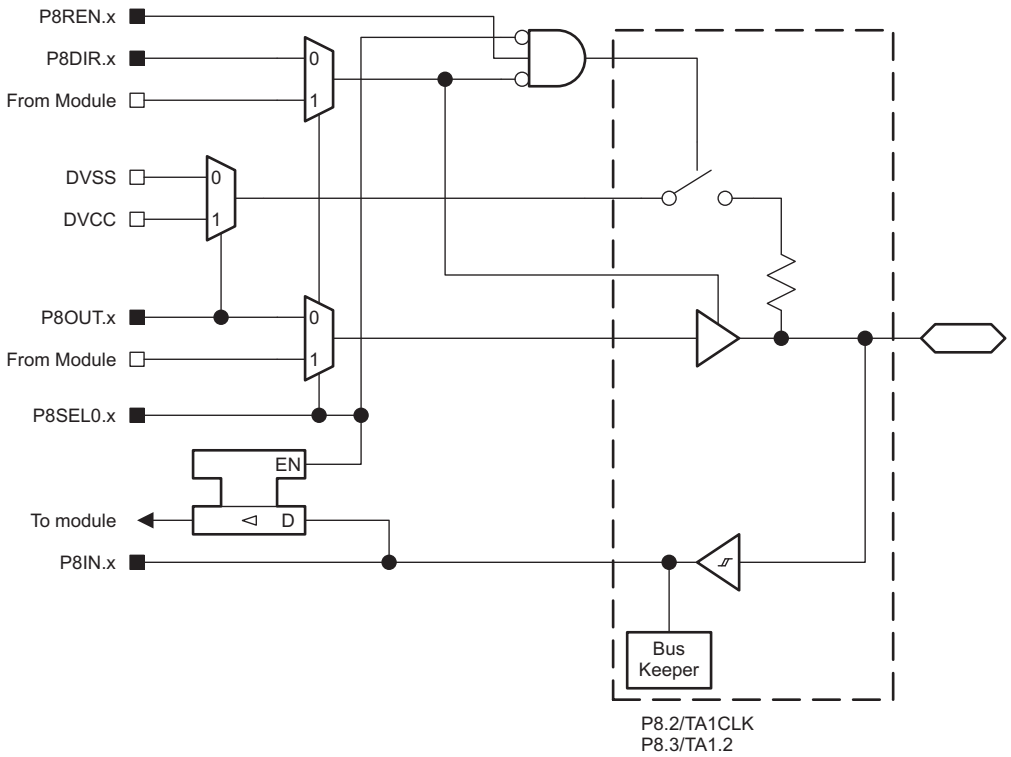


Figure 6-14. Port P8.2 and P8.3 Input/Output With Schmitt Trigger

Table 6-25. Port P8.2 and P8.3 Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS AND SIGNALS	
			P8DIR.x	P8SEL0.x
P8.2/TA1CLK	2	P8.2 (I/O)	I: 0; O: 1	0
		TA1 CLK	0	1
		VSS	1	
P8.3/TA1.2	3	P8.3 (I/O)	I: 0; O: 1	0
		TA1.CCI2A	0	1
		TA1.2	1	

6.10 Device Descriptors (TLV)

Table 6-26 lists the Device IDs of the MSP430FR413x devices. Table 6-27 lists the contents of the device descriptor tag-length-value (TLV) structure for the MSP430FR413x devices.

Table 6-26. Device IDs

DEVICE	DEVICE ID	
	1A04h	1A05h
MSP430FR4133	F0h	81h
MSP430FR4132	F1h	81h
MSP430FR4131	F2h	81h

Table 6-27. Device Descriptors

	DESCRIPTION	MSP430FR413x	
		ADDRESS	VALUE
Information Block	Info length	1A00h	06h
	CRC length	1A01h	06h
	CRC value(1)	1A02h	Per unit
		1A03h	Per unit
	Device ID	1A04h	See Table 6-26
		1A05h	
	Hardware revision	1A06h	Per unit
	Firmware revision	1A07h	Per unit
Die Record	Die Record Tag	1A08h	08h
	Die Record length	1A09h	0Ah
	Lot Wafer ID	1A0Ah	Per unit
		1A0Bh	Per unit
		1A0Ch	Per unit
		1A0Dh	Per unit
	Die X position	1A0Eh	Per unit
		1A0Fh	Per unit
	Die Y position	1A10h	Per unit
		1A11h	Per unit
	Test Result	1A12h	Per unit
		1A13h	Per unit
ADC Calibration	ADC Calibration Tag	1A14h	11h
	ADC Calibration Length	1A15h	08h
	ADC Gain Factor	1A16h	Per unit
		1A17h	Per unit
	ADC Offset	1A18h	Per unit
		1A19h	Per unit
	ADC 1.5-V Reference Temperature Sensor 30°C	1A1Ah	Per unit
		1A1Bh	Per unit
	ADC 1.5-V Reference Temperature Sensor 85°C	1A1Ch	Per unit
		1A1Dh	Per unit

(1) The CRC value covers the checksum from 1A04h to 1A77h by applying the CRC-CCITT-16 polynomial of $x^{16} + x^{12} + x^5 + 1$.

Table 6-27. Device Descriptors (continued)

	DESCRIPTION	MSP430FR413x	
		ADDRESS	VALUE
Reference and DCO Calibration	Calibration Tag	1A1Eh	12h
	Calibration Length	1A1Fh	04h
	1.5-V Reference Factor	1A20h	Per unit
		1A21h	Per unit
	DCO Tap Settings for 16 MHz, Temperature 30°C (2)	1A22h	Per unit
		1A23h	Per unit

(2) This value can be directly loaded into DCO bits in CSCTL0 register to get accurate 16-MHz frequency at room temperature, especially when MCU exits from LPM3 and below. It is also suggested to use predivider to decrease the frequency if the temperature drift might result an overshoot beyond 16 MHz.

6.11 Memory

Table 6-28 shows the memory organization of the MSP430FR413x devices.

Table 6-28. Memory Organization

	ACCESS	MSP430FR4133	MSP430FR4132	MSP430FR4131
Memory (FRAM) Main: interrupt vectors and signatures Main: code memory	Read/Write (Optional Write Protect) (1)	15KB FFFFh to FF80h FFFFh to C400h	8KB FFFFh to FF80h FFFFh to E000h	4KB FFFFh to FF80h FFFFh to F000h
RAM	Read/Write	2KB 27FFh to 2000h	1KB 23FFh to 2000h	512 bytes 21FFh to 2000h
Information Memory (FRAM)	Read/Write (Optional Write Protect) (2)	512 bytes 19FFh to 1800h	512 bytes 19FFh to 1800h	512 bytes 19FFh to 1800h
Bootloader (BSL) Memory (ROM)	Read only	1KB 13FFh to 1000h	1KB 13FFh to 1000h	1KB 13FFh to 1000h
Peripherals	Read/Write	4KB 0FFFh to 0000h	4KB 0FFFh to 0000h	4KB 0FFFh to 0000h

(1) The Program FRAM can be write protected by setting PFWP bit in SYSCFG0 register. See the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more details.
(2) The Information FRAM can be write protected by setting DFWP bit in SYSCFG0 register. See the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more details.

6.11.1 Peripheral File Map

Table 6-29 shows the base address and the memory size of the registers of each peripheral, and Table 6-30 through Table 6-49 show all of the available registers for each peripheral and their address offsets.

Table 6-29. Peripherals Summary

MODULE NAME	BASE ADDRESS	SIZE
Special Functions (see Table 6-30)	0100h	0010h
PMM (see Table 6-31)	0120h	0020h
SYS (see Table 6-32)	0140h	0030h
CS (see Table 6-33)	0180h	0020h
FRAM (see Table 6-34)	01A0h	0010h
CRC (see Table 6-35)	01C0h	0008h
WDT (see Table 6-36)	01CCh	0002h
Port P1, P2 (see Table 6-37)	0200h	0020h
Port P3, P4 (see Table 6-38)	0220h	0020h
Port P5, P6 (see Table 6-39)	0240h	0020h
Port P7, P8 (see Table 6-40)	0260h	0020h
Capacitive Touch I/O (see Table 6-41)	02E0h	0010h
Timer0_A3 (see Table 6-42)	0300h	0030h
Timer1_A3 (see Table 6-43)	0340h	0030h
RTC (see Table 6-44)	03C0h	0010h
eUSCI_A0 (see Table 6-45)	0500h	0020h
eUSCI_B0 (see Table 6-46)	0540h	0030h
LCD (see Table 6-47)	0600h	0060h
Backup Memory (see Table 6-48)	0660h	0020h
ADC (see Table 6-49)	0700h	0040h

Table 6-30. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 6-31. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM Control 0	PMMCTL0	00h
PMM Control 1	PMMCTL1	02h
PMM Control 2	PMMCTL2	04h
PMM interrupt flags	PMMIFG	0Ah
PM5 Control 0	PM5CTL0	10h

Table 6-32. SYS Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus Error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh
System configuration 0	SYSCFG0	20h
System configuration 1	SYSCFG1	22h
System configuration 2	SYSCFG2	24h

Table 6-33. CS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CS control register 0	CSCTL0	00h
CS control register 1	CSCTL1	02h
CS control register 2	CSCTL2	04h
CS control register 3	CSCTL3	06h
CS control register 4	CSCTL4	08h
CS control register 5	CSCTL5	0Ah
CS control register 6	CSCTL6	0Ch
CS control register 7	CSCTL7	0Eh
CS control register 8	CSCTL8	10h

Table 6-34. FRAM Registers (Base Address: 01A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
FRAM control 0	FRCTL0	00h
General control 0	GCCTL0	04h
General control 1	GCCTL1	06h

Table 6-35. CRC Registers (Base Address: 01C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

Table 6-36. WDT Registers (Base Address: 01CCh)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 6-37. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pulling register enable	P1REN	06h
Port P1 selection 0	P1SEL0	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pulling register enable	P2REN	07h
Port P2 selection 0 (1)	P2SEL0	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

(1) Port P2 selection register does not feature any valid bits. P2SEL0 presents for 16-bit Port A operation with P1SEL0.

Table 6-38. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pulling register enable	P3REN	06h
Port P3 selection 0 (1)	P3SEL0	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pulling register enable	P4REN	07h
Port P4 selection 0	P4SEL0	0Bh

(1) Port P3 selection register does not feature any valid bits. P3SEL0 presents for 16-bit Port B operation with P4SEL0.

Table 6-39. Port P5, P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pulling register enable	P5REN	06h
Port P5 selection 0	P5SEL0	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 pulling register enable	P6REN	07h
Port P6 selection 0 (1)	P6SEL0	0Bh

(1) Port P6 selection register does not feature any valid bits. P6SEL0 presents for 16-bit Port C operation with P5SEL0.

Table 6-40. Port P7, P8 Registers (Base Address: 0260h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 input	P7IN	00h
Port P7 output	P7OUT	02h
Port P7 direction	P7DIR	04h
Port P7 pulling register enable	P7REN	06h
Port P7 selection 0 (1)	P7SEL0	0Ah
Port P8 input	P8IN	01h
Port P8 output	P8OUT	03h
Port P8 direction	P8DIR	05h
Port P8 pulling register enable	P8REN	07h
Port P8 selection 0	P8SEL0	0Bh

(1) Port P7 selection register does not feature any valid bits. P7SEL0 presents for 16-bit Port D operation with P8SEL0.

Table 6-41. Capacitive Touch IO Registers (Base Address: 02E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capacitive Touch IO 0 control	CAPTIO0CTL	0Eh

Table 6-42. Timer0_A3 Registers (Base Address: 0300h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
TA0 counter register	TA0R	10h
Capture/compare register 0	TA0CCR0	12h
Capture/compare register 1	TA0CCR1	14h
Capture/compare register 2	TA0CCR2	16h
TA0 expansion register 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 6-43. Timer1_A3 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter register	TA1R	10h
Capture/compare register 0	TA1CCR0	12h
Capture/compare register 1	TA1CCR1	14h
Capture/compare register 2	TA1CCR2	16h
TA1 expansion register 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 6-44. RTC Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control	RTCCTL	00h
RTC interrupt vector	RTCIV	04h
RTC modulo	RTCMOD	08h
RTC counter	RTCCNT	0Ch

Table 6-45. eUSCI_A0 Registers (Base Address: 0500h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA0CTLW0	00h
eUSCI_A control word 1	UCA0CTLW1	02h
eUSCI_A control rate 0	UCA0BR0	06h
eUSCI_A control rate 1	UCA0BR1	07h
eUSCI_A modulation control	UCA0MCTLW	08h
eUSCI_A status	UCA0STAT	0Ah
eUSCI_A receive buffer	UCA0RXBUF	0Ch
eUSCI_A transmit buffer	UCA0TXBUF	0Eh
eUSCI_A LIN control	UCA0ABCTL	10h
eUSCI_A IrDA transmit control	lUCA0IRTCTL	12h
eUSCI_A IrDA receive control	lUCA0IRRCTL	13h
eUSCI_A interrupt enable	UCA0IE	1Ah
eUSCI_A interrupt flags	UCA0IFG	1Ch
eUSCI_A interrupt vector word	UCA0IV	1Eh

Table 6-46. eUSCI_B0 Registers (Base Address: 0540h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B control word 0	UCB0CTLW0	00h
eUSCI_B control word 1	UCB0CTLW1	02h
eUSCI_B bit rate 0	UCB0BR0	06h
eUSCI_B bit rate 1	UCB0BR1	07h
eUSCI_B status word	UCB0STATW	08h
eUSCI_B byte counter threshold	UCB0TBCNT	0Ah
eUSCI_B receive buffer	UCB0RXBUF	0Ch
eUSCI_B transmit buffer	UCB0TXBUF	0Eh
eUSCI_B I2C own address 0	UCB0I2COA0	14h
eUSCI_B I2C own address 1	UCB0I2COA1	16h
eUSCI_B I2C own address 2	UCB0I2COA2	18h
eUSCI_B I2C own address 3	UCB0I2COA3	1Ah
eUSCI_B receive address	UCB0ADDRX	1Ch
eUSCI_B address mask	UCB0ADDMASK	1Eh
eUSCI_B I2C slave address	UCB0I2CSA	20h
eUSCI_B interrupt enable	UCB0IE	2Ah
eUSCI_B interrupt flags	UCB0IFG	2Ch
eUSCI_B interrupt vector word	UCB0IV	2Eh

Table 6-47. LCD Registers (Base Address: 0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
LCD control register 0	LCDCTL0	00h
LCD control register 1	LCDCTL1	02h
LCD blink control register	LCDBLKCTL	04h
LCD memory control register	LCDMEMCTL	06h
LCD voltage control register	LCDVCTL	08h
LCD port control 0	LCDPCTL0	0Ah
LCD port control 1	LCDPCTL1	0Ch
LCD port control 2	LCDPCTL2	0Eh
LCD COM/SEG select register	LCDCSS0	14h
LCD COM/SEG select register	LCDCSS1	16h
LCD COM/SEG select register	LCDCSS2	18h
LCD interrupt vector	LCDIV	1Eh
Display memory Static and 2 to 4 mux modes		
LCD memory 0	LCDM0	20h
LCD memory 1	LCDM1	21h
LCD memory 2	LCDM2	22h
⋮	⋮	⋮
LCD memory 19	LCDM19	33h
Reserved(1)		34h
⋮	⋮	⋮
Reserved(1)		3Fh

(1) In static and 2-mux to 4-mux modes, LCD memory and blink memory 40 to 63 are not physically implemented.

Table 6-47. LCD Registers (Base Address: 0600h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Blinking memory for Static and 2 to 4 mux modes		
LCD blinking memory 0	LCDBM0	40h
LCD blinking memory 1	LCDBM1	41h
⋮	⋮	⋮
LCD blinking memory 19	LCDBM19	53h
Reserved(1)		54h
⋮	⋮	⋮
Reserved(1)		5Fh
Display memory for 5 to 8 mux modes		
LCD memory 0	LCDM0	20h
LCD memory 1	LCDM1	21h
LCD memory 2	LCDM2	22h
⋮	⋮	⋮
LCD memory 39	LCDM39	47h
Reserved(2)		48h
⋮	⋮	⋮
Reserved(2)		5Fh

(2) In 5-mux to 8-mux modes, LCD memory and blink memory 40 to 63 are not physically implemented.

Table 6-48. Backup Memory Registers (Base Address: 0660h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Backup Memory 0	BAKMEM0	00h
Backup Memory 1	BAKMEM1	02h
Backup Memory 2	BAKMEM2	04h
Backup Memory 3	BAKMEM3	06h
Backup Memory 4	BAKMEM4	08h
Backup Memory 5	BAKMEM5	0Ah
Backup Memory 6	BAKMEM6	0Ch
Backup Memory 7	BAKMEM7	0Eh
Backup Memory 8	BAKMEM8	10h
Backup Memory 9	BAKMEM9	12h
Backup Memory 10	BAKMEM10	14h
Backup Memory 11	BAKMEM11	16h
Backup Memory 12	BAKMEM12	18h
Backup Memory 13	BAKMEM13	1Ah
Backup Memory 14	BAKMEM14	1Ch
Backup Memory 15	BAKMEM15	1Eh

Table 6-49. ADC Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC control register 0	ADCCTL0	00h
ADC control register 1	ADCCTL1	02h
ADC control register 2	ADCCTL2	04h
ADC window comparator low threshold	ADCLO	06h
ADC window comparator high threshold	ADCHI	08h
ADC memory control register 0	ADCMCTL0	0Ah
ADC conversion memory register	ADCMEM0	12h
ADC interrupt enable	ADCIE	1Ah
ADC interrupt flags	ADCIFG	1Ch
ADC interrupt vector word	ADCIV	1Eh

6.12 Identification

6.12.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see 节 8.4.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in Section 6.10.

6.12.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see 节 8.4.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in Section 6.10.

6.12.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in *MSP430 Programming With the JTAG Interface*.

7 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430FR413x devices. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 10-µF plus a 100-nF low-ESR ceramic decoupling capacitor to the DVCC and DVSS pins (see Figure 7-1). Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters).

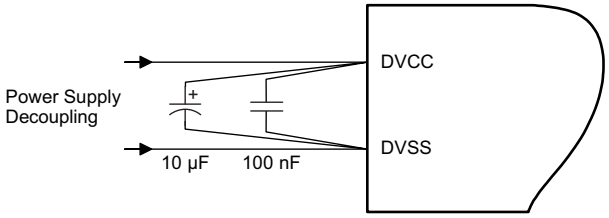


Figure 7-1. Power Supply Decoupling

7.1.2 External Oscillator

This device supports only a low-frequency crystal (32 kHz) on the XIN and XOUT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the XIN input pin that meet the specifications of the respective oscillator if the appropriate XT1BYPASS mode is selected. In this case, the associated XOUT pin can be used for other purposes. If they are left unused, they must be terminated according to Section 4.4.

Figure 7-2 shows a typical connection diagram.

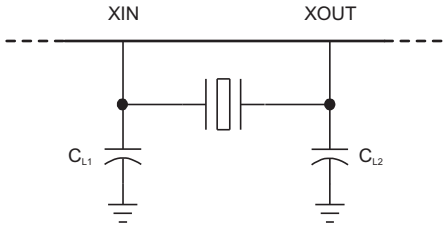


Figure 7-2. Typical Crystal Connection

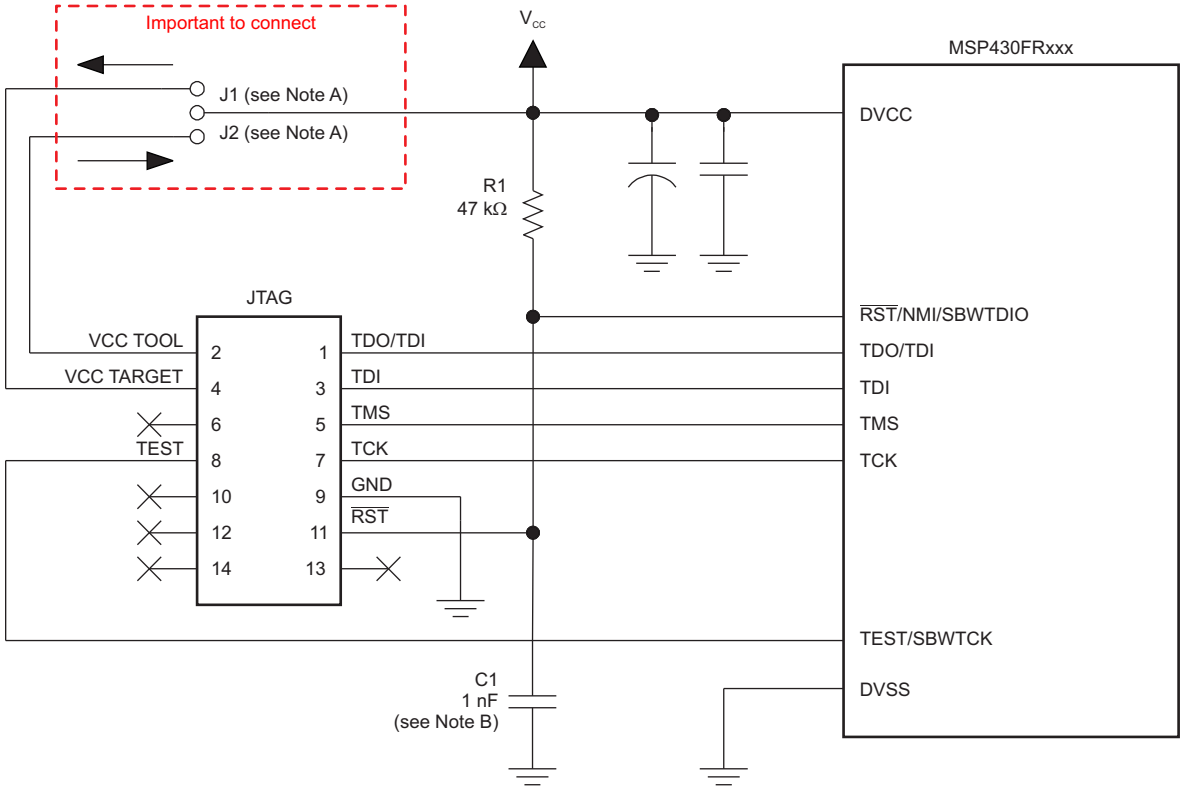
See *MSP430 32-kHz Crystal Oscillators* for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. Figure 7-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. Figure 7-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply V_{CC} to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a V_{CC}-sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The V_{CC}-sense feature senses the local VCC present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. Figure 7-3 and Figure 7-4 show a jumper block that supports both scenarios of supplying V_{CC} to the target board. If this flexibility is not required, the desired V_{CC} connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

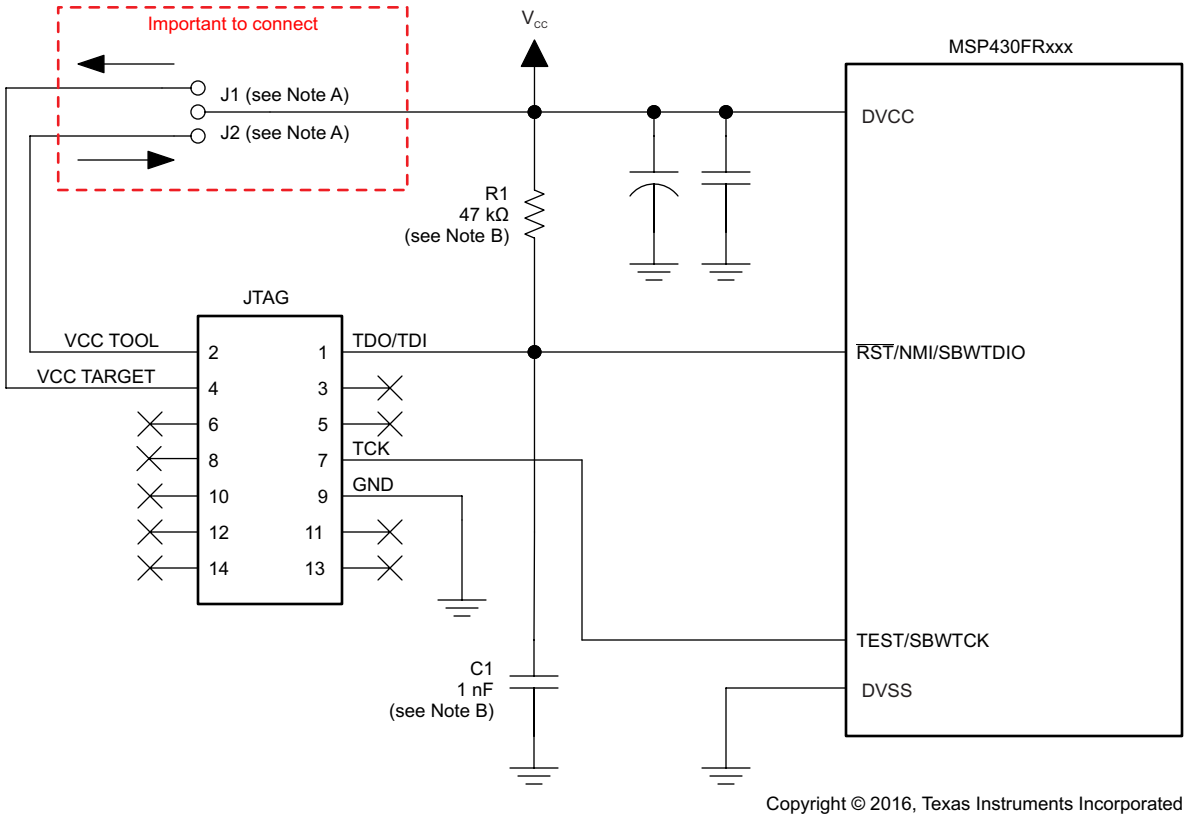
For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide*.



A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.

B. The upper limit for C1 is 1.1 nF when using current TI tools.

Figure 7-3. Signal Connections for 4-Wire JTAG Communication



A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.

B. The device $\overline{\text{RST}}$/NMI/SBWTDIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 1.1 nF when using current TI tools.

Figure 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the $\overline{\text{RST}}$/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST}}$/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST}}$/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST}}$/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the $\overline{\text{RST}}$/NMI pin with a 1.1-nF pulldown capacitor. The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more information on the referenced control registers and bits.

7.1.5 Unused Pins

For details on the connection of unused pins, see Section 4.4.

7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See *MSP430 32-kHz Crystal Oscillators* for recommended layout guidelines.
- Proper bypass capacitors on DVCC and reference pins, if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See *MSP430 System-Level ESD Considerations* for guidelines.

7.1.7 Do's and Don'ts

During power up, power down, and device operation, DVCC must not exceed the limits specified in *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

7.2 Peripheral- and Interface-Specific Design Information

7.2.1 ADC Peripheral

7.2.1.1 Partial Schematic

Figure 7-5 shows the recommended circuit for ADC grounding and noise reduction.

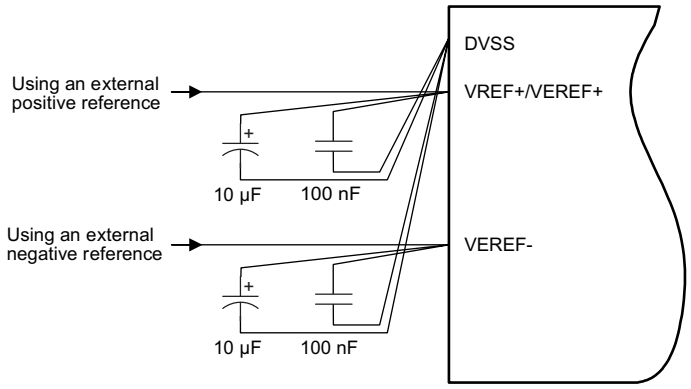


Figure 7-5. ADC Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in Section 7.1.1 combined with the connections shown in Section 7.2.1.1 prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

Figure 7-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as described in the sections *ADC Pin Enable* and *1.2-V Reference Settings* of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-μF capacitor is used to buffer the reference pin and filter any low-frequency ripple. A bypass capacitor of 100 nF is used to filter out any high-frequency noise.

7.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see Figure 7-5) should be placed as close as possible to the respective device pins to avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

7.2.2 LCD_E Peripheral

7.2.2.1 Partial Schematic

Required LCD connections greatly vary by the type of display that is used (static or multiplexed), whether external or internal biasing is used, and also whether the on-chip charge pump is employed. For any display used, LCD_E has configurable segment (Sx) or common (COMx) signals connected to the MCU which allows optimal PCB layout and for the design of the application software.

Because LCD connections are application specific, it is difficult to provide a single one-fits-all schematic. However, for an example of connecting a 4-mux LCD with 27 segment lines that has a total of 4 × 27 = 108 individually addressable LCD segments to an MSP430FR4133, see the MSP-EXP430FR4133 LaunchPad™ development kit as a reference.

7.2.2.2 Design Requirements

Due to the flexibility of the LCD_E peripheral module to accommodate various segment-based LCDs, selecting the right display for the application in combination with determining specific design requirements is often an iterative process. There can be well-defined requirements in terms of how many individually addressable LCD segments must be controlled, what the requirements for LCD contrast are, which device pins are available for LCD use and which are required by other application functions, and what the power budget is, to name just a few. TI strongly recommends reviewing the LCD_E peripheral module chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* during the initial design requirements and decision process. Table 7-1 provides a brief overview over different choices that can be made and their impact.

Table 7-1. LCD_E Design Options

OPTION OR FEATURE	IMPACT OR USE CASE
Multiplexed LCD	• Enable displays with more segments • Use fewer device pins • LCD contrast decreases as mux level increases • Power consumption increases with mux level • Requires multiple intermediate bias voltages
Static LCD	• Limited number of segments that can be addressed • Use a relatively large number of device pins • Use the least amount of power • Use only V_{CC} and GND to drive LCD signals
Internal Bias Generation	• Simpler solution – no external circuitry • Independent of V_{LCD} source • Somewhat higher power consumption
External Bias Generation	• Requires external resistor ladder divider • Resistor size depends on display • Ability to adjust drive strength to optimize tradeoff between power consumption and good drive of large segments (high capacitive load) • External resistor ladder divider can be stabilized through capacitors to reduce ripple
Internal Charge Pump	• Helps ensure a constant level of contrast despite decaying supply voltage conditions (battery-powered applications) • Programmable voltage levels allow software-driven contrast control • Requires an external capacitor on the LCDCAP pins • Higher current consumption than simply using V_{CC} for the LCD driver

7.2.2.3 Detailed Design Procedure

A major component in designing the LCD solution is determining the exact connections between the LCD_E peripheral module and the display itself. Two basic design processes can be employed for this step, although often a balanced co-design approach is recommended:

- PCB layout-driven design
- Software-driven design

In the PCB layout-driven design process, LCD_E offers configurable segment Sx and common COMx signals which are connected to the respective MSP430 device pins so that the routing of the PCB can be optimized to minimize signal crossings and to keep signals on one side of the PCB only, typically the top layer. For example, using a multiplexed LCD, it is possible to arbitrarily connect the Sx and COMx signals between the LCD and the MSP430 device as long as segment lines are swapped with segment lines and common lines are swapped with common lines. It is also possible to not contiguously connect all segment lines but rather skip LCD_E module segment connections to optimize layout or to allow access to other functions that may be multiplexed on a particular device port pin. Employing a purely layout-driven design approach, however, can result in the LCD_E module control bits that are responsible for turning on and off segments to appear scattered throughout the memory map of the LCD controller (LCDMx registers). This approach potentially places a rather large burden on the software design that may also result in increased energy consumption due to the computational overhead required to work with the LCD.

The other extreme is a purely software-driven approach that starts with the idea that control bits for LCD segments that are frequently turned on and off together should be co-located in memory in the same LCDMx register or in adjacent registers. For example, in case of a 4-mux display that contains several 7-segment digits, from a software perspective it can be very desirable to control all 7 segments of each digit though a single byte-wide access to an LCDMx register. And consecutive segments are mapped to

consecutive LCDMx registers. This allows use of simple look-up tables or software loops to output numbers on an LCD, reducing computational overhead and optimizing the energy consumption of an application. Establishing of the most convenient memory layout needs to be performed in conjunction with the specific LCD that is being used to understand its design constraints in terms of which segment and which common signals are connected to, for example, a digit.

For design information regarding the LCD controller input voltage selection including internal and external options, contrast control, and bias generation, see the LCD_E controller chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

7.2.2.4 Layout Guidelines

LCD segment (Sx) and common (COMx) signal traces are continuously switching while the LCD is enabled and should, therefore, be kept away from sensitive analog signals such as ADC inputs to prevent any noise coupling. TI recommends keeping the LCD signal traces on one side of the PCB grouped together in a bus-like fashion. A ground plane underneath the LCD traces and guard traces employed alongside the LCD traces can provide shielding.

If the internal charge pump of the LCD module is used, the externally provided capacitor on the LCDCAP0 and LCDCAP1 pins should be located as close as possible to the MCU. The capacitor should be connected to the device using a short and direct trace.

For an example layout of connecting a 4-mux LCD with 27 segments to an MSP430FR4133 and using the charge pump feature, see the MSP-EXP430FR4133 LaunchPad development kit.

7.3 Typical Applications

Table 7-2 lists several TI Designs that reflect the use of the MSP430FR413x family of devices in different real-world application scenarios. Consult these designs for additional guidance regarding schematic, layout, and software implementation. For the most up-to-date list of available TI Designs, see the device-specific product folders listed in 节 8.5.

Table 7-2. TI Designs

DESIGN NAME	LINK
Thermostat Implementation With MSP430FR4xx	TIDM-FRAM-THERMOSTAT
Water Meter Implementation With MSP430FR4xx	TIDM-FRAM-WATERMETER
Remote Controller of Air Conditioner Using Low-Power Microcontroller	TIDM-REMOTE-CONTROLLER-FOR-AC

的组织形式

8 器件和文档支持

8.1 入门和后续步骤

关于 MSP430 系列器件以及开发协助工具和库的简介，请访问入门页面。

8.2 器件命名规则

为了标示产品开发周期所处的阶段，TI 为所有 MSP MCU 器件的部件号分配了前缀。每个 MSP MCU 商用系列产品成员都具有以下两个前缀之一：MSP 或 XMS。这些前缀代表了产品开发的发展阶段，即从工程原型 (XMS) 直到完全合格的生产器件 (MSP)。

XMS - 实验器件，不一定代表最终器件的电气规格

MSP - 完全合格的生产器件

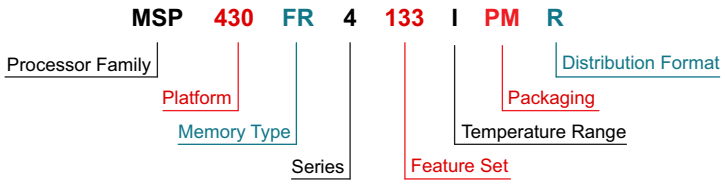
XMS 器件在供货时附带如下免责声明：

“开发中的产品用于内部评估用途。”

MSP 器件的特性已经全部明确，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书对该器件适用。

预测显示原型器件 (XMS) 的故障率大于标准生产器件。由于这些器件的预计最终使用故障率尚不确定，德州仪器 (TI) 建议不要将它们用于任何生产系统。请仅使用合格的生产器件。

TI 器件的命名规则还包括一个带有器件系列名称的后缀。此后缀表示温度范围、封装类型和配送形式。图 8-1 提供了解读完整器件名称的图例。



Processor Family	MSP = Mixed-Signal Processor XMS = Experimental Silicon	
Platform	430 = TI's 16-Bit MSP430 Low-Power Microcontroller Platform	
Memory Type	FR = FRAM	
Series	4 = FRAM 4 series up to 16 MHz with LCD	
Feature Set	**First and Second Digits: ADC Channels / 16-bit Timers / I/Os** 13 = Up to 10 / 3 / Up to 60	**Third Digit: FRAM (KB) / SRAM (KB)** 3 = 16 / 2 2 = 8 / 1 1 = 4 / 0.5
Temperature Range	I = –40°C to 85°C	
Packaging	http://www.ti.com/packaging	
Distribution Format	T = Small reel R = Large reel No marking = Tube or tray	

图 **8-1.** 器件命名规则

8.3 工具和软件

表 8-1 列出 了 MSP430FR413x 微控制器支持的调试特性。关于可用特性的详细信息，请参见《适用于 MSP430 的 Code Composer Studio 用户指南》的详细信息。

表 8-1. 硬件 特性

MSP430 架构	四线制 JTAG	两线制 JTAG	断点 (N)	范围断点	时钟控制	状态序列发生器	跟踪缓冲器	LPMX.5 调试支持
MSP430Xv2	有	有	3	有	是	否	否	否

设计套件与评估模块

MSP430FR4133 LaunchPad 开发套件 MSP-EXP430FR4133 LaunchPad 开发套件是适用于 MSP430FR4133 微控制器的简单易用的评估模块 (EVM)。它包含在基于 FRAM 的 MSP430 超低功耗 (ULP) 微控制器 (MCU) 平台上进行开发所需的全部资源，包括用于编程、调试和能量测量的板载仿真。

适用于 MSP430FR2x/4x MCU 的 MSP-TS430PM64D 目标开发板 MSP-TS430PM64D 是一款独立的 64 引脚 ZIF 插座目标板，用于通过 JTAG 接口或 Spy Bi-Wire（2 线 JTAG）协议对 MSP430 MCU 系统内置器件进行编程和调试。

适用于 MSP430FR2x/4x MCU 的 MSP-FET430U64D 目标开发板（64 引脚）和 MSP-FET 编程器捆绑包 MSP-FET430U64D 是一款捆绑套件，包含 MSP-FET 仿真器和 MSP-TS430PM64D 64 引脚 ZIF 插座目标板，用于通过 JTAG 接口或 Spy Bi-Wire（2 线式 JTAG）协议对 MSP430 MCU 系统内置器件进行编程和调试。

软件

MSP430Ware™ 软件 MSP430Ware 软件集合了所有 MSP430 器件的代码示例、数据表以及其他设计资源，打包提供给用户。除了提供已有 MSP430 MCU 设计资源的完整集合外，MSP430Ware 软件还包含名为 MSP 驱动程序库的高级 API。借助该库可以轻松地对 MSP430 硬件进行编程。MSP430Ware 软件以 CCS 组件或独立软件包两种形式提供。

MSP430FR413x、MSP430FR203x 代码示例 根据不同应用需求配置各集成外设的每个 MSP 器件均具备相应的 C 代码示例。

适用于 MSP 超低功耗微控制器的 FRAM 嵌入式软件实用程序 TI FRAM 实用程序软件旨在用作不断扩充的嵌入式软件实用程序集合，其中的实用程序充分利用了 FRAM 的超低功耗和近乎无限次的写入寿命。这些实用程序适用于 MSP430FRxx FRAM 微控制器并提供示例代码，以帮助开始进行应用程序开发。

MSP430 Touch Pro GUI MSP430 Touch Pro 工具是一款基于 PC 的工具，可用于验证电容式触控按钮、滑块和滚轮设计。此工具可接收并显示 CapTouch 传感器数据，帮助用户快速轻松地评估、诊断和调整按钮、滑块和滚轮设计。

MSP430 触控电源设计器 GUI 使用 MSP430 电容式触控电源设计器，可以计算给定的 MSP430 电容式触控系统的估计平均电流消耗。通过输入系统参数（如工作电压、频率、按钮数量和按钮选通时间），用户可以在数分钟内估计给定的器件系列的指定电容式触控配置的功耗。

适用于 MSP 微控制器的数字信号处理 (DSP) 库 该数字信号处理库是一组经高度优化的函数，可针对 MSP430 和 MSP432 微控制器对定点数字执行许多常见的信号处理操作。该功能集通常 用于要求完成实时密集处理转换，从而以最低能耗实现高精度的应用。针对定点数学对 MSP 固有硬件的最佳利用可以极大地提高性能。

MSP 驱动程序库 MSP 驱动程序库的抽象 API 提供易用的函数调用，无需直接操纵 MSP430 硬件的位与字节。完整的文档通过具有帮助意义的 API 指南交付，其中包括有关每个函数调用和经过验证的参数的详细信息。开发人员可使用驱动程序库函数以尽可能低的费用编写全部项目。

MSP EnergyTrace 技术 适用于 MSP430 微控制器的 EnergyTrace 技术是基于电能的代码分析工具，适用于测量和显示应用的电能系统配置并帮助优化应用以实现超低功耗。

ULP（超低功耗）Advisor ULP Advisor™软件是一款辅助工具，旨在指导开发人员编写更为高效的代码，从而充分利用 MSP430 和 MSP432 微控制器 独特 功能。ULP Advisor 的目标人群是微控制器的资深开发者和开发新手，可以根据详尽的 ULP 检验表检查代码，以便最大限度地减少应用程序的能耗。在编译时，ULP Advisor 会提供通知和备注以突出显示代码中可以进一步优化的区域，进而实现更低功耗。

适用于 MSP 的定点数学库 MSP IQmath 和 Qmath 库是为 C 语言开发者提供的一套经过高度优化的高精度数学运算函数集合，能够将浮点算法无缝嵌入 MSP430 和 MSP432 器件的定点代码中。这些例程通常用于计算密集型实时 应用， 而优化的执行速度、高精度以及超低能耗通常是影响这些实时应用的关键因素。与使用浮点数学算法编写的同等代码相比，使用 IQmath 和 Qmath 库可以大幅提高执行速度并显著降低能耗。

适用于 MSP430 的浮点数学运算库 TI 在低功耗和低成本微控制器领域锐意创新，为您提供 MSPMATHLIB。该标量函数的浮点数学运算库能够利用我们的器件的智能外设，其速度最高可为标准 MSP430 数学函数的 26 倍。Mathlib 能够轻松集成到您的设计中。该运算库免费使用并集成在 Code Composer Studio IDE 和 IAR Embedded Workbench IDE 中。

开发工具

适用于 MSP 微控制器的 Code Composer Studio™ 集成开发环境 Code Composer Studio (CCS) 集成开发环境 (IDE) 支持所有 MSP 微控制器器件。CCS 包含一整套用于开发和调试嵌入式 应用的嵌入式软件实用程序。CCS 包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他众多 功能。

命令行编程器 MSP Flasher 是一款基于 shell 的开源接口，可使用 JTAG 或 Spy-Bi-Wire (SBW) 通信通过 FET 编程器或 eZ430 对 MSP 微控制器进行编程。MSP Flasher 可用于将二进制文件（.txt 或 .hex 文件）直接下载到 MSP 微控制器，而无需使用 IDE。

MSP MCU 编程器和调试器 MSP-FET 是一款强大的仿真开发工具（通常称为调试探针），可帮助用户在 MSP 低功耗微控制器 (MCU) 中快速开发应用。创建 MCU 软件通常需要将生成的二进制程序下载到 MSP 器件中，从而进行验证和调试。

MSP-GANG 生产编程器 MSP Gang 编程器是一款 MSP430 或 MSP432 器件编程器，可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。

8.4 文档支持

以下文档介绍了 MSP430FR413x 微控制器。www.ti.com.cn 网站上提供了这些文档的副本。

接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 ti.com.cn 上您的器件对应的产品文件夹（关于产品文件夹的链接，请参见节 8.5）。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

勘误

《MSP430FR4133 器件勘误表》 介绍了这款器件所有芯片修订版本的功能技术规格的已知例外情况。

《MSP430FR4132 器件勘误表》 介绍了这款器件所有芯片修订版本的功能技术规格的已知例外情况。

《MSP430FR4131 器件勘误表》 介绍了这款器件所有芯片修订版本的功能技术规格的已知例外情况。

用户指南

《MSP430FR4xx 和 MSP430FR2xx 系列用户指南》 详细地 说明 。

《MSP430 FRAM 器件引导加载程序 (BSL) 用户指南》 MSP430 MCU 上的引导加载程序 (BSL) 允许用户在原型设计、投产和维护等各阶段与 MSP430 MCU 中的嵌入式存储器进行通信。可编程存储器（FRAM 存储器）和数据存储器 (RAM) 均可按要求予以修改。

《通过 JTAG 接口对 MSP430 进行编程》 此文档介绍了使用 JTAG 通信端口擦除、编程和验证基于 MSP430 闪存和 FRAM 的微控制器系列的存储器模块所需的功能。此外，该文档还介绍了如何编程所有 MSP430 器件上均具备的 JTAG 访问安全保险丝。此文档介绍了使用标准四线制 JTAG 接口和两线制 JTAG 接口（也称为 Spy-Bi-Wire (SBW)）的器件访问。

《MSP430 硬件工具用户指南》 此手册介绍了 TI MSP-FET430 闪存仿真工具 (FET) 的硬件。FET 是针对 MSP430 超低功耗微控制器的程序开发工具。文中对提供的接口类型，即并行端口接口和 USB 接口进行了说明。

应用报告

MSP430 FRAM 技术 – 操作方法和最佳实践 FRAM 采用非易失性存储器技术，行为与 SRAM 类似，支持大量新 应用的同时，还改变了固件的设计方式。该应用程序报告从嵌入式软件开发方面概述了 FRAM 技术在 MSP430 中的使用方法和最佳实践。其中介绍了如何按照应用程序特定的代码、常量、数据空间要求实施存储器布局以及如何使用 FRAM 优化应用程序的能耗。

《MSP430 32kHz 晶体振荡器》 选择合适的晶体、正确的负载电路和适当的电路板布局是实现稳定的晶体振荡器的关键。该应用报告总结了晶体振荡器的功能，介绍了用于选择合适的晶体以实现 MSP430 超低功耗运行的参数。此外，还给出了正确电路板布局的提示和示例。此外，为了确保振荡器在大规模生产后能够稳定运行，还可能需要进行一些振荡器测试，该文档中提供了有关这些测试的详细信息。

《MSP430 系统级 ESD 注意事项》 随着硅晶技术向更低电压方向发展以及设计具有成本效益的超低功耗组件的需求的出现，系统级 ESD 要求变得越来越苛刻。该应用报告介绍了三个不同的 ESD 主题，旨在帮助电路板设计人员和 OEM 理解并设计出稳健耐用的系统级设计。

8.5 相关链接

表 8-2 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具与软件，以及申请样片或购买产品的快速链接。

表 **8-2.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
MSP430FR4133	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR4132	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR4131	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

8.6 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参见 TI 的 《使用条款》 。

TI E2E™ 社区
TI 的工程师交流 (E2E) 社区. 此社区的创建目的是为了促进工程师之间协作。在 e2e.ti.com 中，您可以提问、共享知识、拓展思路，在同领域工程师的帮助下解决问题。

TI 嵌入式处理器维基网页
德州仪器 (TI) 嵌入式处理器维基网页。此网站的建立是为了帮助开发人员熟悉德州仪器 (TI) 的嵌入式处理器，并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

8.7 商标

LaunchPad, MSP430Ware, MSP430, Code Composer Studio, E2E, ULP Advisor, 适用于 MSP 微控制器的 Code Composer Studio are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

8.8 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

9.1 封装信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430FR4131IG48	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4131	Samples
MSP430FR4131IG48R	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4131	Samples
MSP430FR4131IG56	ACTIVE	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4131	Samples
MSP430FR4131IG56R	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4131	Samples
MSP430FR4131IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4131	Samples
MSP430FR4132IG48	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4132	Samples
MSP430FR4132IG48R	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4132	Samples
MSP430FR4132IG56	ACTIVE	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4132	Samples
MSP430FR4132IG56R	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4132	Samples
MSP430FR4132IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4132	Samples
MSP430FR4133IG48	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4133	Samples
MSP430FR4133IG48R	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4133	Samples
MSP430FR4133IG56	ACTIVE	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4133	Samples
MSP430FR4133IG56R	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4133	Samples
MSP430FR4133IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4133	Samples
MSP430FR4133IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR4133	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

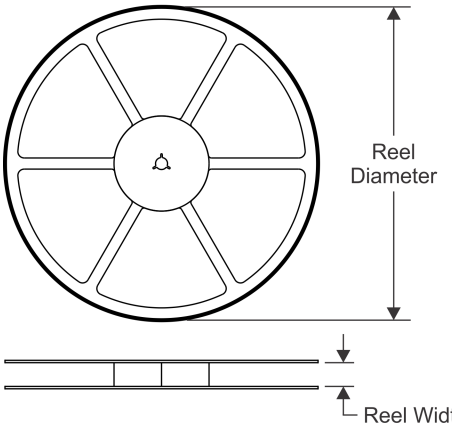
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

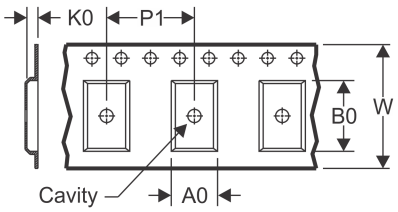
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

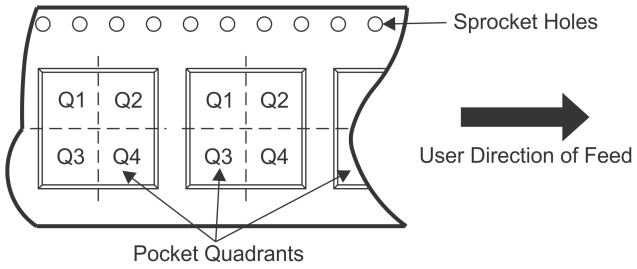


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

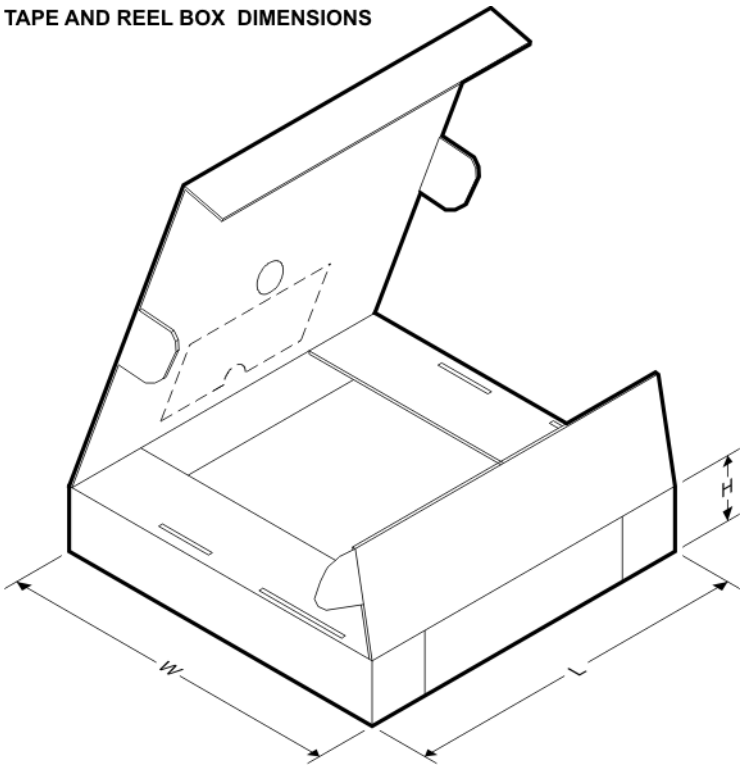
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FR4131IG48R	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430FR4131IG56R	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
MSP430FR4131IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR4132IG48R	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430FR4132IG56R	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
MSP430FR4132IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR4133IG48R	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430FR4133IG56R	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
MSP430FR4133IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

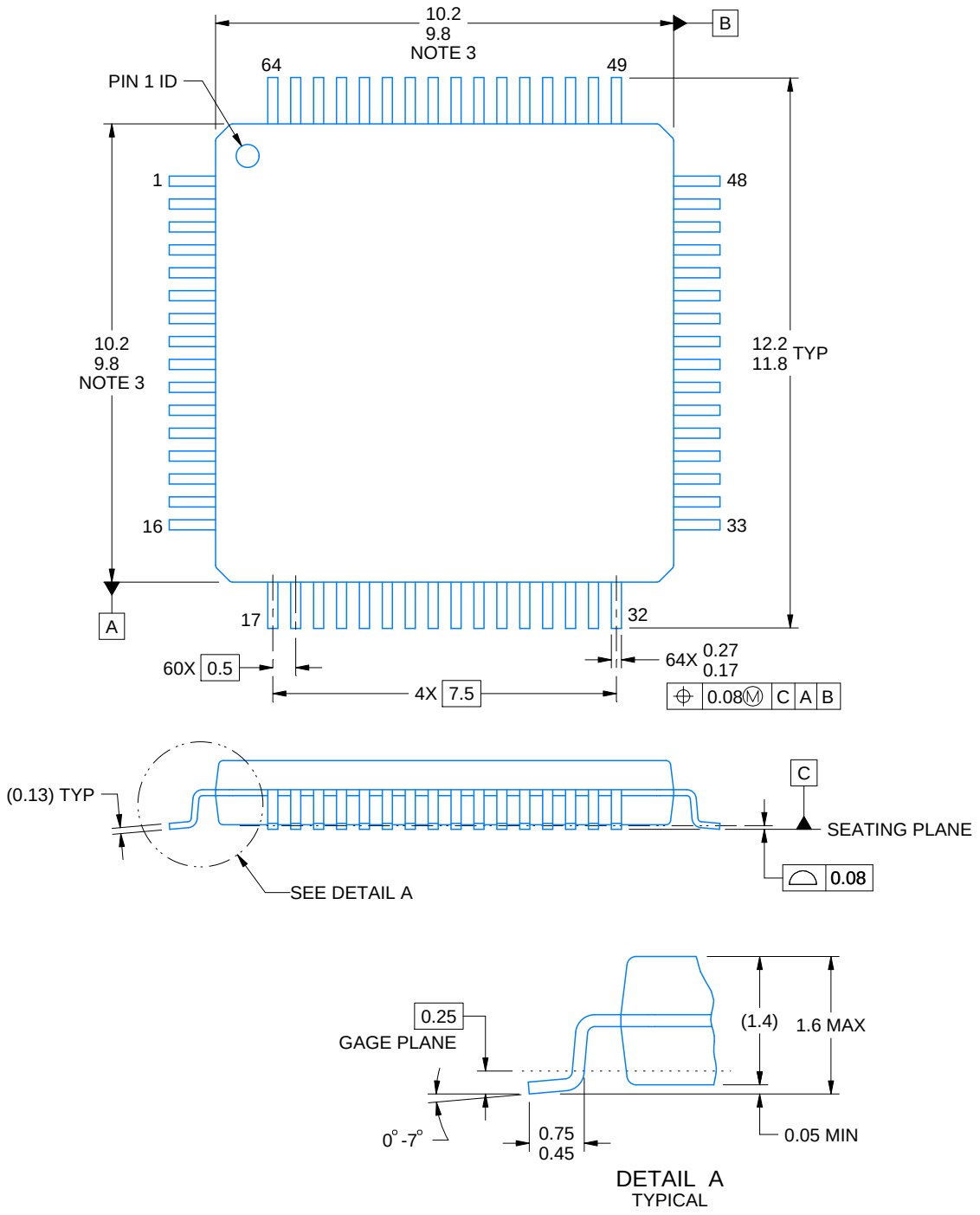
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FR4131IG48R	TSSOP	DGG	48	2000	350.0	350.0	43.0
MSP430FR4131IG56R	TSSOP	DGG	56	2000	350.0	350.0	43.0
MSP430FR4131IPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430FR4132IG48R	TSSOP	DGG	48	2000	350.0	350.0	43.0
MSP430FR4132IG56R	TSSOP	DGG	56	2000	350.0	350.0	43.0
MSP430FR4132IPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430FR4133IG48R	TSSOP	DGG	48	2000	350.0	350.0	43.0
MSP430FR4133IG56R	TSSOP	DGG	56	2000	350.0	350.0	43.0
MSP430FR4133IPMR	LQFP	PM	64	1000	350.0	350.0	43.0

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

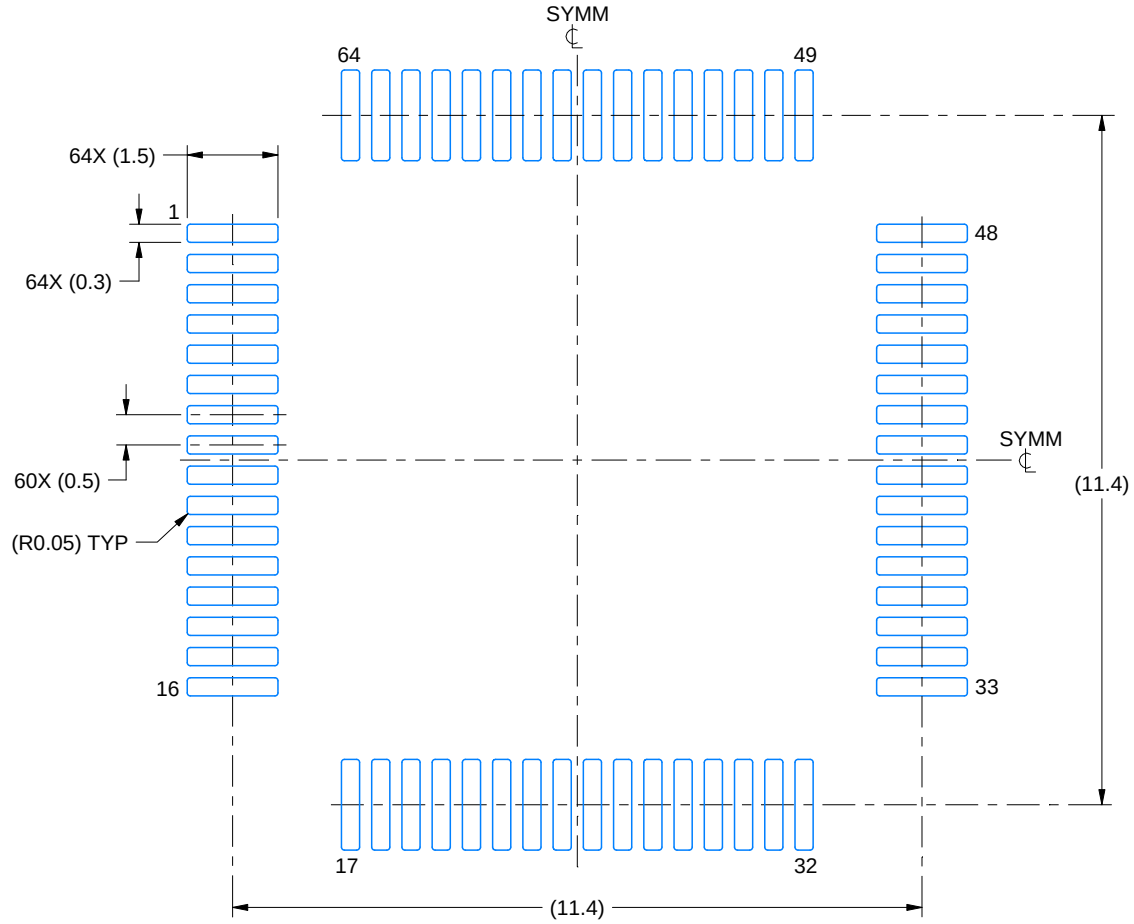
PLASTIC QUAD FLATPACK



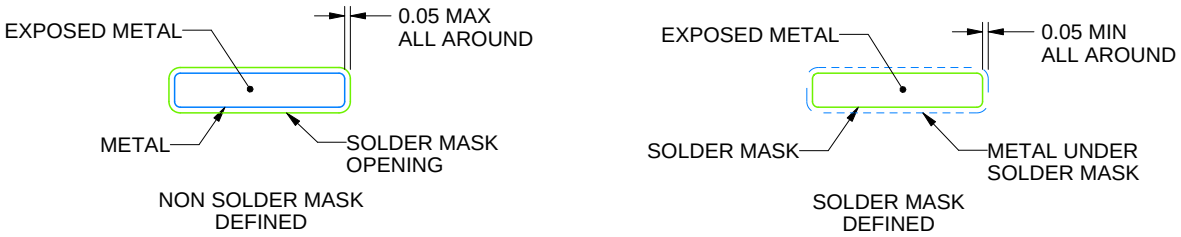
4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

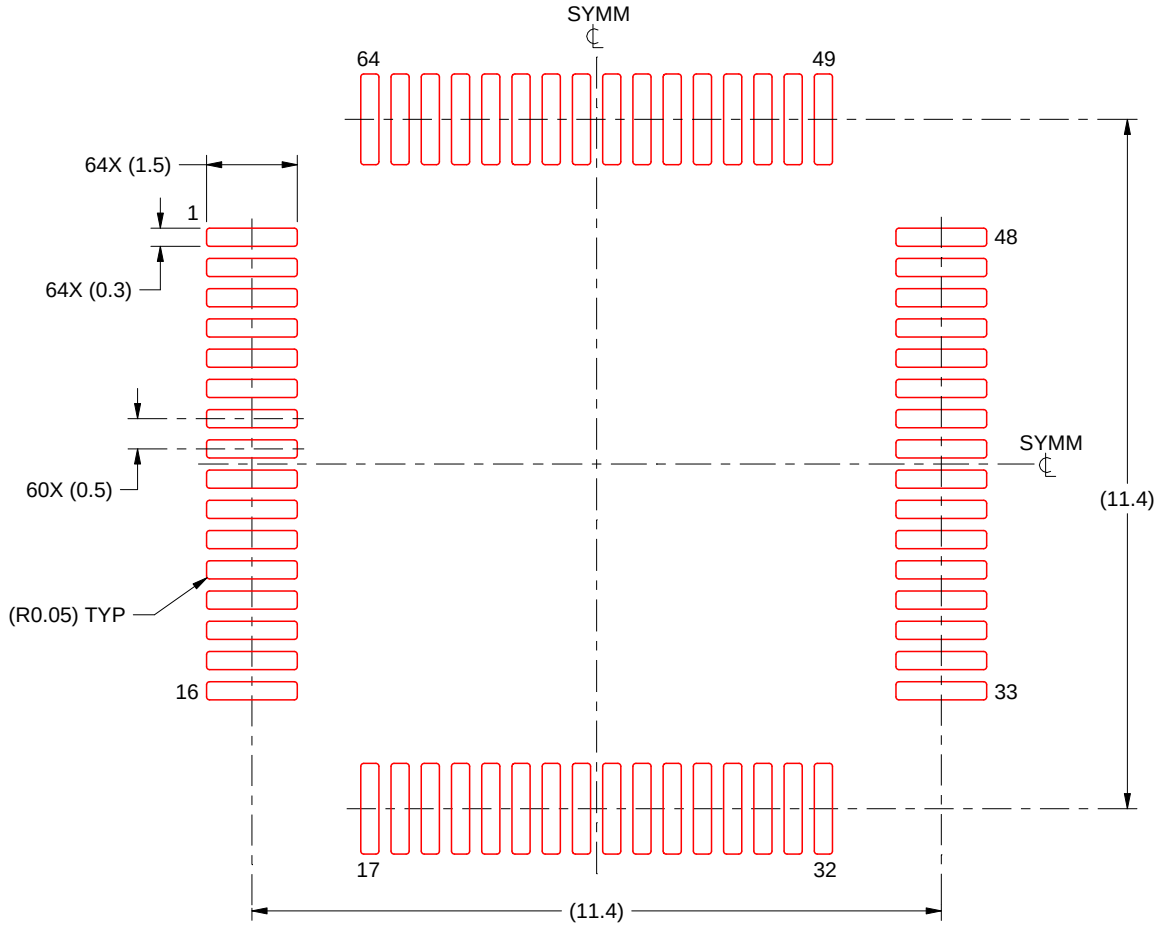


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

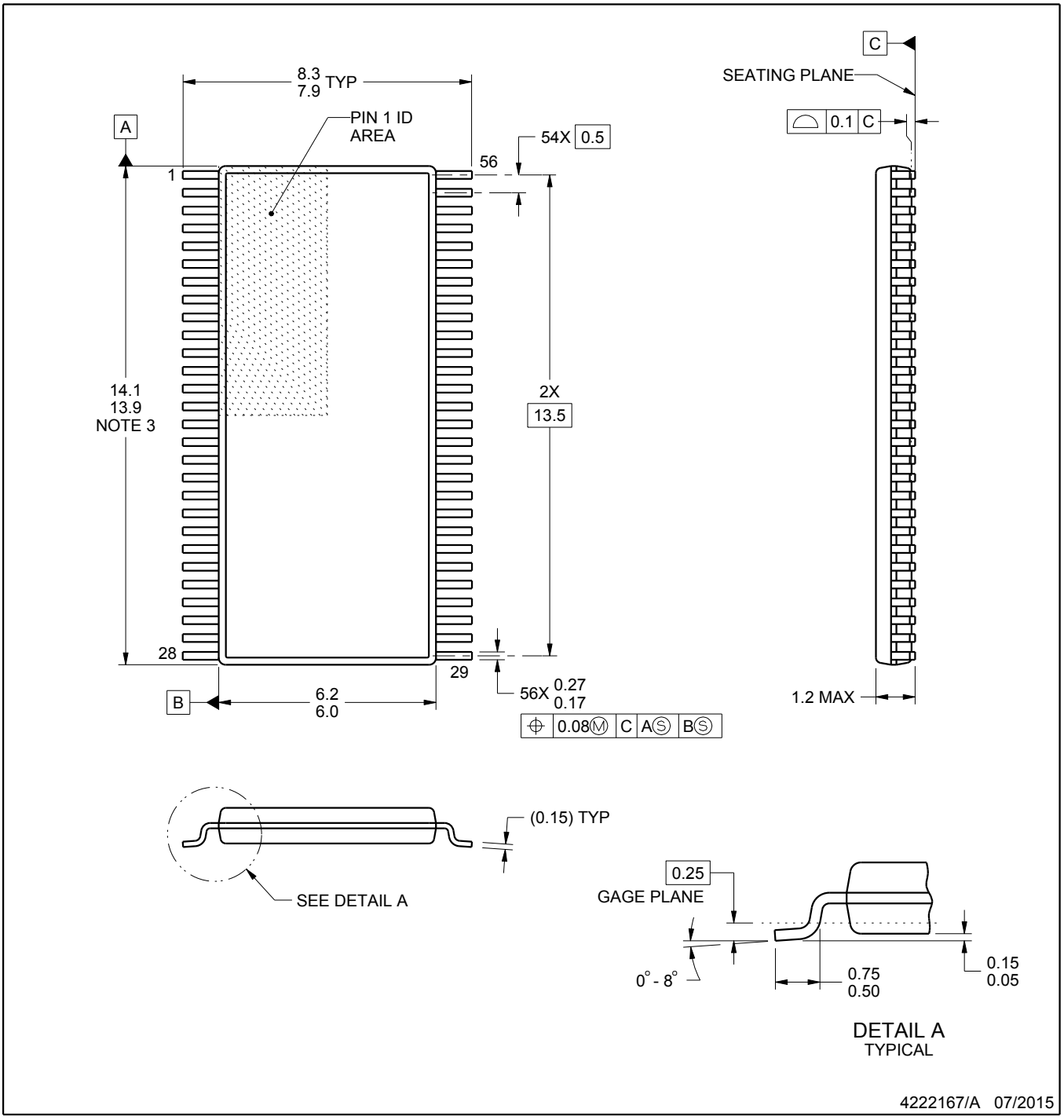
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGG0056A

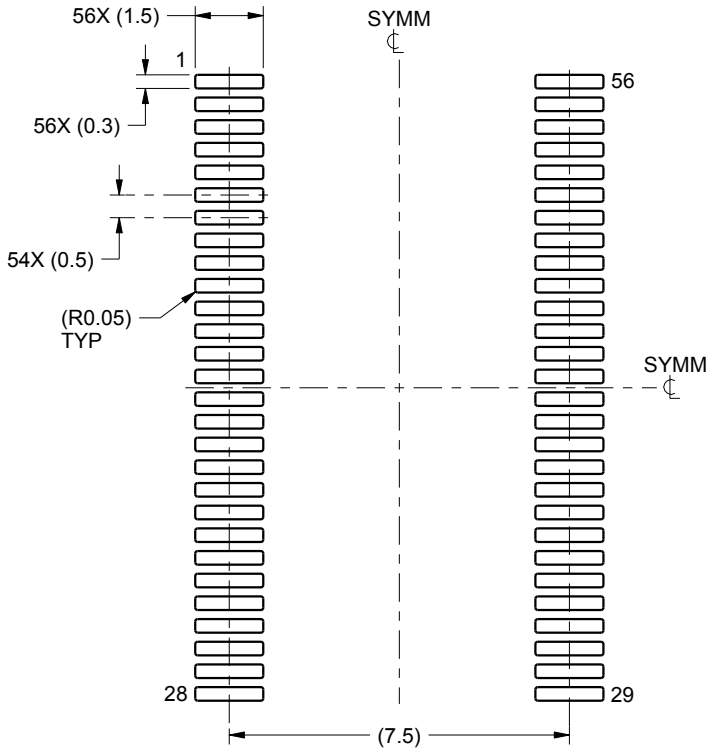
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

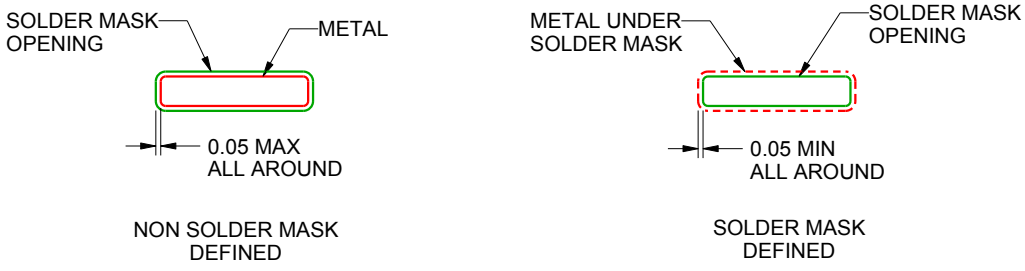


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

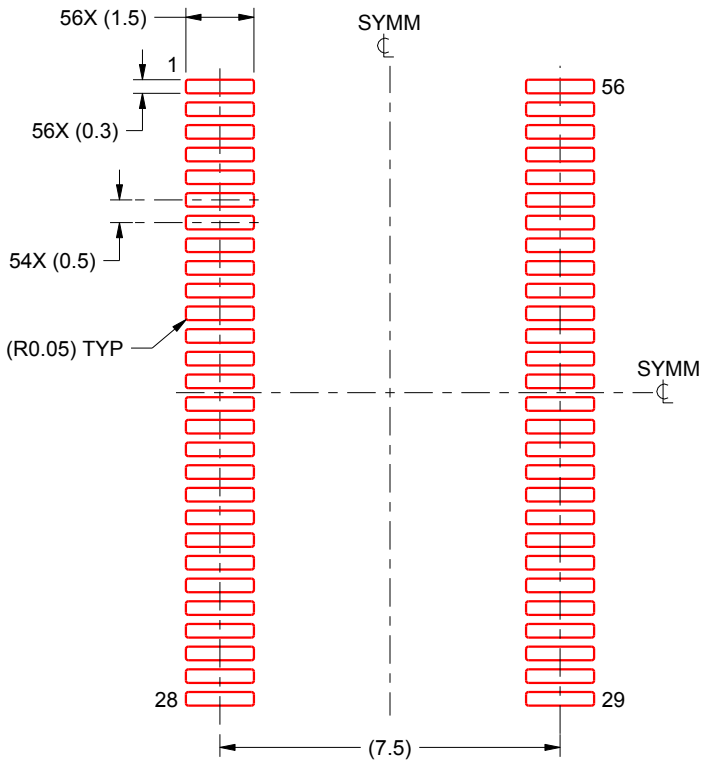


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

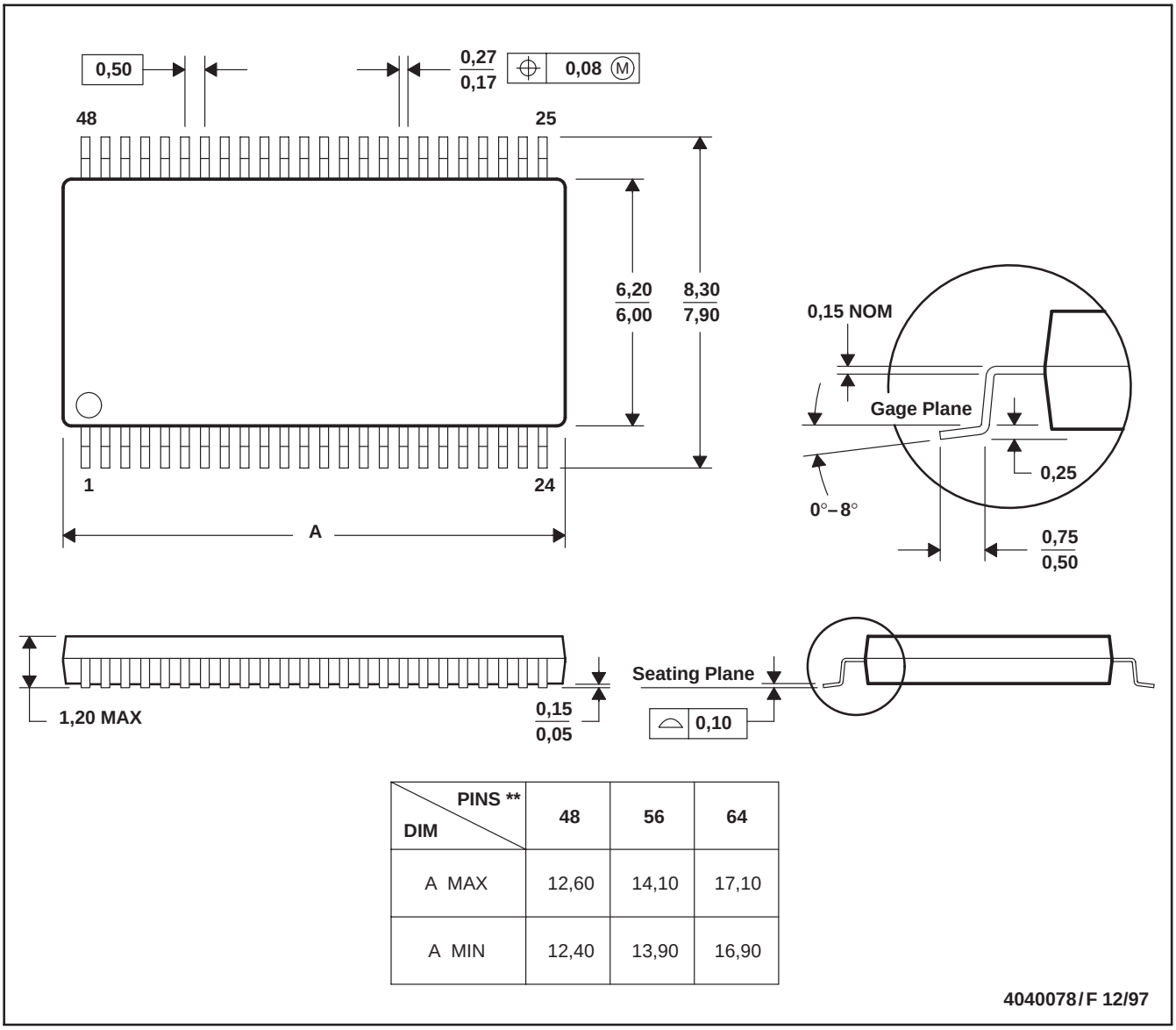
4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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