适用于成本敏感型系统的 TLV906xS 10MHz、RRIO、CMOS 运算放大器

1 具有

- 轨至轨输入和输出
- 低输入偏移电压：±0.3mV
- 单位增益带宽：10MHz
- 低宽带噪声：10nV/√Hz
- 低输入偏置电流：0.5pA
- 低静态电流：538µA
- 单位增益稳定
- 内部射频干扰 (RFI) 和电磁干扰 (EMI) 滤波器
- 可在电源电压低至 1.8V 的电压下运行
- 由于采用了电阻式开环输出阻抗，因此在更高的容性负载下可更轻松地实现稳定
- 关断版本：TLV906xS
- 扩展温度范围：–40°C 至 +125°C

2 应用

- 电动自行车
- 烟雾探测器
- HVAC：采暖、通风和空调
- 电机控制：交流感应
- 冰箱
- 可穿戴设备
- 笔记本电脑
- 洗衣机
- 传感器信号调节
- 电源模块
- 条形码扫描器
- 有源滤波器
- 低侧电流检测

3 说明

TLV9061（单通道）、TLV9062（双通道）和 TLV9064（四通道）是单路、双路和四路低压（1.8V 至 5.5V）运算放大器，具有轨至轨输入和输出摆幅能力。这些器件是具有高成本效益的解决方案，适用于需要低工作 电压、 小型封装尺寸和高容性负载驱动能力的应用。虽然 TLV906x 的容性负载驱动能力为 100pF，但电阻式开环输出阻抗便于在更高的容性负载下更轻松地实现稳定。此类运算放大器专为低工作电压（1.8V 至 5.5V）而设计，性能规格类似于 OPAx316 和 TLVx316 器件。

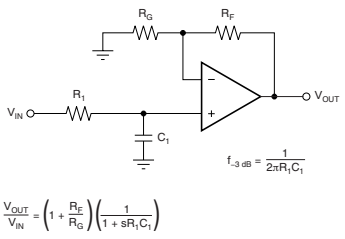
中 TLV9061 DPW (X2SON) 封装中的封装预览说明

器件信息(1)

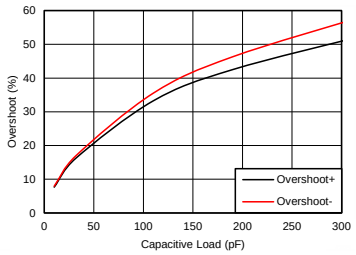
器件型号	封装	封装尺寸（标称值）
TLV9061	SOT-23 (5)	1.60mm × 2.90mm
	SC70 (5)	1.25mm × 2.00mm
	SOT553 (5)	1.65mm × 1.20mm
	X2SON (5)	0.80mm × 0.80mm
TLV9002S 中增加了 TLV9061S 器件	SOT-23 (6)	1.60mm × 2.90mm
TLV9062	SOIC (8)	3.91mm × 4.90mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
	WSON (8)	2.00mm × 2.00mm
	X2QFN (10)	1.50mm x 2.00mm
TLV9062S 中增加了 TLV9062S 器件	VSSOP (10)	3.00mm × 3.00mm
	X2QFN (10)	1.50mm x 2.00mm
TLV9064	SOIC (14)	8.65mm × 3.91mm
	TSSOP (14)	4.40mm × 5.00mm
	WQFN (16)	3.00mm × 3.00mm
	WQFN (14)	2.00mm × 2.00mm
TLV9064S 中增加了 TLV9064S 器件	WQFN (16)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

单极低通滤波器



小信号过冲与负载电容间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (June 2018) to Revision E — **Page**

- 已添加 在*器件信息*表 ... 1
- 已添加 在*器件信息* 表 ... 1
- Added 在*器件比较* 表 ... 5
- Added 在*引脚配置和功能* 部分中增加了 TLV9061S DBV (SOT-23) 引脚图 ... 7
- Added 在*引脚功能：TLV9061S* 表中 ... 7
- Added 在*引脚配置和功能* 部分中增加了 TLV9064 RTE (WQFN) 引脚图 ... 10
- Added 在*引脚功能：TLV9064* 表 ... 10
- Added 在*引脚功能：TLV9064* 表 ... 11
- Added 在*引脚配置和功能* 部分中增加了 TLV9064S RTE (WQFN) 引脚图 ... 11

Changes from Revision C (March 2018) to Revision D — **Page**

- 已添加 对文档标题中的“TLV906x”添加了关断后缀 ... 1
- 已添加 在*特性* 列表中增加了“关断版本”项目符号 ... 1
- 已添加 在*器件信息* 表 ... 1
- 已添加 在*说明 （续）*部分增加了关断文字 ... 4
- Added 在*绝对最大额定值* 表 ... 12
- Added 在*建议运行条件* 表 ... 12
- Added 在*建议运行条件* 表 ... 12
- Added 在*建议运行条件* 表的“额定温度”参数中增加了 ... 12
- Added *热性能信息：TLV9062S* 热性能表数据 ... 13
- 已添加 *关断功能* 部分 ... 23
- 已添加 *比较器典型应用* 部分 ... 26

Changes from Revision B (October 2017) to Revision C **Page**

- 已更改 将器件状态从“生产数据/混合状态”改为“生产数据” 1
- 已删除 删除了*器件信息* 表 1
- Deleted 删除了 TLV9061 DPW (X2SON) 封装引脚图中的封装预览说明 6
- Changed 更改了 *ESD 额定值* 表的格式以显示所有封装所对应的不同结果 12
- Deleted 删除了*热性能信息：TLV9061* 表 13

Changes from Revision A (June 2017) to Revision B **Page**

- Added 在*引脚配置和功能* 部分中添加 8 引脚 PW 封装 8
- Added 在*热性能信息* 表中添加了 DSG (WSON) 封装 13
- Added 在 TLV9062 *热性能信息* 表中添加了 PW (TSSOP) 13
- Changed 将最大输入失调电压值从 ±1.6mV 更改为 2mV 14
- Changed 将最大输入失调电压值从 ±1.5V 更改为 ±1.6mV 14
- Changed 将最小共模抑制比输入电压范围从 86dB 更改为 80dB 14
- Changed 将典型输入电流噪声密度值从 10 更改为 23fA/$\sqrt{Hz}$ 14
- Changed 将 THD + N 测试条件从 V_S = 5V 更改为 V_S = 5.5V 14
- Added 在 THD + N 参数中添加 V_{CM} = 2.5V 测试条件（位于*电气特性* 表中） 14
- Added 将最大输出电压摆幅值从 25mV 更改为 60mV 14
- Changed 将最大输出电压摆幅值从 15mV 更改为 20mV 14

Changes from Original (March 2017) to Revision A **Page**

- 已更改 将器件状态从“预告信息”改为“生产数据” 1

5 说明（续）

TLV900x 器件具有关断模式，允许放大器切换至典型电流消耗低于 1µA 的待机模式。

TLV906xS 系列有助于简化系统设计，因为该系列具有稳定的单位增益，集成了 RFI 和 EMI 抑制滤波器，而且在过驱条件下不会出现反相。

针对所有通道类型（单通道、双通道和四通道）提供*微型*封装（如 SOT-553 和 WSON、）以及行业标准封装（如 SOIC、MSOP、SOT-23 和 TSSOP）。

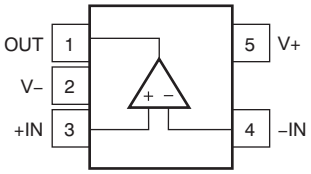
6 器件比较表

中增加了 RUC 和 RUG 封装

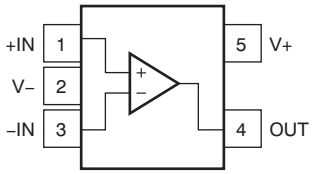
器件	通道数	封装引线											
		DBV	DCK	DRL	DPW	D	DSG	DGK	DGS	PW	RTE	RUC	RUG
TLV9061	1	5、6	5	5	5	8	—	—	—	—	—	—	—
TLV9062	2	—	—	—	—	8	8	8	10	8	—	—	10
TLV9064	4	—	—	—	—	14	—	—	—	14	16	14	—

7 引脚配置和功能

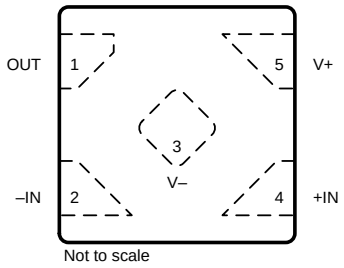
TLV9061 DBV 和 DRL 封装
5 引脚 SOT-23 和 SOT-553
俯视图



TLV9061 DCK 封装
5 引脚 SC70
俯视图



TLV9061 DPW 封装
5 引脚 X2SON
俯视图

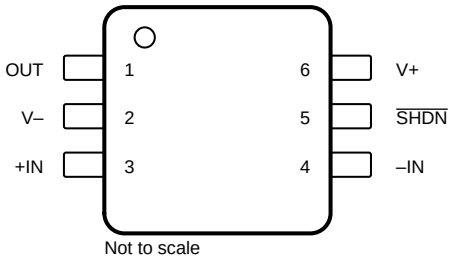


Not to scale

引脚功能：TLV9061

引脚				I/O	说明
名称	SOT-23、SOT-553	SC70	X2SON		
–IN	4	3	2	I	反相输入
+IN	3	1	4	I	同相输入
OUT	1	4	1	O	输出
$\overline{\text{SHDN}}$	—	—	—	I	关断（低电平有效）
V–	2	2	3	—	负（最低）电源或接地（对于单电源供电）
V+	5	5	5	—	正（最高）电源

TLV9061S DBV 封装
6 引脚 SOT-23
俯视图

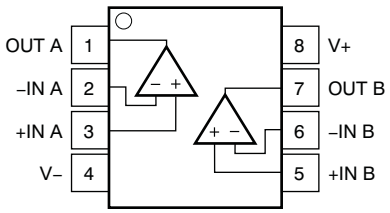


Not to scale

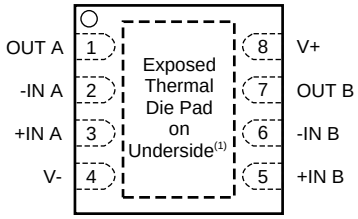
引脚功能：TLV9061S

引脚		I/O	说明增加了 TLV9061S DBV (SOT-23) 封装引脚信息
名称	编号		
–IN	4	I	反相输入
+IN	3	I	同相输入
OUT	1	O	输出
$\overline{\text{SHDN}}$	5	I	关断（低电平有效）
V–	2	—	负（最低）电源或接地（对于单电源供电）
V+	6	—	正（最高）电源

TLV9062 D、DGK、PW 封装
8 引脚 SOIC、VSSOP、TSSOP
俯视图



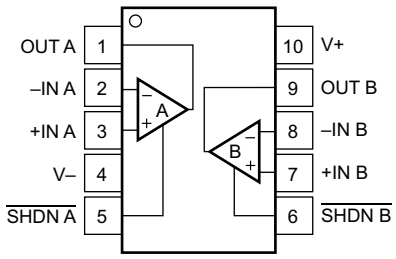
TLV9062 DSG 封装
带有外露散热焊盘的 8 引脚 WSON 封装
俯视图



引脚功能：TLV9062

引脚		I/O	说明
名称	编号		
–IN A	2	I	反相输入，通道 A
+IN A	3	I	同相输入，通道 A
–IN B	6	I	反相输入，通道 B
+IN B	5	I	同相输入，通道 B
OUT A	1	O	输出，通道 A
OUT B	7	O	输出，通道 B
NC	—	—	无内部连接
$\overline{\text{SHDN A}}$	—	I	关断（逻辑低电平），启用（逻辑高电平），通道 A
$\overline{\text{SHDN B}}$	—	I	关断（逻辑低电平），启用（逻辑高电平），通道 B
V–	4	—	负（最低）电源或接地（对于单电源供电）
V+	8	—	正（最高）电源

TLV9062S DGS 封装
10 引脚 VSSOP
俯视图



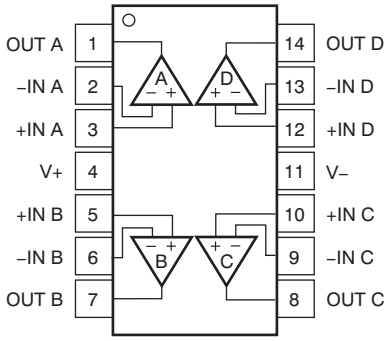
引脚功能：TLV9062S

引脚		I/O	说明
名称	编号		
–IN A	2	I	反相输入，通道 A
+IN A	3	I	同相输入，通道 A
–IN B	8	I	反相输入，通道 B
+IN B	7	I	同相输入，通道 B
OUT A	1	O	输出，通道 A
OUT B	9	O	输出，通道 B
NC	—	—	无内部连接
$\overline{\text{SHDN A}}$	5	I	关断（逻辑低电平），启用（逻辑高电平），通道 A
$\overline{\text{SHDN B}}$	6	I	关断（逻辑低电平），启用（逻辑高电平），通道 B
V–	4	—	负（最低）电源或接地（对于单电源供电）

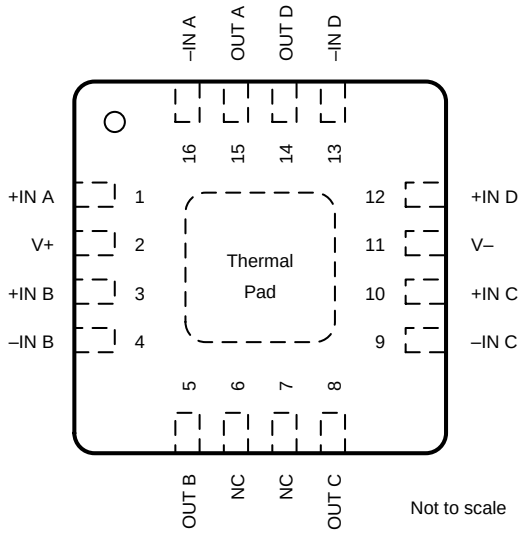
引脚功能：TLV9062S (continued)

引脚		I/O	说明
名称	编号		
V+	10	—	正（最高）电源

TLV9064 D、PW 封装
14 引脚 SOIC、TSSOP
俯视图



TLV9064 RTE 封装
带有外露散热焊盘的 16 引脚 WQFN 封装
俯视图



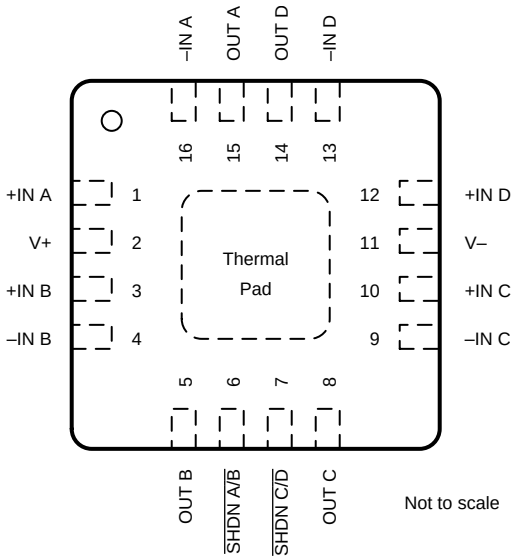
引脚功能：TLV9064

引脚			I/O	说明中增加了 RUC 封装引脚信息中增加了 TLV9064 RTE 引脚信息
名称	SOIC、TSSOP	WQFN		
–IN A	2	16	I	反相输入，通道 A
+IN A	3	1	I	同相输入，通道 A
–IN B	6	4	I	反相输入，通道 B
+IN B	5	3	I	同相输入，通道 B
–IN C	9	9	I	反相输入，通道 C
+IN C	10	10	I	同相输入，通道 C
–IN D	13	13	I	反相输入，通道 D
+IN D	12	12	I	同相输入，通道 D
NC	—	6、7	—	无内部连接
OUT A	1	15	O	输出，通道 A
OUT B	7	5	O	输出，通道 B
OUT C	8	8	O	输出，通道 C
OUT D	14	14	O	输出，通道 D

引脚功能：TLV9064 (continued)

引脚			I/O	说明中增加了 RUC 封装引脚信息中增加了 TLV9064 RTE 引脚信息
名称	SOIC、TSSOP	WQFN		
$\overline{\text{SHDN A/B}}$	—	—	I	关断（逻辑低电平），启用（逻辑高电平），通道 A/B
$\overline{\text{SHDN C/D}}$	—	—	I	关断（逻辑低电平），启用（逻辑高电平），通道 C/D
V–	11	11	—	负（最低）电源或接地（对于单电源供电）
V+	4	2	—	正（最高）电源

TLV9064S RTE 封装
带有外露散热焊盘的 16 引脚 WQFN 封装
俯视图



引脚功能：TLV9064S

引脚		I/O	说明
名称	编号		
–IN A	16	I	反相输入，通道 A
+IN A	1	I	同相输入，通道 A
–IN B	4	I	反相输入，通道 B
+IN B	3	I	同相输入，通道 B
–IN C	9	I	反相输入，通道 C
+IN C	10	I	同相输入，通道 C
–IN D	13	I	反相输入，通道 D
+IN D	12	I	同相输入，通道 D
OUT A	15	O	输出，通道 A
OUT B	5	O	输出，通道 B
OUT C	8	O	输出，通道 C
OUT D	14	O	输出，通道 D
$\overline{\text{SHDN A/B}}$	6	I	关断（逻辑低电平），启用（逻辑高电平），通道 A/B
$\overline{\text{SHDN C/D}}$	7	I	关断（逻辑低电平），启用（逻辑高电平），通道 C/D
V–	11	—	负（最低）电源或接地（对于单电源供电）
V+	2	—	正（最高）电源

8 规格

8.1 绝对最大额定值

在自然通风温度下测得（除非另有说明）(1)

			最小值	最大值	单位
电源电压				6	V
信号输入引脚	电压(2)	共模	(V–) – 0.5	(V+) + 0.5	V
		差模		(V+) – (V–) + 0.2	
	电流(2)		-10	10	mA
输出短路(3)			连续		mA
温度	额定温度，T_A		–40	125	°C
	结温，T_J			150	
	贮存温度，T_{stg}		–65	150	

(1) 应力超出"绝对最大额定值"下所列的值可能会对器件造成永久损坏。这些列出的值仅仅是极端条件下的应力额定值，并不表示器件在这些条件下以及在"建议运行条件"以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 输入引脚被二极管钳制至电源轨。对于摆幅能超过电源轨 0.5V 的输入信号，应将其电流限制在 10mA 或者更低。
(3) 接地短路，每个封装对应一个放大器。

8.2 ESD 额定值

		值	单位
TLV9061 DPW (X2SON) 封装			
$V_{(ESD)}$ 静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001(1)	±2500	V
	充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101(2)	±1500	
所有其他封装			
$V_{(ESD)}$ 静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101(2)	±1500	

(1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 时能够在标准 ESD 控制流程下安全生产。

中增加了 (V_S = [V+] – [V–]) 电源电压参数中增加了"输入电压范围"和"输出电压范围"参数和值中增加了关断引脚建议运行条件"T_A"符号

8.3 建议的工作条件

在自然通风温度范围内测得（除非另有说明）

		最小值	最大值	单位
V_S	电源电压 (V_S = [V+] – [V–])	1.8	5.5	V
V_I	输入电压范围	(V–) – 0.1	(V+)+0.1	V
V_O	输出电压范围	V–	V+	V
V_{SHDN_IH}	关断引脚上的高电平输入电压（放大器为启用状态）	1.1	V+	V
V_{SHDN_IL}	关断引脚上的低电平输入电压（放大器为禁用状态）	V-	0.2	V
T_A	额定温度范围	–40	125	°C

中 DPW (X2SON) 封装中的封装预览说明

8.4 热性能信息：TLV9061

热指标(1)		TLV9061			单位
		DBV (SOT-23)	DCK (SC70)	DPW (X2SON)	
		5/6 引脚	5 引脚	5 引脚	
$R_{\theta JA}$	结至环境热阻	221.7	263.3	467	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	144.7	75.5	211.6	°C/W
$R_{\theta JB}$	结至电路板热阻	49.7	51	332.2	°C/W
ψ_{JT}	结至顶部特征参数	26.1	1	29.3	°C/W
ψ_{JB}	结至电路板特征参数	49	50.3	330.6	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	125	°C/W

(1) 有关传统和新热指标的更多信息，请参阅应用报告《*半导体和 IC 封装热指标*》。

8.5 热性能信息：TLV9062

热指标(1)		TLV9062				单位
		D (SOIC)	DGK (VSSOP)	DSG (WSON)	PW (TSSOP)	
		8 引脚	8 引脚	8 引脚	8 引脚	
$R_{\theta JA}$	结至环境热阻	157.6	201.2	94.4	205.8	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	104.6	85.7	116.5	106.7	°C/W
$R_{\theta JB}$	结至电路板热阻	99.7	122.9	61.3	133.9	°C/W
ψ_{JT}	结至顶部特征参数	55.6	21.2	13	34.4	°C/W
ψ_{JB}	结至电路板特征参数	99.2	121.4	61.7	132.6	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	34.4	不适用	°C/W

(1) 有关传统和新热指标的更多信息，请参阅应用报告《*半导体和 IC 封装热指标*》。

8.6 热性能信息：TLV9062S

热指标(1)		TLV9062S	单位
		DGS (VSSOP)	
		10 引脚	
$R_{\theta JA}$	结至环境热阻	170.4	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	84.9	°C/W
$R_{\theta JB}$	结至电路板热阻	113.5	°C/W
ψ_{JT}	结至顶部特征参数	16.4	°C/W
ψ_{JB}	结至电路板特征参数	112.3	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	°C/W

(1) 有关传统和新热指标的更多信息，请参阅应用报告《*半导体和 IC 封装热指标*》。

8.7 热性能信息：TLV9064

热指标(1)		TLV9064		单位
		PW (TSSOP)	D (SOIC)	
		14 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	135.8	106.9	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	64	64	°C/W
$R_{\theta JB}$	结至电路板热阻	79	63	°C/W
ψ_{JT}	结至顶部特征参数	15.7	25.9	°C/W
ψ_{JB}	结至电路板特征参数	78.4	62.7	°C/W

(1) 有关传统和新热指标的更多信息，请参阅应用报告《*半导体和 IC 封装热指标*》。

8.8 电气特性：V_S（总电源电压）= (V+) – (V–) = 1.8V 至 5.5V

T_A = 25°C，R_L = 10kΩ（连接至 V_S / 2），V_{CM} = V_S / 2，且 V_{OUT} = V_S / 2（除非另有说明）

参数		测试条件	最小值	典型值	最大值	单位
失调电压						
V_{OS}	输入失调电压	V_S = 5V		±0.3	±1.6	mV
		V_S = 5V，T_A = –40°C 至 +125°C			±2	
dV_{OS}/dT	漂移	V_S = 5V，T_A = –40°C 至 +125°C		±0.53		µV/°C
PSRR	电源抑制比	V_S = 1.8V – 5.5V，V_{CM} = (V–)		±7	±80	µV/V
	通道分离，直流	直流时		100		dB
输入电压范围						
V_{CM}	共模电压范围	V_S = 1.8V 至 5.5V	(V–) – 0.1		(V+)+0.1	V
CMRR	共模抑制比	V_S = 5.5V，(V–) – 0.1 V < V_{CM} < (V+) – 1.4V T_A = –40°C 至 +125°C	80	103		dB
		V_S = 5.5V，V_{CM} = –0.1V 至 5.6V T_A = –40°C 至 +125°C	57	87		
		V_S = 1.8V，(V–) – 0.1 V < V_{CM} < (V+) – 1.4V， T_A = –40°C 至 +125°C		88		
		V_S = 1.8V，V_{CM} = –0.1V 至 1.9V T_A = –40°C 至 +125°C		81		
输入偏置电流						
I_B	输入偏置电流			±0.5		pA
I_{OS}	输入失调电流			±0.05		pA
噪声						
E_n	输入电压噪声（峰峰值）	V_S = 5V，f = 0.1Hz 至 10Hz		4.77		μV_{PP}
e_n	输入电压噪声密度	V_S = 5V，f = 10kHz		10		nV/√Hz
		V_S = 5V，f = 1kHz		16		nV/√Hz
i_n	输入电流噪声密度	f = 1kHz		23		fA/√Hz
输入电容						
C_{ID}	差分			2		pF
C_{IC}	共模			4		pF
开环增益						
A_{OL}	开环电压增益	V_S = 1.8V，(V–) + 0.04V < V_O < (V+) – 0.04V， R_L = 10kΩ		100		dB
		V_S = 5.5V，(V–) + 0.05V < V_O < (V+) – 0.05V， R_L = 10kΩ	104	130		
		V_S = 1.8V，(V–) + 0.06V < V_O < (V+) – 0.06V， R_L = 2kΩ		100		
		V_S = 5.5V，(V–) + 0.15V < V_O < (V+) – 0.15V， R_L = 2kΩ		130		
频率响应						
GBP	增益带宽积	V_S = 5V，G = +1		10		MHz
φ_m	相位裕度	V_S = 5V，G = +1		55		°
SR	压摆率	V_S = 5V，G = +1		6.5		V/µs
t_S	建立时间	精度达到 0.1%，V_S = 5V，2V 阶跃，G = +1，C_L = 100pF		0.5		µs
		精度达到 0.01%，V_S = 5V，2V 阶跃， G = +1，C_L = 100pF		1		
t_{OR}	过载恢复时间	V_S = 5V，V_{IN} × 增益 > V_S		0.2		µs
THD + N	总谐波失真 + 噪声(1)	V_S = 5.5V，V_{CM} = 2.5V，V_O = 1V_{RMS}，G = +1，f = 1kHz		0.0008%		
输出						
V_O	相对于电源轨的电压输出摆幅	V_S = 5.5V，R_L = 10kΩ			20	mV
		V_S=5.5V，R_L=2kΩ			60	
I_{SC}	短路电流	V_S = 5V		±50		mA
Z_O	开环输出阻抗	V_S = 5V，f = 10MHz		100		Ω

(1) 三阶滤波器；–3dB 时的带宽 = 80kHz。

电气特性：V_S（总电源电压）= (V+) – (V–) = 1.8V 至 5.5V (continued)

T_A = 25°C，R_L = 10kΩ（连接至 V_S / 2），V_{CM} = V_S / 2，且 V_{OUT} = V_S / 2（除非另有说明）

参数		测试条件	最小值	典型值	最大值	单位
电源						
I_Q	每个放大器的静态电流	V_S = 5.5V，I_O = 0mA		538	750	μA
		V_S = 5.5V，I_O = 0mA，T_A = –40°C 至 +125°C			800	
关断						
I_{QSD}	静态电流（每个放大器）	V_S = 1.8V 至 5.5V，所有放大器为禁用状态，$\overline{SHDN}$ = V_S–		0.5	1.5	μA
Z_{SHDN}	关断时的输出阻抗	V_S = 1.8V 至 5.5V，放大器为禁用状态		10 || 8		GΩ || pF
$V_{SHDN\_THR\_HI}$	高电平电压关断阈值（放大器为启用状态）	V_S = 1.8V 至 5.5V		(V–) + 0.9V	(V–) + 1.1V	V
$V_{SDHN\_THR\_LO}$	低电平电压关断阈值（放大器为禁用状态）	V_S = 1.8V 至 5.5V	(V–) + 0.2V	(V–) + 0.7V		V
t_{ON}	放大器启用时间（完全关断）(2)(3)	V_S = 1.8V 至 5.5V，完全关断；G = 1，V_{OUT} = 0.9 × V_S/2，R_L 连接到 V–		10		μs
	放大器启用时间（部分关断）(2)(3)	V_S = 1.8V 至 5.5V，部分关断；G = 1，V_{OUT} = 0.9 × V_S/2，R_L 连接到 V–		6		μs
t_{OFF}	放大器禁用时间(2)	V_S = 1.8V 至 5.5V，G = 1，V_{OUT} = 0.1 × V_S/2，R_L 连接到 V–		0.5		μs
	$\overline{SHDN}$ 引脚输入偏置电流（每个引脚）	V_S = 1.8V 至 5.5V，V+ ≥ $\overline{SHDN}$ ≥ (V+) - 0.8V		130		pA
		V_S = 1.8V 至 5.5V，V- ≤ $\overline{SHDN}$ ≤ V- + 0.8V		40		

(2) 禁用时间 (t_{OFF}) 和启用时间 (t_{ON}) 是指施加给 $\overline{SHDN}$ 引脚的信号为 50% 时到输出电压达到 10%（禁用）或 90%（启用）电平时之间的时间间隔。

(3) 完全关断是指双通道 TLV9062S 将 A、B 两个通道都禁用 ($\overline{SHDN\_A}$ = $\overline{SHDN\_B}$ = V_) 以及四通道 TLV9064S 将 A、B、C、D 四个通道都禁用 (SHDN_A/B = $\overline{SHDN\_C/D}$ = V_–)。部分关断是指仅使用一个 $\overline{SHDN}$ 引脚；在这种模式下，内部偏置电路仍然保持正常工作，并且启用时间更短。

8.9 典型特性

T_A = 25°C，V_S = 5.5V，R_L = 10kΩ（连接至 V_S / 2），V_{CM} = V_S / 2，且 V_{OUT} = V_S / 2（除非另有说明）

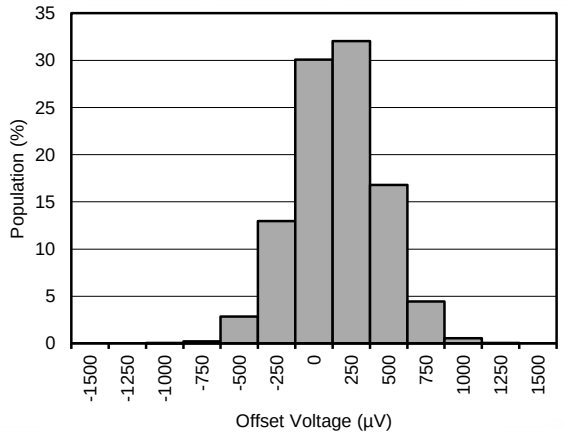
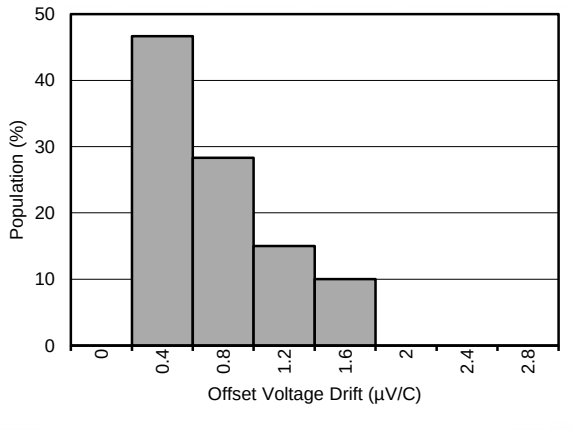


图 1. 失调电压产生分布



T_A = –40°C 至 +125°C

图 2. 失调电压漂移分布

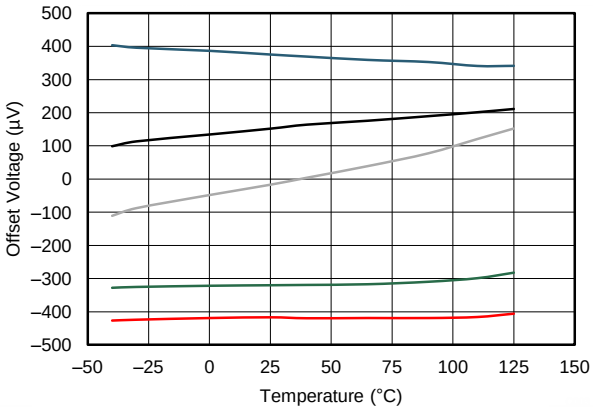
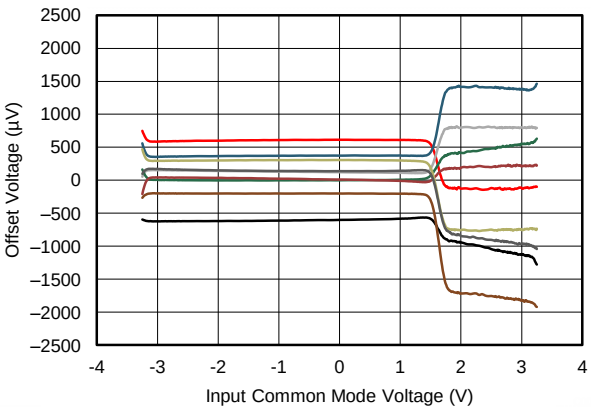
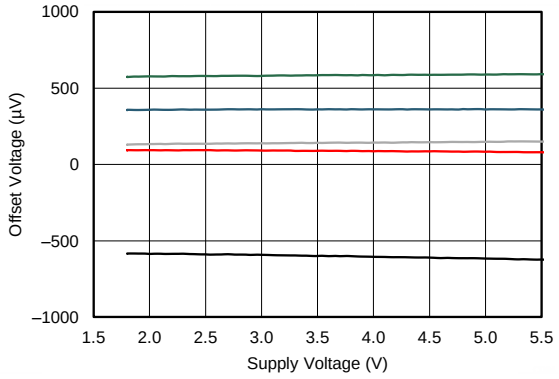


图 3. 失调电压与温度间的关系



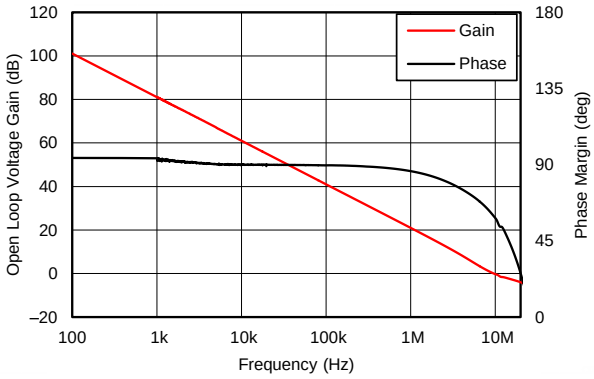
V+ = 2.75V，V– = –2.75V

图 4. 失调电压与共模电压间的关系



V_S = 1.8V 至 5.5V

图 5. 失调电压与电源间的关系

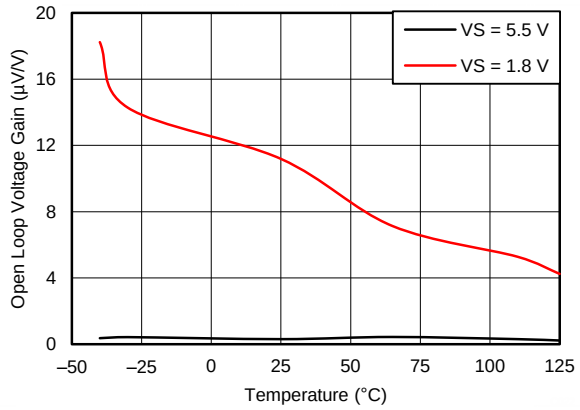


C_L = 10pF

图 6. 开环增益和相位与频率间的关系

典型特性 (接下页)

T_A = 25°C，V_S = 5.5V，R_L = 10kΩ（连接至 V_S / 2），V_{CM} = V_S / 2，且 V_{OUT} = V_S / 2（除非另有说明）



R_L = 2kΩ

图 7. 开环增益与温度间的关系

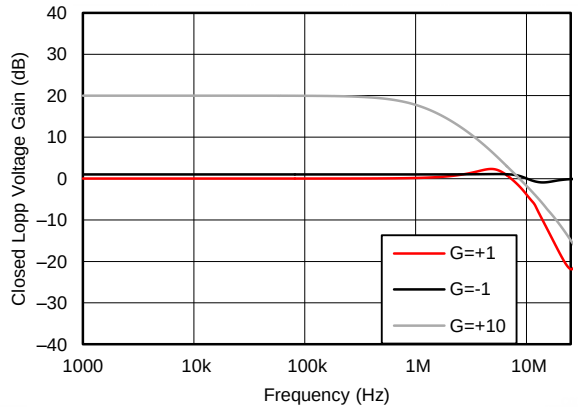


图 8. 闭环增益与频率间的关系

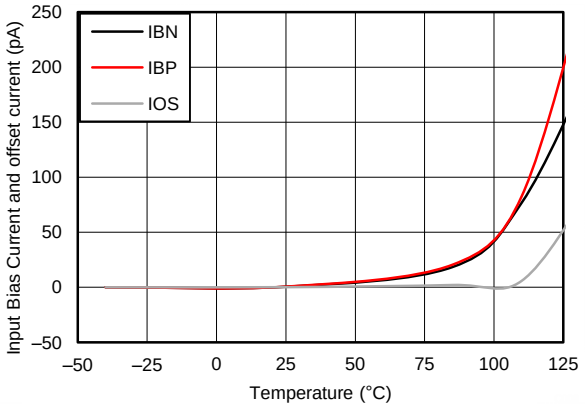
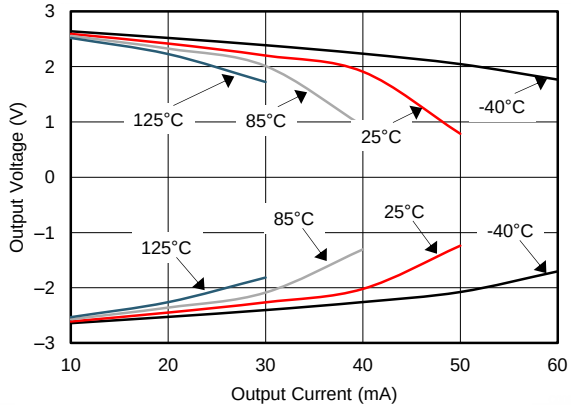


图 9. 输入偏置电流与温度间的关系



V+ = 2.75V，V– = –2.75V

图 10. 输出电压摆幅与输出电流间的关系

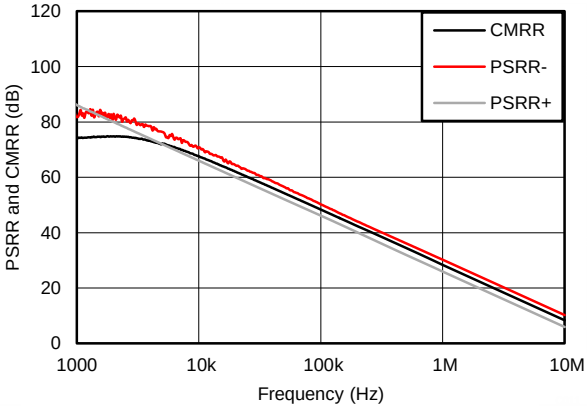
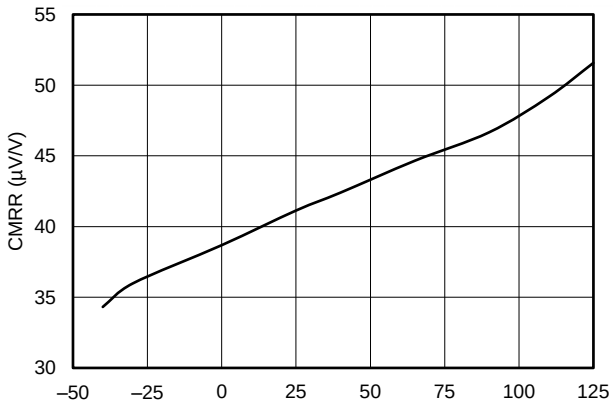


图 11. CMRR 和 PSRR 与频率间的关系（以输入为基准）

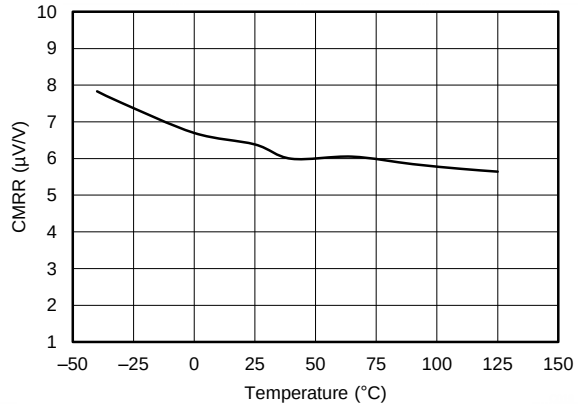


V_S = 5.5V，V_{CM} = –0.1V 至 5.6V
T_A = –40°C 至 +125°C，R_L = 10kΩ

图 12. CMRR 与温度间的关系

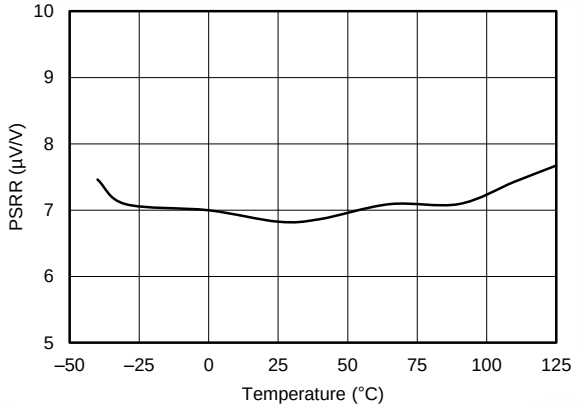
典型特性 (接下页)

T_A = 25°C，V_S = 5.5V，R_L = 10kΩ（连接至 V_S / 2），V_{CM} = V_S / 2，且 V_{OUT} = V_S / 2（除非另有说明）



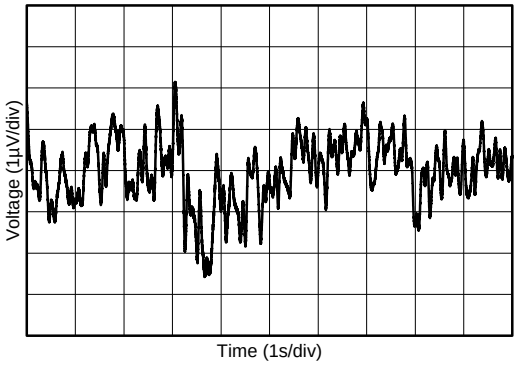
V_S = 5.5V，V_{CM} = (V–) – 0.1V 至 (V+) – 1.4V
T_A= –40°C 至 +125°C，R_L= 10kΩ

图 13. CMRR 与温度间的关系



V_S = 1.8V 至 5.5V

图 14. PSRR 与温度间的关系



V_S = 1.8V 至 5.5V

图 15. 0.1Hz 至 10Hz 输入电压噪声

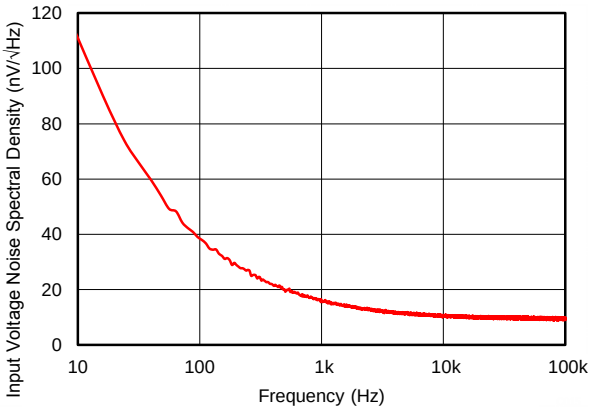
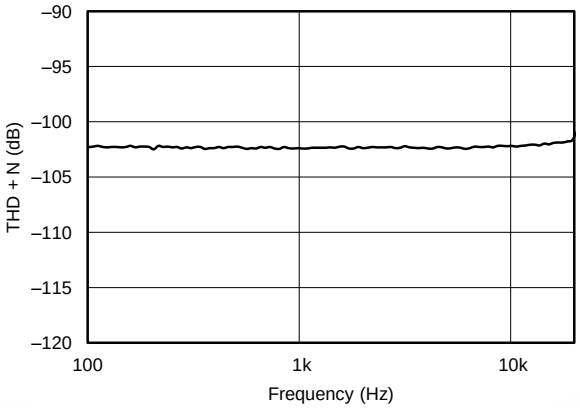
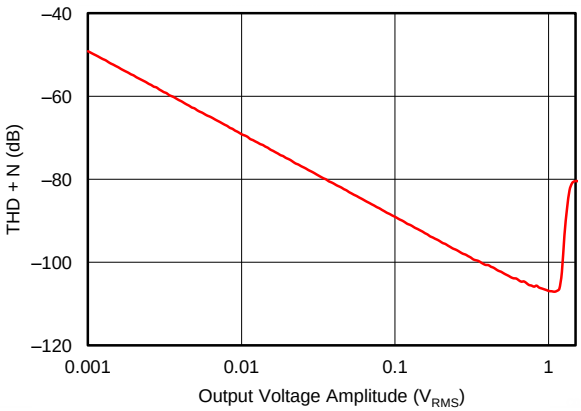


图 16. 输入电压噪声频谱密度与频率间的关系



V_S = 5.5V，V_{CM} = 2.5V，R_L = 2kΩ，G = +1，BW = 80kHz
V_{OUT} = 0.5V_{RMS}

图 17. THD + N 与频率间的关系

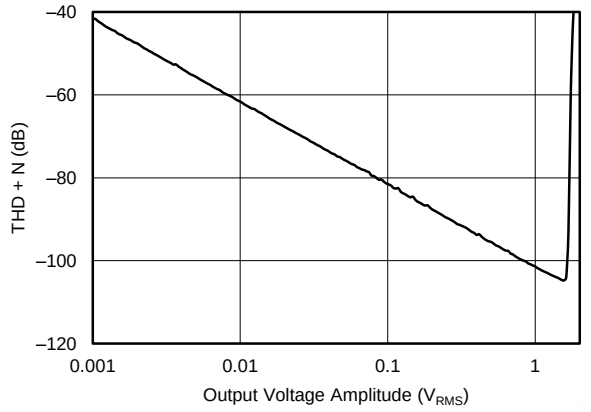


V_S = 5.5V，V_{CM} = 2.5V，R_L = 2kΩ，G = +1
BW = 80kHz，f = 1kHz

图 18. THD + N 与幅度间的关系

典型特性 (接下页)

T_A = 25°C，V_S = 5.5V，R_L = 10kΩ（连接至 V_S / 2），V_{CM} = V_S / 2，且 V_{OUT} = V_S / 2（除非另有说明）



V_S = 5.5V，V_{CM} = 2.5V，R_L = 2kΩ，G = –1
BW = 80kHz，f = 1kHz

图 19. THD + N 与幅度间的关系

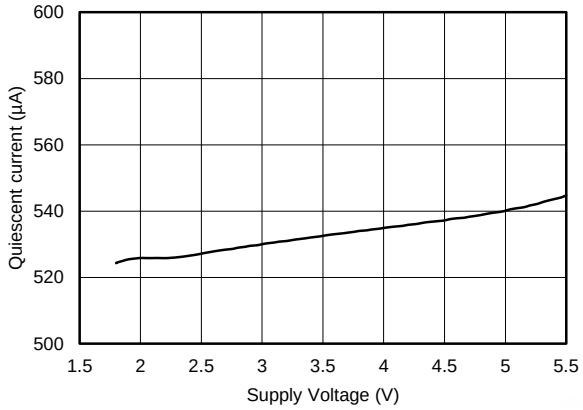


图 20. 静态电流与电源电压间的关系

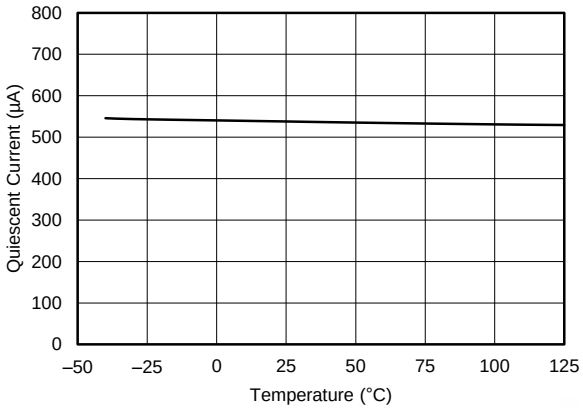


图 21. 静态电流与温度间的关系

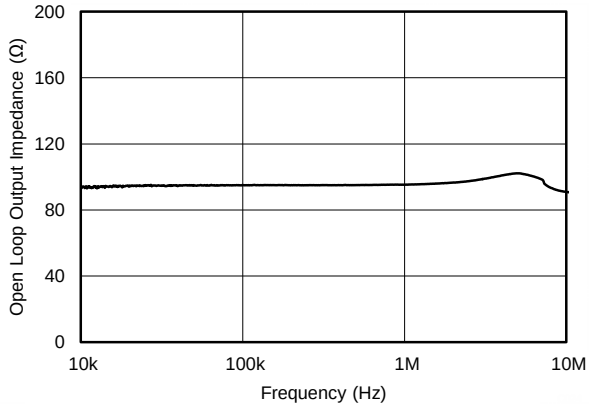
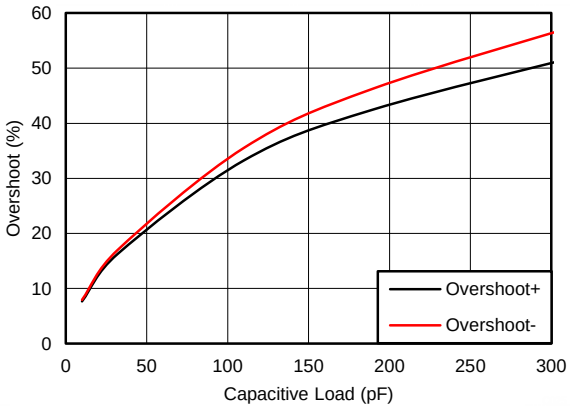
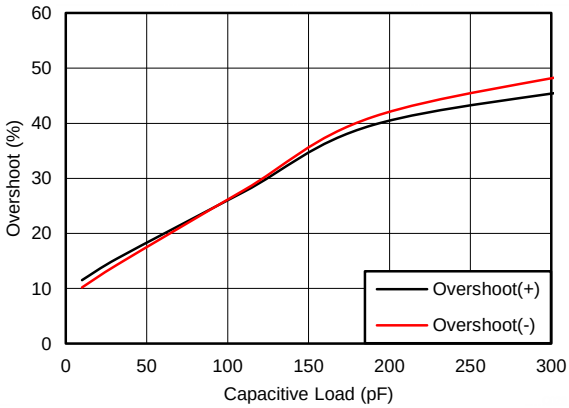


图 22. 开环输出阻抗与频率间的关系



V+ = 2.75V，V– = –2.75V，G = +1V/V，R_L = 10kΩ
V_{OUT} 阶跃 = 100mV_{p-p}

图 23. 小信号过冲与负载电容间的关系

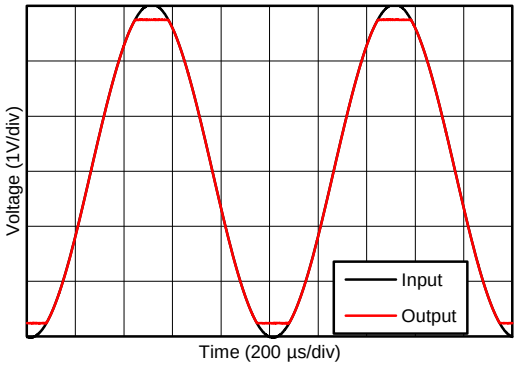


V+ = 2.75V，V– = –2.75V，G = -1V/V，R_L = 10kΩ
V_{OUT} 阶跃 = 100mV_{p-p}

图 24. 小信号过冲与负载电容间的关系

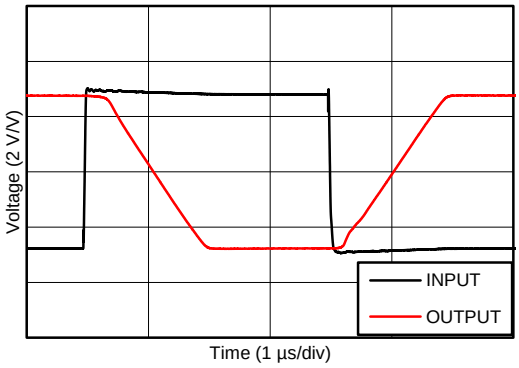
典型特性 (接下页)

T_A = 25°C，V_S = 5.5V，R_L = 10kΩ（连接至 V_S / 2），V_{CM} = V_S / 2，且 V_{OUT} = V_S / 2（除非另有说明）



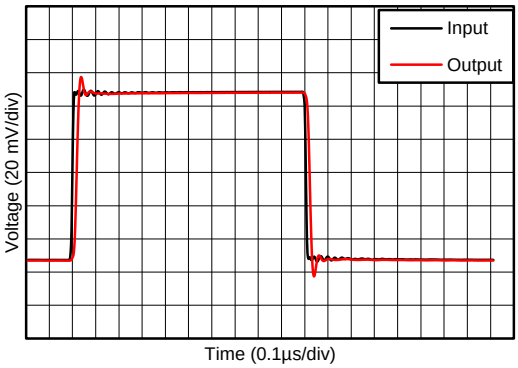
V+ = 2.75V，V– = –2.75V

图 25. 无相位反转



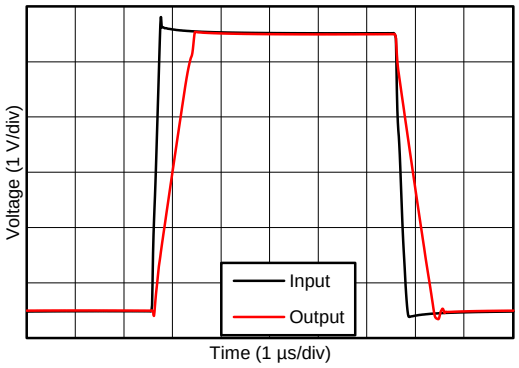
V+ = 2.75V，V– = –2.75V，G = –10V/V

图 26. 过载恢复



V+ = 2.75V，V– = –2.75V，G = 1V/V

图 27. 小信号阶跃响应



V+ = 2.75V，V– = –2.75V，C_L = 100pF，G = 1V/V

图 28. 大信号阶跃响应

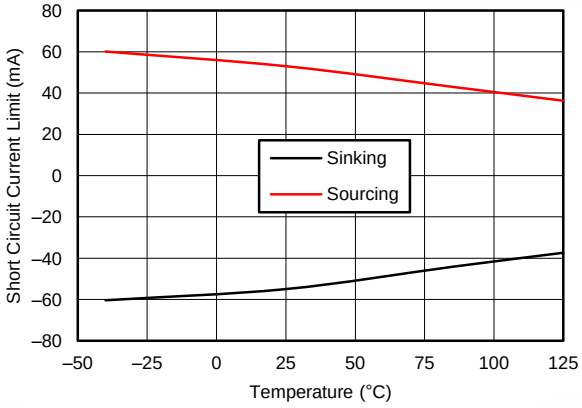
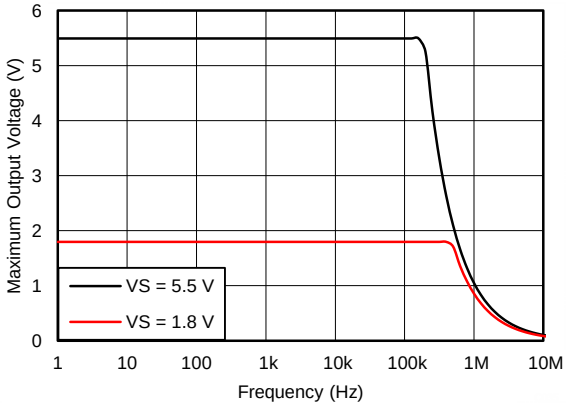


图 29. 短路电流与温度间的关系



R_L = 10kΩ，C_L = 10pF

图 30. 最大输出电压与频率和电源电压间的关系

典型特性 (接下页)

T_A = 25°C，V_S = 5.5V，R_L = 10kΩ（连接至 V_S / 2），V_{CM} = V_S / 2，且 V_{OUT} = V_S / 2（除非另有说明）

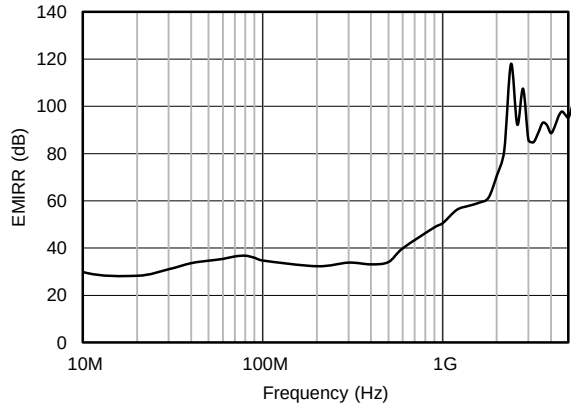


图 31. 以同相输入为基准的电磁干扰抑制比 (EMIRR+) 与频率间的关系

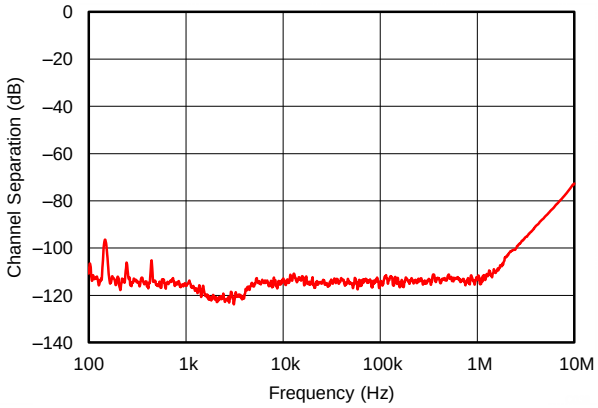


图 32. 通道分离与频率间的关系

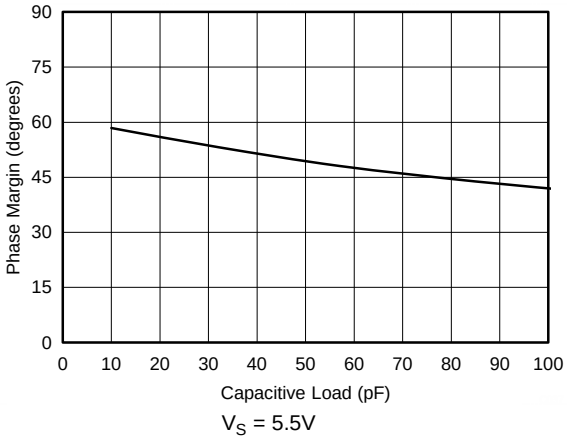


图 33. 相位裕度与容性负载间的关系

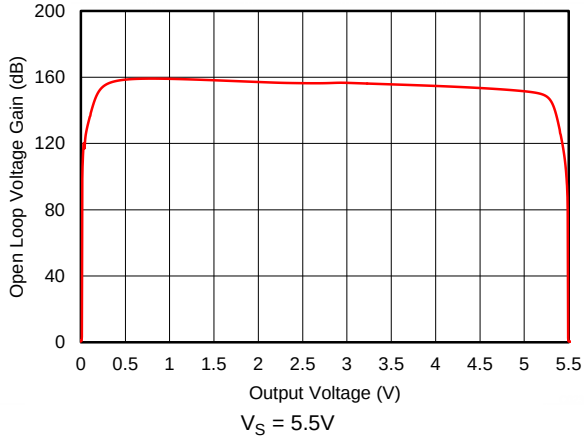


图 34. 开环电压增益与输出电压间的关系

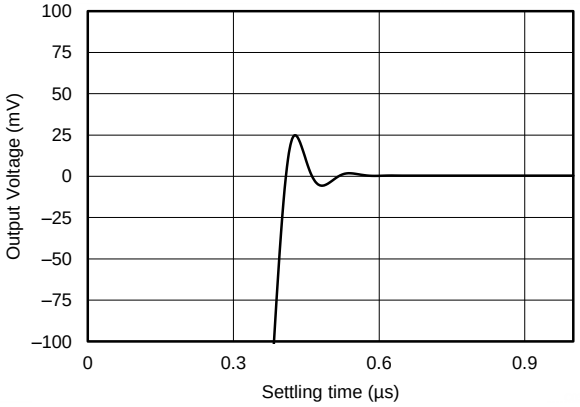


图 35. 大信号建立时间（正）

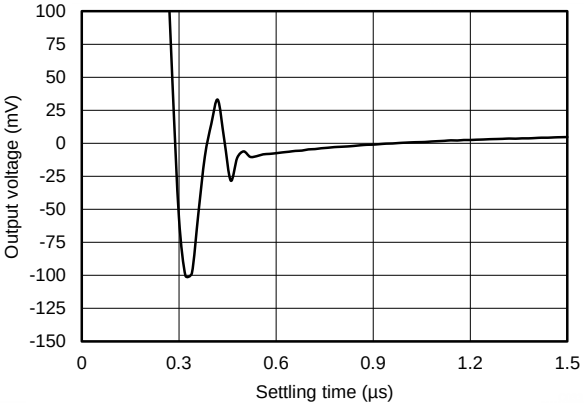


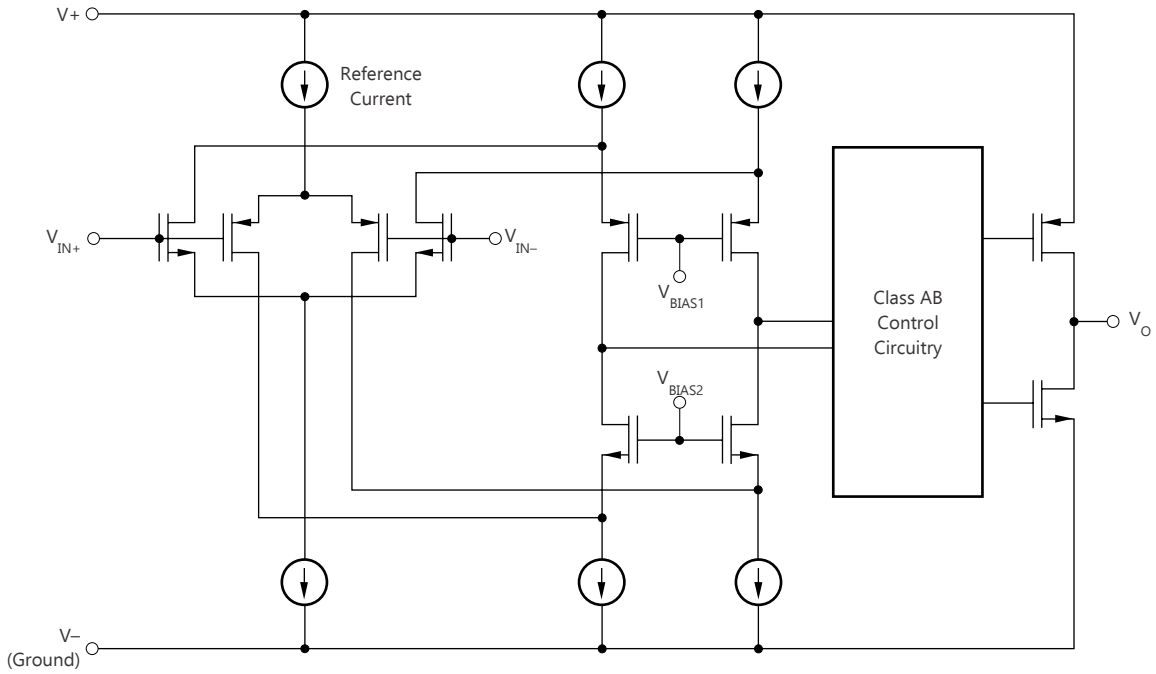
图 36. 大信号建立时间（负）

9 详细 说明

9.1 概要

TLV906x 是低功耗、轨至轨输入和输出运算放大器系列。这些器件的工作电压范围为 1.8V 至 5.5V，具有单位增益稳定特性，并且适用于各种通用 应用。输入共模电压范围包括两个电源轨，并支持将 TLV906x 系列器件用于几乎任何单电源应用。轨至轨输入和输出摆幅可大幅扩大动态范围（尤其在低电源 应用中），并且适用于驱动采样模数转换器 (ADC)。

9.2 功能框图



9.3 特性 描述

9.3.1 轨至轨输入

TLV906x 系列的输入共模电压范围相对于电源轨向外扩展了 100mV，从而支持 1.8V 至 5.5V 的完整电源电压范围。此性能由一个互补输入级实现：一个 N 沟道输入差分对和一个 P 沟道差分对并联，如*功能框图* 所示。当输入电压靠近正轨（通常在 (V+) – 1.4V 到高于正电源电压 200mV 之间）时，N 沟道对有效；而当输入在低于负电源电压 200mV 到大约 (V+) – 1.4V 之间时，P 沟道对有效。在一个通常介于 (V+) – 1.2V 到 (V+) – 1V 之间的小转换区域内，两个通道对都会打开。此 200mV 转换区域可能会随工艺不同而发生变化，最高可达 200mV。因此，此转换区域（两个级都打开）在低端上的范围介于 (V+) – 1.4V 至 (V+) – 1.2V 之间，而在高端上的范围高达 (V+) – 1V 至 (V+) – 0.8V。在此转换区域内，与器件在该区域外运行相比，PSRR、CMRR、失调电压、温漂和 THD 等性能可能会下降。

9.3.2 轨至轨输出

TLV906x 系列器件设计为一种低功耗、低电压运算放大器，可提供强大的输出驱动能力。一个具有共源晶体管的 AB 类输出级可实现完全的轨至轨输出摆幅功能。对于 10kΩ 的阻性负载，无论施加的电源电压是多少，输出摆幅都在两个电源轨的 15mV 范围内。不同的负载情况会改变放大器在靠近电源轨范围内摆动的能力。

9.3.3 过载恢复

过载恢复定义为运算放大器输出从饱和状态恢复到线性状态所需的时间。当输出电压由于高输入电压或高增益而超过额定工作电压时，运算放大器的输出器件进入饱和区。器件进入饱和区后，输出器件中的电荷载体需要时间回到线性状态。当电荷载体回到线性状态时，器件开始以指定的压摆率进行转换。因此，传播延迟（过载情况下）等于过载恢复时间与转换时间之和。TLV906x 系列器件的过载恢复时间大约为 200ns。

9.3.4 关断功能

TLV906xS 器件具有 $\overline{\text{SHDN}}$ 引脚，可禁用运算放大器，将其置于低功耗待机模式。在此模式下，运算放大器消耗的电流通常低于 1uA。$\overline{\text{SHDN}}$ 引脚为低电平有效，这意味着当 $\overline{\text{SHDN}}$ 引脚的输入为有效逻辑低电平时启用关断模式。

$\overline{\text{SHDN}}$ 引脚以运算放大器的负电源电压为基准。关断特性的阈值约为 800mV（典型值），且不随电源电压改变。开关阈值中包含了迟滞，以确保顺畅的开关特性。为了确保最佳的关断行为，应通过有效逻辑信号驱动 $\overline{\text{SHDN}}$ 引脚。有效逻辑低电平是指介于 V– 和 V– + 0.2V 之间的电压。有效逻辑高电平是指介于 V– + 1.2V 和 V+ 之间的电压。关断引脚必须连接到有效的高电压或低电压或者被驱动，而不是处于开路状态。

$\overline{\text{SHDN}}$ 引脚为高阻抗 CMOS 输入。双通道运算放大器版本是独立控制的，而四通道运算放大器版本是采用逻辑输入成对控制的。对于电池供电的 应用，这种特性可能用于大幅降低平均电流并延长电池使用寿命。所有通道全部关闭时，启用时间为 10µs；禁用时间为 3µs。禁用时，输出呈现高阻抗状态。该架构允许将 TLV906xS 作为门控放大器使用（或将器件输出复用到公共模拟输出总线上）。关断时间 (t_{OFF}) 取决于负载条件，并随负载电阻的增加而增加。为确保在特定的关断时间内关断（禁用），需要将 10kΩ 额定负载连接到中间电源 (V_S/2)。如果在没有负载的情况下使用 TLV906xS，则所需的关断时间会显著增加。

9.4 器件功能模式

TLV906x 系列可在 1.8V (±0.9V) 和 5.5V (±2.75V) 的电源电压范围内正常工作。TLV906xS 器件具有关断模式，当在关断引脚上施加有效逻辑低电平时可将器件关断。

10 应用和实现

注

以下应用部分中的 信息 不属于 TI 组件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定组件是否适用于其应用。客户应验证并测试其设计实现，以确认系统功能。

10.1 应用信息

TLV906x 系列器件 具有 10MHz 带宽和 6.5V/µs 压摆率，且每个通道仅有 538µA 的电源电流，从而在功耗极低的情况下提供良好的交流性能。在直流 应用 中也具有良好性能，其输入噪声电压极低（在 10kHz 时为 10nV/√Hz），输入偏置电流低，且典型输入失调电压为 0.3mV。

10.2 典型 应用

10.2.1 典型的低侧电流检测应用

图 37 显示了低侧电流检测应用中配置的 TLV906x。

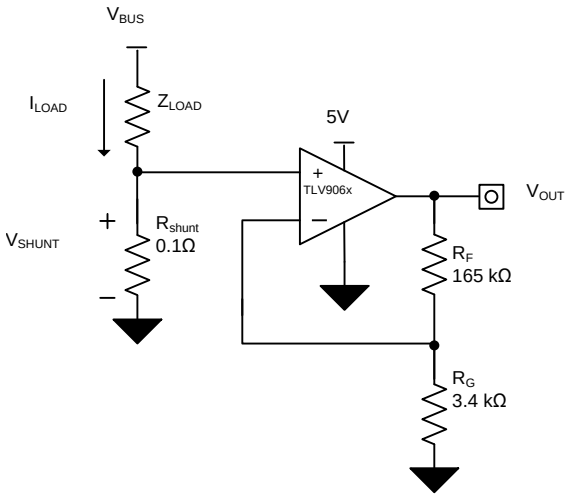


图 37. 低侧电流检测应用中的 TLV906x

10.2.1.1 设计要求

此设计的设计要求如下：

- 负载电流：0A 至 1A
- 输出电压：4.95V
- 最大分流电压：100mV

典型 应用 (接下页)

10.2.1.2 详细设计流程

图 37 中的传递函数如公式 1 所示

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

负载电流 (I_{LOAD}) 在分流电阻器 (R_{SHUNT}) 上产生压降。负载电流设置为 0A 至 1A。为了在最大负载电流下保持分流电压低于 100mV，公式 2 中定义了最大分流电阻。

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

根据公式 2 可知，R_{SHUNT} 等于 100mΩ。I_{LOAD} 和 R_{SHUNT} 产生的压降由 TLV906x 放大，从而产生大约 0V 至 4.95V 的输出电压。根据公式 3 可计算 TLV906x 产生所需输出电压需要的增益。

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \quad (3)$$

根据公式 3 计算出的所需增益等于 49.5V/V，通过 R_F 和 R_G 电阻器进行设置。公式 4 可确定 R_F 和 R_G 电阻器的大小，从而将 TLV906x 的增益设置为 49.5V/V。

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \quad (4)$$

当 R_F 选定为 165kΩ 而 R_G 选定为 3.4kΩ 时，可获得大约 49.5V/V 的增益。图 38 显示了图 37 所示电路的测量传递函数。

10.2.1.3 应用曲线

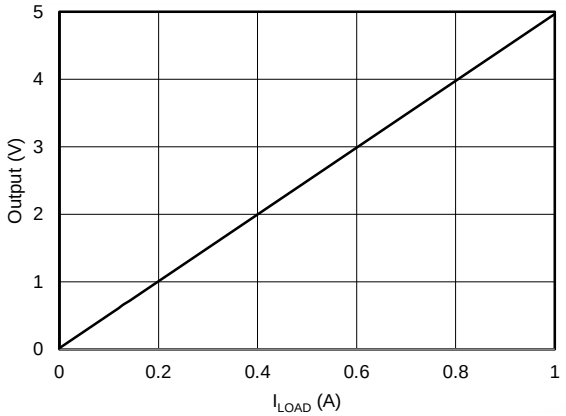


图 38. 低侧电流检测传递函数

典型 应用 (接下页)

10.2.2 比较器典型应用

比较器用于区分两种不同的信号电平。例如，比较器可用于区分过压情况和正常运行状态。TLV9062 可作为比较器使用，方法是将待比较的两个电压施加到相应的每个输入，从输出到反相输入无任何反馈。

TLV9062 具有 一个轨至轨输入和输出级，其输入共模范围超出电源轨 100mV。TLV9062 适用于在整个输入共模范围内防止相位反转。用作比较器的 TLV9062 的传播延迟等于过载恢复时间与压摆率之和。过驱动电压低于 100mV 将导致传播延迟延长，因为过载恢复时间将增加，而压摆率将降低。

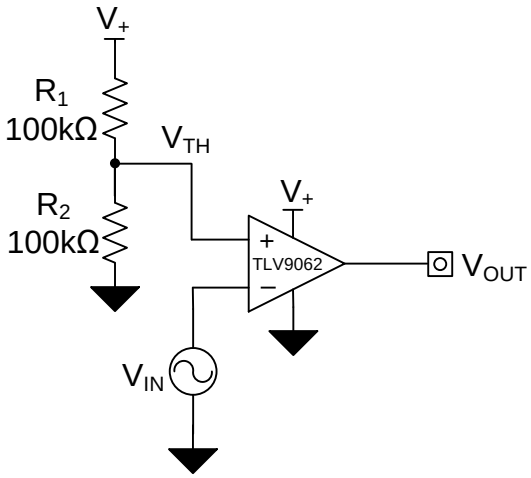


图 39. 比较器典型应用

10.2.2.1 设计要求

此设计的设计要求如下：

- 电源电压 (V_+)：5V
- 输入电压 (V_{IN})：0 – 5V
- 阈值电压 (V_{TH}) = 2.5V

10.2.2.2 详细设计流程

反相比较器电路在运算放大器的反相端施加输入电压 (V_{IN})。两个电阻器（R1 和 R2）分摊输入电压 (V_{CC}) 以建立中间阈值电压 (V_{TH})（根据公式 1 计算得出）。具体电路如图 39 所示。当 V_{IN} 低于 V_{TH} 时，输出电压将切换到正电源，并等于高电平输出电压。当 V_{IN} 高于 V_{TH} 时，输出电压将切换为负电源，并等于低电平输出电压。V_{TH}。

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_+ = 2.5V \tag{5}$$

典型 应用 (接下页)

10.2.2.3 应用曲线

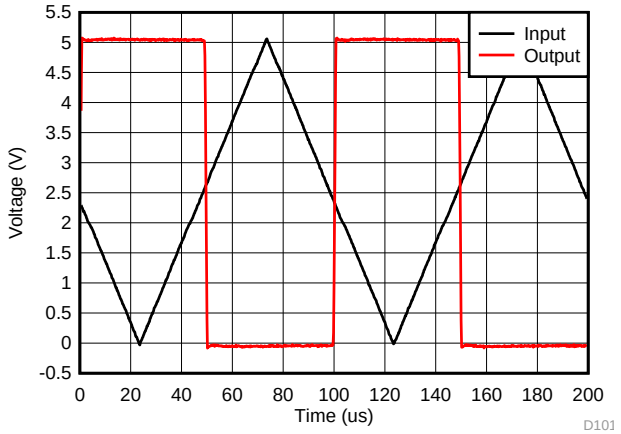


图 40. 比较器对输入电压的响应（包括传播延迟）

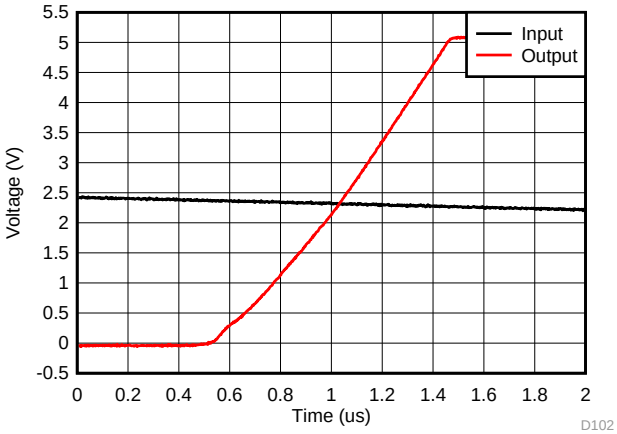


图 41. 上升沿

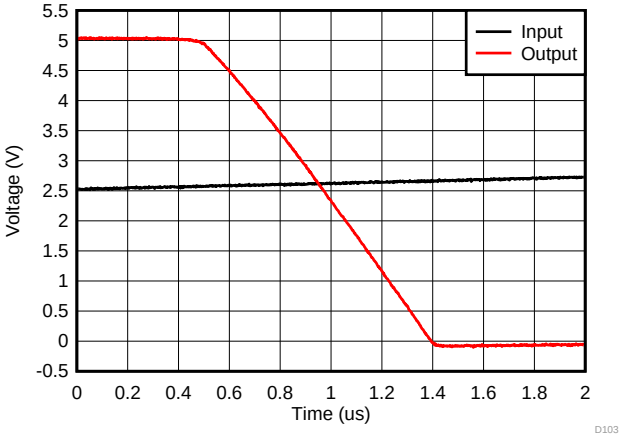


图 42. 下降沿

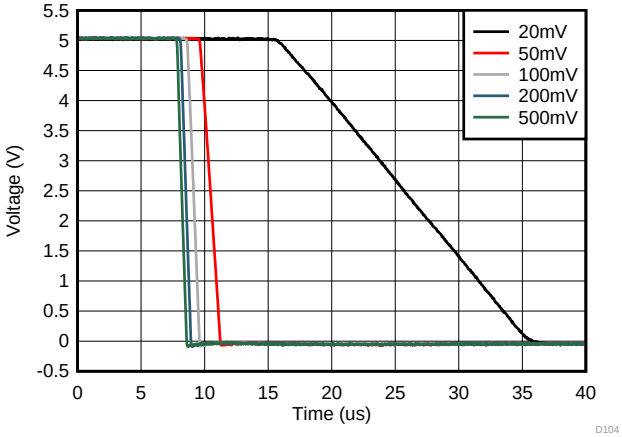


图 43. 下降沿传播延迟与输入过驱电压间的关系

11 电源建议

TLV906x 系列器件的额定工作电压范围是 1.8V 至 5.5V（±0.9V 至 ±2.75V）；许多规格在 –40°C 至 +125°C 的温度下适用。*典型特性* 部分提供的参数可能随工作电压或温度的变化而出现显著变化。

CAUTION

电源电压超过 6V 可能会对器件造成永久损坏；请参阅*绝对最大额定值* 表。

将 0.1µF 旁路电容器置于电源引脚附近，以减小从高噪声电源或高阻抗电源中耦合进来的误差。有关旁路电容器位置的更多详细信息，请参阅 部分。

11.1 输入和 ESD 保护

TLV906x 系列器件在所有引脚上均整合了内部 ESD 保护电路。对于输入和输出引脚，这种保护主要包括输入和电源引脚之间连接的导流二极管。如*绝对最大额定值* 表所示，只要电流不超过 10mA，这些 ESD 保护二极管就能提供电路内输入过驱保护。图 44 显示了如何通过将串联输入电阻器添加到被驱动的输入端来限制输入电流。添加的电阻器会增加放大器输入端的热噪声；在对噪声敏感的应用中，该值必须保持在最低　值中，该值必须保持在最低值。

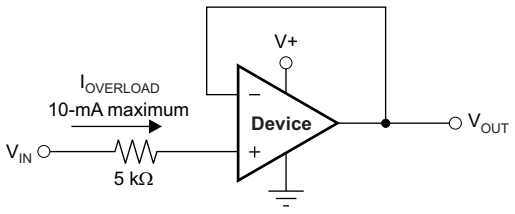


图 44. 输入电流保护

12 布局

12.1 布局指南

为了实现器件的最佳运行性能，应使用良好的印刷电路板 (PCB) 布局规范，包括：

- 噪声可以通过整个电路的电源引脚和运算放大器本身的电源引脚传入模拟电路。旁路电容为局部模拟电路提供低阻抗电源，用于降低耦合噪声。
  - 在每个电源引脚和接地端之间连接低 ESR 0.1μF 陶瓷旁路电容器，放置位置尽量靠近器件。从 V+ 到接地端的单个旁路电容器适用于单通道电源 应用。
- 将电路的模拟和数字部分单独接地是最简单和最有效的噪声抑制方法之一。多层 PCB 中通常将一层或多层专门作为接地层。接地层有助于散热和降低电磁干扰 (EMI) 噪声拾取。请小心地对数字接地和模拟接地进行物理隔离，同时应注意接地电流。有关更多详细信息，请参阅*《电路板布局技巧》*。
- 为降低寄生耦合，输入迹线应尽量远离电源或输出迹线。如果这些走线不能保持分离，则敏感走线与有噪声走线垂直相交比平行更好。
- 外部组件的位置应尽量靠近器件。如图 46 所示，使 RF 和 RG 接近反相输入可最大限度地减小反相输入端的寄生电容。
- 尽可能缩短输入迹线。切记：输入走线是电路中最敏感的部分。
- 考虑在关键走线周围设定驱动型低阻抗保护环。这样可显著减少附近走线在不同电势下产生的泄漏电流。
- 为获得最佳性能，建议在组装 PCB 板后进行清洗。
- 任何精密集成电路都可能因湿气渗入塑料封装中而出现性能变化。请遵循所有的 PCB 水清洁流程，建议将 PCB 组装烘干，以去除清洗时渗入器件封装中的湿气。大多数情形下，清洗后在 85°C 下低温烘干 30 分钟即可。

12.2 布局示例

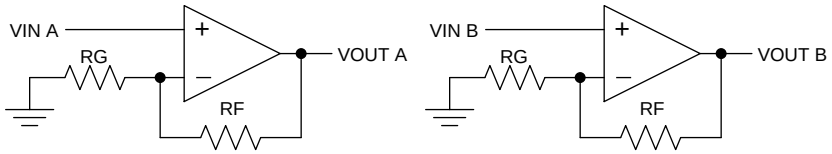


图 45. 图 46 的原理图表示

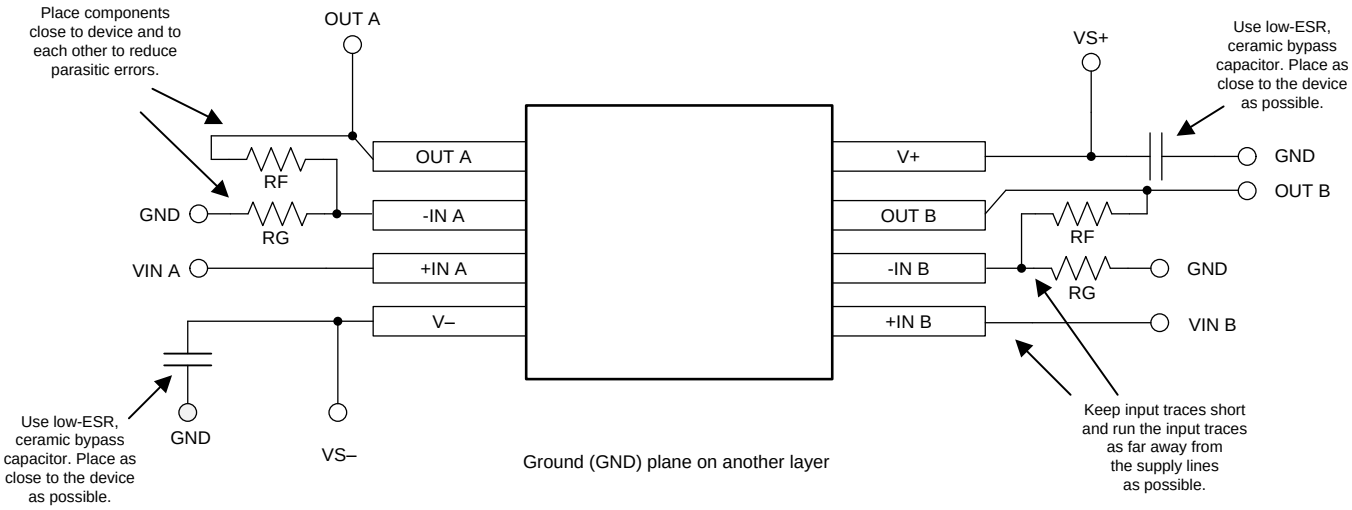


图 46. 布局示例

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

德州仪器 (TI)，*《适用于成本敏感型系统的 TLVx313 低功耗、轨至轨输入/输出、500μV 典型失调电压、1MHz 运算放大器》*。

德州仪器 (TI)，*《TLVx314 3MHz、低功耗、内置 EMI 滤波器、RRIO 运算放大器》*。

德州仪器 (TI)，*《运算放大器的 EMI 抑制比》*。

德州仪器 (TI)，*《QFN/SON PCB 连接》*。

Texas Instruments, *《四方扁平封装无引线逻辑封装》*。

德州仪器 (TI)，*《电路板布局技巧》*。

德州仪器 (TI)，*《单端输入至差分输出转换电路参考设计》*。

13.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **1.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TLV9061	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV9062S	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV9062	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV9064	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV9064S	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

13.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9061IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OAF	Samples
TLV9061IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	1CA	Samples
TLV9061IDPWR	ACTIVE	X2SON	DPW	5	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	CG	Samples
TLV9061SIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OEF	Samples
TLV9062IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062	Samples
TLV9062IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T062	Samples
TLV9062IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T062	Samples
TLV9062IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	TL9062	Samples
TLV9062IDSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T062	Samples
TLV9062IDSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T062	Samples
TLV9062IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	TL9062	Samples
TLV9062SIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1TDX	Samples
TLV9062SIRUGR	ACTIVE	X2QFN	RUG	10	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	EOF	Samples
TLV9064IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9064D	Samples
TLV9064IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	TLV9064	Samples
TLV9064IPWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	TLV9064	Samples
TLV9064IRTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9064	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9064IRUCR	ACTIVE	QFN	RUC	14	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1DD	Samples
TLV9064SIRTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9064S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

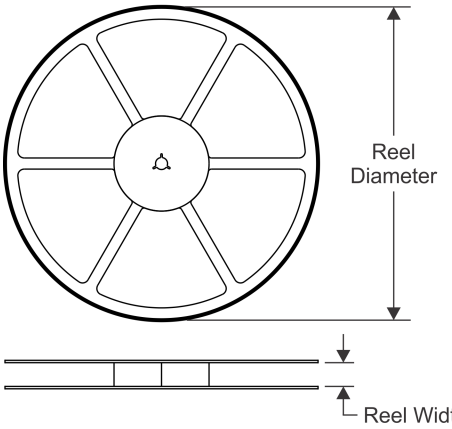
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

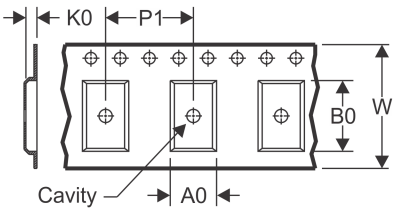
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

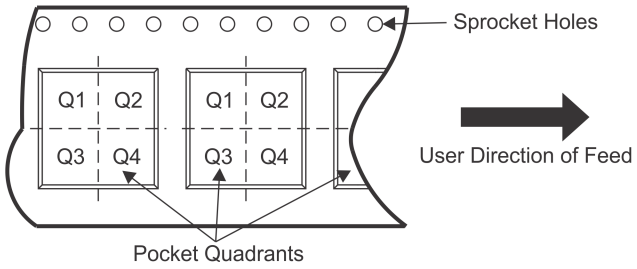


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

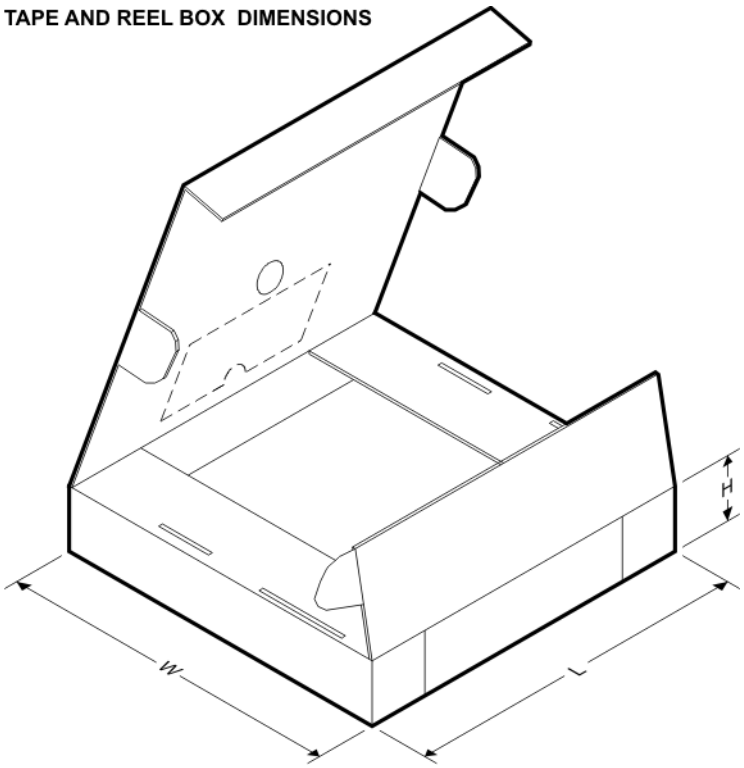


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9061IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9061IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9061IDPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV9061SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9062IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9062IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9062IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9062IDR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9062IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9062IDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9062IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9062SIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9062SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1
TLV9064IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9064IDR	SOIC	D	14	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9064IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9064IPWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9064IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV9064IRUCR	QFN	RUC	14	3000	180.0	9.5	2.16	2.16	0.5	4.0	8.0	Q2
TLV9064SIRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

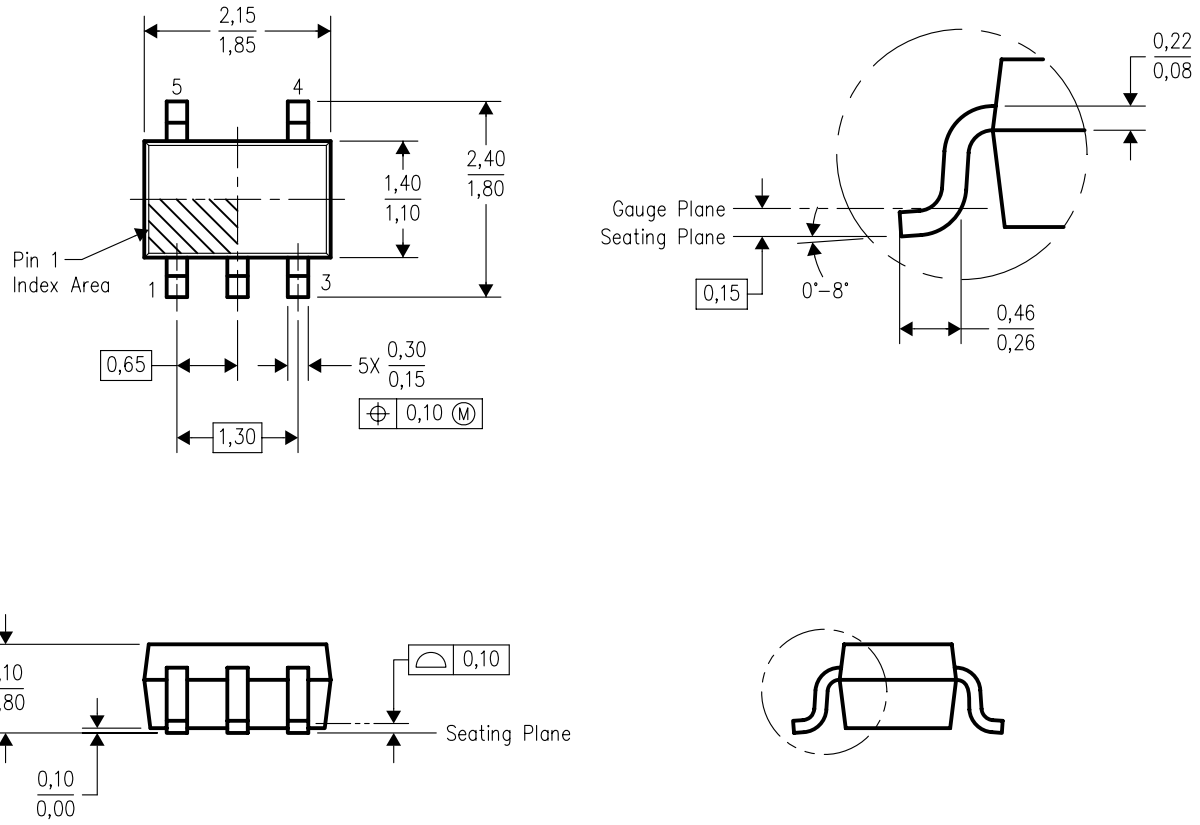


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9061IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9061IDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV9061IDPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV9061SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9062IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9062IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9062IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TLV9062IDR	SOIC	D	8	2500	336.6	336.6	41.3
TLV9062IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9062IDSGT	WSON	DSG	8	250	210.0	185.0	35.0
TLV9062IPWR	TSSOP	PW	8	2000	366.0	364.0	50.0
TLV9062SIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TLV9062SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0
TLV9064IDR	SOIC	D	14	2500	367.0	367.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9064IDR	SOIC	D	14	2500	336.6	336.6	41.3
TLV9064IPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
TLV9064IPWT	TSSOP	PW	14	250	366.0	364.0	50.0
TLV9064IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TLV9064IRUCR	QFN	RUC	14	3000	205.0	200.0	30.0
TLV9064SIRTER	WQFN	RTE	16	3000	367.0	367.0	35.0

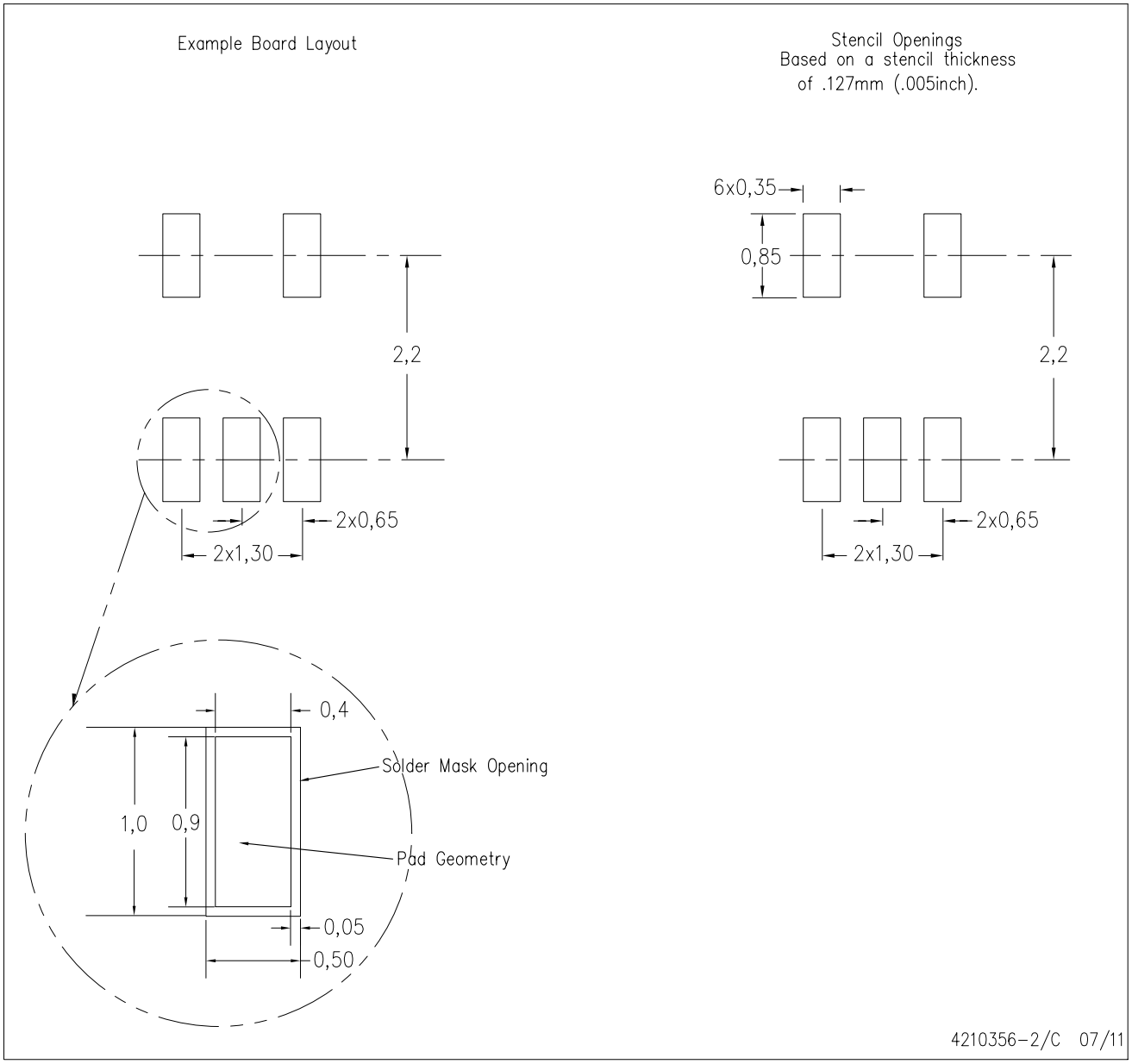
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



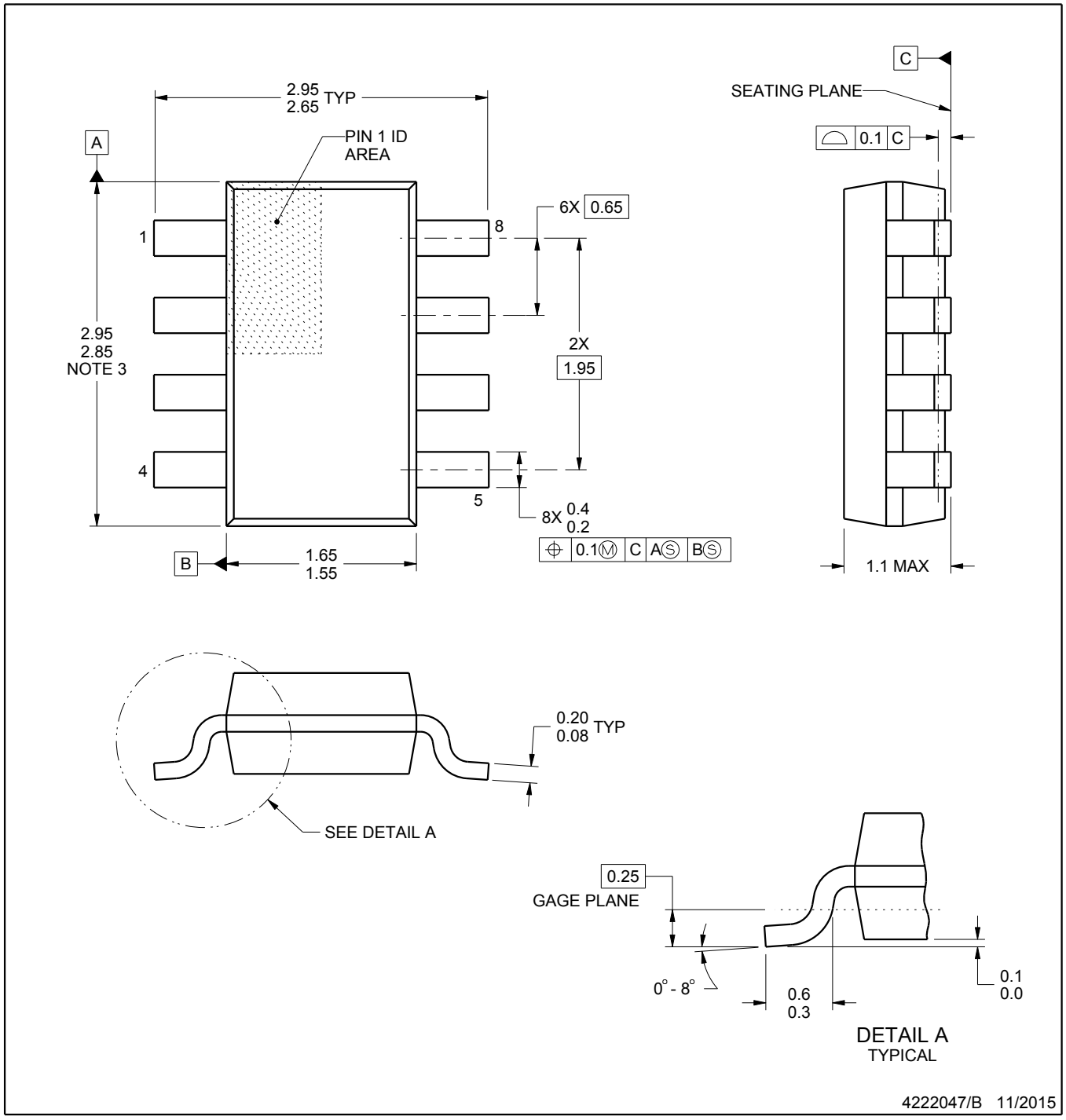
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DDF0008A

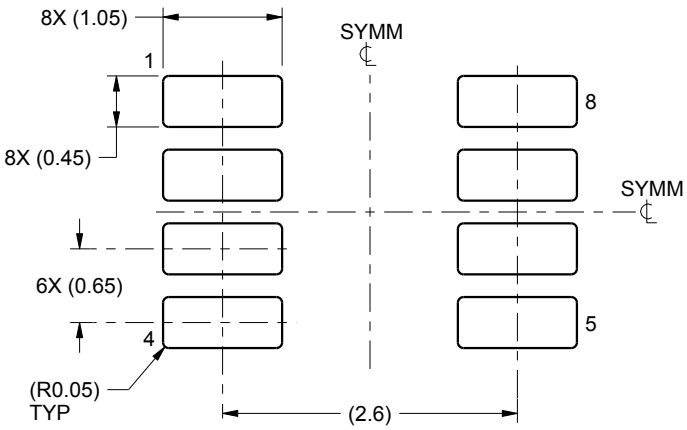
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

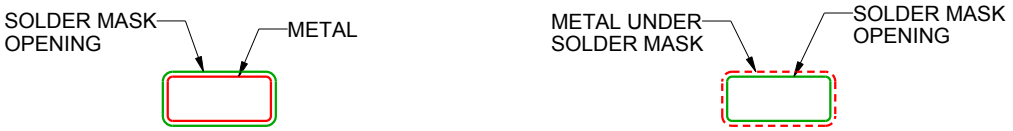


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

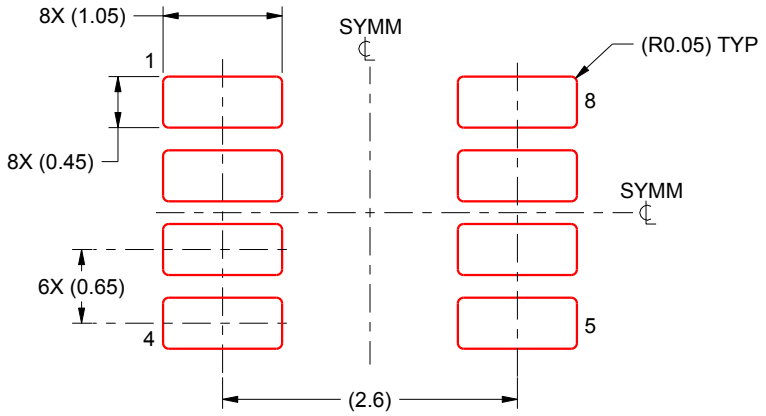
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



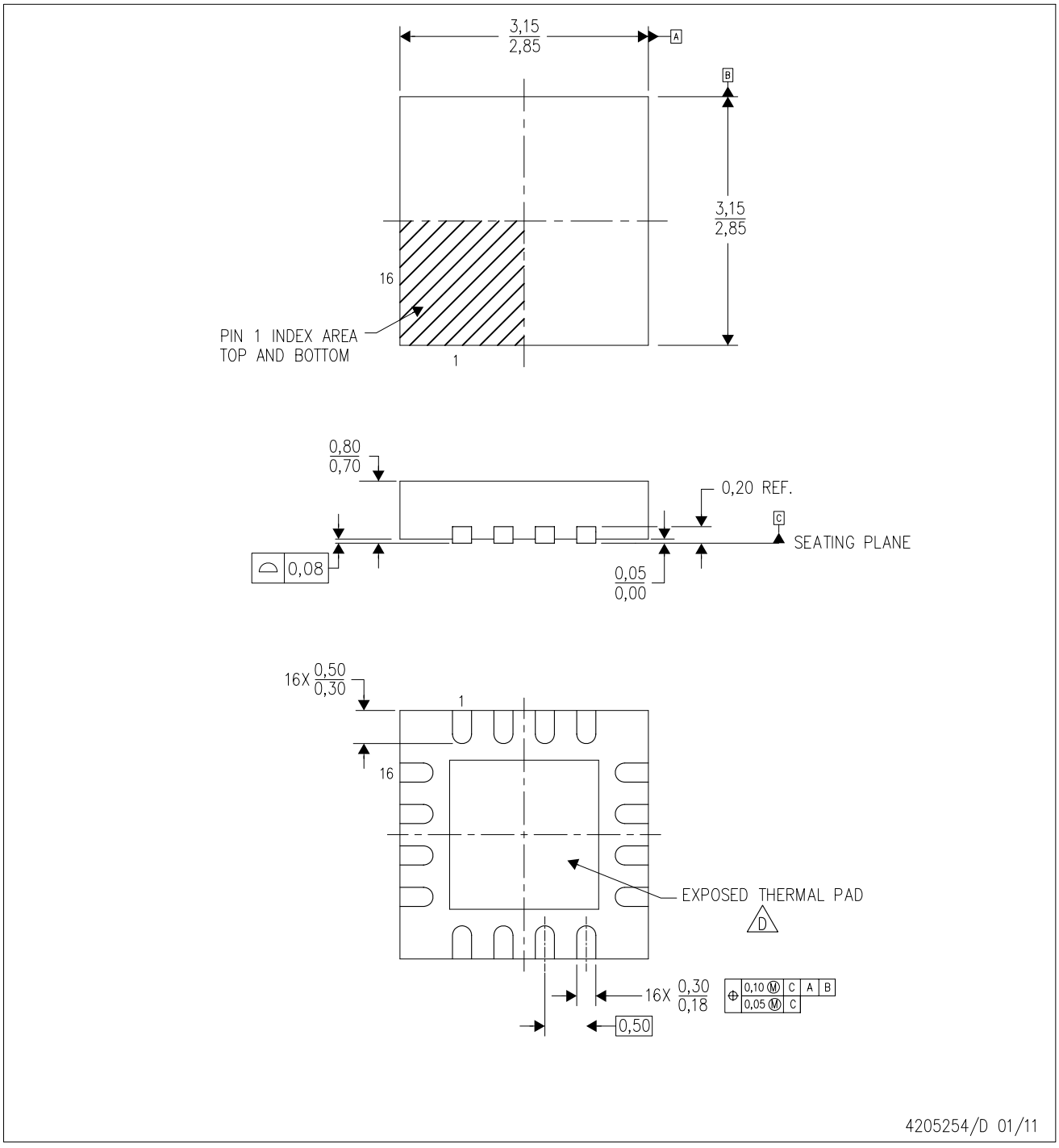
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

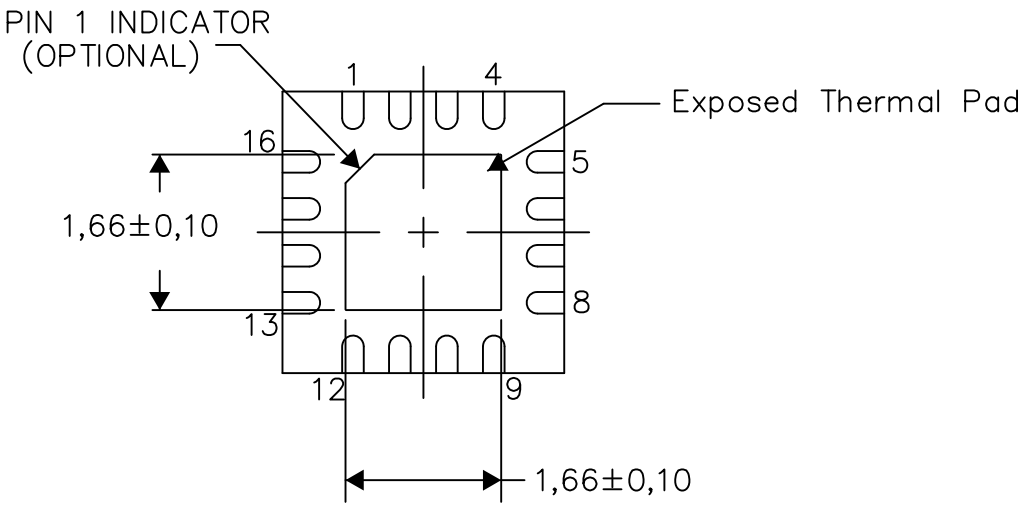
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



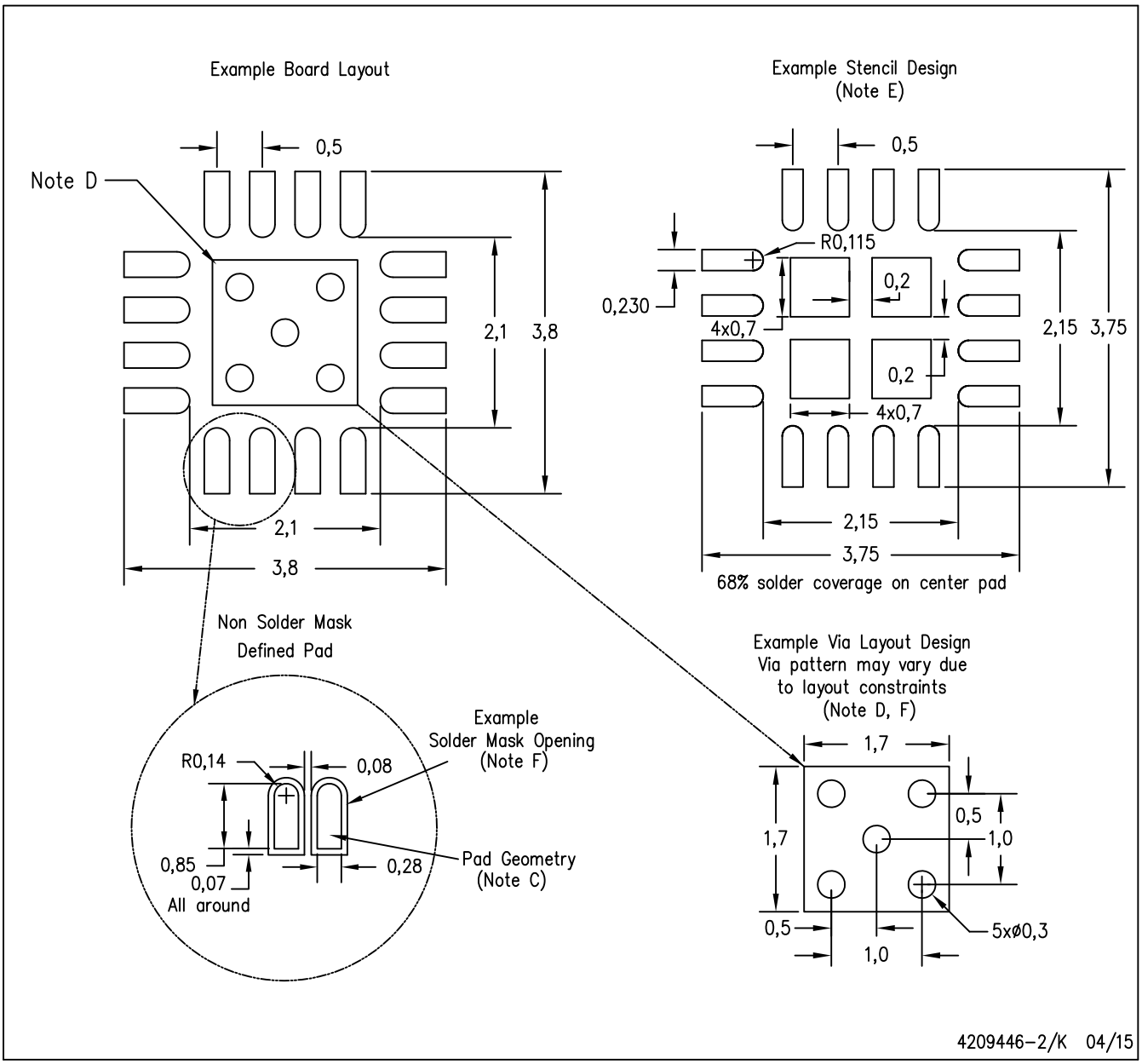
Bottom View

Exposed Thermal Pad Dimensions

4206446–8/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



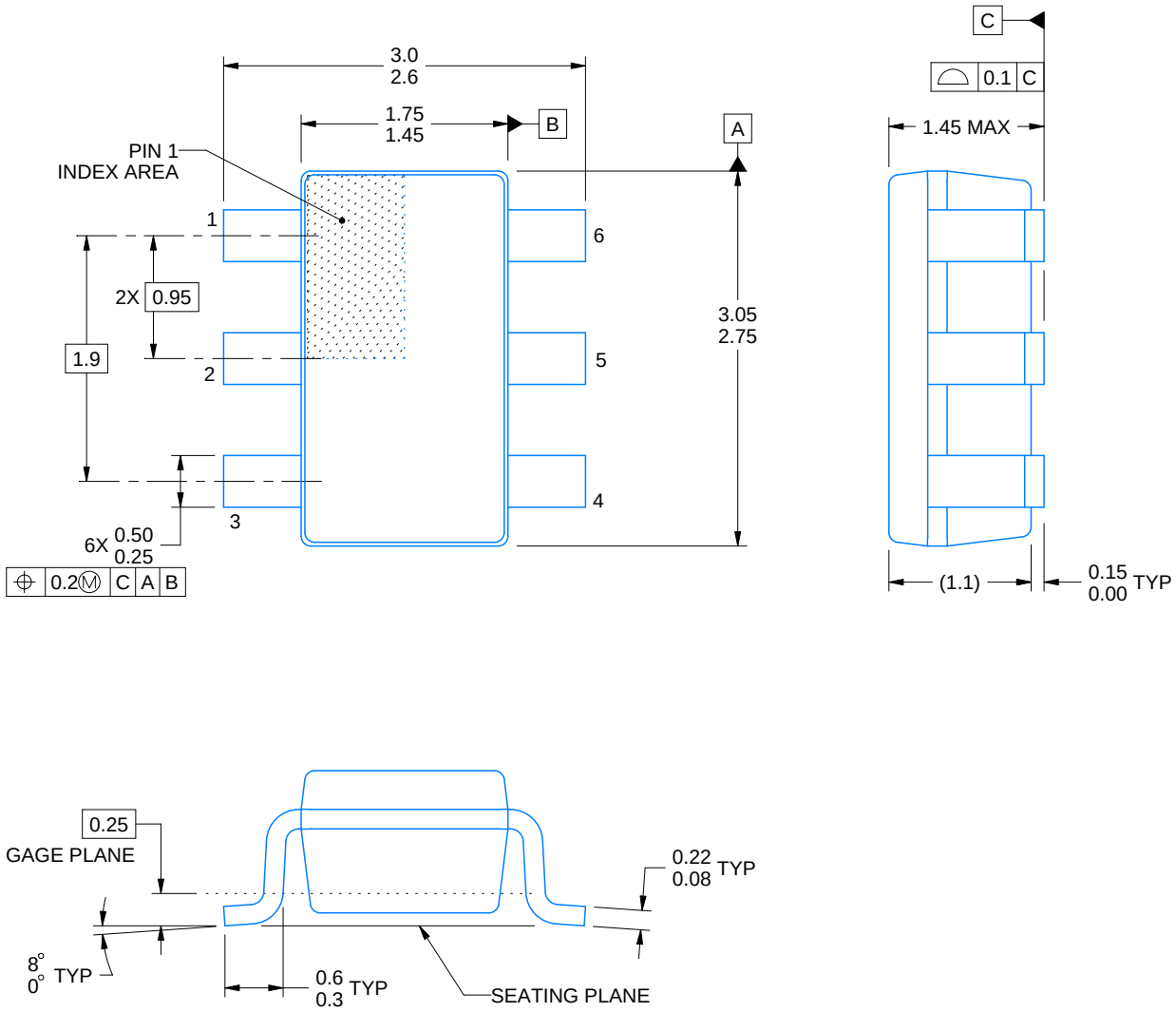
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

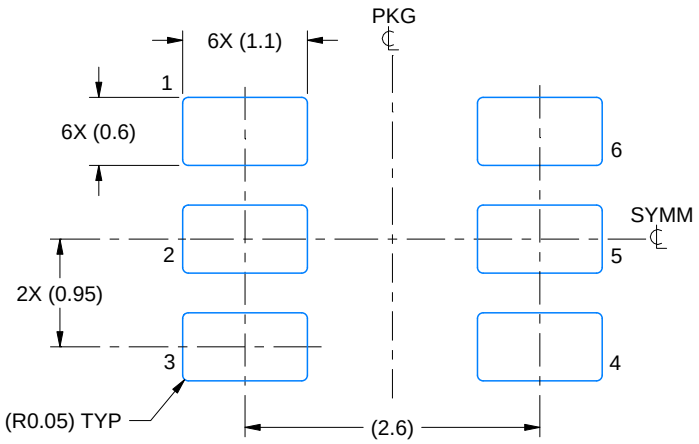
SMALL OUTLINE TRANSISTOR



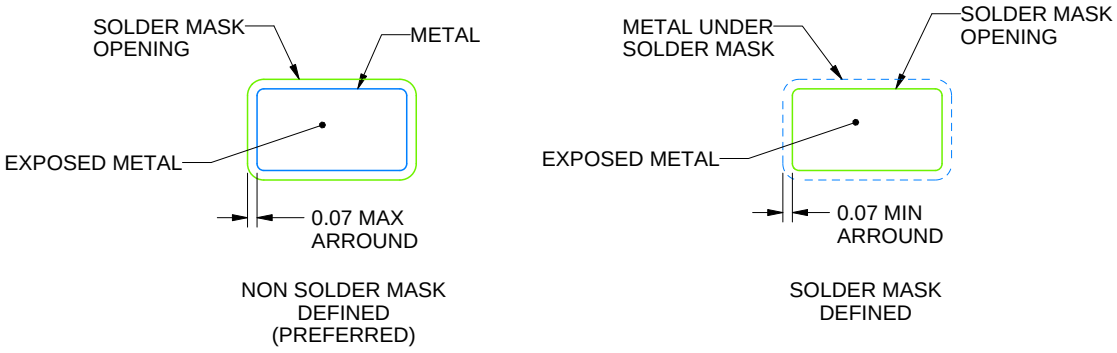
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

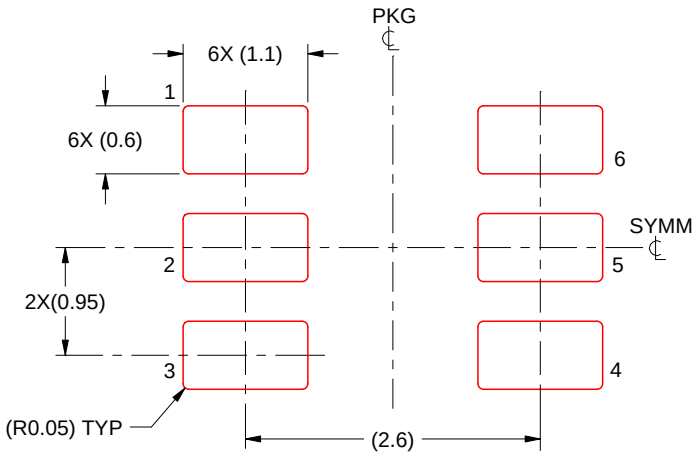


SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

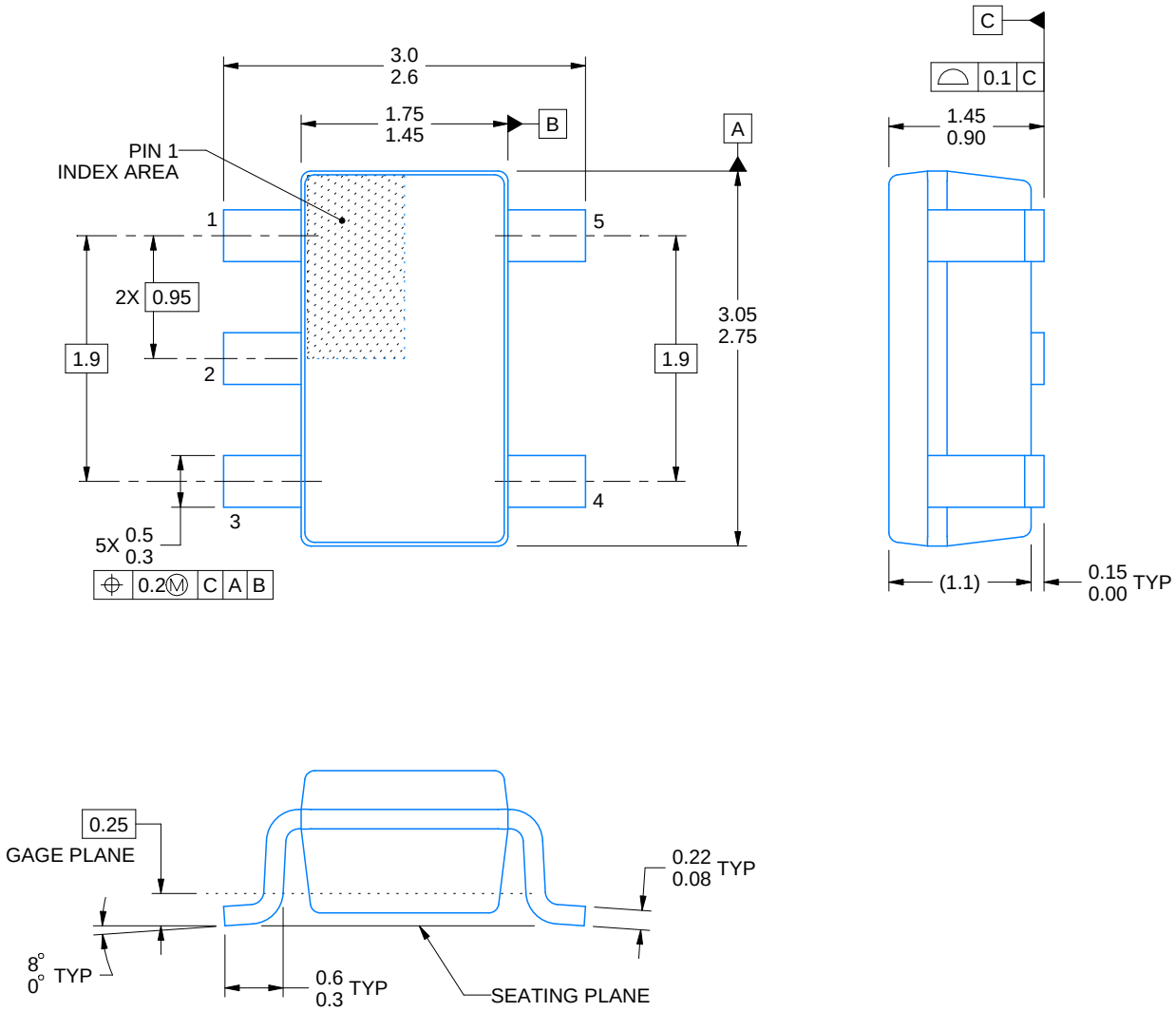
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

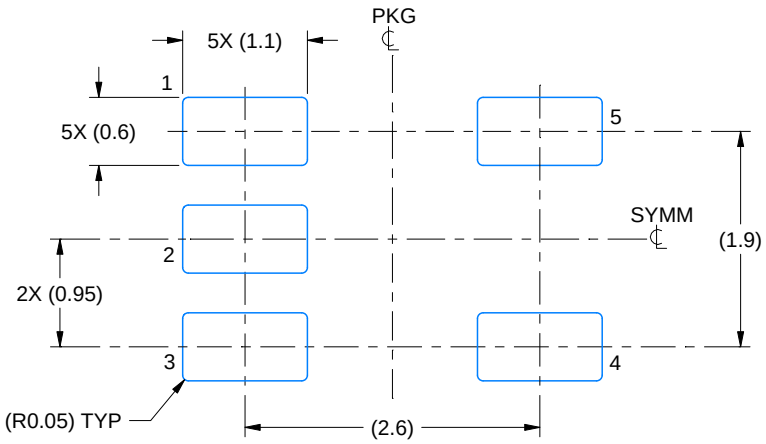
SMALL OUTLINE TRANSISTOR



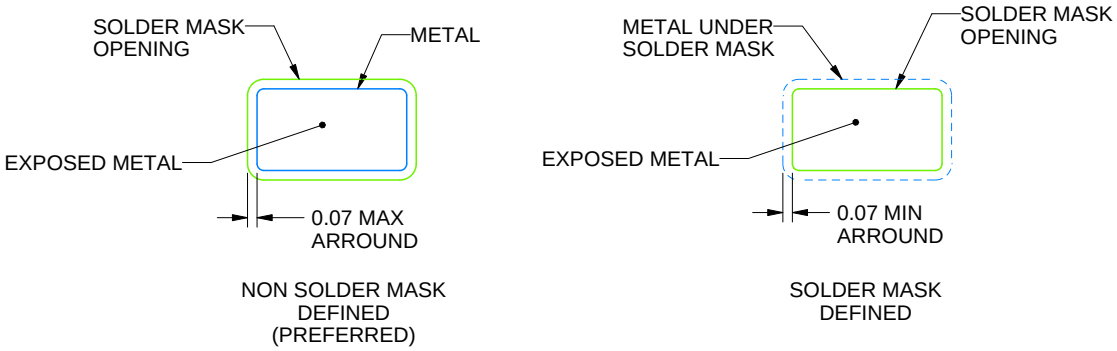
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

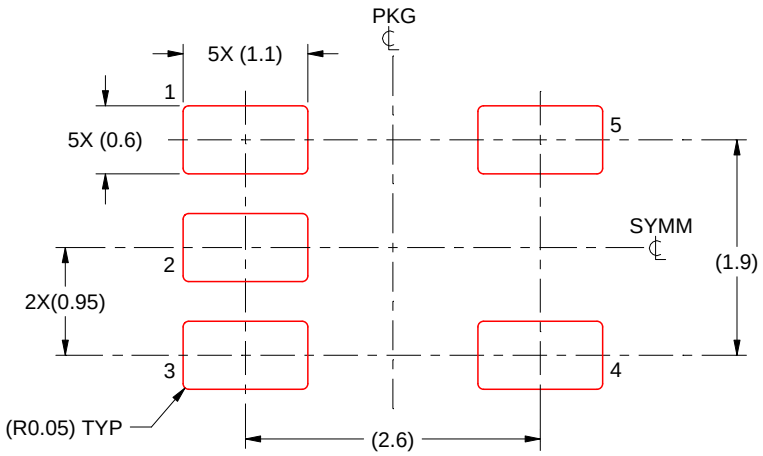


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

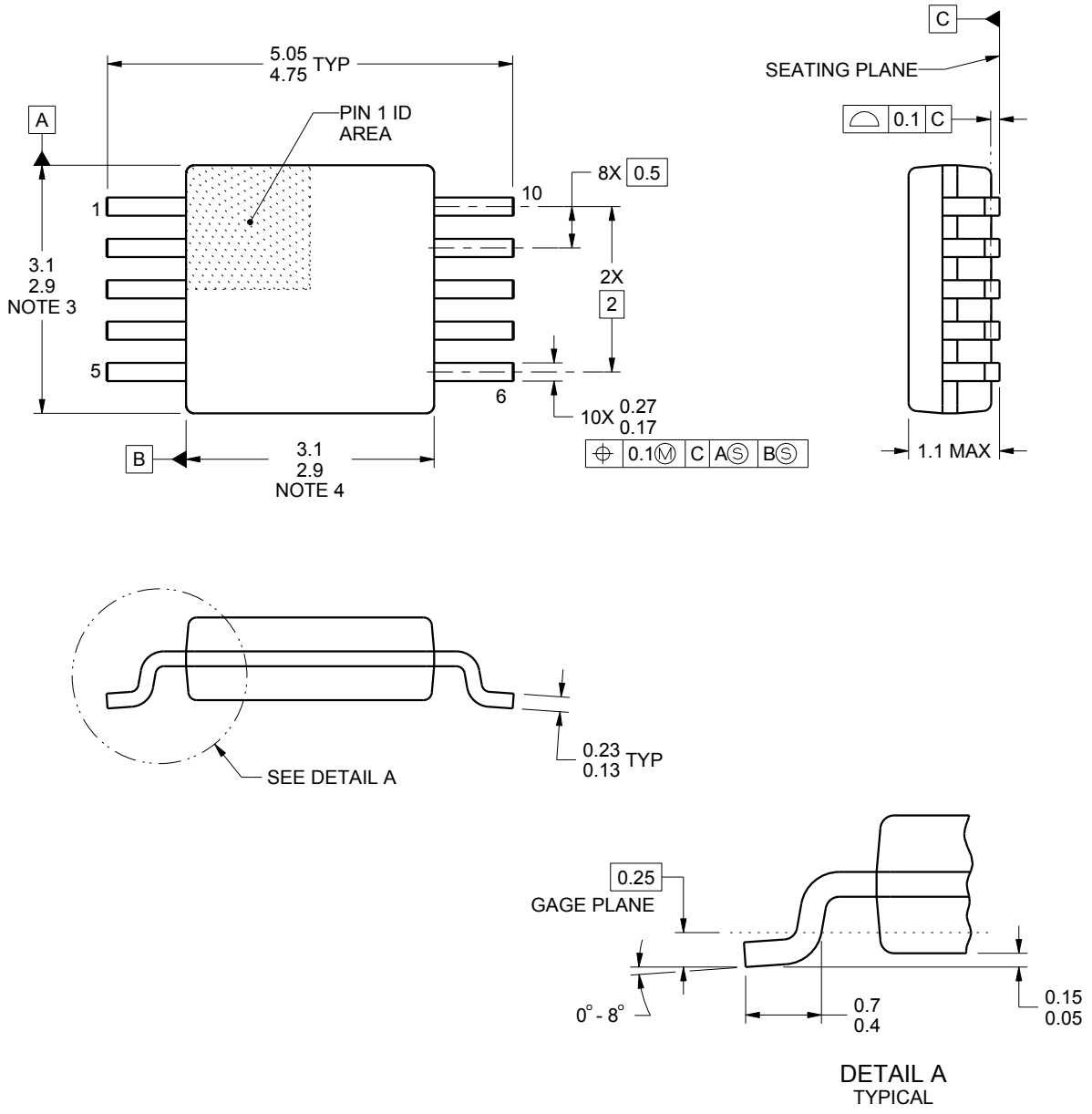
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0010A

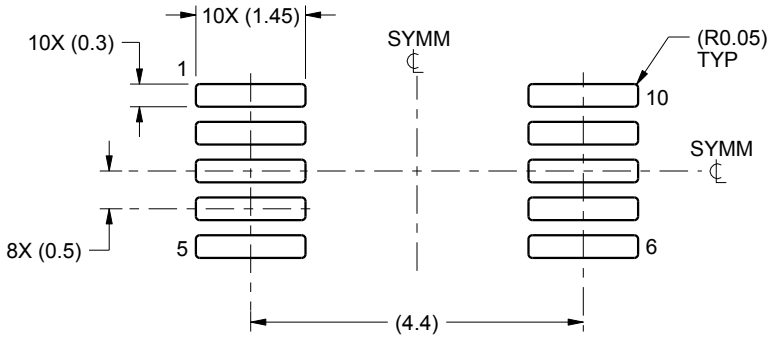
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

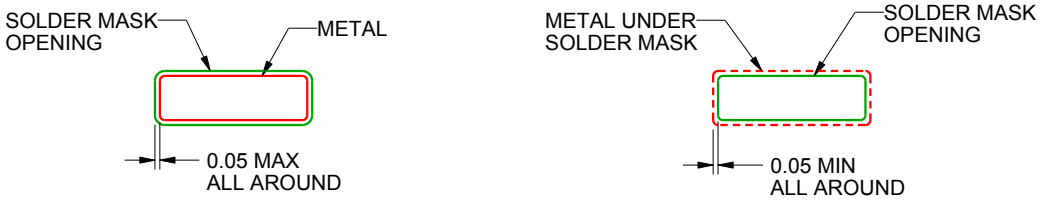


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

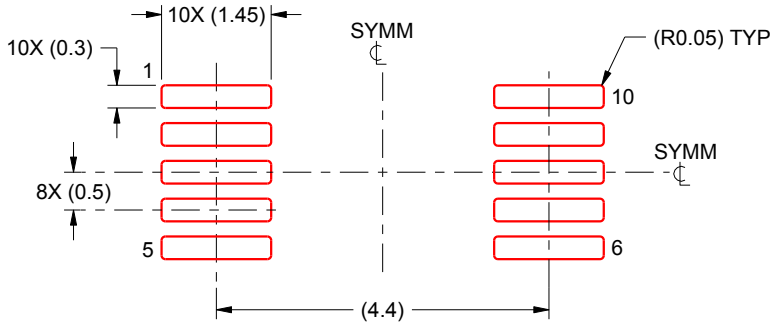


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

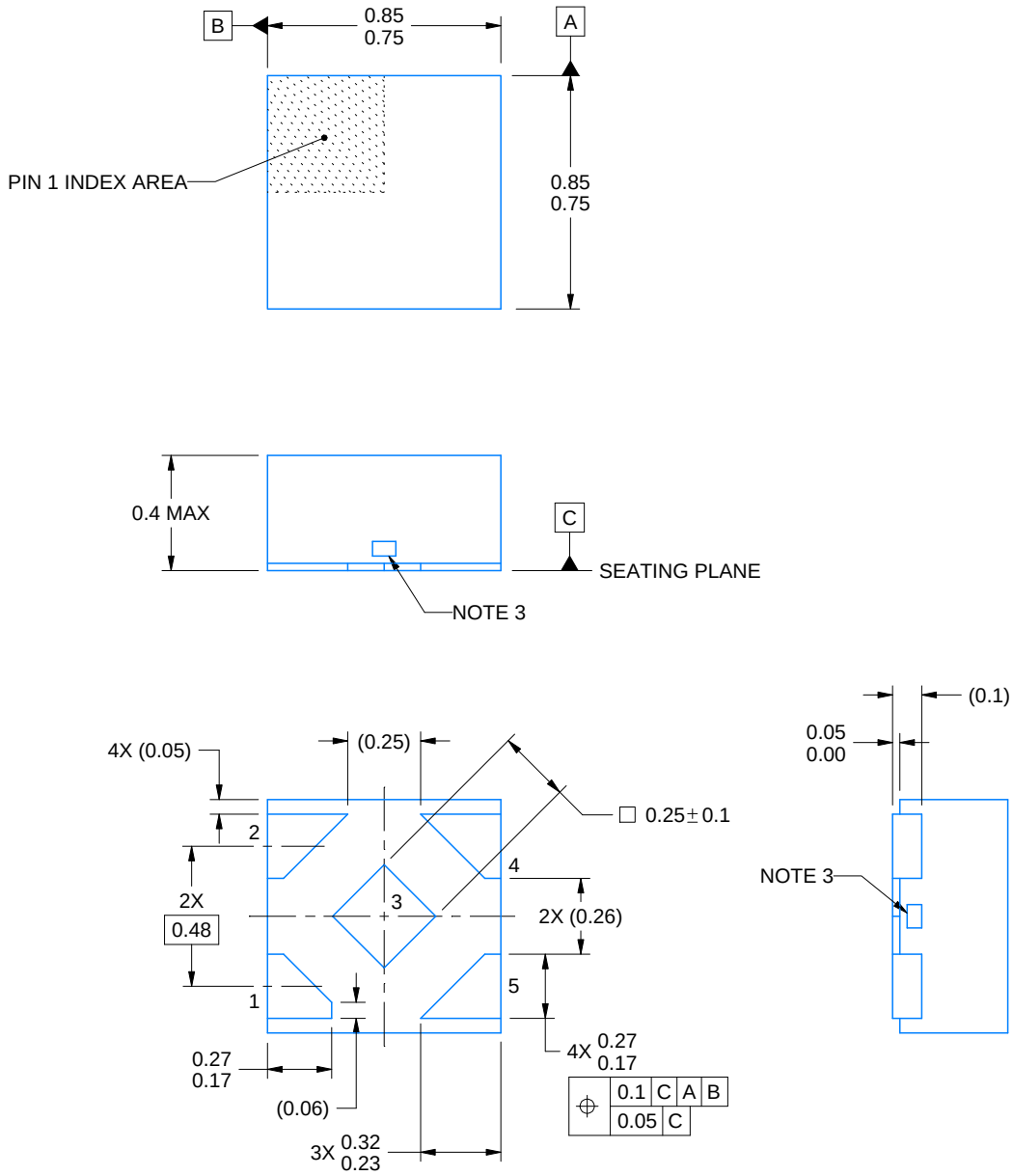
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

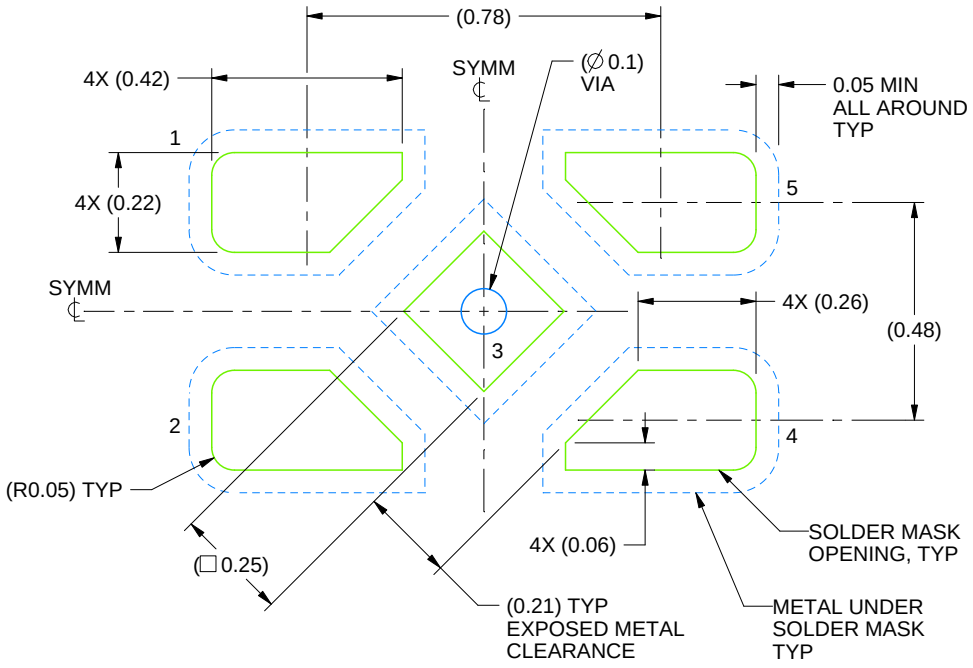
PLASTIC SMALL OUTLINE - NO LEAD



4223102/B 09/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

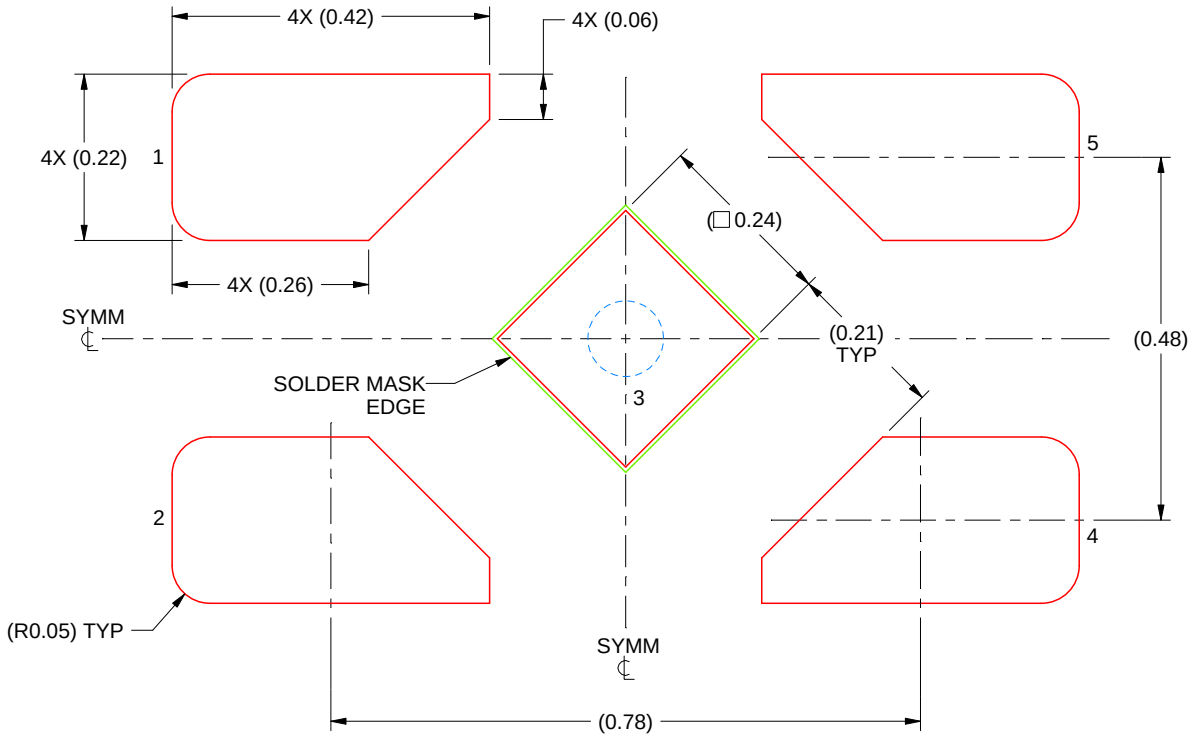


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/B 09/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

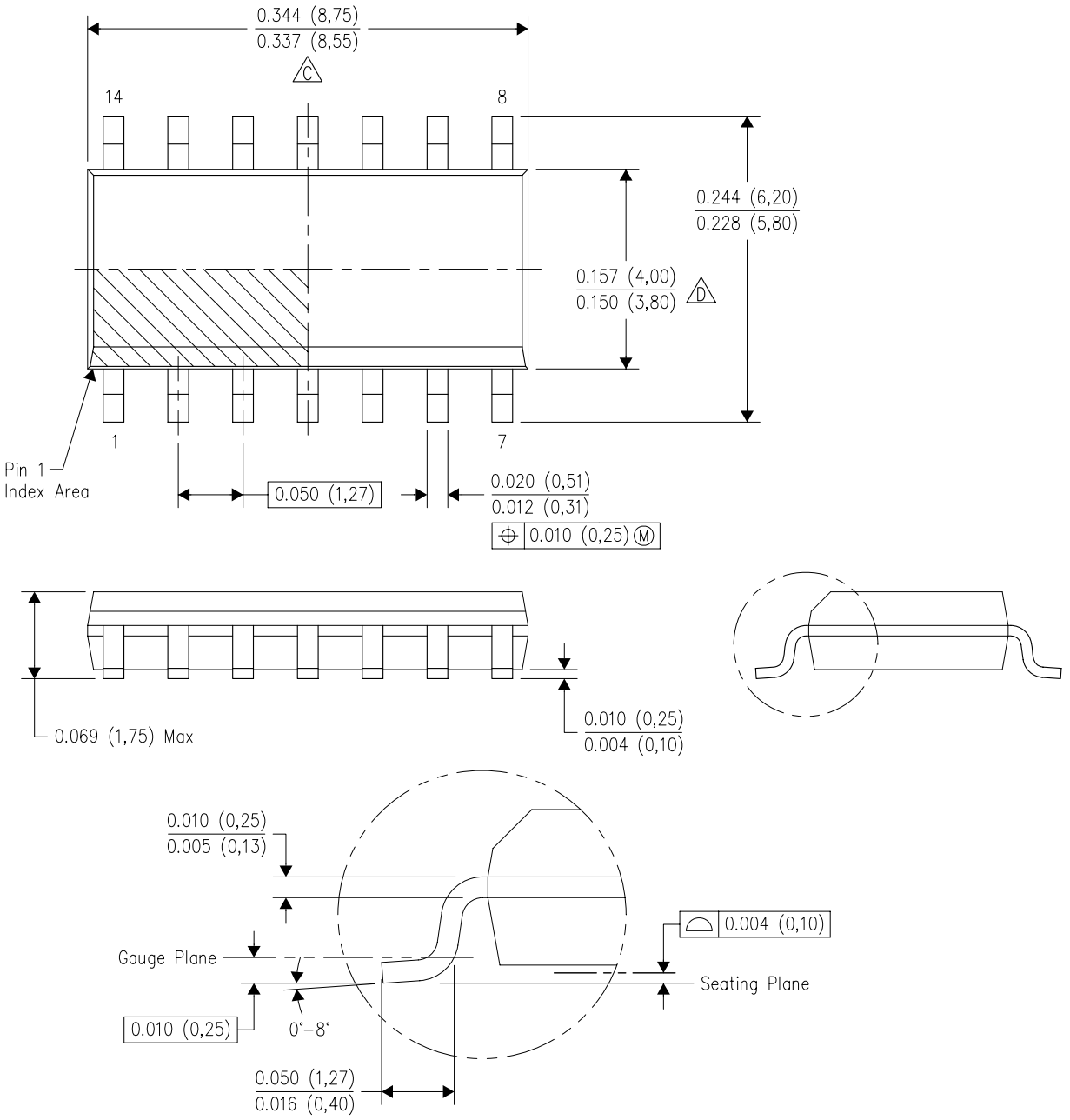
EXPOSED PAD
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

4223102/B 09/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

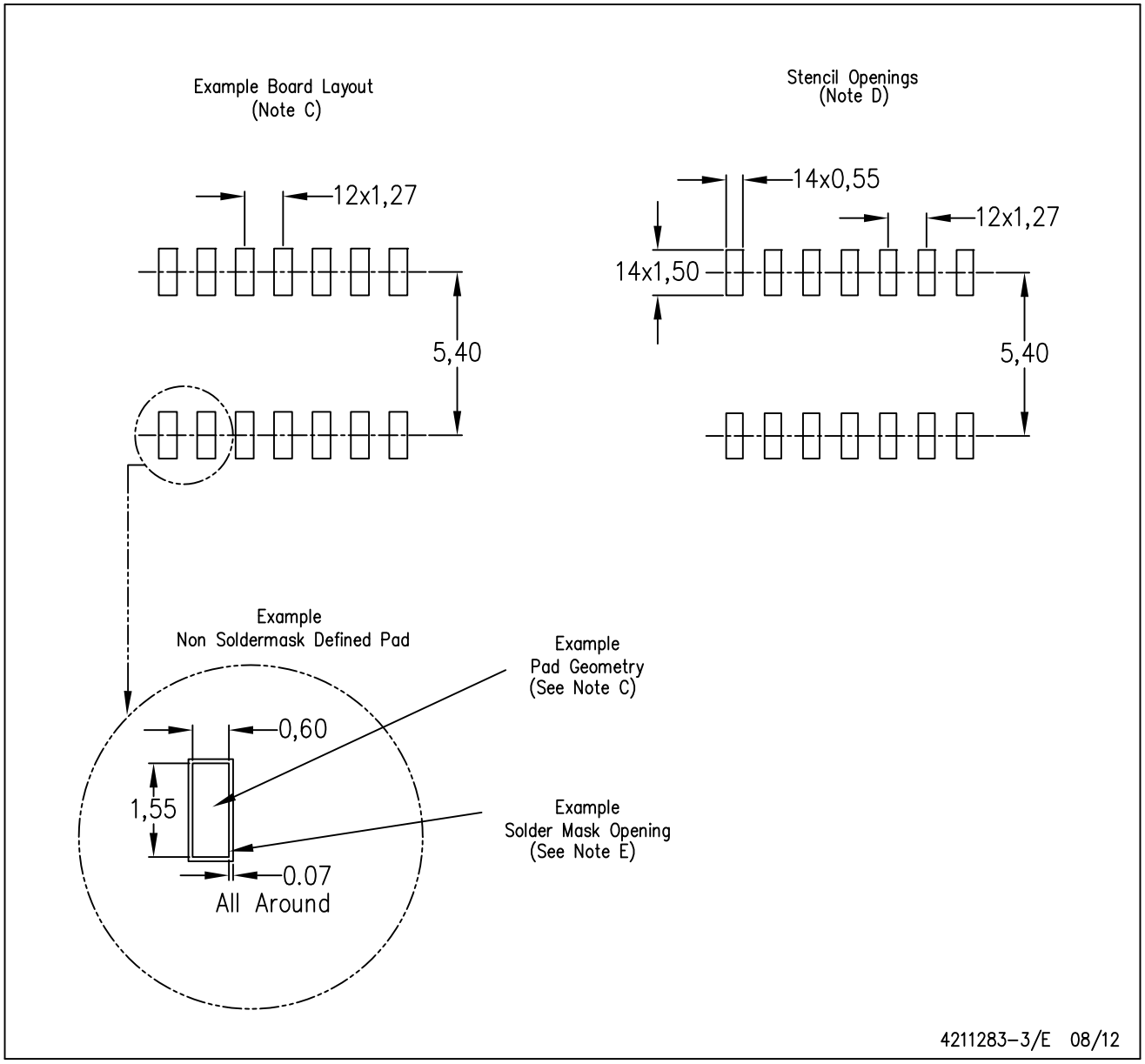
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

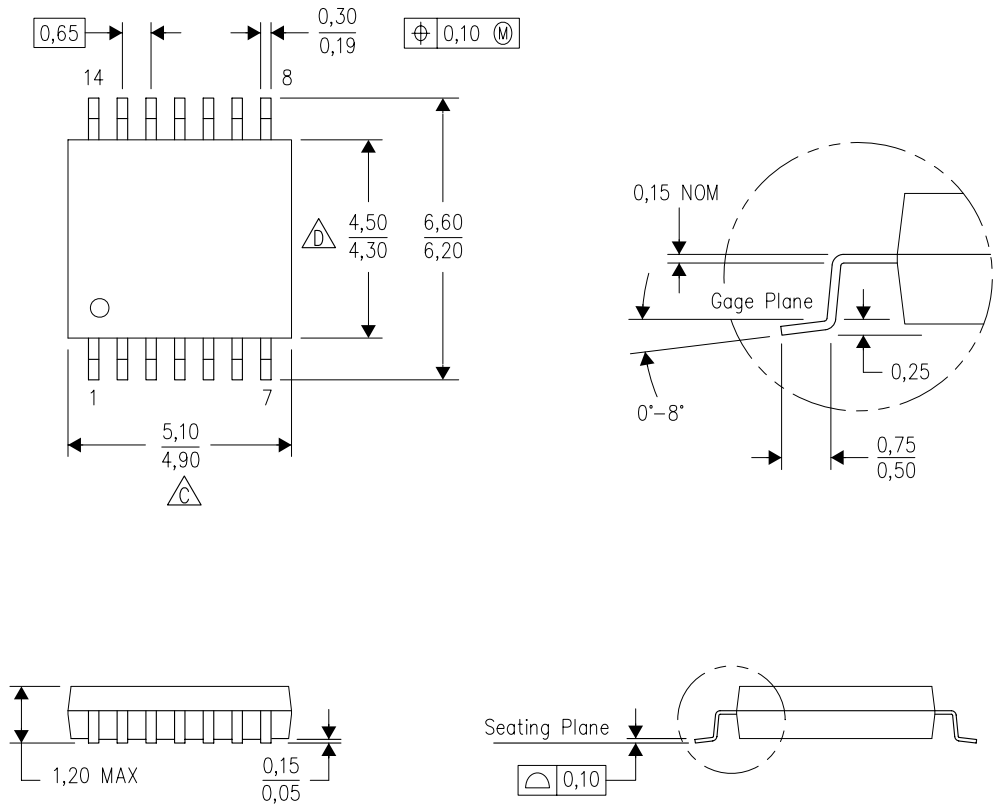
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

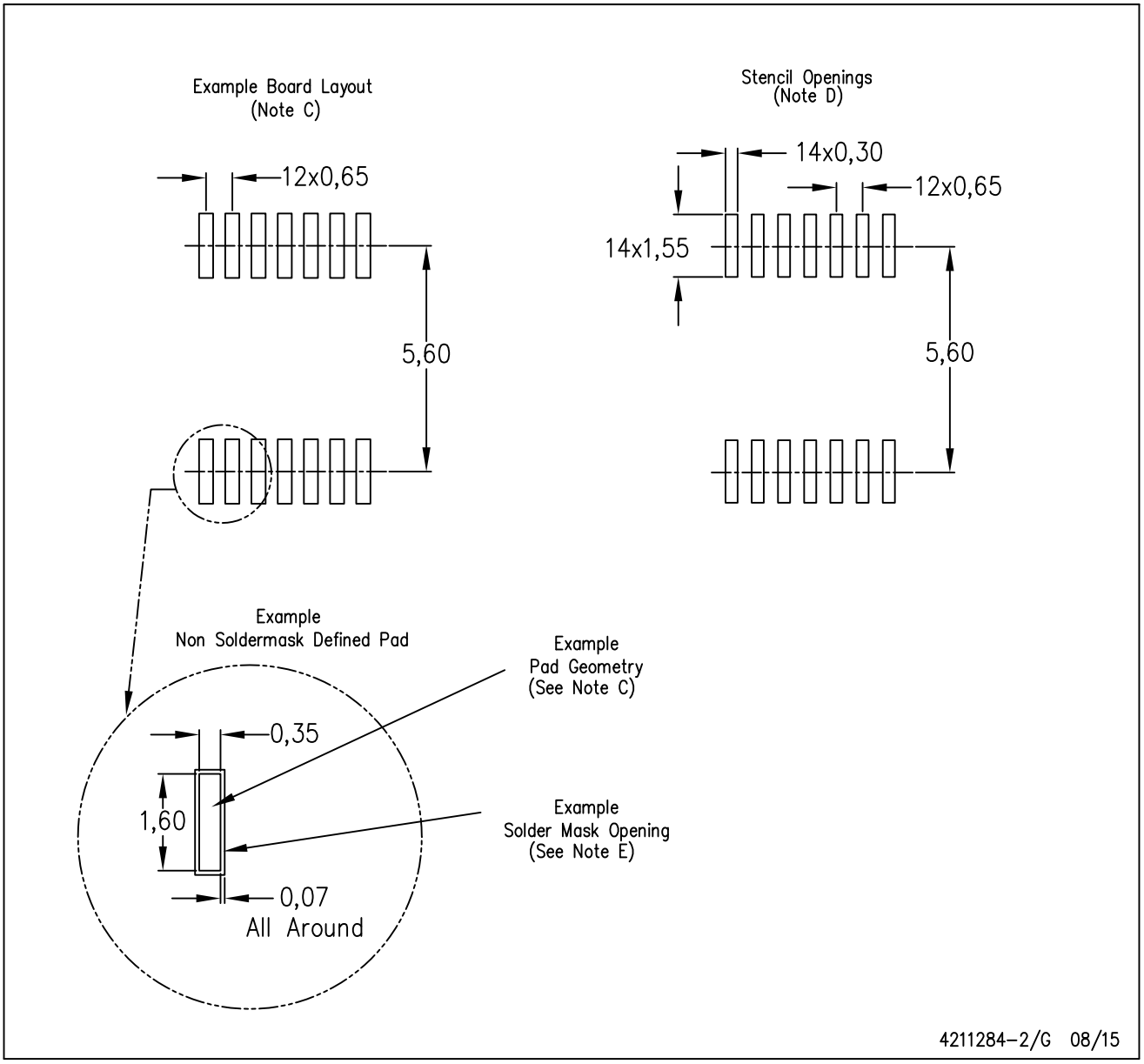
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

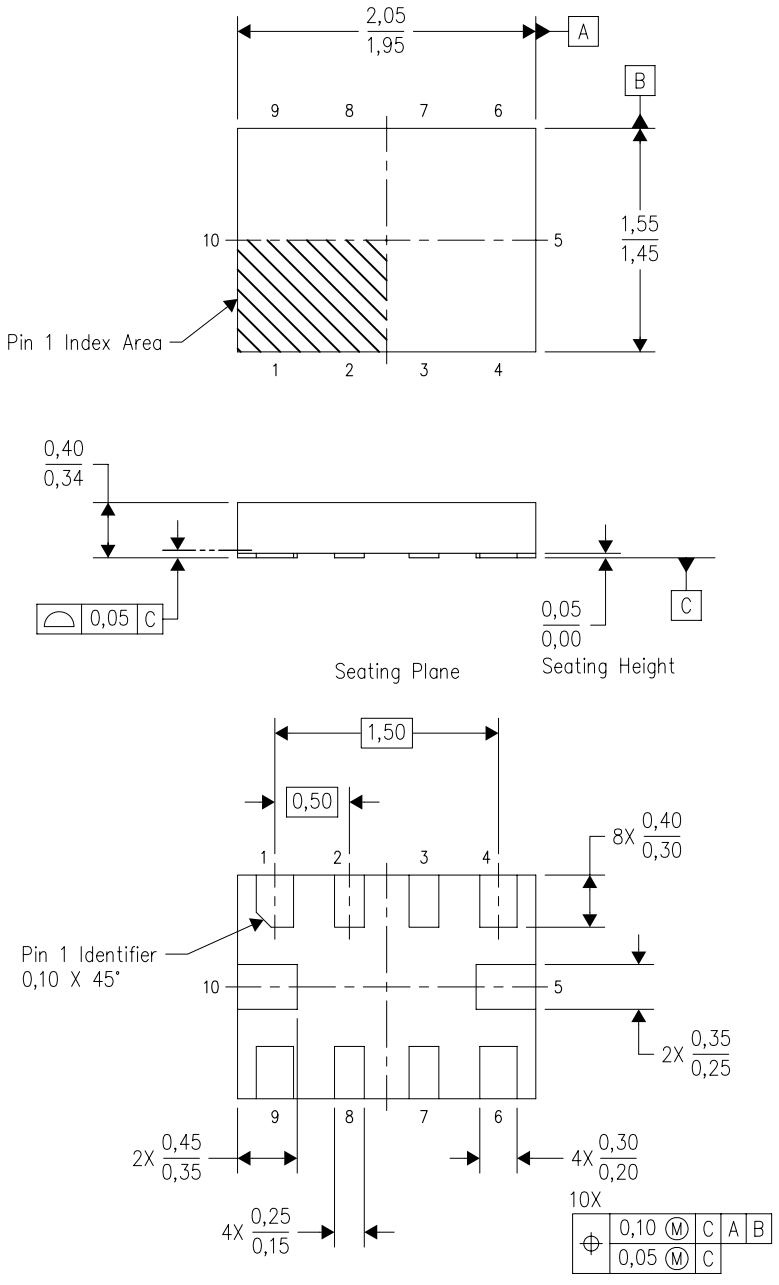
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

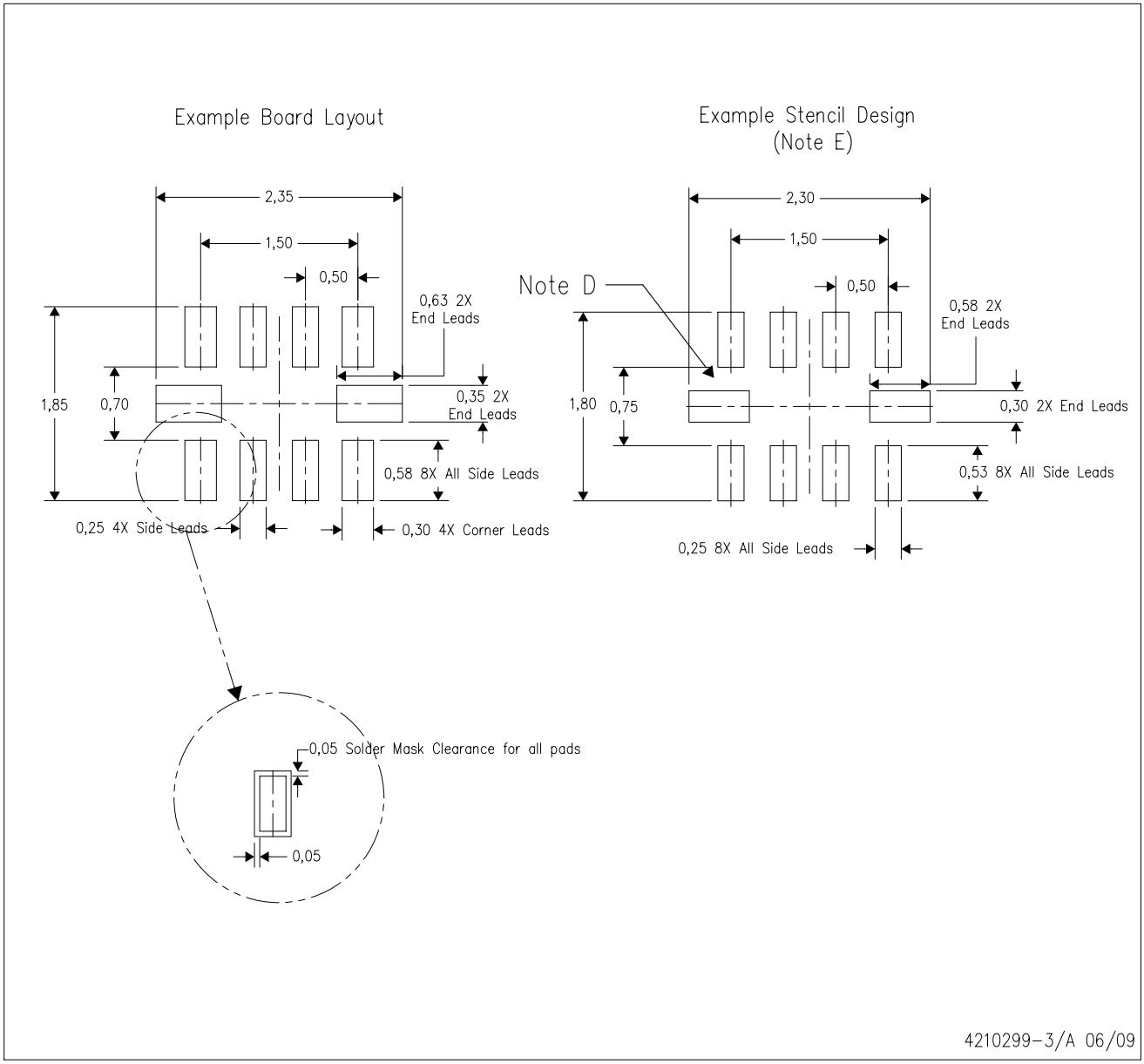
RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



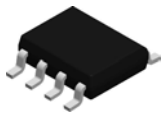
4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

RUG (R–PQFP–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

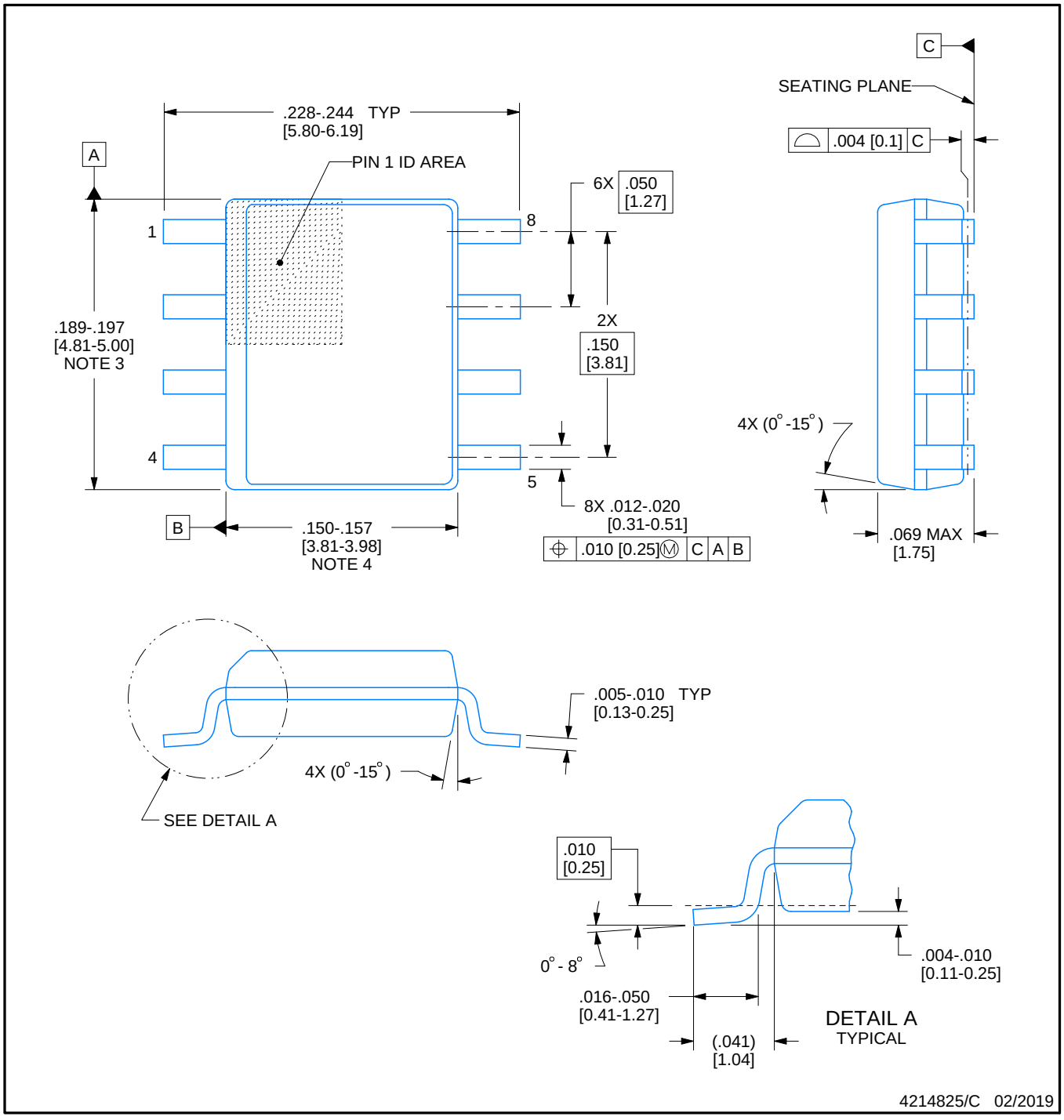


PACKAGE OUTLINE

D0008A

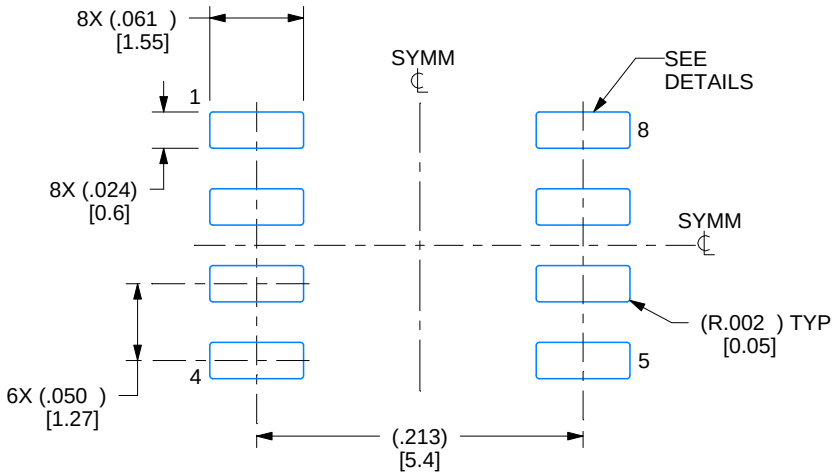
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

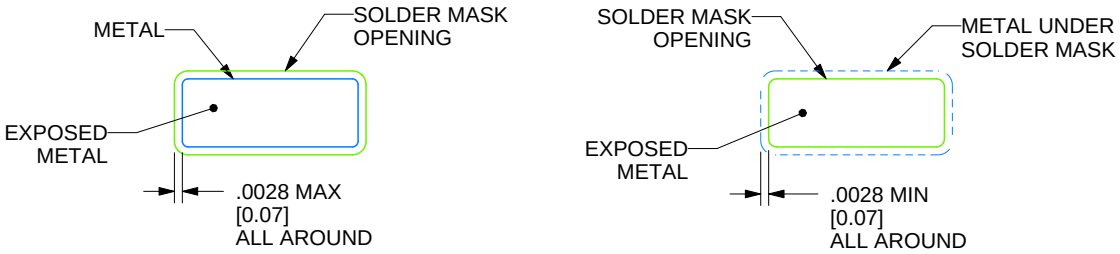


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

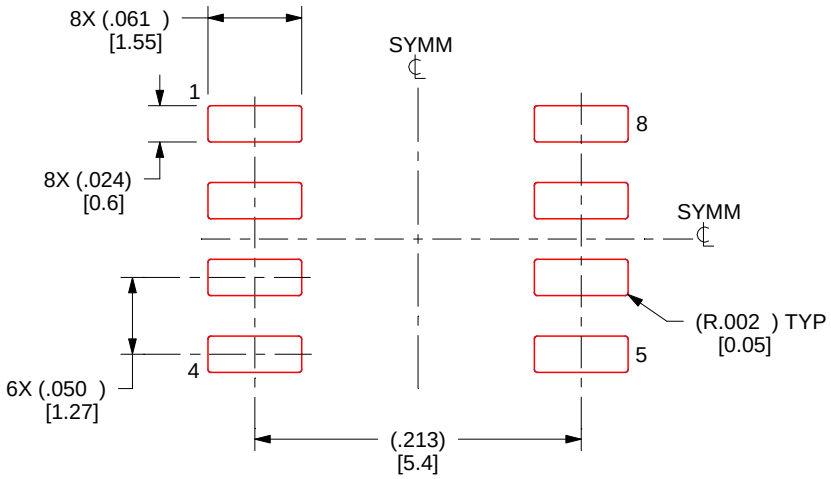
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



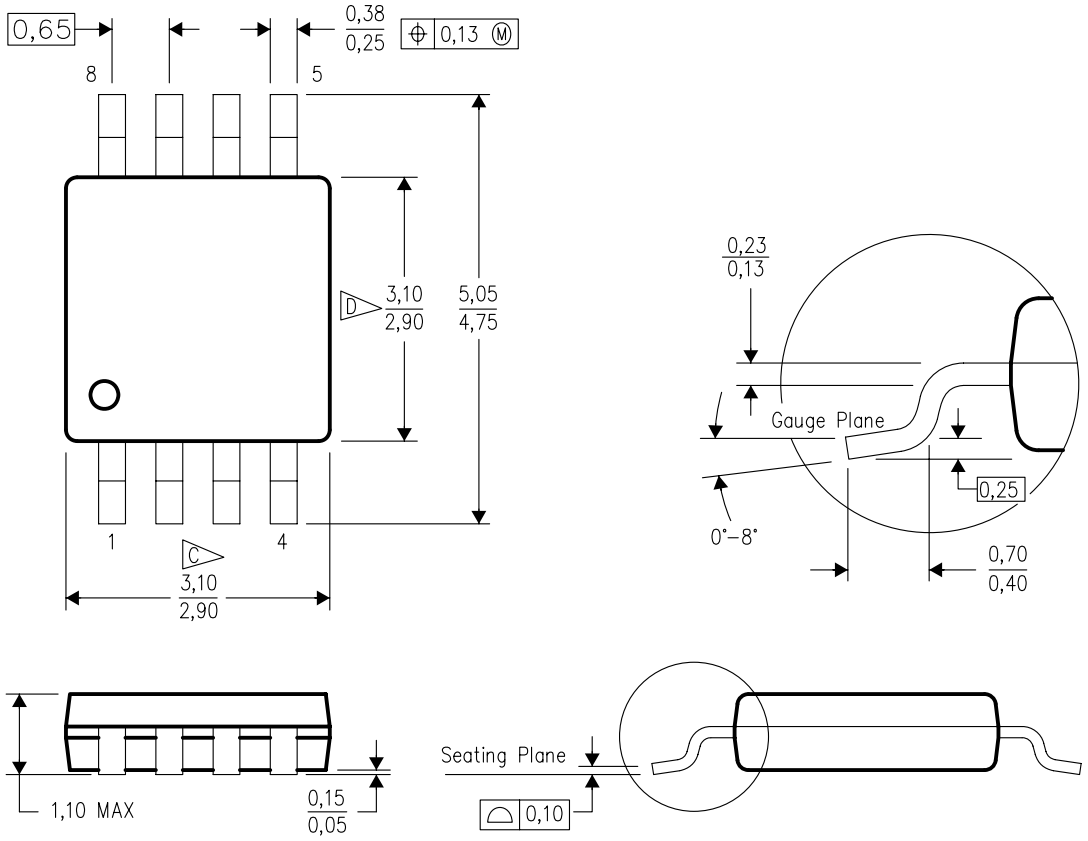
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

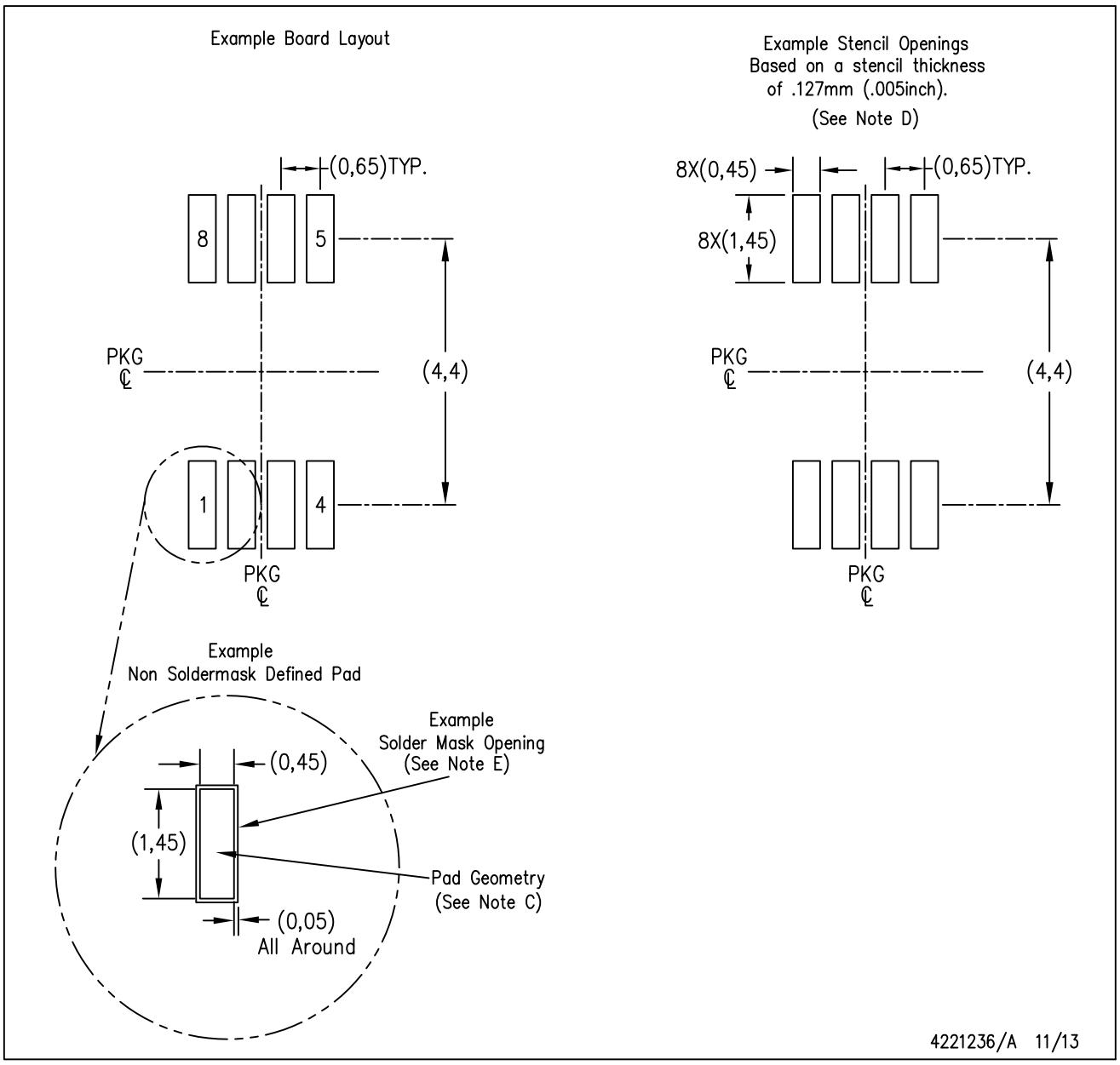
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

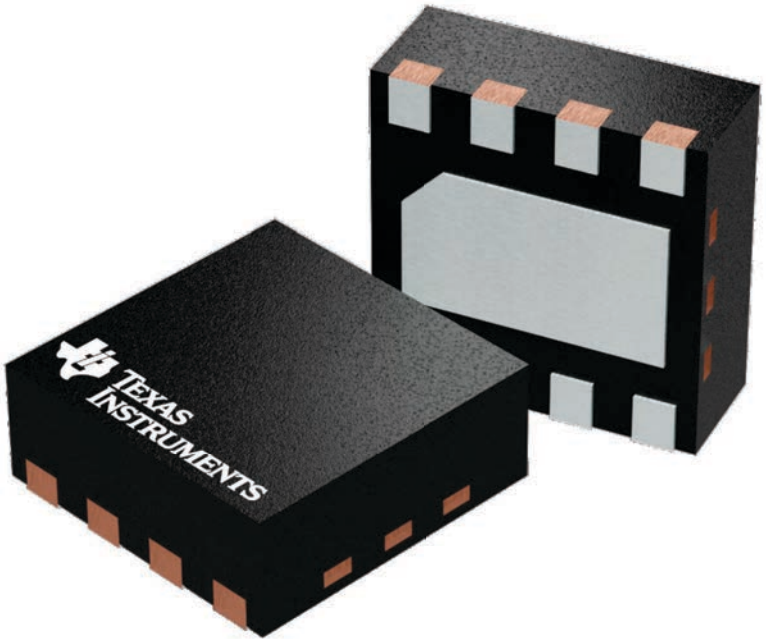
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



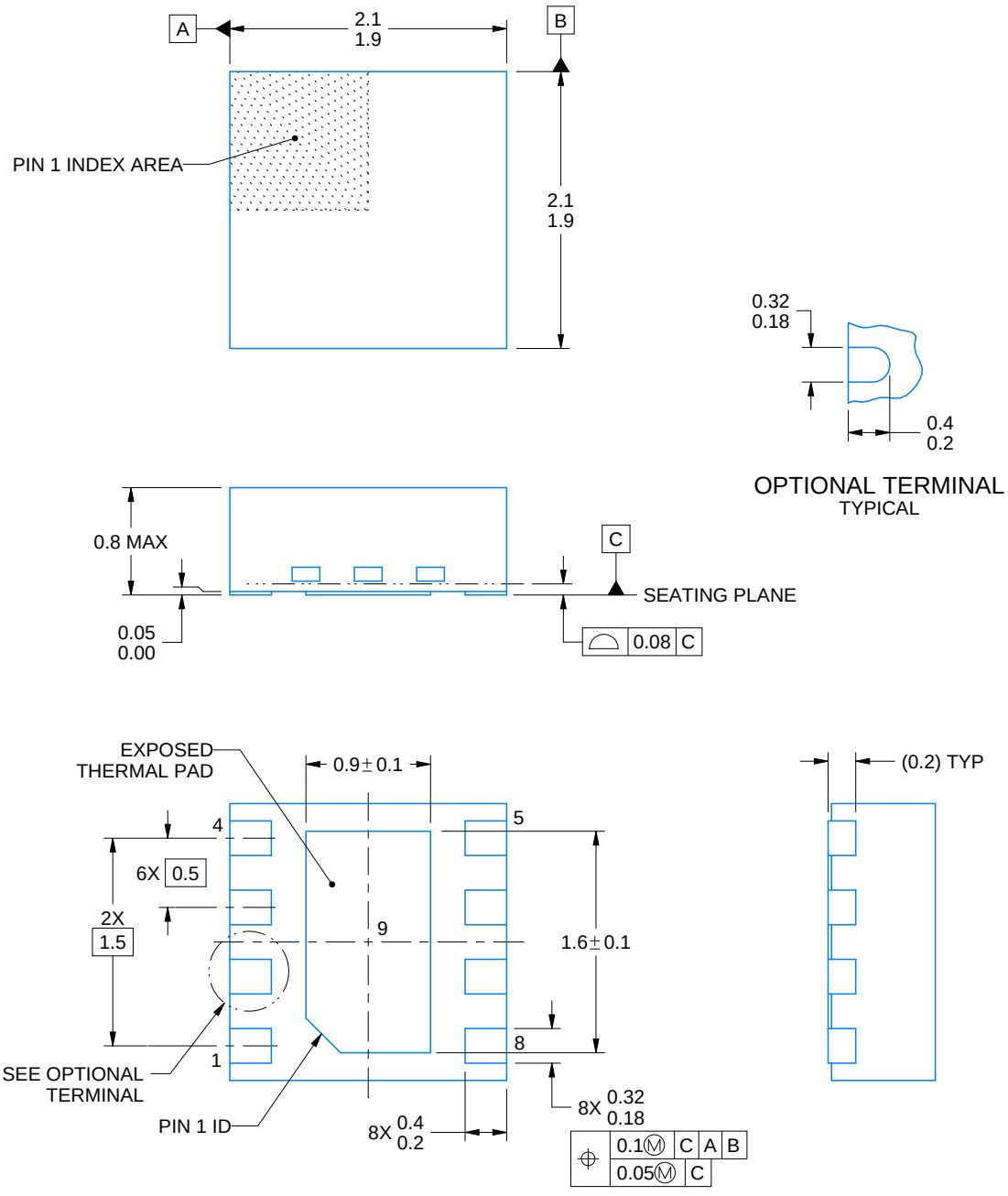
4224783/A

PACKAGE OUTLINE

DSG0008A

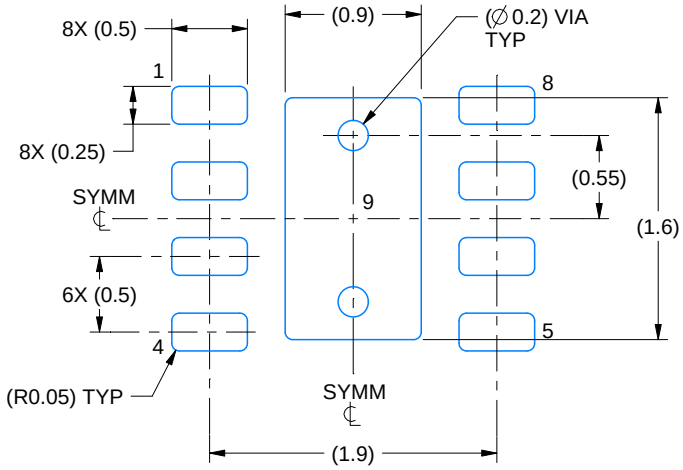
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

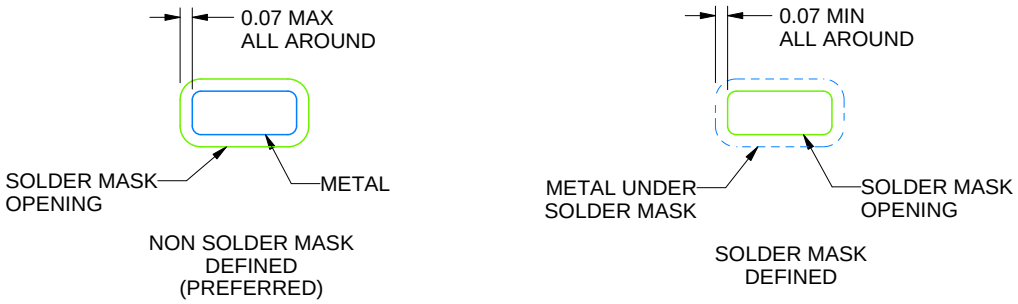


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

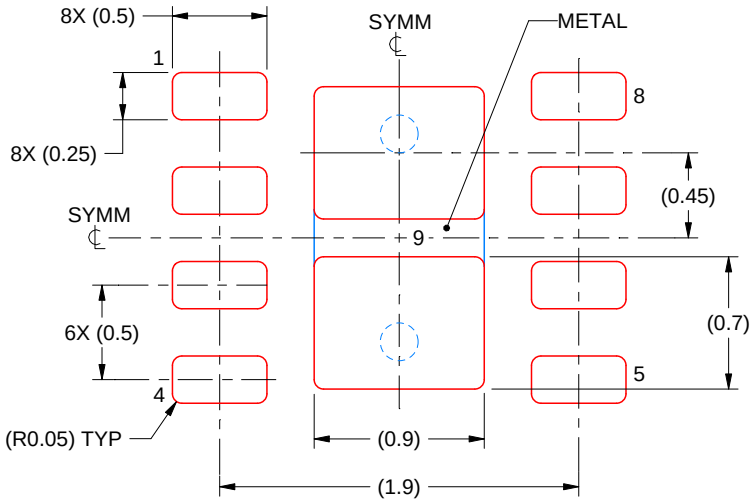


SOLDER MASK DETAILS

4218900/C 04/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/C 04/2019

NOTES: (continued)

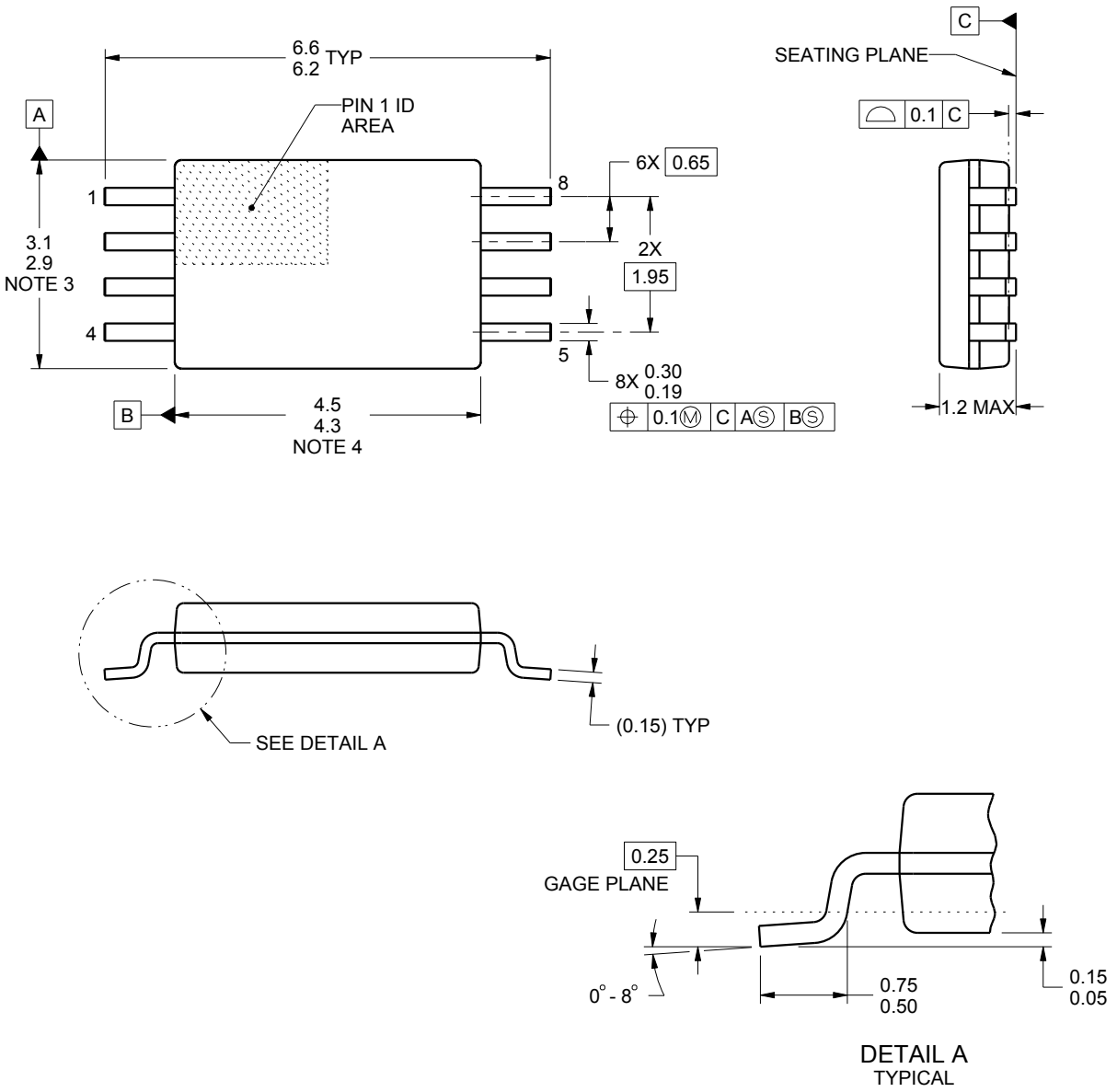
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0008A

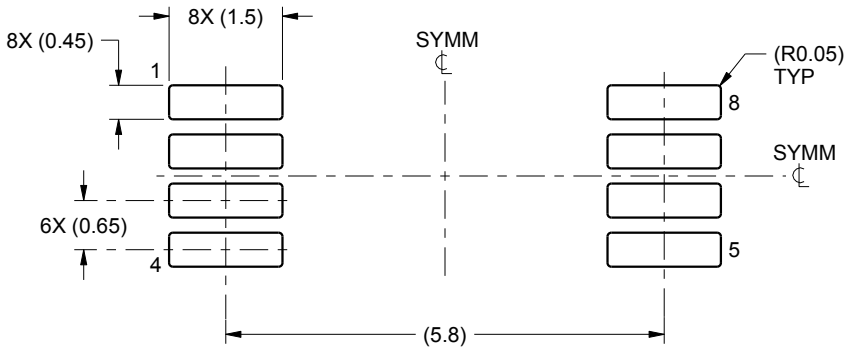
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

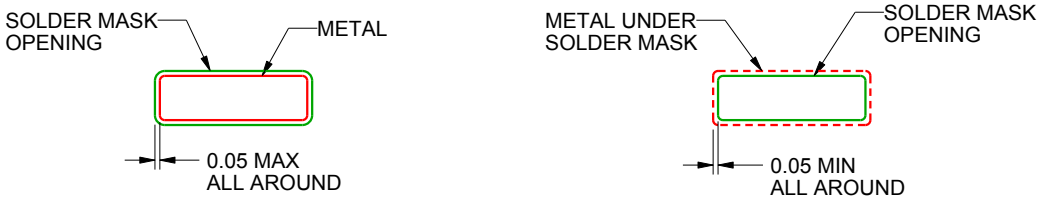


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

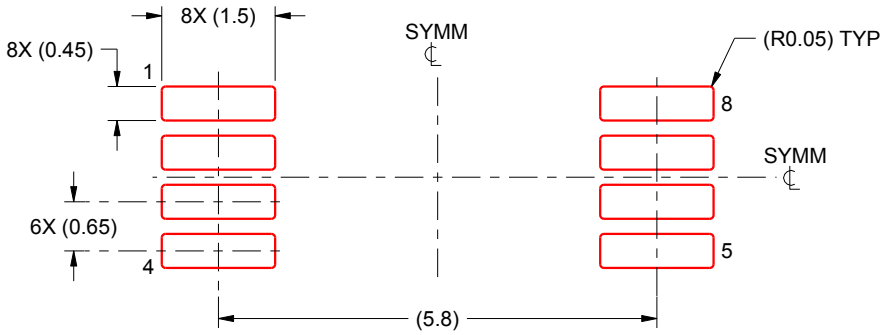


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

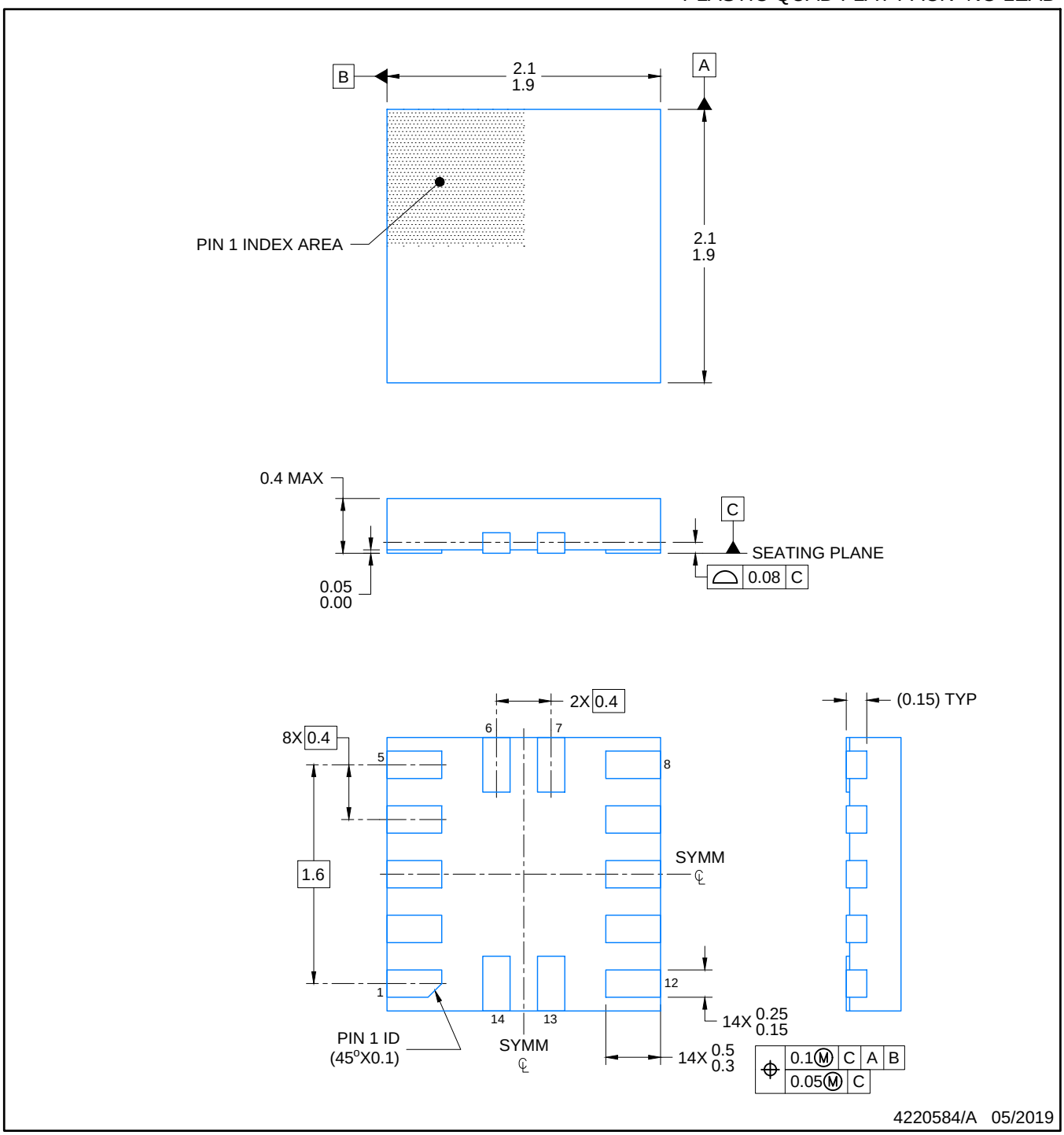
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RUC0014A

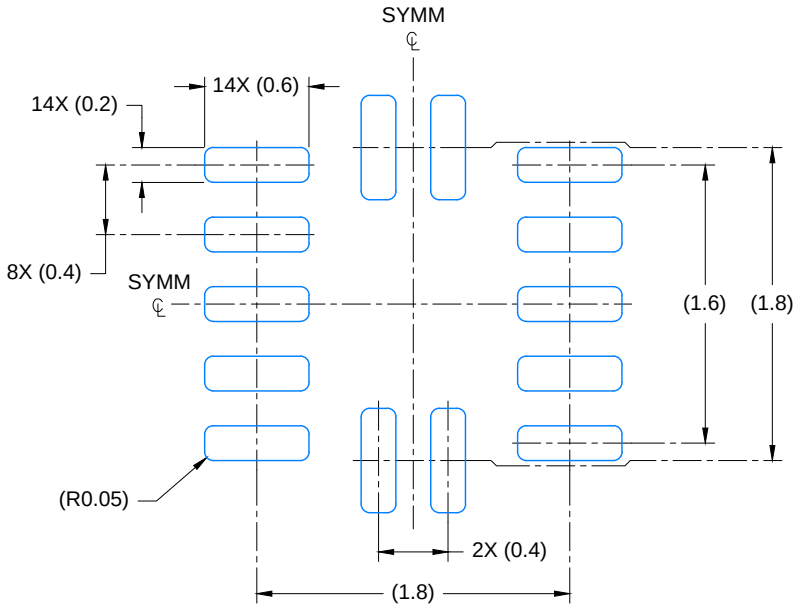
X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

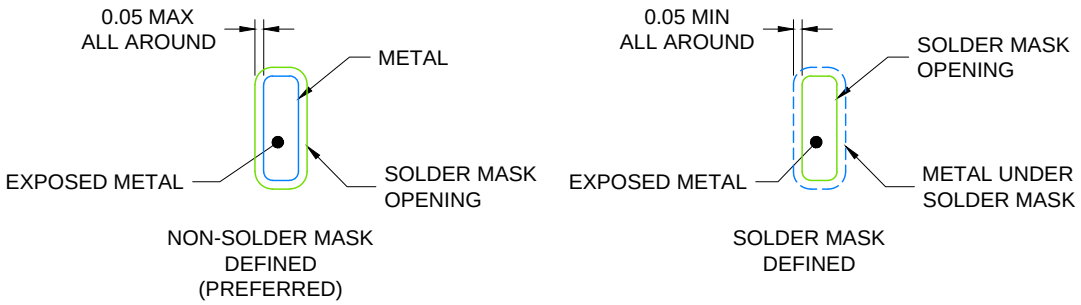


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X

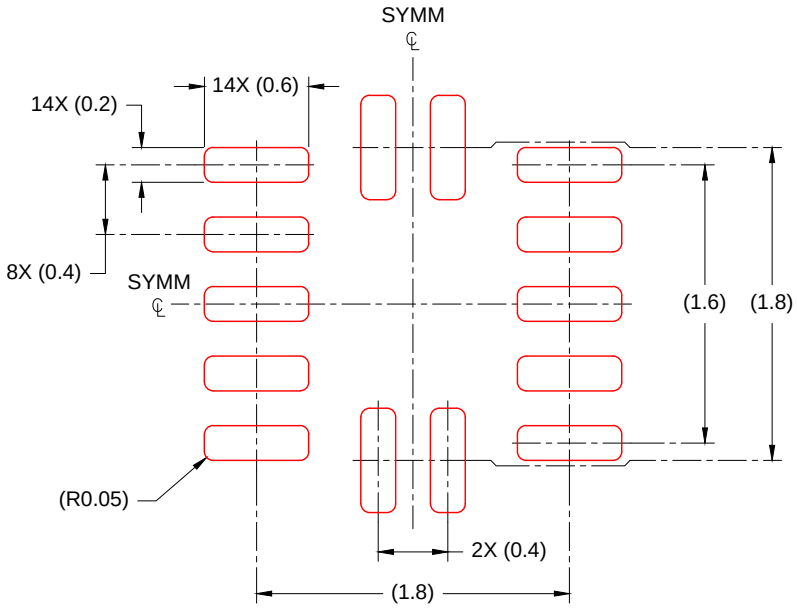


SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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