# IWR6843 单芯片 60GHz 至 64GHz 毫米波传感器



## 1 器件概述

### 1.1 特性

- FMCW 收发器
  - 集成 PLL、发送器、接收器、基带和 A2D
  - 60GHz 至 64GHz 的覆盖范围，具有 4GHz 的连续带宽
  - 四个接收通道
  - 三个发送通道
  - 基于分数 N PLL 的超精确调频脉冲引擎
  - TX 功率：10dBm
  - RX 噪声系数：
    - 14dB
  - 1MHz 时的相位噪声：
    - –92dBc/Hz
- 内置校准和自检
  - 基于 ARM® Cortex®-R4F 的无线电控制系统
  - 内置固件 (ROM)
  - 针对频率和温度进行自校准的系统
- 用于高级信号处理的 C674x DSP
- 用于 FFT、滤波和 CFAR 处理的硬件加速器
- 用于物体检测和接口控制的 ARM-R4F 微控制器
  - 支持自主模式（从 QSPI 闪存加载用户应用）
- 具有 ECC 的内部存储器
  - 1.75MB，分为 MSS 程序 RAM (512KB)、MSS 数据 RAM (192KB)、DSP L1 RAM (64KB) 和 L2 RAM (256KB) 以及 L3 雷达数据立方体 RAM (768KB)
  - 技术参考手册包括允许的大小修改
- 为用户应用提供的其他接口
  - 多达 6 个 ADC 通道（低采样率监控）
  - 多达 2 个 SPI 端口
  - 多达 2 个 UART
  - 1 个 CAN-FD 接口
  - I2C
  - GPIO
  - 用于原始 ADC 数据和调试仪表的双通道 LVDS 接口
- 以 SIL-2 级为目标
- 电源管理
  - 内置 LDO 网络，可增强 PSRR
  - I/O 支持双电压 3.3V/1.8V
- 时钟源
  - 具有内部振荡器的 40.0MHz 晶体
  - 支持频率为 40MHz 的外部振荡器
  - 支持外部驱动、频率为 40MHz 的时钟（方波/正弦波）
- 轻松的硬件设计
  - 0.65mm 间距、161 引脚 10.4mm × 10.4mm 覆晶 BGA 封装，可实现轻松组装和低成本 PCB 设计
  - 小尺寸解决方案
- 运行条件：
  - 结温范围为 –40ºC 至 105ºC

### 1.2 应用

- 用于测量距离、速度和角度的工业传感器
- 楼宇自动化
- 位移感应
- 手势
- 机器人
- 交通监控
- 接近和位置感应
- 安全和监控
- 工厂自动化
- 安全防护装置
- 人数统计
- 运动检测
- 占位检测

### 1.3 说明

IWR6843 是一款能够在 60GHz 至 64GHz 频带中运行且基于 FMCW 雷达技术的集成式单芯片毫米波传感器。该器件采用 TI 的低功耗 45nm RFCMOS 工艺进行构建，并且在极小的封装中实现了前所未有的集成度。IWR6843 是适用于工业领域中的低功耗、自监控、超精确雷达系统的理想解决方案。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸 |
|---|---|---|
| XI6843QGABL | FCBGA (161) | 10.4mm × 10.4mm |
| XI6843AAQGALB | FCBGA (209) | 15mm × 15mm |

(1) 有关更多信息，请参阅 节 9，*机械、封装和可订购产品信息*。

## 1.4 功能方框图

图 1-1 展示器件的功能方框图

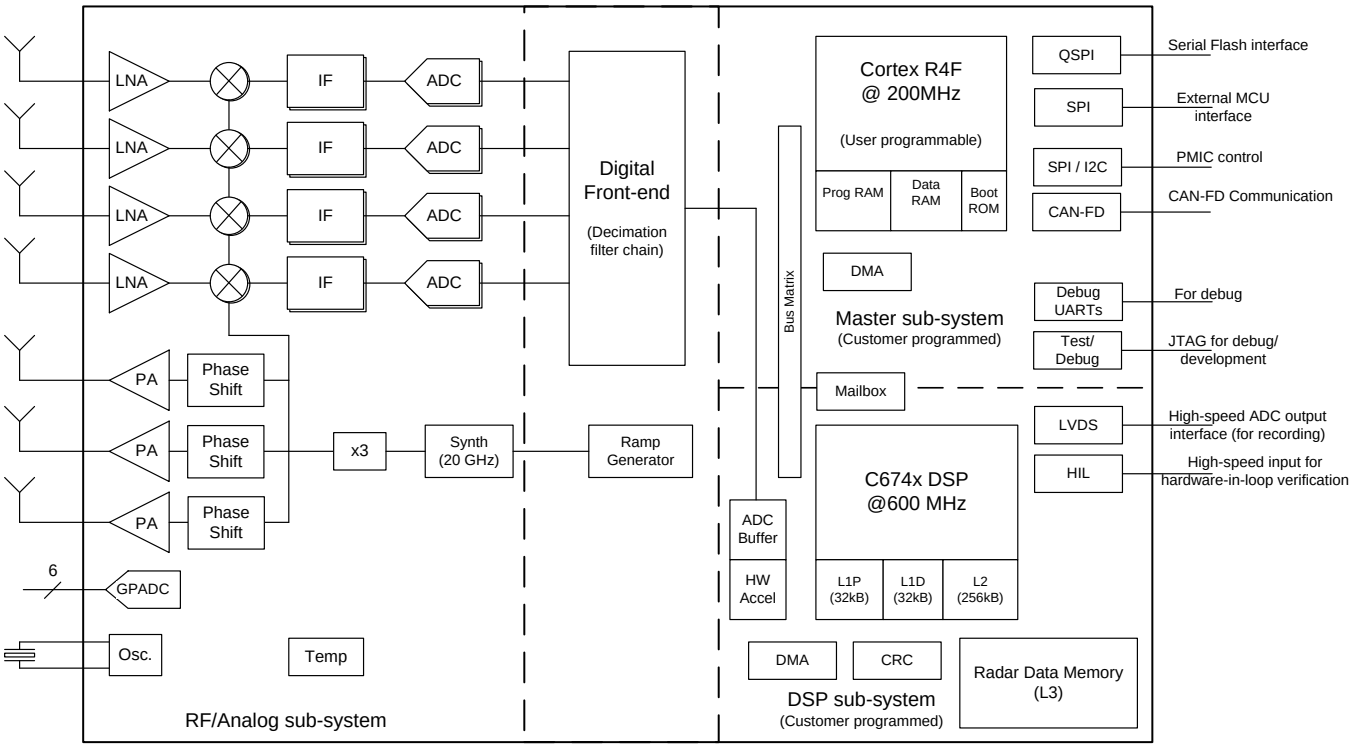


图 **1-1.** 功能方框图

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# 内容



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## 2 修订历史记录

**Changes from October 15, 2018 to June 15, 2019 (from * Revision (October 2018) to A Revision)** **Page**

- （器件信息）：添加了“XI6843AAQGALB”器件号。 ..... 2
- Table 4-2(PAD IO Control Registers): Updated/Changed table. ..... 19
- Section 5.7 (RF Specification): Updated/Change Ramp rate from "266" to "250" MHz/µs ..... 28
- Figure 5-1 (Device Wake-Up Sequence): Removed the 1v4 signal . ..... 30
- Figure 5-10 (LVDS Interface Lane Configuration And Relative Timings): Updated image. ..... 41
- Table 5-10 (LVDS Electrical Characteristics): Updated characteristics table ..... 41
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- 图 8-1（器件命名规则）：更新/更改了“特性”字段 ..... 63

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# 3 Device Comparison

**Table 3-1. Device Features Comparison**

| FUNCTION | | IWR6843 | IWR1642 | IWR1443 |
|---|---|---|---|---|
| Number of receivers | | 4 | 4 | 4 |
| Number of transmitters | | 3 | 2 | 3 |
| RF frequency range | | 60 to 64 GHz | 76 to 81 GHz | 76 to 81 GHz |
| On-chip memory | | 1.75MB | 1.5MB | 576KB |
| Max I/F (Intermediate Frequency) (MHz) | | 10 | 5 | 15 |
| Max real sampling rate (Msps) | | 25 | 12.5 | 37.5 |
| Max complex sampling rate (Msps) | | 12.5 | 6.25 | 18.75 |
| Processor | | | | |
| MCU (R4F) | | Yes | Yes | Yes |
| DSP (C674x) | | Yes | Yes | — |
| Peripherals | | | | |
| Serial Peripheral Interface (SPI) ports | | 2 | 2 | 1 |
| Quad Serial Peripheral Interface (QSPI) | | Yes | Yes | Yes |
| Inter-Integrated Circuit ($I^2C$) interface | | 1 | 1 | 1 |
| Controller Area Network (DCAN) interface | | — | Yes | Yes |
| Controller Area Network (CAN-FD) interface | | Yes | — | — |
| Trace | | Yes | Yes | — |
| PWM | | Yes | Yes | — |
| Hardware In Loop (HIL/DMM) | | Yes | Yes | — |
| GPADC | | Yes | Yes | Yes |
| LVDS/Debug | | Yes | Yes | Yes |
| CSI2 | | — | — | Yes |
| Hardware accelerator | | Yes | — | Yes |
| 1-V bypass mode | | Yes | Yes | Yes |
| JTAG | | Yes | Yes | Yes |
| Product status | Product Preview (PP), Advance Information (AI), or Production Data (PD) | AI(1) | PD(2) | PD(2) |

(1) ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.
(2) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## 3.1 Related Products

For information about other devices in this family of products or related products see the links that follow.

**mmWave Sensors** TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for industrial applications.

**mmWave IWR** The Texas Instruments IWRxxxx family of mmWave Sensors are highly integrated and built on RFCMOS technology operating in 76- to 81-GHz or 60- to 64-GHz frequency band. The devices have a closed-loop PLL for precise and linear chirp synthesis, includes a built-in radio processor (BIST) for RF calibration and safety monitoring. The devices have a very small-form factor, low power consumption, and are highly accurate. Industrial applications from long range to ultra short range can be realized using these devices.

**Companion Products for IWR6843** Review products that are frequently purchased or used in conjunction with this product.

**Reference Designs for IWR6843** The IWR6843 TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

# 4 Terminal Configuration and Functions

## 4.1 Pin Diagram

Figure 4-1 shows the pin locations for the 161-pin FCBGA package. Figure 4-2, Figure 4-3, Figure 4-4, and Figure 4-5 show the same pins, but split into four quadrants.

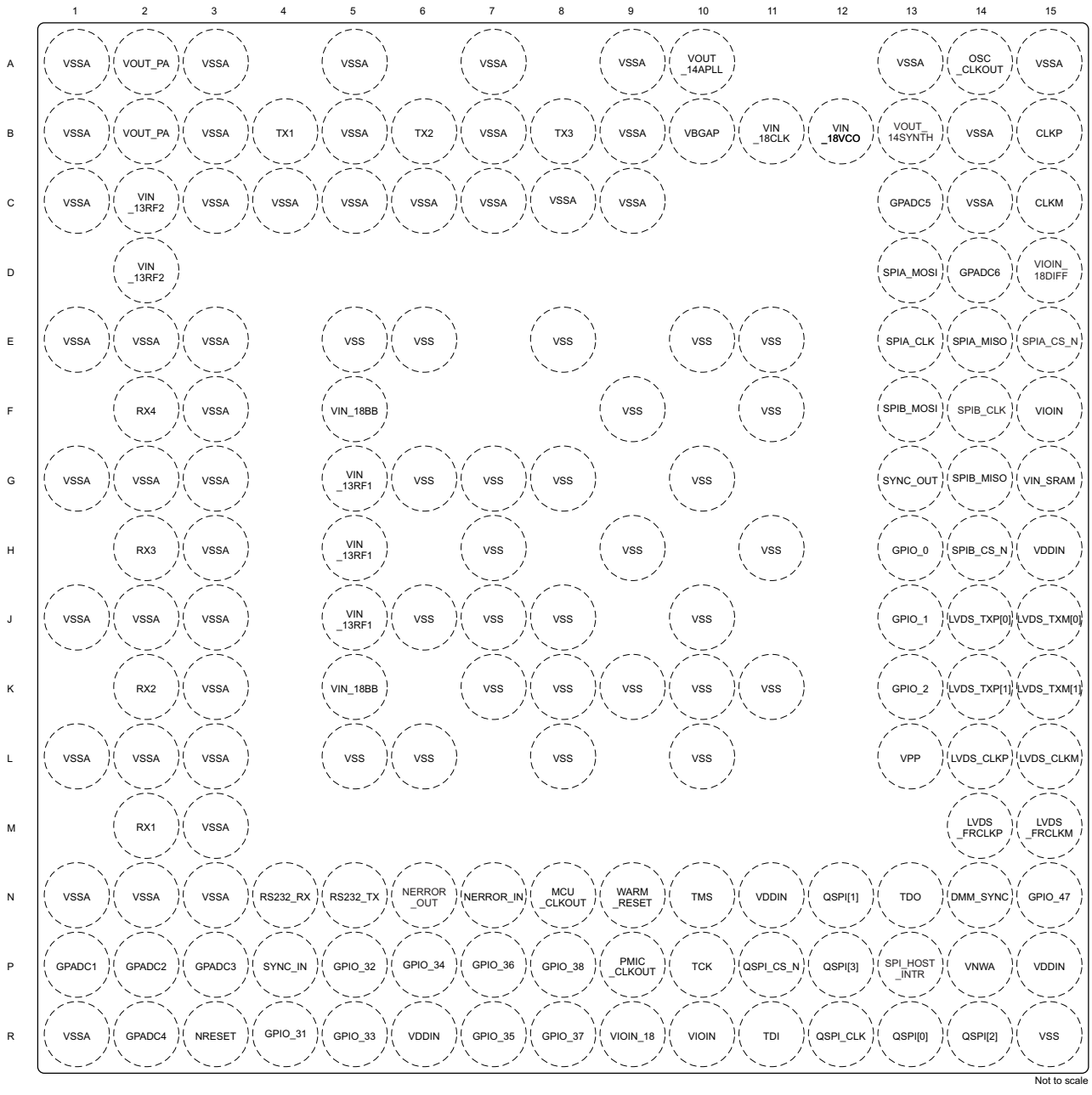


**Figure 4-1. Pin Diagram**

ADVANCE INFORMATION

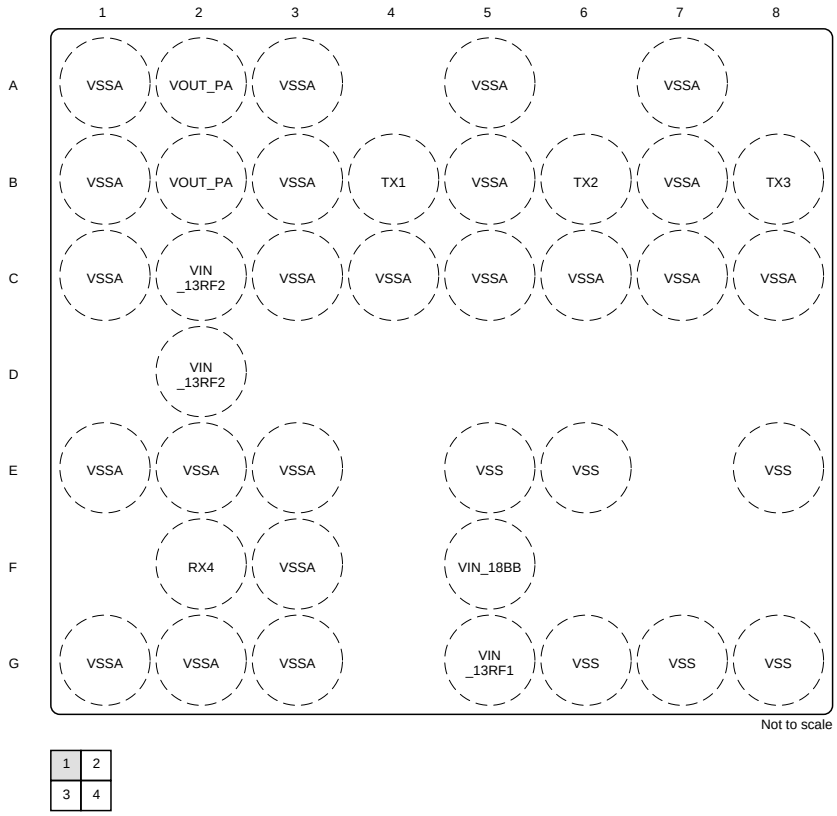


**Figure 4-2. Top Left Quadrant**

ADVANCE INFORMATION

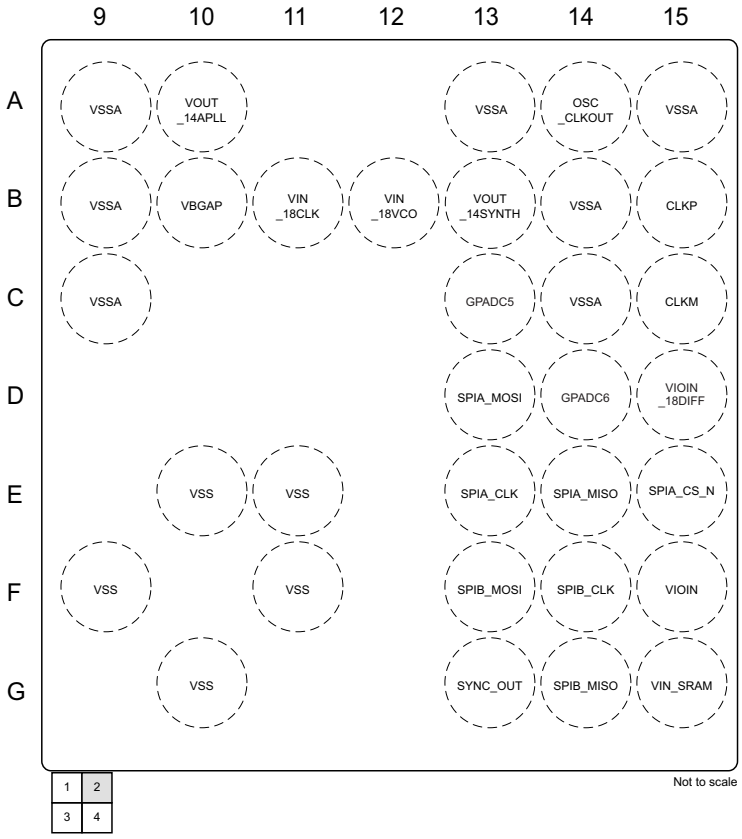


**Figure 4-3. Top Right Quadrant**

ADVANCE INFORMATION

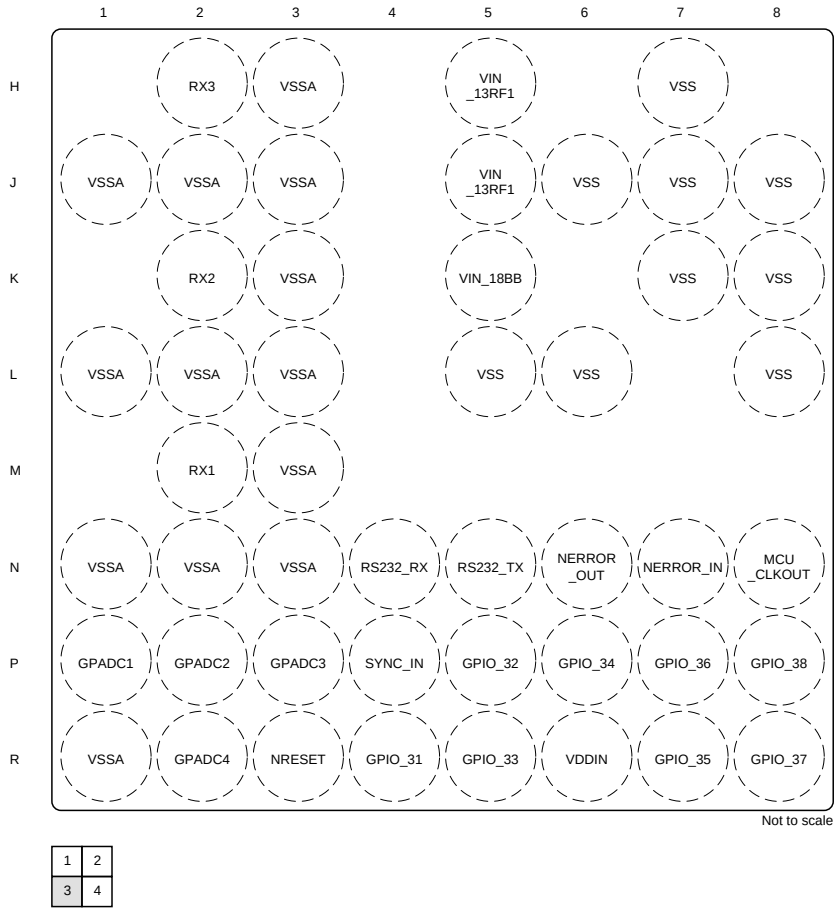


**Figure 4-4. Bottom Left Quadrant**

ADVANCE INFORMATION

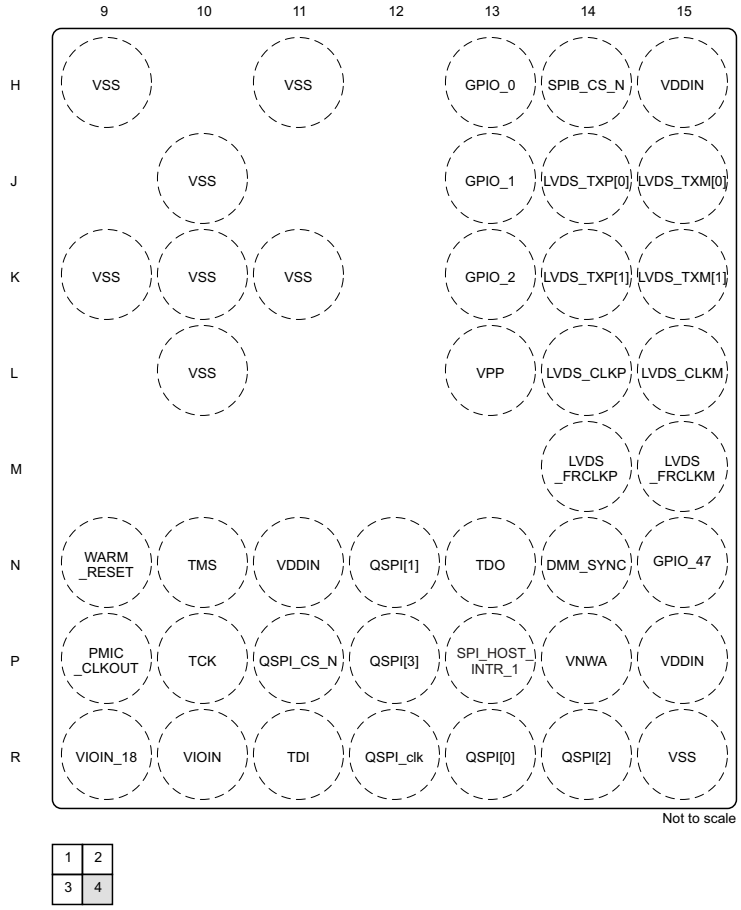


**Figure 4-5. Bottom Right Quadrant**

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## 4.2 Pin Attributes

**Table 4-1. Pin Attributes (ABL0161 Package)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PINCNTL ADDRESS [4] | MODE [5] | TYPE [6] | BALL RESET STATE [7] | PULL UP/DOWN TYPE [8] |
|---|---|---|---|---|---|---|---|
| H13 | GPIO_0 | GPIO_13 | 0xFFFFEA04 | 0 | IO | Output Disabled | Pull Down |
| | | GPIO_0 | | 1 | IO | | |
| | | PMIC_CLKOUT | | 2 | O | | |
| | | ADC_VALID | | 9 | O | | |
| | | EPWM1B | | 10 | O | | |
| | | ePWM2A | | 11 | O | | |
| J13 | GPIO_1 | GPIO_16 | 0xFFFFEA08 | 0 | IO | Output Disabled | Pull Down |
| | | GPIO_1 | | 1 | IO | | |
| | | SYNC_OUT | | 2 | O | | |
| | | ADC_VALID | | 7 | O | | |
| | | DMM_MUX_IN | | 12 | I | | |
| | | SPIB_CS_N_1 | | 13 | IO | | |
| | | SPIB_CS_N_2 | | 14 | IO | | |
| | | EPWM1SYNCI | | 15 | I | | |
| K13 | GPIO_2 | GPIO_26 | 0xFFFFEA64 | 0 | IO | Output Disabled | Pull Down |
| | | GPIO_2 | | 1 | IO | | |
| | | OSC_CLKOUT | | 2 | O | | |
| | | MSS_UARTB_TX | | 7 | O | | |
| | | BSS_UART_TX | | 8 | O | | |
| | | SYNC_OUT | | 9 | O | | |
| | | PMIC_CLKOUT | | 10 | O | | |
| | | CHIRP_START | | 11 | O | | |
| | | CHIRP_END | | 12 | O | | |
| | | FRAME_START | | 13 | O | | |
| R4 | GPIO_31 | TRACE_DATA_0 | 0xFFFFEA7C | 0 | O | Output Disabled | Pull Down |
| | | GPIO_31 | | 1 | IO | | |
| | | DMM0 | | 2 | I | | |
| | | MSS_UARTA_TX | | 4 | IO | | |
| P5 | GPIO_32 | TRACE_DATA_1 | 0xFFFFEA80 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_32 | | 1 | IO | | |
| | | DMM1 | | 2 | I | | |
| R5 | GPIO_33 | TRACE_DATA_2 | 0xFFFFEA84 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_33 | | 1 | IO | | |
| | | DMM2 | | 2 | I | | |

**Table 4-1. Pin Attributes (ABL0161 Package) (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PINCNTL ADDRESS [4] | MODE [5] | TYPE [6] | BALL RESET STATE [7] | PULL UP/DOWN TYPE [8] |
|---|---|---|---|---|---|---|---|
| P6 | GPIO_34 | TRACE_DATA_3 | 0xFFFFEA88 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_34 | | 1 | IO | | |
| | | DMM3 | | 2 | I | | |
| | | EPWM3SYNCO | | 4 | O | | |
| R7 | GPIO_35 | TRACE_DATA_4 | 0xFFFFEA8C | 0 | O | Output Disabled | Pull Down |
| | | GPIO_35 | | 1 | IO | | |
| | | DMM4 | | 2 | I | | |
| | | EPWM2SYNCO | | 4 | O | | |
| P7 | GPIO_36 | TRACE_DATA_5 | 0xFFFFEA90 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_36 | | 1 | IO | | |
| | | DMM5 | | 2 | I | | |
| | | MSS_UARTB_TX | | 5 | O | | |
| R8 | GPIO_37 | TRACE_DATA_6 | 0xFFFFEA94 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_37 | | 1 | IO | | |
| | | DMM6 | | 2 | I | | |
| | | BSS_UART_TX | | 5 | O | | |
| P8 | GPIO_38 | TRACE_DATA_7 | 0xFFFFEA98 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_38 | | 1 | IO | | |
| | | DMM7 | | 2 | I | | |
| | | DSS_UART_TX | | 5 | O | | |
| N15 | GPIO_47 | TRACE_CLK | 0xFFFFEABC | 0 | O | Output Disabled | Pull Down |
| | | GPIO_47 | | 1 | IO | | |
| | | DMM_CLK | | 2 | I | | |
| N14 | DMM_SYNC | TRACE_CTL | 0xFFFFEAC0 | 0 | O | Output Disabled | Pull Down |
| | | DMM_SYNC | | 2 | I | | |
| N8 | MCU_CLKOUT | GPIO_25 | 0xFFFFEA60 | 0 | IO | Output Disabled | Pull Down |
| | | MCU_CLKOUT | | 1 | O | | |
| | | CHIRP_START | | 2 | O | | |
| | | CHIRP_END | | 6 | O | | |
| | | FRAME_START | | 7 | O | | |
| | | EPWM1A | | 12 | O | | |
| N7 | NERROR_IN | NERROR_IN | 0xFFFFEA44 | 0 | I | Input | |
| N6 | NERROR_OUT | NERROR_OUT | 0xFFFFEA4C | 0 | O | Hi-Z (Open Drain) | |

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**Table 4-1. Pin Attributes (ABL0161 Package) (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PINCNTL ADDRESS [4] | MODE [5] | TYPE [6] | BALL RESET STATE [7] | PULL UP/DOWN TYPE [8] |
|---|---|---|---|---|---|---|---|
| P9 | PMIC_CLKOUT | SOP[2] | 0xFFFFEA68 | During Power Up | I | Output Disabled | Pull Down |
| | | GPIO_27 | | 0 | IO | | |
| | | PMIC_CLKOUT | | 1 | O | | |
| | | CHIRP_START | | 6 | O | | |
| | | CHIRP_END | | 7 | O | | |
| | | FRAME_START | | 8 | O | | |
| | | EPWM1B | | 11 | O | | |
| | | EPWM2A | | 12 | O | | |
| R13 | QSPI[0] | GPIO_8 | 0xFFFFEA2C | 0 | IO | Output Disabled | Pull Down |
| | | QSPI[0] | | 1 | IO | | |
| | | SPIB_MISO | | 2 | IO | | |
| N12 | QSPI[1] | GPIO_9 | 0xFFFFEA30 | 0 | IO | Output Disabled | Pull Down |
| | | QSPI[1] | | 1 | I | | |
| | | SPIB_MOSI | | 2 | IO | | |
| | | SPIB_CS_N_2 | | 8 | IO | | |
| R14 | QSPI[2] | GPIO_10 | 0xFFFFEA34 | 0 | IO | Output Disabled | Pull Down |
| | | QSPI[2] | | 1 | I | | |
| | | CAN_FD_TX | | 8 | O | | |
| P12 | QSPI[3] | GPIO_11 | 0xFFFFEA38 | 0 | IO | Output Disabled | Pull Down |
| | | QSPI[3] | | 1 | I | | |
| | | CAN_FD_RX | | 8 | I | | |
| R12 | QSPI_CLK | GPIO_7 | 0xFFFFEA3C | 0 | IO | Output Disabled | Pull Down |
| | | QSPI_CLK | | 1 | O | | |
| | | SPIB_CLK | | 2 | IO | | |
| | | DSS_UART_TX | | 6 | O | | |
| P11 | QSPI_CS_N | GPIO_6 | 0xFFFFEA40 | 0 | IO | Output Disabled | Pull Up |
| | | QSPI_CS_N | | 1 | O | | |
| | | SPIB_CS_N | | 2 | IO | | |
| N4 | RS232_RX | GPIO_15 | 0xFFFFEA74 | 0 | IO | Input Enabled | Pull Up |
| | | RS232_RX | | 1 | I | | |
| | | MSS_UARTA_RX | | 2 | I | | |
| | | BSS_UART_TX | | 6 | IO | | |
| | | MSS_UARTB_RX | | 7 | IO | | |
| | | CAN_FD_RX | | 8 | I | | |
| | | I2C_SCL | | 9 | IO | | |
| | | EPWM2A | | 10 | O | | |
| | | EPWM2B | | 11 | O | | |
| | | EPWM3A | | 12 | O | | |

**Table 4-1. Pin Attributes (ABL0161 Package) (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PINCNTL ADDRESS [4] | MODE [5] | TYPE [6] | BALL RESET STATE [7] | PULL UP/DOWN TYPE [8] |
|---|---|---|---|---|---|---|---|
| N5 | RS232_TX | GPIO_14 | 0xFFFFEA78 | 0 | IO | Output Enabled | |
| | | RS232_TX | | 1 | O | | |
| | | MSS_UARTA_TX | | 5 | IO | | |
| | | MSS_UARTB_TX | | 6 | IO | | |
| | | BSS_UART_TX | | 7 | IO | | |
| | | CAN_FD_TX | | 10 | O | | |
| | | I2C_SDA | | 11 | IO | | |
| | | EPWM1A | | 12 | O | | |
| | | EPWM1B | | 13 | O | | |
| | | NDMM_EN | | 14 | I | | |
| | | EPWM2A | | 15 | O | | |
| E13 | SPIA_CLK | GPIO_30 | 0xFFFFEA14 | 0 | IO | Output Disabled | Pull Up |
| | | SPIA_CLK | | 1 | IO | | |
| | | DSS_UART_TX | | 7 | O | | |
| E15 | SPIA_CS_N | GPIO_30 | 0xFFFFEA18 | 0 | IO | Output Disabled | Pull Up |
| | | SPIA_CS_N | | 1 | IO | | |
| E14 | SPIA_MISO | GPIO_20 | 0xFFFFEA10 | 0 | IO | Output Disabled | Pull Up |
| | | SPIA_MISO | | 1 | IO | | |
| | | CAN_FD_TX | | 2 | O | | |
| D13 | SPIA_MOSI | GPIO_19 | 0xFFFFEA0C | 0 | IO | Output Disabled | Pull Up |
| | | SPIA_MOSI | | 1 | IO | | |
| | | CAN_FD_RX | | 2 | I | | |
| | | DSS_UART_TX | | 8 | O | | |
| F14 | SPIB_CLK | GPIO_5 | 0xFFFFEA24 | 0 | IO | Output Disabled | Pull Up |
| | | SPIB_CLK | | 1 | IO | | |
| | | MSS_UARTA_RX | | 2 | I | | |
| | | MSS_UARTB_TX | | 6 | O | | |
| | | BSS_UART_TX | | 7 | O | | |
| | | CAN_FD_RX | | 8 | I | | |
| H14 | SPIB_CS_N | GPIO_4 | 0xFFFFEA28 | 0 | IO | Output Disabled | Pull Up |
| | | SPIB_CS_N | | 1 | IO | | |
| | | MSS_UARTA_TX | | 2 | O | | |
| | | MSS_UARTB_TX | | 6 | O | | |
| | | BSS_UART_TX | | 7 | IO | | |
| | | QSPI_CLK_EXT | | 8 | I | | |
| | | CAN_FD_TX | | 9 | O | | |

ADVANCE INFORMATION

**Table 4-1. Pin Attributes (ABL0161 Package) (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PINCNTL ADDRESS [4] | MODE [5] | TYPE [6] | BALL RESET STATE [7] | PULL UP/DOWN TYPE [8] |
|---|---|---|---|---|---|---|---|
| G14 | SPIB_MISO | GPIO_22 | 0xFFFFEA20 | 0 | IO | Output Disabled | Pull Up |
| | | SPIB_MISO | | 1 | IO | | |
| | | I2C_SCL | | 2 | IO | | |
| | | DSS_UART_TX | | 6 | O | | |
| F13 | SPIB_MOSI | GPIO_21 | 0xFFFFEA1C | 0 | IO | Output Disabled | Pull Up |
| | | SPIB_MOSI | | 1 | IO | | |
| | | I2C_SDA | | 2 | IO | | |
| P13 | SPI_HOST_INTR | GPIO_12 | 0xFFFFEA00 | 0 | IO | Output Disabled | Pull Down |
| | | SPI_HOST_INTR | | 1 | O | | |
| | | ADC_VALID | | 2 | O | | |
| | | SPIB_CS_N_1 | | 6 | IO | | |
| P4 | SYNC_IN | GPIO_28 | 0xFFFFEA6C | 0 | IO | Output Disabled | Pull Down |
| | | SYNC_IN | | 1 | I | | |
| | | MSS_UARTB_RX | | 6 | IO | | |
| | | DMM_MUX_IN | | 7 | I | | |
| | | SYNC_OUT | | 9 | O | | |
| G13 | SYNC_OUT | SOP[1] | 0xFFFFEA70 | During Power Up | I | Output Disabled | Pull Down |
| | | GPIO_29 | | 0 | IO | | |
| | | SYNC_OUT | | 1 | O | | |
| | | DMM_MUX_IN | | 9 | I | | |
| | | SPIB_CS_N_1 | | 10 | IO | | |
| | | SPIB_CS_N_2 | | 11 | IO | | |
| P10 | TCK | GPIO_17 | 0xFFFFEA50 | 0 | IO | Input Enabled | Pull Down |
| | | TCK | | 1 | I | | |
| | | MSS_UARTB_TX | | 2 | O | | |
| | | CAN_FD_TX | | 8 | O | | |
| R11 | TDI | GPIO_23 | 0xFFFFEA58 | 0 | IO | Input Enabled | Pull Up |
| | | TDI | | 1 | I | | |
| | | MSS_UARTA_RX | | 2 | I | | |
| N13 | TDO | SOP[0] | 0xFFFFEA5C | During Power Up | I | Output Enabled | |
| | | GPIO_24 | | 0 | IO | | |
| | | TDO | | 1 | O | | |
| | | MSS_UARTA_TX | | 2 | O | | |
| | | MSS_UARTB_TX | | 6 | O | | |
| | | BSS_UART_TX | | 7 | O | | |
| | | NDMM_EN | | 9 | I | | |

**Table 4-1. Pin Attributes (ABL0161 Package) (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PINCNTL ADDRESS [4] | MODE [5] | TYPE [6] | BALL RESET STATE [7] | PULL UP/DOWN TYPE [8] |
|---|---|---|---|---|---|---|---|
| N10 | TMS | GPIO_18 | 0xFFFFEA54 | 0 | IO | Input Enabled | Pull Down |
| | | TMS | | 1 | I | | |
| | | BSS_UART_TX | | 2 | O | | |
| | | CAN_FD_RX | | 6 | I | | |
| N9 | WARM_RESET | WARM_RESET | 0xFFFFEA48 | 0 | IO | Hi-Z Input (Open Drain) | |

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The following list describes the table column headers:

1. **BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.
2. **BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
3. **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).
4. **PINCNTL ADDRESS:** MSS Address for PinMux Control
5. **MODE:** Multiplexing mode number: value written to PinMux Cntl register to select specific Signal name for this Ball number. Mode column has bit range value.
6. **TYPE:** Signal type and direction:
   - I = Input
   - O = Output
   - IO = Input or Output
7. **BALL RESET STATE:** The state of the terminal at power-on reset
8. **PULL UP/DOWN TYPE:** indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
   - Pull Up: Internal pullup
   - Pull Down: Internal pulldown
   - An empty box means No pull.
9. Pin Mux Control Value maps to lower 4 bits of register.

IO MUX registers are available in the MSS memory map and the respective mapping to device pins is as follows:

**Table 4-2. PAD IO Control Registers**

| Default Pin/Ball Name | Package Ball /Pin (Address) | Pin Mux Config Register |
|---|---|---|
| SPI_HOST_INTR | P13 | 0xFFFFEA00 |
| GPIO_0 | H13 | 0xFFFFEA04 |
| GPIO_1 | J13 | 0xFFFFEA08 |
| SPIA_MOSI | D13 | 0xFFFFEA0C |
| SPIA_MISO | E14 | 0xFFFFEA10 |
| SPIA_CLK | E13 | 0xFFFFEA14 |
| SPIA_CS_N | E15 | 0xFFFFEA18 |
| SPIB_MOSI | F13 | 0xFFFFEA1C |
| SPIB_MISO | G14 | 0xFFFFEA20 |
| SPIB_CLK | F14 | 0xFFFFEA24 |
| SPIB_CS_N | H14 | 0xFFFFEA28 |
| QSPI[0] | R13 | 0xFFFFEA2C |
| QSPI[1] | N12 | 0xFFFFEA30 |
| QSPI[2] | R14 | 0xFFFFEA34 |
| QSPI[3] | P12 | 0xFFFFEA38 |
| QSPI_CLK | R12 | 0xFFFFEA3C |
| QSPI_CS_N | P11 | 0xFFFFEA40 |
| NERROR_IN | N7 | 0xFFFFEA44 |
| WARM_RESET | N9 | 0xFFFFEA48 |
| NERROR_OUT | N6 | 0xFFFFEA4C |
| TCK | P10 | 0xFFFFEA50 |
| TMS | N10 | 0xFFFFEA54 |
| TDI | R11 | 0xFFFFEA58 |
| TDO | N13 | 0xFFFFEA5C |
| MCU_CLKOUT | N8 | 0xFFFFEA60 |
| GPIO_2 | K13 | 0xFFFFEA64 |
| PMIC_CLKOUT | P9 | 0xFFFFEA68 |
| SYNC_IN | P4 | 0xFFFFEA6C |
| SYNC_OUT | G13 | 0xFFFFEA70 |
| RS232_RX | N4 | 0xFFFFEA74 |
| RS232_TX | N5 | 0xFFFFEA78 |
| GPIO_31 | R4 | 0xFFFFEA7C |
| GPIO_32 | P5 | 0xFFFFEA80 |
| GPIO_33 | R5 | 0xFFFFEA84 |
| GPIO_34 | P6 | 0xFFFFEA88 |
| GPIO_35 | R7 | 0xFFFFEA8C |
| GPIO_36 | P7 | 0xFFFFEA90 |
| GPIO_37 | R8 | 0xFFFFEA94 |
| GPIO_38 | P8 | 0xFFFFEA98 |
| GPIO_47 | N15 | 0xFFFFEABC |
| DMM_SYNC | N14 | 0xFFFFEAC0 |

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The register layout is as follows:

**Table 4-3. PAD IO Register Bit Descriptions**

| BIT | FIELD | TYPE | RESET (POWER ON DEFAULT) | DESCRIPTION |
|---|---|---|---|---|
| 31-11 | NU | RW | 0 | Reserved |
| 10 | SC | RW | 0 | IO slew rate control:<br>0 = Higher slew rate<br>1 = Lower slew rate |
| 9 | PUPDSEL | RW | 0 | Pullup/PullDown Selection<br>0 = Pull Down<br>1 = Pull Up (This field is valid only if Pull Inhibit is set as '0') |
| 8 | PI | RW | 0 | Pull Inhibit/Pull Disable<br>0 = Enable<br>1 = Disable |
| 7 | OE_OVERRIDE | RW | 1 | Output Override |
| 6 | OE_OVERRIDE_CTRL | RW | 1 | Output Override Control:<br>(A '1' here overrides any o/p manipulation of this IO by any of the peripheral block hardware it is associated with for example a SPI Chip select) |
| 5 | IE_OVERRIDE | RW | 0 | Input Override |
| 4 | IE_OVERRIDE_CTRL | RW | 0 | Input Override Control:<br>(A '1' here overrides any i/p value on this IO with a desired value) |
| 3-0 | FUNC_SEL | RW | 1 | Function select for Pin Multiplexing (Refer to the Pin Mux Sheet) |

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## 4.3 Signal Descriptions

**Table 4-4. Signal Descriptions - Digital**

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BALL NO. |
|---|---|---|---|
| BSS_UART_TX | O | Debug UART Transmit [Radar Block] | F14, H14, K13, N10, N13, N4, N5, R8 |
| CAN_FD_RX | I | CAN FD (MCAN) Receive Signal | D13, F14, N10, N4, P12 |
| CAN_FD_TX | O | CAN FD (MCAN) Transmit Signal | E14, H14, N5, P10, R14 |
| DMM0 | I | Debug Interface (Hardware In Loop) - Data Line | R4 |
| DMM1 | I | Debug Interface (Hardware In Loop) - Data Line | P5 |
| DMM2 | I | Debug Interface (Hardware In Loop) - Data Line | R5 |
| DMM3 | I | Debug Interface (Hardware In Loop) - Data Line | P6 |
| DMM4 | I | Debug Interface (Hardware In Loop) - Data Line | R7 |
| DMM5 | I | Debug Interface (Hardware In Loop) - Data Line | P7 |
| DMM6 | I | Debug Interface (Hardware In Loop) - Data Line | R8 |
| DMM7 | I | Debug Interface (Hardware In Loop) - Data Line | P8 |
| DMM_CLK | I | Debug Interface (Hardware In Loop) - Clock | N15 |
| DMM_MUX_IN | I | Debug Interface (Hardware In Loop) Mux Select between DMM1 and DMM2 (Two Instances) | G13, J13, P4 |
| DMM_SYNC | I | Debug Interface (Hardware In Loop) - Sync | N14 |
| DSS_UART_TX | O | Debug UART Transmit [DSP] | D13, E13, G14, P8, R12 |
| EPWM1A | O | PWM Module 1 - Output A | N5, N8 |
| EPWM1B | O | PWM Module 1 - Output B | H13, N5, P9 |
| EPWM1SYNCI | I | | J13 |
| EPWM2A | O | PWM Module 2- Output A | H13, N4, N5, P9 |
| EPWM2B | O | PWM Module 2 - Output B | N4 |
| EPWM2SYNCO | O | | R7 |
| EPWM3A | O | PWM Module 3 - Output A | N4 |
| EPWM3SYNCO | O | | P6 |
| GPIO_0 | IO | General-purpose I/O | H13 |
| GPIO_1 | IO | General-purpose I/O | J13 |
| GPIO_2 | IO | General-purpose I/O | K13 |
| GPIO_3 | IO | General-purpose I/O | E13 |
| GPIO_4 | IO | General-purpose I/O | H14 |
| GPIO_5 | IO | General-purpose I/O | F14 |
| GPIO_6 | IO | General-purpose I/O | P11 |
| GPIO_7 | IO | General-purpose I/O | R12 |
| GPIO_8 | IO | General-purpose I/O | R13 |
| GPIO_9 | IO | General-purpose I/O | N12 |
| GPIO_10 | IO | General-purpose I/O | R14 |
| GPIO_11 | IO | General-purpose I/O | P12 |
| GPIO_12 | IO | General-purpose I/O | P13 |
| GPIO_13 | IO | General-purpose I/O | H13 |
| GPIO_14 | IO | General-purpose I/O | N5 |
| GPIO_15 | IO | General-purpose I/O | N4 |
| GPIO_16 | IO | General-purpose I/O | J13 |
| GPIO_17 | IO | General-purpose I/O | P10 |
| GPIO_18 | IO | General-purpose I/O | N10 |
| GPIO_19 | IO | General-purpose I/O | D13 |
| GPIO_20 | IO | General-purpose I/O | E14 |

**Table 4-4. Signal Descriptions - Digital (continued)**

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BALL NO. |
|---|---|---|---|
| GPIO_21 | IO | General-purpose I/O | F13 |
| GPIO_22 | IO | General-purpose I/O | G14 |
| GPIO_23 | IO | General-purpose I/O | R11 |
| GPIO_24 | IO | General-purpose I/O | N13 |
| GPIO_25 | IO | General-purpose I/O | N8 |
| GPIO_26 | IO | General-purpose I/O | K13 |
| GPIO_27 | IO | General-purpose I/O | P9 |
| GPIO_28 | IO | General-purpose I/O | P4 |
| GPIO_29 | IO | General-purpose I/O | G13 |
| GPIO_30 | IO | General-purpose I/O | C13 |
| GPIO_31 | IO | General-purpose I/O | R4 |
| GPIO_32 | IO | General-purpose I/O | P5 |
| GPIO_33 | IO | General-purpose I/O | R5 |
| GPIO_34 | IO | General-purpose I/O | P6 |
| GPIO_35 | IO | General-purpose I/O | R7 |
| GPIO_36 | IO | General-purpose I/O | P7 |
| GPIO_37 | IO | General-purpose I/O | R8 |
| GPIO_38 | IO | General-purpose I/O | P8 |
| GPIO_47 | IO | General-purpose I/O | N15 |
| I2C_SCL | IO | I2C Clock | G14, N4 |
| I2C_SDA | IO | I2C Data | F13, N5 |
| LVDS_TXP[0] | O | Differential data Out – Lane 0 | J14 |
| LVDS_TXM[0] | O | | J15 |
| LVDS_TXP[1] | O | Differential data Out – Lane 1 | K14 |
| LVDS_TXM[1] | O | | K15 |
| LVDS_CLKP | O | Differential clock Out | L14 |
| LVDS_CLKM | O | | L15 |
| LVDS_FRCLKP | O | Differential Frame Clock | M14 |
| LVDS_FRCLKM | O | | M15 |
| MCU_CLKOUT | O | Programmable clock given out to external MCU or the processor | N8 |
| MSS_UARTA_RX | I | Master Subsystem - UART A Receive | F14, N4, R11 |
| MSS_UARTA_TX | O | Master Subsystem - UART A Transmit | H14, N13, N5, R4 |
| MSS_UARTB_RX | IO | Master Subsystem - UART B Receive | N4, P4 |
| MSS_UARTB_TX | O | Master Subsystem - UART B Transmit | F14, H14, K13, N13, N5, P10, P7 |
| NDMM_EN | I | Debug Interface (Hardware In Loop) Enable - Active Low Signal | N13, N5 |
| NERROR_IN | I | Failsafe input to the device. Nerror output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by Firmware | N7 |
| NERROR_OUT | O | Open drain fail safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset. | N6 |
| PMIC_CLKOUT | O | Output Clock from IWR6843 device for PMIC | H13, K13, P9 |
| QSPI[0] | IO | QSPI Data Line #0 (Used with Serial Data Flash) | R13 |
| QSPI[1] | I | QSPI Data Line #1 (Used with Serial Data Flash) | N12 |
| QSPI[2] | I | QSPI Data Line #2 (Used with Serial Data Flash) | R14 |
| QSPI[3] | I | QSPI Data Line #3 (Used with Serial Data Flash) | P12 |
| QSPI_CLK | O | QSPI Clock (Used with Serial Data Flash) | R12 |
| QSPI_CLK_EXT | I | QSPI Clock (Used with Serial Data Flash) | H14 |

**Table 4-4. Signal Descriptions - Digital (continued)**

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BALL NO. |
|---|---|---|---|
| QSPI_CS_N | O | QSPI Chip Select (Used with Serial Data Flash) | P11 |
| RS232_RX | I | Debug UART (Operates as Bus Master) - Receive Signal | N4 |
| RS232_TX | O | Debug UART (Operates as Bus Master) - Transmit Signal | N5 |
| SOP[0] | I | Sense On Power - Line#0 | N13 |
| SOP[1] | I | Sense On Power - Line#1 | G13 |
| SOP[2] | I | Sense On Power - Line#2 | P9 |
| SPIA_CLK | IO | SPI Channel A - Clock | E13 |
| SPIA_CS_N | IO | SPI Channel A - Chip Select | E15 |
| SPIA_MISO | IO | SPI Channel A - Master In Slave Out | E14 |
| SPIA_MOSI | IO | SPI Channel A - Master Out Slave In | D13 |
| SPIB_CLK | IO | SPI Channel B - Clock | F14, R12 |
| SPIB_CS_N | IO | SPI Channel B Chip Select (Instance ID 0) | H14, P11 |
| SPIB_CS_N_1 | IO | SPI Channel B Chip Select (Instance ID 1) | G13, J13, P13 |
| SPIB_CS_N_2 | IO | SPI Channel B Chip Select (Instance ID 2) | G13, J13, N12 |
| SPIB_MISO | IO | SPI Channel B - Master In Slave Out | G14, R13 |
| SPIB_MOSI | IO | SPI Channel B - Master Out Slave In | F13, N12 |
| SPI_HOST_INTR | O | Out of Band Interrupt to an external host communicating over SPI | P13 |
| SYNC_IN | I | Low frequency Synchronization signal input | P4 |
| SYNC_OUT | O | Low Frequency Synchronization Signal output | G13, J13, K13, P4 |
| TCK | I | JTAG Test Clock | P10 |
| TDI | I | JTAG Test Data Input | R11 |
| TDO | O | JTAG Test Data Output | N13 |
| TMS | I | JTAG Test Mode Signal | N10 |
| TRACE_CLK | O | Debug Trace Output - Clock | N15 |
| TRACE_CTL | O | Debug Trace Output - Control | N14 |
| TRACE_DATA_0 | O | Debug Trace Output - Data Line | R4 |
| TRACE_DATA_1 | O | Debug Trace Output - Data Line | P5 |
| TRACE_DATA_2 | O | Debug Trace Output - Data Line | R5 |
| TRACE_DATA_3 | O | Debug Trace Output - Data Line | P6 |
| TRACE_DATA_4 | O | Debug Trace Output - Data Line | R7 |
| TRACE_DATA_5 | O | Debug Trace Output - Data Line | P7 |
| TRACE_DATA_6 | O | Debug Trace Output - Data Line | R8 |
| TRACE_DATA_7 | O | Debug Trace Output - Data Line | P8 |
| FRAME_START | O | Pulse signal indicating the start of each frame | N8, K13, P9 |
| CHIRP_START | O | Pulse signal indicating the start of each chirp | N8, K13, P9 |
| CHIRP_END | O | Pulse signal indicating the end of each chirp | N8, K13, P9 |
| ADC_VALID | O | When high, indicating valid ADC samples | P13, H13 |
| WARM_RESET | IO | Open drain fail safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset. | N9 |

**Table 4-5. Signal Descriptions - Analog**

| INTERFACE | SIGNAL NAME | PIN TYPE | DESCRIPTION | BALL NO. |
|---|---|---|---|---|
| Transmitters | TX1 | O | Single ended transmitter1 o/p | B4 |
| | TX2 | O | Single ended transmitter2 o/p | B6 |
| | TX3 | O | Single ended transmitter3 o/p | B8 |

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**Table 4-5. Signal Descriptions - Analog (continued)**

| INTERFACE | SIGNAL NAME | PIN TYPE | DESCRIPTION | BALL NO. |
|---|---|---|---|---|
| Receivers | RX1 | I | Single ended receiver1 i/p | M2 |
| | RX2 | I | Single ended receiver2 i/p | K2 |
| | RX3 | I | Single ended receiver3 i/p | H2 |
| | RX4 | I | Single ended receiver4 i/p | F2 |
| Reset | NRESET | I | Power on reset for chip. Active low | R3 |
| Reference Oscillator | CLKP | I | In XTAL mode: Differential port for reference crystal In External clock mode: Single ended input reference clock port | B15 |
| | CLKM | I | In XTAL mode: Differential port for reference crystal In External clock mode: Connect this port to ground | C15 |
| Reference clock | OSC_CLKOUT | O | Reference clock output from clocking sub system after cleanup PLL (1.4V output voltage swing). | A14 |
| Bandgap voltage | VBGAP | O | Device's Band Gap Reference Output | B10 |
| Power supply | VDDIN | Power | 1.2V digital power supply | H15, N11, P15, R6 |
| | VIN_SRAM | Power | 1.2V power rail for internal SRAM | G15 |
| | VNWA | Power | 1.2V power rail for SRAM array back bias | P14 |
| | VIOIN | Power | I/O Supply (3.3V or 1.8V): All CMOS I/Os would operate on this supply | R10, F15 |
| | VIOIN_18 | Power | 1.8V supply for CMOS IO | R9 |
| | VIN_18CLK | Power | 1.8V supply for clock module | B11 |
| | VIOIN_18DIFF | Power | 1.8V supply for LVDS port | D15 |
| | VPP | Power | Voltage supply for fuse chain | L13 |
| Power supply | VIN_13RF1 | Power | 1.3V Analog and RF supply,VIN_13RF1 and VIN_13RF2 could be shorted on the board | G5, H5, J5 |
| | VIN_13RF2 | Power | 1.3V Analog and RF supply | C2,D2 |
| | VIN_18BB | Power | 1.8V Analog base band power supply | K5, F5 |
| | VIN_18VCO | Power | 1.8V RF VCO supply | B12 |
| | VSS | Ground | Digital ground | L5, L6, L8, L10, K7, K8, K9, K10, K11, J6, J7, J8, J10, H7, H9, H11, G6, G7, G8, G10, F9, F11, E5, E6, E8, E10, E11, R15 |
| | VSSA | Ground | Analog ground | A1, A3, A5, A7, A9, A13, A15, B1, B3, B5, B7, B9, B14, C1, C3, C4, C5, C6, C7, C8, C9, C14, E1, E2, E3, F3, G1, G2, G3, H3, J1, J2, J3, K3, L1, L2, L3, M3, N1, N2, N3, R1 |
| Internal LDO output/inputs | VOUT_14APLL | O | Internal LDO output | A10 |
| | VOUT_14SYNTH | O | Internal LDO output | B13 |
| | VOUT_PA | IO | Internal LDO output | A2, B2 |
| Test and Debug output for pre-production phase. Can be pinned out on production hardware for field debug | Analog Test1 / GPADC1 | IO | Analog IO dedicated for ADC service | P1 |
| | Analog Test2 / GPADC2 | IO | Analog IO dedicated for ADC service | P2 |
| | Analog Test3 / GPADC3 | IO | Analog IO dedicated for ADC service | P3 |
| | Analog Test4 / GPADC4 | IO | Analog IO dedicated for ADC service | R2 |
| | ANAMUX / GPADC5 | IO | Analog IO dedicated for ADC service | C13 |
| | VSENSE / GPADC6 | IO | Analog IO dedicated for ADC service | D14 |

ADVANCE INFORMATION

# 5 Specifications

## 5.1 Absolute Maximum Ratings(1)(2)

| PARAMETERS | | MIN | MAX | UNIT |
|---|---|---|---|---|
| VDDIN | 1.2 V digital power supply | –0.5 | 1.4 | V |
| VIN_SRAM | 1.2 V power rail for internal SRAM | –0.5 | 1.4 | V |
| VNWA | 1.2 V power rail for SRAM array back bias | –0.5 | 1.4 | V |
| VIOIN | I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply. | –0.5 | 3.8 | V |
| VIOIN_18 | 1.8 V supply for CMOS IO | –0.5 | 2 | V |
| VIN_18CLK | 1.8 V supply for clock module | –0.5 | 2 | V |
| VIOIN_18DIFF | 1.8 V supply for LVDS port | –0.5 | 2 | V |
| VIN_13RF1 | 1.3 V Analog and RF supply, VIN_13RF1 and VIN_13RF2 could be shorted on the board. | –0.5 | 1.45 | V |
| VIN_13RF2 | | | | |
| VIN_13RF1 (1-V Internal LDO bypass mode) | Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed. | –0.5 | 1.4 | V |
| VIN_13RF2 (1-V Internal LDO bypass mode) | | | | |
| VIN_18BB | 1.8-V Analog baseband power supply | –0.5 | 2 | V |
| VIN_18VCO supply | 1.8-V RF VCO supply | –0.5 | 2 | V |
| Input and output voltage range | Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State) | –0.3V | VIOIN + 0.3 | V |
| | Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input | | VIOIN + 20% up to 20% of signal period | |
| CLKP, CLKM | Input ports for reference crystal | –0.5 | 2 | V |
| Clamp current | Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O. | –20 | 20 | mA |
| $T_J$ | Operating junction temperature range | –40 | 105 | ºC |
| $T_{STG}$ | Storage temperature range after soldered onto PC board | –55 | 150 | ºC |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to $V_{SS}$, unless otherwise noted.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM)(1) | ±1000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 TBDAddHistory | ±250 | |

(1) ANSI/ESDA/JEDEC JS0991 specification.

## 5.3 Power-On Hours (POH)(1)

| JUNCTION TEMPERATURE ($T_j$) | OPERATING CONDITION | NOMINAL CVDD VOLTAGE (V) | POWER-ON HOURS [POH] (HOURS) |
|---|---|---|---|
| 105ºC $T_j$ | TBD | 1.2 | 100,000 |

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

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## 5.4 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VDDIN | 1.2 V digital power supply | 1.14 | 1.2 | 1.32 | V |
| VIN_SRAM | 1.2 V power rail for internal SRAM | 1.14 | 1.2 | 1.32 | V |
| VNWA | 1.2 V power rail for SRAM array back bias | 1.14 | 1.2 | 1.32 | V |
| VIOIN | I/O supply (3.3 V or 1.8 V):<br>All CMOS I/Os would operate on this supply. | 3.15 | 3.3 | 3.45 | V |
| | | 1.71 | 1.8 | 1.89 | |
| VIOIN_18 | 1.8 V supply for CMOS IO | 1.71 | 1.8 | 1.9 | V |
| VIN_18CLK | 1.8 V supply for clock module | 1.71 | 1.8 | 1.9 | V |
| VIOIN_18DIFF | 1.8 V supply for LVDS port | 1.71 | 1.8 | 1.9 | V |
| VIN_13RF1 | 1.3 V Analog and RF supply. VIN_13RF1 and VIN_13RF2 could be shorted on the board | 1.23 | 1.3 | 1.36 | V |
| VIN_13RF2 | | | | | |
| VIN_13RF1 (1-V Internal LDO bypass mode) | Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed. | 0.95 | 1 | 1.05 | V |
| VIN_13RF2 (1-V Internal LDO bypass mode) | | | | | |
| VIN18BB | 1.8-V Analog baseband power supply | 1.71 | 1.8 | 1.9 | V |
| VIN_18VCO | 1.8V RF VCO supply | 1.71 | 1.8 | 1.9 | V |
| $V_{IH}$ | Voltage Input High (1.8 V mode) | 1.17 | | | V |
| | Voltage Input High (3.3 V mode) | 2.25 | | | |
| $V_{IL}$ | Voltage Input Low (1.8 V mode) | | | 0.3*VIOIN | V |
| | Voltage Input Low (3.3 V mode) | | | 0.62 | |
| $V_{OH}$ | High-level output threshold ($I_{OH}$ = 6 mA) | VIOIN – 450 | | | mV |
| $V_{OL}$ | Low-level output threshold ($I_{OL}$ = 6 mA) | | | 450 | mV |
| NRESET<br>SOP[2:0] | $V_{IL}$ (1.8V Mode) | | | 0.2 | V |
| | $V_{IH}$ (1.8V Mode) | 0.96 | | | |
| | $V_{IL}$ (3.3V Mode) | | | 0.3 | |
| | $V_{IH}$ (3.3V Mode) | 1.57 | | | |

## 5.5 Power Supply Specifications

Table 5-1 describes the four rails from an external power supply block of the IWR6843 device.

**Table 5-1. Power Supply Rails Characteristics**

| SUPPLY | DEVICE BLOCKS POWERED FROM THE SUPPLY | RELEVANT IOS IN THE DEVICE |
|---|---|---|
| 1.8 V | Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, LVDS | Input: VIN_18VCO, VIN18CLK, VIN_18BB, VIOIN_18DIFF, VIOIN_18<br>LDO Output: VOUT_14SYNTH, VOUT_14APLL |
| 1.3 V (or 1 V in internal LDO bypass mode) | Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution | Input: VIN_13RF2, VIN_13RF1<br>LDO Output: VOUT_PA |
| 3.3 V (or 1.8 V for 1.8 V I/O mode) | Digital I/Os | Input VIOIN |
| 1.2 V | Core Digital and SRAMs | Input: VDDIN, VIN_SRAM |

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## 5.6 Power Consumption Summary

Table 5-2 and Table 5-3 summarize the power consumption at the power terminals.

**Table 5-2. Maximum Current Ratings at Power Terminals**

| PARAMETER | SUPPLY NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Current consumption | VDDIN, VIN_SRAM, VNWA | Total current drawn by all nodes driven by 1.2V rail | | | 1000 | mA |
| | VIN_13RF1, VIN_13RF2 | Total current drawn by all nodes driven by 1.3V rail | | | 2000 | |
| | VIOIN_18, VIN_18CLK, VIOIN_18DIFF, VIN_18BB, VIN_18VCO | Total current drawn by all nodes driven by 1.8V rail | | | 850 | |
| | VIOIN | Total current drawn by all nodes driven by 3.3V rail | | | 50 | |

**Table 5-3. Average Power Consumption at Power Terminals**

| PARAMETER | CONDITION | | | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| Average power consumption | 1.0-V internal LDO bypass mode | 25% Duty Cycle | 1TX, 4RX | Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 128 chirps, 128 samples/chirp, 8-µs interchirp time (25% duty cycle), DSP active | | TBD | | W |
| | | | 2TX, 4RX(1) | | | TBD | | |
| | | 50% Duty Cycle | 1TX, 4RX | Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 256 chirps, 128 samples/chirp, 8-µs interchirp time (50% duty cycle), DSP active | | TBD | | |
| | | | 2TX, 4RX(1) | | | TBD | | |
| | 1.3-V internal LDO enabled mode | 25% Duty Cycle | 1TX, 4RX | Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 128 chirps, 128 samples/chirp, 8-µs interchirp time (25% duty cycle), DSP active | | TBD | | |
| | | | 2TX, 4RX(1) | | | TBD | | |
| | | 50% Duty Cycle | 1TX, 4RX | Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 256 chirps, 128 samples/chirp, 8-µs interchirp time (50% duty cycle), DSP active | | TBD | | |
| | | | 2TX, 4RX(1) | | | TBD | | |

(1) Two TX antennas are on simultaneously.

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## 5.7 RF Specification

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Receiver | Noise figure | 60 to 64 GHz | | 14 | | dB |
| | IF bandwidth(1) | | | | 10 | MHz |
| | A2D sampling rate (real) | | | | 25 | Msps |
| | A2D sampling rate (complex 1x) | | | | 12.5 | Msps |
| | A2D resolution | | | 12 | | Bits |
| | Idle Channel Spurs | | | –90 | | dBFS |
| Transmitter | Output power | | | 10 | | dBm |
| Clock subsystem | Frequency range | | 60 | | 64 | GHz |
| | Ramp rate | | | | 250 | MHz/µs |
| | Phase noise at 1-MHz offset | 60 to 64 GHz | | –92 | | dBc/Hz |

(1) The analog IF stages include high-pass filtering, with two independently configurable first-order high-pass corner frequencies. The set of available HPF corners is summarized as follows:

Available HPF Corner Frequencies (kHz)

| HPF1 | HPF2 |
|---|---|
| 175, 235, 350, 700 | 350, 700, 1400, 2800 |

The filtering performed by the digital baseband chain is targeted to provide:
- Less than ±0.5 dB pass-band ripple/droop, and
- Better than 60 dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

## 5.8 CPU Specifications

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| DSP Subsystem (C674 Family) | Clock Speed | | 600 | | MHz |
| | L1 Code Memory | | 32 | | KB |
| | L1 Data Memory | | 32 | | KB |
| | L2 Memory | | 256 | | KB |
| Master Controller Subsystem (R4F Family) | Clock Speed | | 200 | | MHz |
| | Tightly Coupled Memory - A (Program) | | 512 | | KB |
| | Tightly Coupled Memory - B (Data) | | 192 | | KB |
| Shared Memory | Shared L3 Memory | | 768 | | KB |

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## 5.9 Thermal Resistance Characteristics for FCBGA Package [ABL0161]

| THERMAL METRICS (1) | | °C/W (2) (3) |
|---|---|---|
| $R\Theta_{JC}$ | Junction-to-case | 4.92 |
| $R\Theta_{JB}$ | Junction-to-board | 6.57 |
| $R\Theta_{JA}$ | Junction-to-free air | 22.3 |
| $R\Theta_{JMA}$ | Junction-to-moving air | N/A (4) |
| $Psi_{JT}$ | Junction-to-package top | 4.92 |
| $Psi_{JB}$ | Junction-to-board | 6.4 |

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

A junction temperature of 105ºC is assumed.
(4) N/A = not applicable

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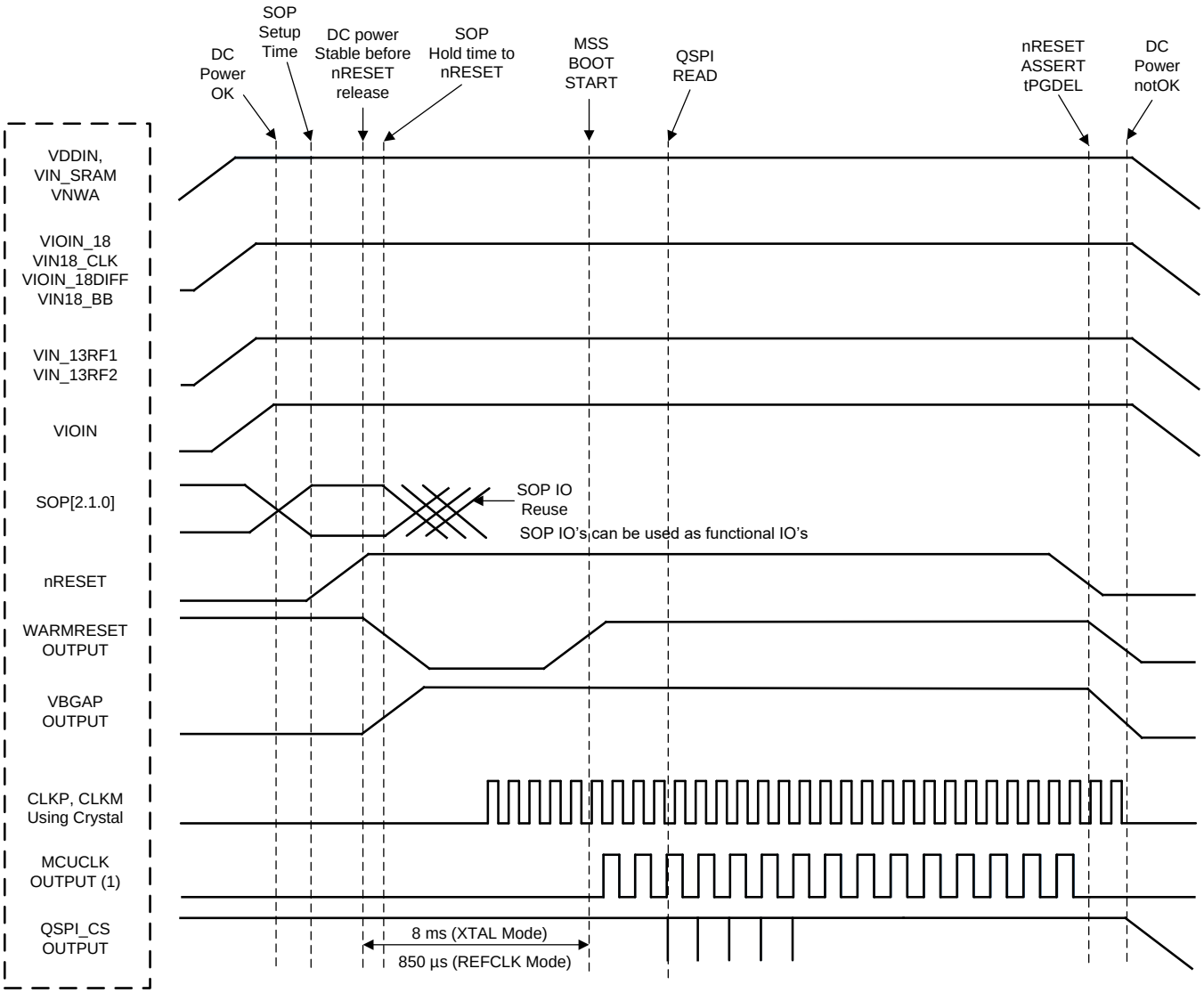
## 5.10 Timing and Switching Characteristics

### 5.10.1 Power Supply Sequencing and Reset Timing

The IWR6843 device expects all external voltage rails to be stable before reset is deasserted. Figure 5-1 describes the device wake-up sequence.




(1) MCU_CLK_OUT in autonomous mode, where IWR6843 application is booted from the serial flash, MCU_CLK_OUT is not enabled by default by the device bootloader.

**Figure 5-1. Device Wake-up Sequence**

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### 5.10.2 Input Clocks and Oscillators

#### 5.10.2.1 Clock Specifications

The IWR6843 requires external clock source (that is, a 40-MHz crystal or external oscillator to CLKP) for initial boot and as a reference for an internal APLL hosted in the device. An external crystal is connected to the device pins. Figure 5-2 shows the crystal implementation.

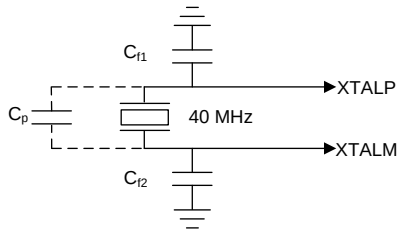


**Figure 5-2. Crystal Implementation**

**NOTE**

The load capacitors, $C_{f1}$ and $C_{f2}$ in Figure 5-2, should be chosen such that Equation 1 is satisfied. $C_L$ in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

Table 5-4 lists the electrical characteristics of the clock crystal.

**Table 5-4. Crystal Electrical Characteristics (Oscillator Mode)**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_P$ | Parallel resonance crystal frequency | | 40 | | MHz |
| $C_L$ | Crystal load capacitance | 5 | 8 | 12 | pF |
| ESR | Crystal ESR | | | 50 | Ω |
| Temperature range | Expected temperature range of operation | –40 | | 105 | ºC |
| Frequency tolerance | Crystal frequency tolerance(1)(2)(3) | –50 | | 50 | ppm |
| Drive level | | | 50 | 200 | µW |

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
(3) Crystal tolerance affects radar sensor accuracy.

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In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 40-MHz clock is fed externally. Table 5-5 lists the electrical characteristics of the external clock signal.

**Table 5-5. External Clock Mode Specifications**

| PARAMETER | | SPECIFICATION | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referred to 40 MHz | Frequency | | 40 | | MHz |
| | AC-Amplitude | 700 | | 1200 | mV (pp) |
| | DC-$V_{il}$ | 0.00 | | 0.20 | V |
| | DC-$V_{ih}$ | 1.6 | | 1.95 | V |
| | Phase Noise at 1 kHz | | | –132 | dBc/Hz |
| | Phase Noise at 10 kHz | | | –143 | dBc/Hz |
| | Phase Noise at 100 kHz | | | –152 | dBc/Hz |
| | Phase Noise at 1 MHz | | | –153 | dBc/Hz |
| | Duty Cycle | 35 | | 65 | % |
| | Freq Tolerance | –50 | | 50 | ppm |
| | Freq Tolerance | –50 | | 50 | ppm |

ADVANCE INFORMATION

### 5.10.3 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

#### 5.10.3.1 Peripheral Description

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The MibSPI/SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit baud clock generator
- SPICLK can be internally-generated (master mode) or received from an external clock source (slave mode)
- Each word transferred can have a unique format.
- SPI I/Os not used in the communication can be used as digital input/output signals

#### 5.10.3.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 256 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

Table 5-7 and Table 5-8 assume the operating conditions stated in Table 5-6.

**Table 5-6. SPI Timing Conditions**

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input Conditions | | | | | |
| $t_R$ | Input rise time | 1 | | 3 | ns |
| $t_F$ | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| $C_{LOAD}$ | Output load capacitance | 2 | | 15 | pF |

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**Table 5-7. SPI Master Mode Switching Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)**

| NO. | PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK(4) | | 25 | | $256t_{c(VCLK)}$ | ns |
| 2(4) | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | |
| 3(4) | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | |
| 4(4) | $t_{d(SPCH-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0) | | $0.5t_{c(SPC)M} - 3$ | | | ns |
| | $t_{d(SPCL-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1) | | $0.5t_{c(SPC)M} - 3$ | | | |
| 5(4) | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0) | | $0.5t_{c(SPC)M} - 10.5$ | | | ns |
| | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1) | | $0.5t_{c(SPC)M} - 10.5$ | | | |
| 6(5) | $t_{C2TDELAY}$ | Setup time CS active until SPICLK high (clock polarity = 0) | CSHOLD = 0 | $(C2TDELAY+2)*t_{c(VCLK)} - 7.5$ | | $(C2TDELAY+2) * t_{c(VCLK)} + 7$ | ns |
| | | | CSHOLD = 1 | $(C2TDELAY+3) * t_{c(VCLK)} - 7.5$ | | $(C2TDELAY+3) * t_{c(VCLK)} + 7$ | |
| | | Setup time CS active until SPICLK low (clock polarity = 1) | CSHOLD = 0 | $(C2TDELAY+2)*t_{c(VCLK)} - 7.5$ | | $(C2TDELAY+2) * t_{c(VCLK)} + 7$ | |
| | | | CSHOLD = 1 | $(C2TDELAY+3) * t_{c(VCLK)} - 7.5$ | | $(C2TDELAY+3) * t_{c(VCLK)} + 7$ | |
| 7(5) | $t_{T2CDELAY}$ | Hold time, SPICLK low until CS inactive (clock polarity = 0) | | $0.5*t_{c(SPC)M} + (T2CDELAY + 1) *t_{c(VCLK)} - 7$ | | $0.5*t_{c(SPC)M} + (T2CDELAY + 1) * t_{c(VCLK)} + 7.5$ | ns |
| | | Hold time, SPICLK high until CS inactive (clock polarity = 1) | | $0.5*t_{c(SPC)M} + (T2CDELAY + 1) *t_{c(VCLK)} - 7$ | | $0.5*t_{c(SPC)M} + (T2CDELAY + 1) * t_{c(VCLK)} + 7.5$ | |
| 8(4) | $t_{su(SOMI-SPCL)M}$ | Setup time, SPISOMI before SPICLK low (clock polarity = 0) | | 5 | | | ns |
| | $t_{su(SOMI-SPCH)M}$ | Setup time, SPISOMI before SPICLK high (clock polarity = 1) | | 5 | | | |
| 9(4) | $t_{h(SPCL-SOMI)M}$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0) | | 3 | | | ns |
| | $t_{h(SPCH-SOMI)M}$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1) | | 3 | | | |

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared (where x= 0 or 1).
(2) $t_{c(MSS\_VCLK)}$ = master subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(MSS\_VCLK)} \geq 25ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS\_VCLK)} \geq 25ns$.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

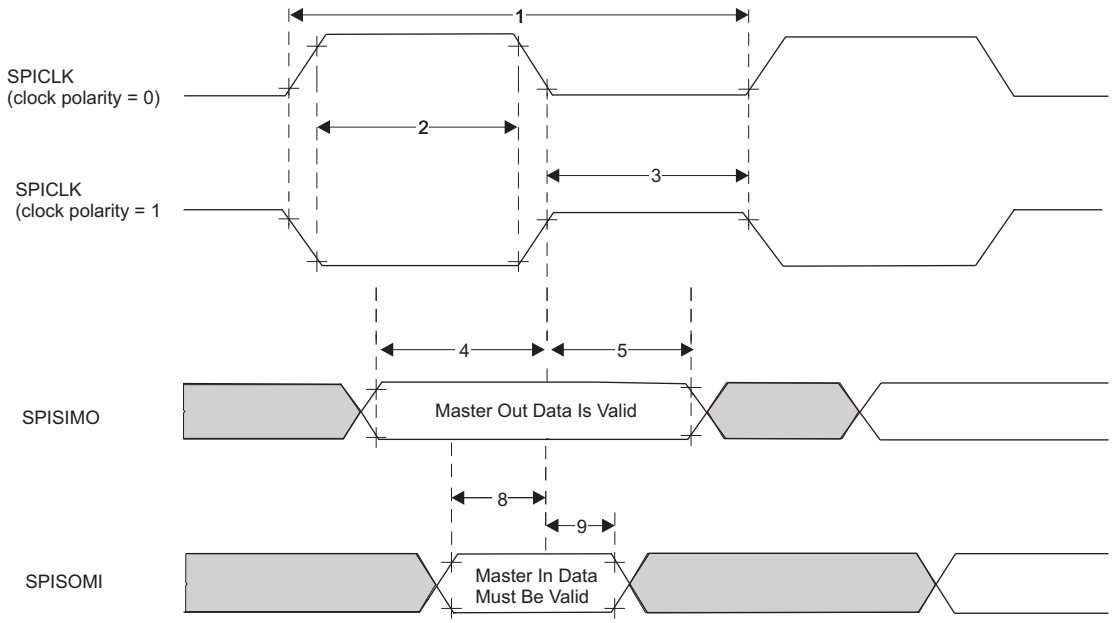


**Figure 5-3. SPI Master Mode External Timing (CLOCK PHASE = 0)**

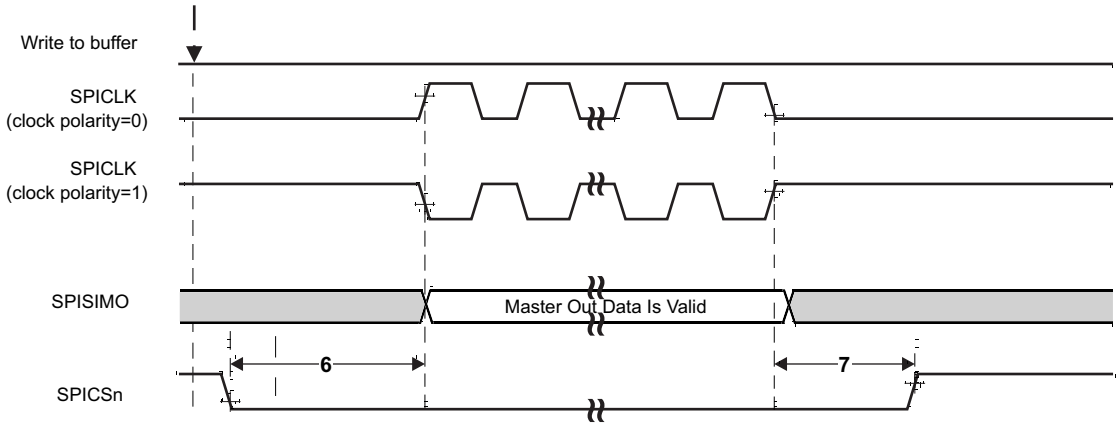


**Figure 5-4. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)**

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**Table 5-8. SPI Master Mode Switching Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)**

| NO. | PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK(4) | | 25 | | $256t_{c(VCLK)}$ | ns |
| 2(4) | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | |
| 3(4) | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | |
| 4(4) | $t_{d(SPCH-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0) | | $0.5t_{c(SPC)M} - 3$ | | | ns |
| | $t_{d(SPCL-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1) | | $0.5t_{c(SPC)M} - 3$ | | | |
| 5(4) | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0) | | $0.5t_{c(SPC)M} - 10.5$ | | | ns |
| | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1) | | $0.5t_{c(SPC)M} - 10.5$ | | | |
| 6(5) | $t_{C2TDELAY}$ | Setup time CS active until SPICLK high (clock polarity = 0) | CSHOLD = 0 | $0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7$ | | $0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$ | ns |
| | | | CSHOLD = 1 | $0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7$ | | $0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$ | |
| | | Setup time CS active until SPICLK low (clock polarity = 1) | CSHOLD = 0 | $0.5*t_{c(SPC)M} + (C2TDELAY+2)*t_{c(VCLK)} - 7$ | | $0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$ | |
| | | | CSHOLD = 1 | $0.5*t_{c(SPC)M} + (C2TDELAY+3)*t_{c(VCLK)} - 7$ | | $0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} + 7.5$ | |
| 7(5) | $t_{T2CDELAY}$ | Hold time, SPICLK low until CS inactive (clock polarity = 0) | | $(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$ | | $(T2CDELAY + 1) *t_{c(VCLK)} + 7$ | ns |
| | | Hold time, SPICLK high until CS inactive (clock polarity = 1) | | $(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$ | | $(T2CDELAY + 1) *t_{c(VCLK)} + 7$ | |
| 8(4) | $t_{su(SOMI-SPCL)M}$ | Setup time, SPISOMI before SPICLK low (clock polarity = 0) | | 5 | | | ns |
| | $t_{su(SOMI-SPCH)M}$ | Setup time, SPISOMI before SPICLK high (clock polarity = 1) | | 5 | | | |
| 9(4) | $t_{h(SPCL-SOMI)M}$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0) | | 3 | | | ns |
| | $t_{h(SPCH-SOMI)M}$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1) | | 3 | | | |

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set ( where x = 0 or 1 ).
(2) $t_{c(MSS\_VCLK)}$ = master subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(MSS\_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS\_VCLK)} \geq 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

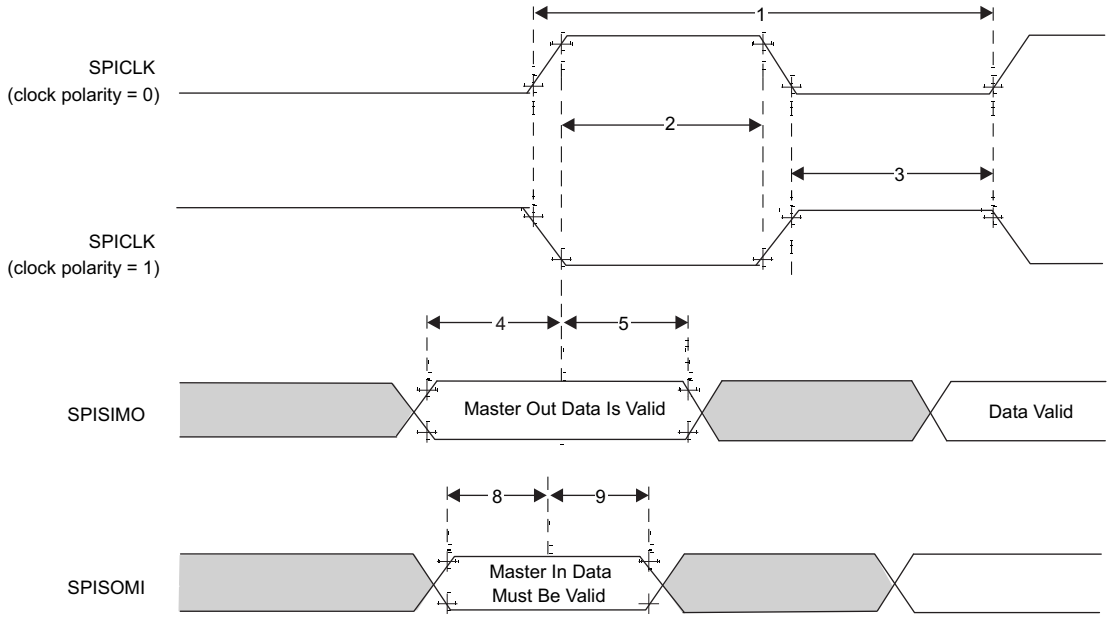


**Figure 5-5. SPI Master Mode External Timing (CLOCK PHASE = 1)**

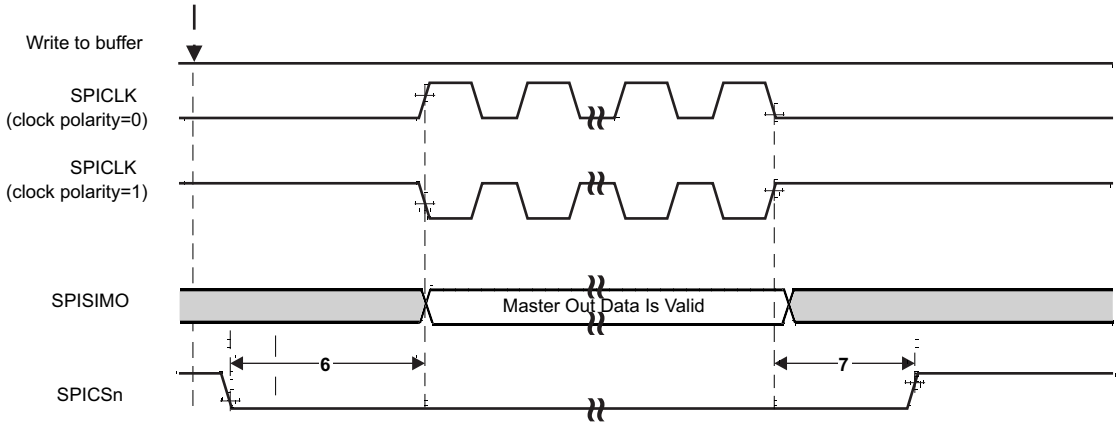


**Figure 5-6. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)**

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### 5.10.3.3 SPI Slave Mode I/O Timings

**Table 5-9. SPI Slave Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)**

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(SPC)S}$ | Cycle time, SPICLK(4) | 25 | | | ns |
| 2(5) | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high (clock polarity = 0) | 10 | | | ns |
| | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low (clock polarity = 1) | 10 | | | |
| 3(5) | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low (clock polarity = 0) | 10 | | | ns |
| | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high (clock polarity = 1) | 10 | | | |
| 4(5) | $t_{d(SPCH-SOMI)S}$ | Delay time, SPISOMI valid after SPICLK high (clock polarity = 0) | | | 10 | ns |
| | $t_{d(SPCL-SOMI)S}$ | Delay time, SPISOMI valid after SPICLK low (clock polarity = 1) | | | 10 | |
| 5(5) | $t_{h(SPCH-SOMI)S}$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0) | 2 | | | ns |
| | $t_{h(SPCL-SOMI)S}$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1) | 2 | | | |
| 4(5) | $t_{d(SPCH-SOMI)S}$ | Delay time, SPISOMI valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1) | | | 10 | ns |
| | $t_{d(SPCL-SOMI)S}$ | Delay time, SPISOMI valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1) | | | 10 | |
| 5(5) | $t_{h(SPCH-SOMI)S}$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1) | 2 | | | ns |
| | $t_{h(SPCL-SOMI)S}$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1) | 2 | | | |
| 6(5) | $t_{su(SIMO-SPCL)S}$ | Setup time, SPISIMO before SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1) | 3 | | | ns |
| | $t_{su(SIMO-SPCH)S}$ | Setup time, SPISIMO before SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1) | 3 | | | |
| 7(5) | $t_{h(SPCL-SIMO)S}$ | Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1) | 1 | | | ns |
| | $t_{h(SPCL-SIMO)S}$ | Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1) | 1 | | | |

(1) The MASTER bit (SPIGCRx.0) is cleared ( where x = 0 or 1 ).
(2) The CLOCK PHASE bit (SPIFMTx.16) is either cleared or set for CLOCK PHASE = 0 or CLOCK PHASE = 1 respectively.
(3) $t_{c(MSS\_VCLK)}$ = master subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(4) When the SPI is in Slave mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(MSS\_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.For PS values of 0: $t_{c(SPC)S} = 2t_{c(MSS\_VCLK)} \geq 25$ ns.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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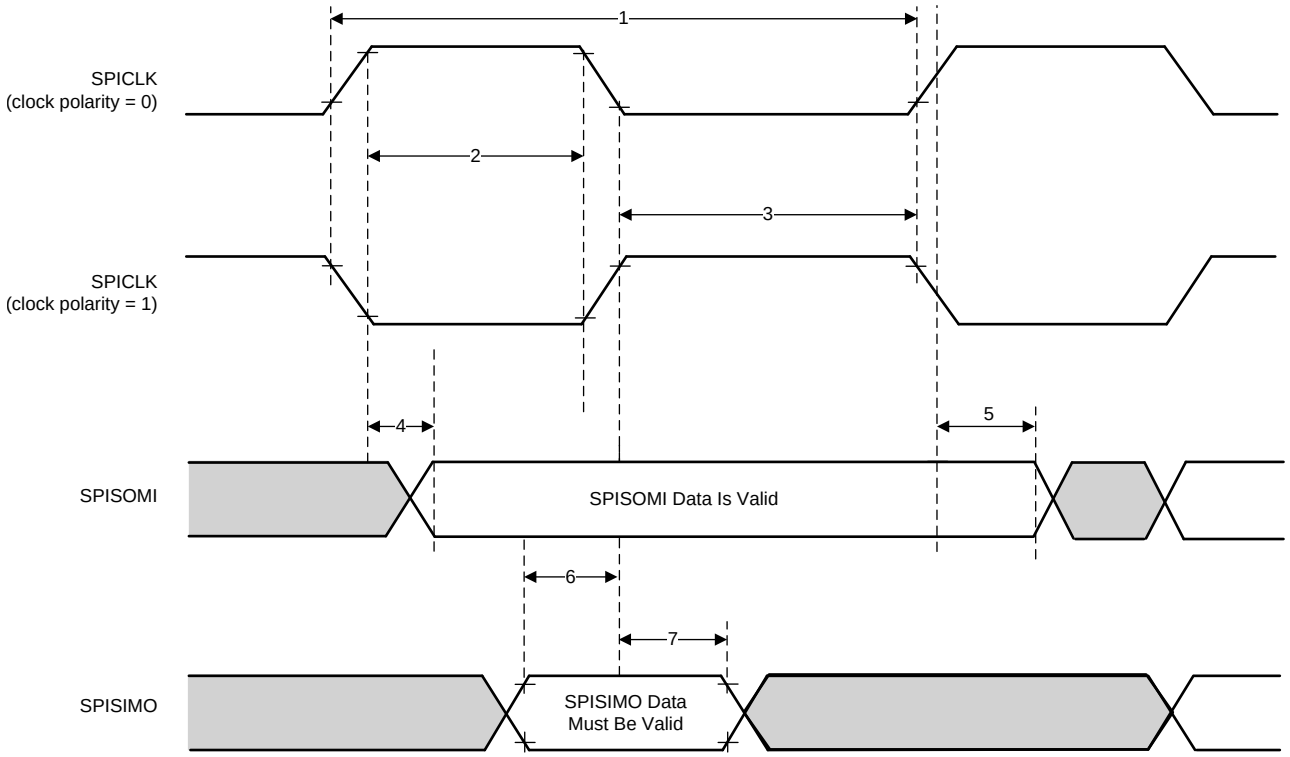


**Figure 5-7. SPI Slave Mode External Timing (CLOCK PHASE = 0)**

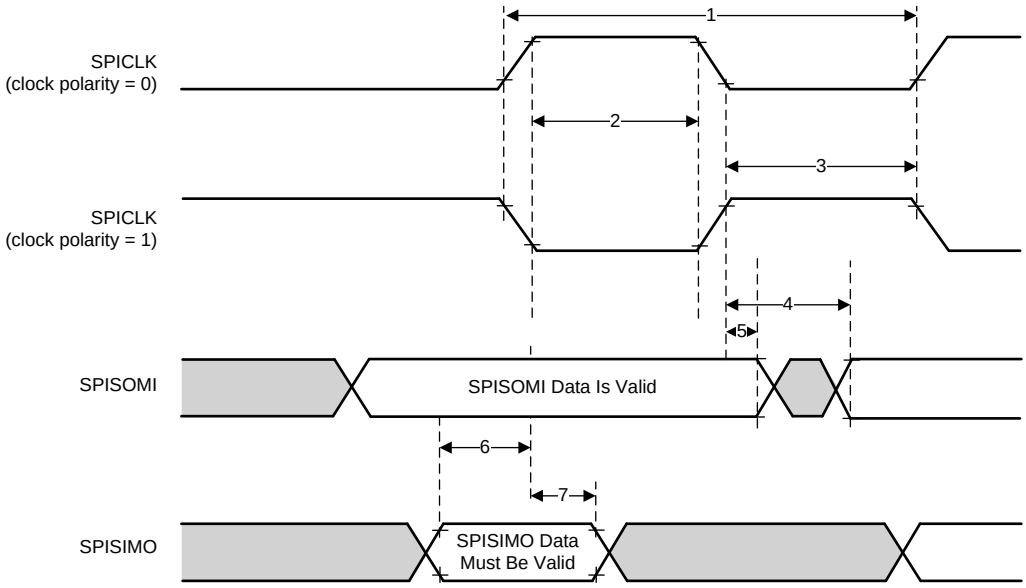


**Figure 5-8. SPI Slave Mode External Timing (CLOCK PHASE = 1)**

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### 5.10.3.4 Typical Interface Protocol Diagram (Slave Mode)

1. Host should ensure that there is a delay of two SPI clocks between CS going low and start of SPI clock.
2. Host should ensure that CS is toggled for every 16 bits of transfer through SPI.

Figure 5-9 shows the SPI communication timing of the typical interface protocol.

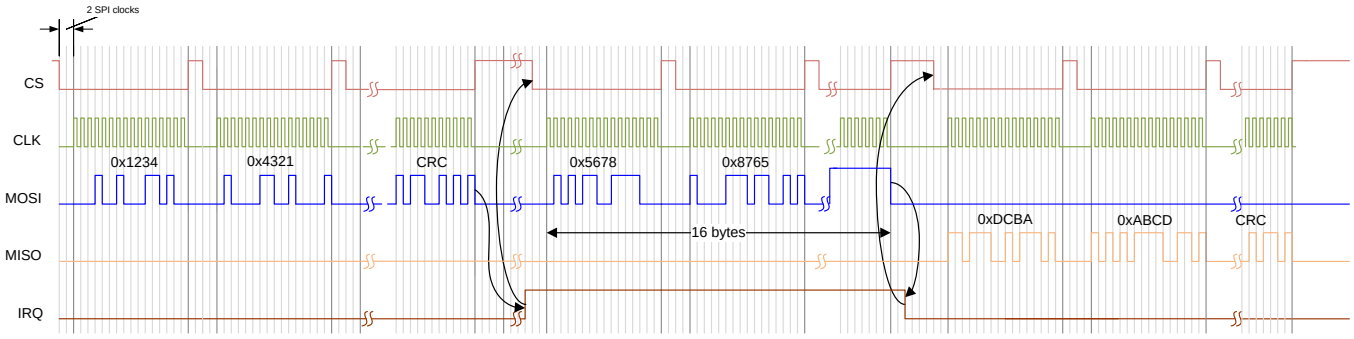


**Figure 5-9. SPI Communication**

### 5.10.4 LVDS Interface Configuration

The supported IWR6843 LVDS lane configuration is two Data lanes (LVDS_TXP/M), one Bit Clock lane (LVDS_CLKP/M) and one Frame clock lane (LVDS_FRCLKP/M). The LVDS interface is used for debugging. The LVDS interface supports the following data rates:

- 900 Mbps (450 MHz DDR Clock)
- 600 Mbps (300 MHz DDR Clock)
- 450 Mbps (225 MHz DDR Clock)
- 400 Mbps (200 MHz DDR Clock)
- 300 Mbps (150 MHz DDR Clock)
- 225 Mbps (112.5 MHz DDR Clock)
- 150 Mbps (75 MHz DDR Clock)

Note that the bit clock is in DDR format and hence the numbers of toggles in the clock is equivalent to data.

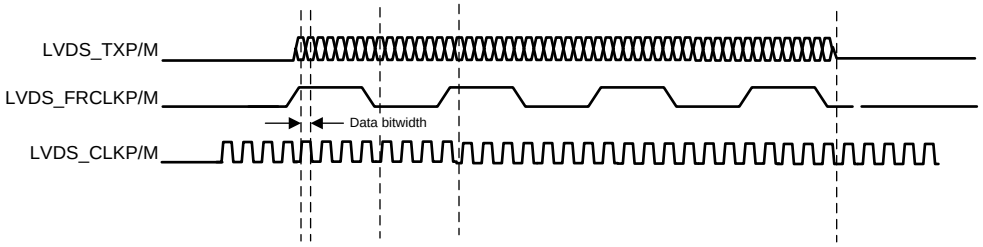


**Figure 5-10. LVDS Interface Lane Configuration And Relative Timings**

#### 5.10.4.1 LVDS Interface Timings

**Table 5-10. LVDS Electrical Characteristics**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Duty Cycle Requirements | max 1 pF lumped capacitive load on LVDS lanes | 48% | | 52% | |
| Output Differential Voltage | peak-to-peak single-ended with 100 Ω resistive load between differential pairs | 250 | | 450 | mV |
| Output Offset Voltage | | 1125 | | 1275 | mV |
| Trise and Tfall | 20%-80%, 900 Mbps | | 330 | | ps |
| Jitter (pk-pk) | 900 Mbps | | 80 | | ps |

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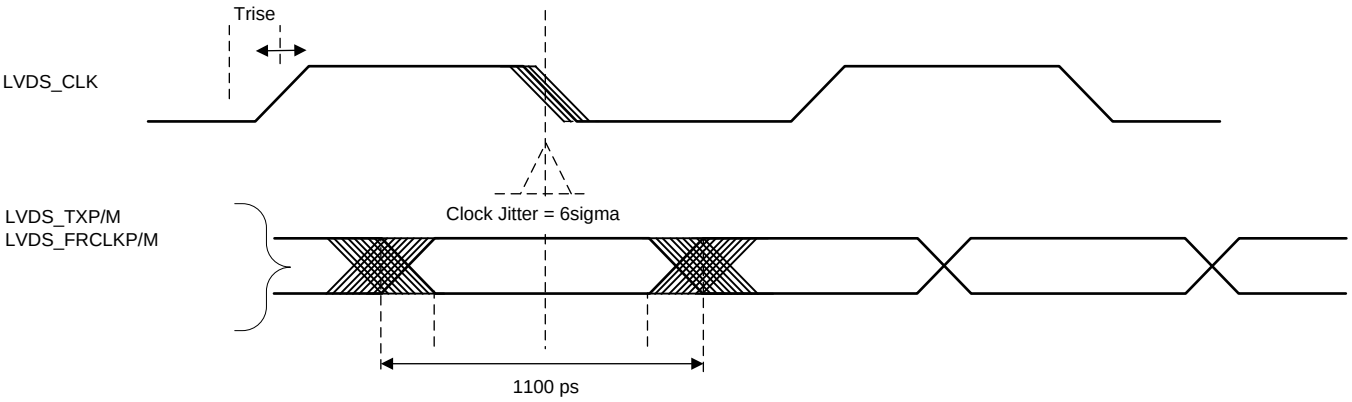


**Figure 5-11. Timing Parameters**

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### 5.10.5 General-Purpose Input/Output

Table 5-11 lists the switching characteristics of output timing relative to load capacitance.

**Table 5-11. Switching Characteristics for Output Timing versus Load Capacitance ($C_L$)(1)(2)**

| PARAMETER | | TEST CONDITIONS | | VIOIN = 1.8V | VIOIN = 3.3V | UNIT |
|---|---|---|---|---|---|---|
| $t_r$ | Max rise time | Slew control = 0 | $C_L$ = 20 pF | 2.8 | 3.0 | ns |
| | | | $C_L$ = 50 pF | 6.4 | 6.9 | |
| | | | $C_L$ = 75 pF | 9.4 | 10.2 | |
| $t_f$ | Max fall time | | $C_L$ = 20 pF | 2.8 | 2.8 | ns |
| | | | $C_L$ = 50 pF | 6.4 | 6.6 | |
| | | | $C_L$ = 75 pF | 9.4 | 9.8 | |
| $t_r$ | Max rise time | Slew control = 1 | $C_L$ = 20 pF | 3.3 | 3.3 | ns |
| | | | $C_L$ = 50 pF | 6.7 | 7.2 | |
| | | | $C_L$ = 75 pF | 9.6 | 10.5 | |
| $t_f$ | Max fall time | | $C_L$ = 20 pF | 3.1 | 3.1 | ns |
| | | | $C_L$ = 50 pF | 6.6 | 6.6 | |
| | | | $C_L$ = 75 pF | 9.6 | 9.6 | |

(1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

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### 5.10.6 Controller Area Network - Flexible Data-rate (CAN-FD)

The CAN-FD module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The CAN-FD has the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1
- Full CAN FD support (up to 64 data bytes per frame)
- AUTOSAR and SAE J1939 support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 11-bit filter elements
- Internal Loopback mode for self-test
- Mask-able interrupts, two interrupt lines
- Two clock domains (CAN clock / Host clock)
- Parity / ECC support - Message RAM single error correction and double error detection (SECDED) mechanism
- Full Message Memory capacity (4352 words).

**Table 5-12. Dynamic Characteristics for the CANx TX and RX Pins**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d(CAN\_FD\_tx)}$ | Delay time, transmit shift register to CAN_FD_tx pin(1) | | | 15 | ns |
| $t_{d(CAN\_FD\_rx)}$ | Delay time, CAN_FD_rx pin to receive shift register(1) | | | 10 | ns |

(1) These values do not include rise/fall times of the output buffer.

### 5.10.7 Serial Communication Interface (SCI)

The SCI has the following features:

- Standard universal asynchronous receiver-transmitter (UART) communication
- Standard non-return to zero (NRZ) format
- Double-buffered receive and transmit functions
- Asynchronous or iso-synchronous communication modes with no CLK pin
- Capability to use Direct Memory Access (DMA) for transmit and receive data
- Two external pins: RS232_RX and RS232_TX

**Table 5-13. SCI Timing Requirements**

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| f(baud) | Supported baud rate at 20 pF | | 921.6 | | kHz |

### 5.10.8 Inter-Integrated Circuit Interface (I2C)

The inter-integrated circuit (I2C) module is a multimaster communication module providing an interface between devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an $I^2C$-bus™. This module will support any slave or master I2C compatible device.

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - General call
  - START byte
  - Multi-master transmitter/ slave receiver mode
  - Multi-master receiver/ slave transmitter mode
  - Combined master transmit/receive and receive/transmit mode
  - Transfer rates of 100 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

**NOTE**

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the slave address second byte every time it sends the slave address first byte)

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**Table 5-14. I2C Timing Requirements(1)**

| | | STANDARD MODE | | FAST MODE | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | µs |
| $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | µs |
| $t_{h(SCLL-SDAL)}$ | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | µs |
| $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | µs |
| $t_{su(SDA-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100 | | µs |
| $t_{h(SCLL-SDA)}$ | Hold time, SDA valid after SCL low | 0 | 3.45(1) | 0 | 0.9 | µs |
| $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | µs |
| $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4 | | 0.6 | | µs |
| $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | | | 0 | 50 | ns |
| $C_b$(2)(3) | Capacitive load for each bus line | | 400 | | 400 | pF |

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum th(SDA-SCLL) for I2C bus devices has only to be met if the device does not stretch the low period (tw(SCLL)) of the SCL signal.
(3) $C_b$ = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

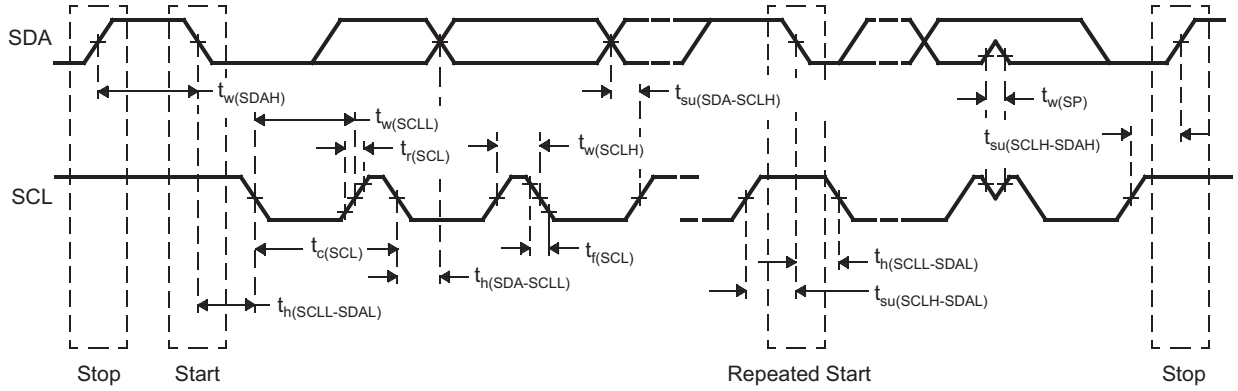


**Figure 5-12. I2C Timing Diagram**

**NOTE**

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum th(SDA-SCLL) has only to be met if the device does not stretch the LOW period (tw(SCLL)) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.

### 5.10.9 Quad Serial Peripheral Interface (QSPI)

The quad serial peripheral interface (QSPI™) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a master only. The QSPI in the device is primarily intended for fast booting from quad-SPI flash memories.

The QSPI supports the following features:

- Programmable clock divider
- Six-pin interface
- Programmable length (from 1 to 128 bits) of the words transferred
- Programmable number (from 1 to 4096) of the words transferred
- Support for 3-, 4-, or 6-pin SPI interface
- Optional interrupt generation on word or frame (number of words) completion
- Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles

Table 5-16 and Table 5-17 assume the operating conditions stated in Table 5-15.

**Table 5-15. QSPI Timing Conditions**

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input Conditions | | | | | |
| $t_R$ | Input rise time | 1 | | 3 | ns |
| $t_F$ | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| $C_{LOAD}$ | Output load capacitance | 2 | | 15 | pF |

**Table 5-16. Timing Requirements for QSPI Input (Read) Timings(1)(2)**

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{su(D-SCLK)}$ | Setup time, d[3:0] valid before falling sclk edge | 7.3 | | | ns |
| $t_{h(SCLK-D)}$ | Hold time, d[3:0] valid after falling sclk edge | 1.5 | | | ns |
| $t_{su(D-SCLK)}$ | Setup time, final d[3:0] bit valid before final falling sclk edge | 7.3 – P(3) | | | ns |
| $t_{h(SCLK-D)}$ | Hold time, final d[3:0] bit valid after final falling sclk edge | 1.5 + P(3) | | | ns |

(1) Clock Mode 0 (clk polarity = 0 ; clk phase = 0 ) is the mode of operation.
(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.
(3) P = SCLK period in ns.

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**Table 5-17. QSPI Switching Characteristics**

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Q1 | $t_{c(SCLK)}$ | Cycle time, sclk | 25 | | | ns |
| Q2 | $t_{w(SCLKL)}$ | Pulse duration, sclk low | Y*P – 3 (1) (2) | | | ns |
| Q3 | $t_{w(SCLKH)}$ | Pulse duration, sclk high | Y*P – 3 (1) | | | ns |
| Q4 | $t_{d(CS-SCLK)}$ | Delay time, sclk falling edge to cs active edge | –M*P – 1 (1) (3) | | –M*P + 2.5 (1) (3) | ns |
| Q5 | $t_{d(SCLK-CS)}$ | Delay time, sclk falling edge to cs inactive edge | N*P – 1 (1) (3) | | N*P + 2.5 (1) (3) | ns |
| Q6 | $t_{d(SCLK-D1)}$ | Delay time, sclk falling edge to d[1] transition | –3.5 | | 7 | ns |
| Q7 | $t_{ena(CS-D1LZ)}$ | Enable time, cs active edge to d[1] driven (lo-z) | –P – 4 (3) | | –P +1 (3) | ns |
| Q8 | $t_{dis(CS-D1Z)}$ | Disable time, cs active edge to d[1] tri-stated (hi-z) | –P – 4 (3) | | –P +1 (3) | ns |
| Q9 | $t_{d(SCLK-D1)}$ | Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only) | –3.5 – P (3) | | 7 – P (3) | ns |
| Q12 | $t_{su(D-SCLK)}$ | Setup time, d[3:0] valid before falling sclk edge | 7.3 | | | ns |
| Q13 | $t_{h(SCLK-D)}$ | Hold time, d[3:0] valid after falling sclk edge | 1.5 | | | ns |
| Q14 | $t_{su(D-SCLK)}$ | Setup time, final d[3:0] bit valid before final falling sclk edge | 7.3 — P (3) | | | ns |
| Q15 | $t_{h(SCLK-D)}$ | Hold time, final d[3:0] bit valid after final falling sclk edge | 1.5 + P (3) | | | ns |

(1) The Y parameter is defined as follows: If DCLK_DIV is 0 or ODD then, Y equals 0.5. If DCLK_DIV is EVEN then, Y equals (DCLK_DIV/2) / (DCLK_DIV+1). For best performance, it is recommended to use a DCLK_DIV of 0 or ODD to minimize the duty cycle distortion. All required details about clock division factor DCLK_DIV can be found in the device-specific Technical Reference Manual.
(2) P = SCLK period in ns.
(3) M = QSPI_SPI_DC_REG.DDx + 1, N = 2

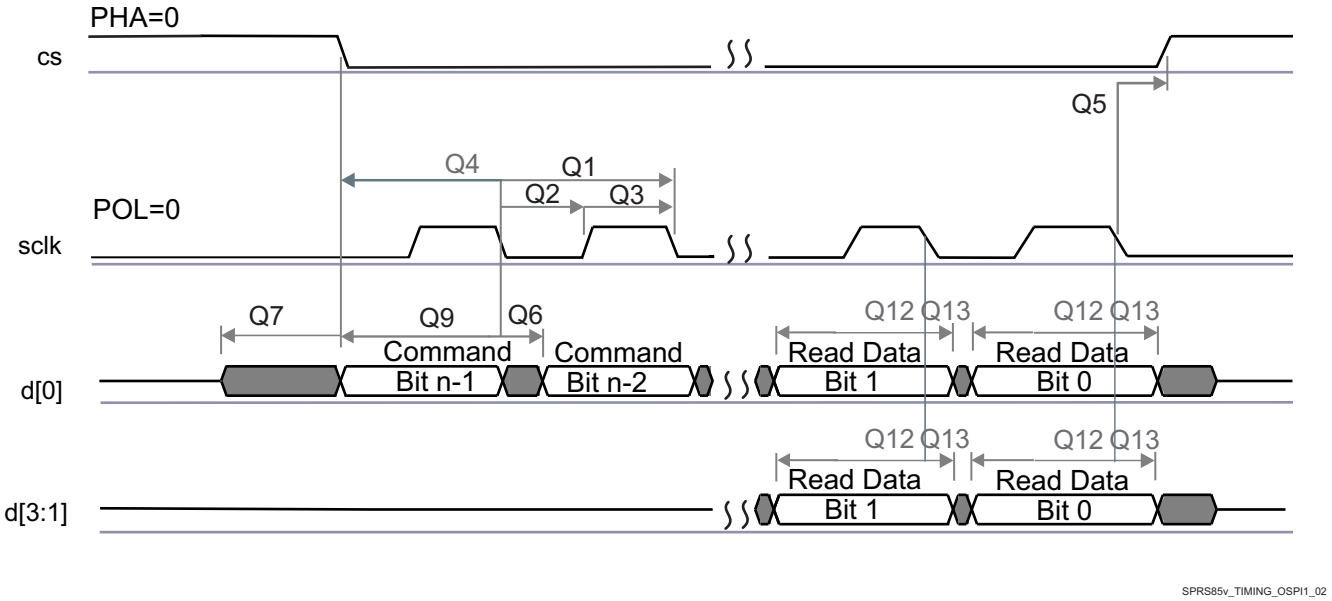


**Figure 5-13. QSPI Read (Clock Mode 0)**

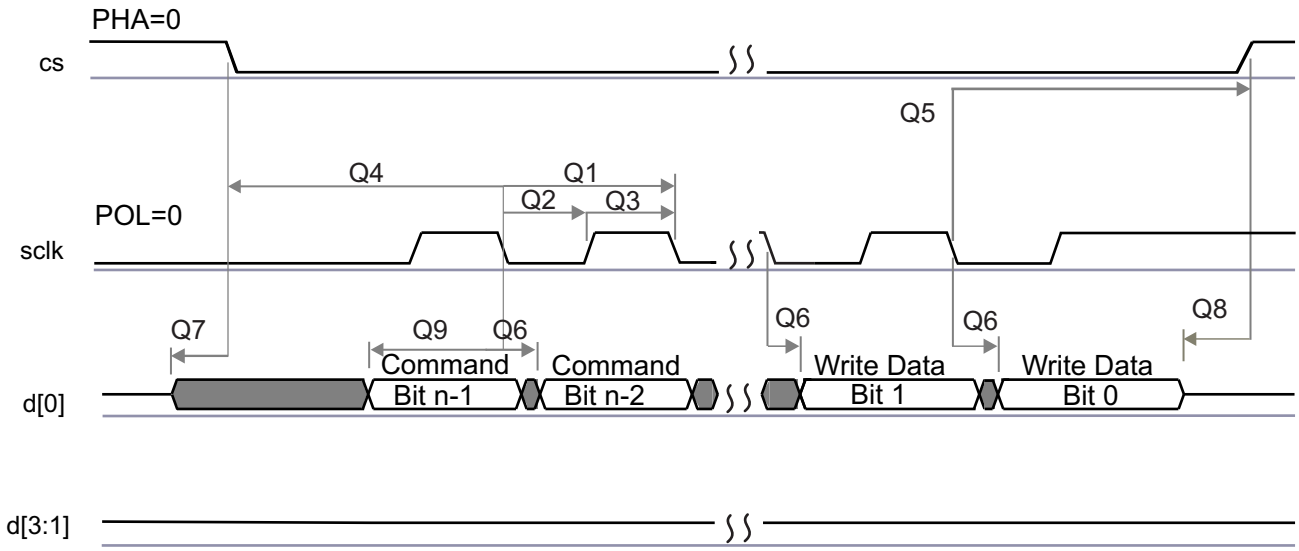


**Figure 5-14. QSPI Write (Clock Mode 0)**

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### 5.10.10 ETM Trace Interface

Table 5-19 and assume the recommended operating conditions stated in Table 5-18.

**Table 5-18. ETMTRACE Timing Conditions**

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Output Conditions | | | | | |
| $C_{LOAD}$ | Output load capacitance | 2 | | 20 | pF |

**Table 5-19. ETM TRACE Switching Characteristics**

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{cyc(ETM)}$ | Cycle time, TRACECLK period | 20 | | | ns |
| 2 | $t_{h(ETM)}$ | Pulse Duration, TRACECLK High | 9 | | | ns |
| 3 | $t_{l(ETM)}$ | Pulse Duration, TRACECLK Low | 9 | | | ns |
| 4 | $t_{r(ETM)}$ | Clock and data rise time | | | 3.3 | ns |
| 5 | $t_{f(ETM)}$ | Clock and data fall time | | | 3.3 | ns |
| 6 | $t_{d(ETMTRACECLKH-ETMDATAV)}$ | Delay time, ETM trace clock high to ETM data valid | 1 | | 7 | ns |
| 7 | $t_{d(ETMTRACECLKl-ETMDATAV)}$ | Delay time, ETM trace clock low to ETM data valid | 1 | | 7 | ns |

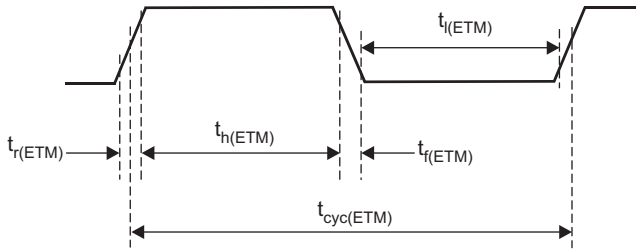


**Figure 5-15. ETMTRACECLKOUT Timing**

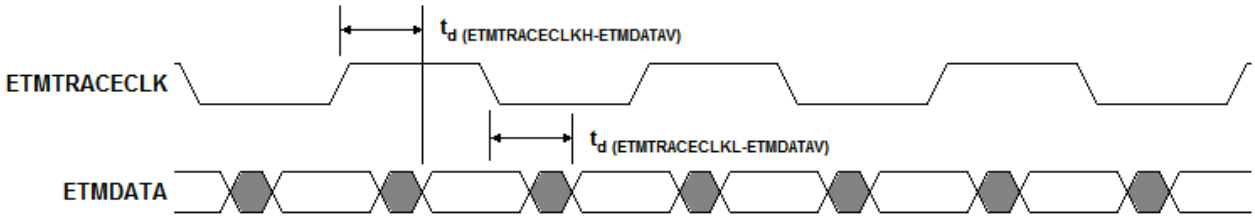


**Figure 5-16. ETMDATA Timing**

### 5.10.11 Data Modification Module (DMM)

A Data Modification Module (DMM) gives the ability to write external data into the device memory.

The DMM has the following features:

- Acts as a bus master, thus enabling direct writes to the 4GB address space without CPU intervention
- Writes to memory locations specified in the received packet (leverages packets defined by trace mode of the RAM trace port [RTP] module)
- Writes received data to consecutive addresses, which are specified by the DMM (leverages packets defined by direct data mode of RTP module)
- Configurable port width (1, 2, 4, 8 pins)
- Up to 100 Mbit/s pin data rate

**Table 5-20. DMM Timing Requirements**

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{cyc(DMM)}$ | Clock period | 10 | | | ns |
| $t_R$ | Clock rise time | 1 | | 3 | ns |
| $t_F$ | Clock fall time | 1 | | 3 | ns |
| $t_{h(DMM)}$ | High pulse width | 6 | | | ns |
| $t_{l(DMM)}$ | Low pulse width | 6 | | | ns |
| $t_{ssu(DMM)}$ | SYNC active to clk falling edge setup time | 2 | | | ns |
| $t_{sh(DMM)}$ | DMM clk falling edge to SYNC deactive hold time | 3 | | | ns |
| $t_{dsu(DMM)}$ | DATA to DMM clk falling edge setup time | 2 | | | ns |
| $t_{dh(DMM)}$ | DMM clk falling edge to DATA hold time | 3 | | | ns |

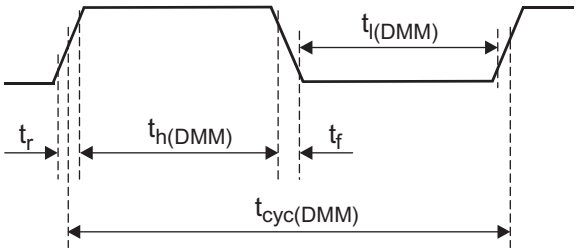


**Figure 5-17. DMMCLK Timing**

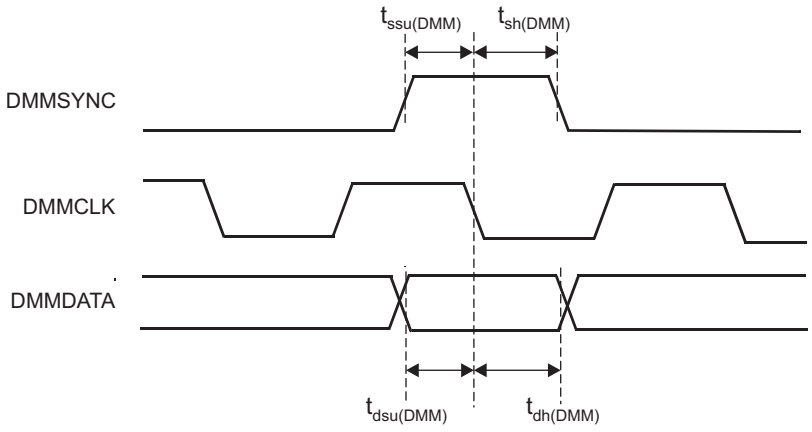


**Figure 5-18. DMMDATA Timing**

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### 5.10.12 JTAG Interface

Table 5-22 and Table 5-23 assume the operating conditions stated in Table 5-21.

**Table 5-21. JTAG Timing Conditions**

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input Conditions | | | | | |
| $t_R$ | Input rise time | 1 | | 3 | ns |
| $t_F$ | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| $C_{LOAD}$ | Output load capacitance | 2 | | 15 | pF |

**Table 5-22. Timing Requirements for IEEE 1149.1 JTAG**

| NO. | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(TCK)}$ | Cycle time TCK | 66.66 | | | ns |
| 1a | $t_{w(TCKH)}$ | Pulse duration TCK high (40% of tc) | 26.67 | | | ns |
| 1b | $t_{w(TCKL)}$ | Pulse duration TCK low(40% of tc) | 26.67 | | | ns |
| 3 | $t_{su(TDI-TCK)}$ | Input setup time TDI valid to TCK high | 2.5 | | | ns |
| | $t_{su(TMS-TCK)}$ | Input setup time TMS valid to TCK high | 2.5 | | | ns |
| 4 | $t_{h(TCK-TDI)}$ | Input hold time TDI valid from TCK high | 18 | | | ns |
| | $t_{h(TCK-TMS)}$ | Input hold time TMS valid from TCK high | 18 | | | ns |

**Table 5-23. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG**

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 2 | $t_{d(TCKL-TDOV)}$ | Delay time, TCK low to TDO valid | 0 | | 25 | ns |

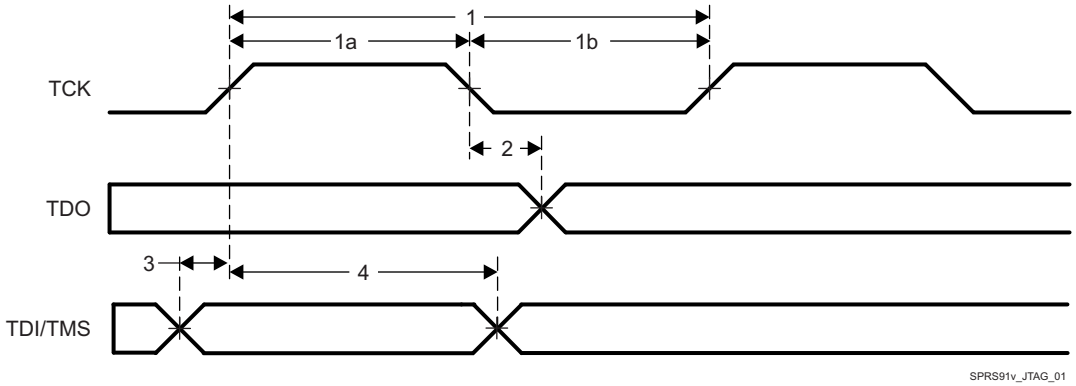



**Figure 5-19. JTAG Timing**

# 6 Detailed Description

## 6.1 Overview

The IWR6843 device includes the entire Millimeter Wave blocks and analog baseband signal chain for three transmitters and four receivers, as well as a customer-programmable MCU and DSP. This device is applicable as a radar-on-a-chip in use-cases with modest requirements for memory, processing capacity and application code size. These could be cost-sensitive industrial radar sensing applications. Examples are:

- Industrial level sensing
- Industrial automation sensor fusion with radar
- Traffic intersection monitoring with radar
- Industrial radar-proximity monitoring
- People counting
- Gesturing

In terms of scalability, the IWR6843 device could be paired with a low-end external MCU, to address more complex applications that might require additional memory for larger application software footprint and faster interfaces. The IWR6843 has an embedded DSP for signal processing, processing the radar signals for FFT, magnitude, detection and other applications.

## 6.2 Functional Block Diagram

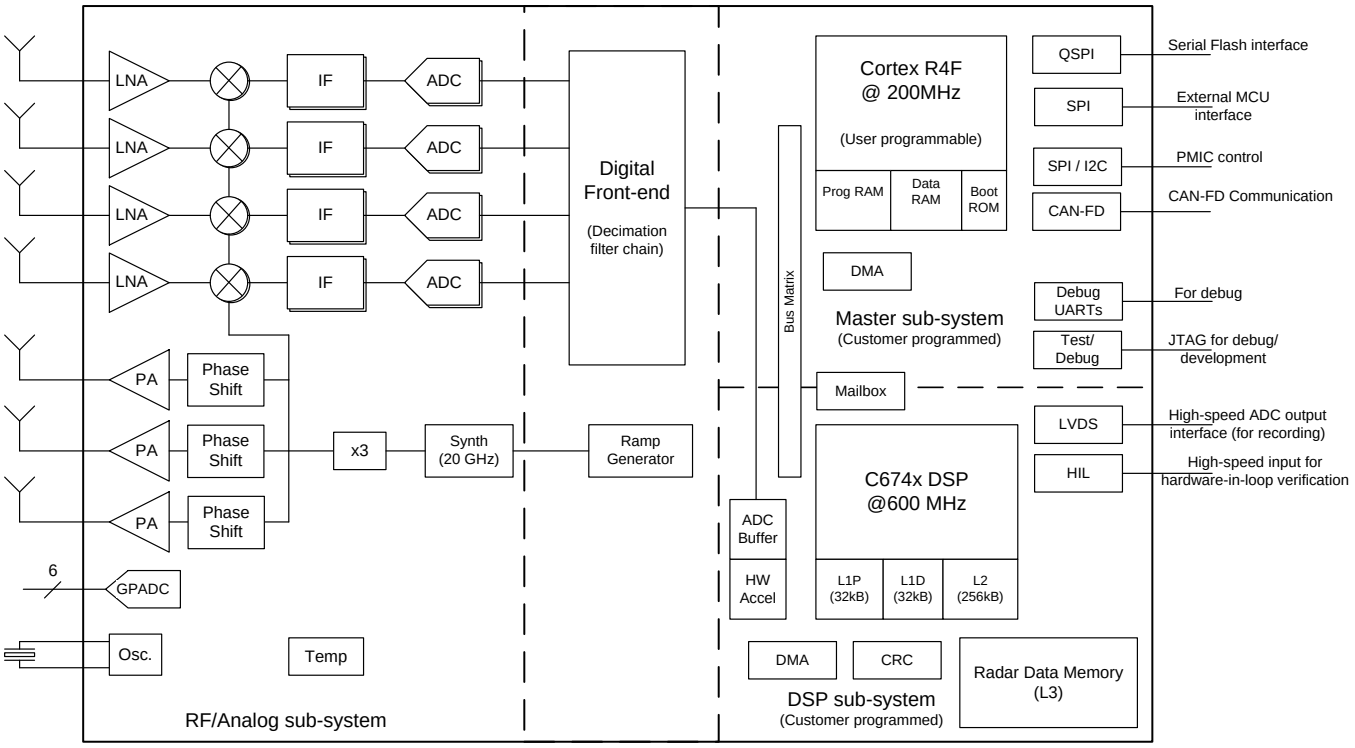



**Figure 6-1. Functional Block Diagram**

ADVANCE INFORMATION

## 6.3 Subsystems

### *6.3.1 RF and Analog Subsystem*

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The three transmit channels can be operated up to a maximum of two at a time (simultaneously) for transmit beamforming purpose as required; whereas the four receive channels can all be operated simultaneously.

#### 6.3.1.1 Clock Subsystem

The IWR6843 clock subsystem generates 60 to 64 GHz from an input reference of 40-MHz crystal. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X3 multiplier to create the required frequency in the 60 to 64 GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

Figure 6-2 describes the clock subsystem.

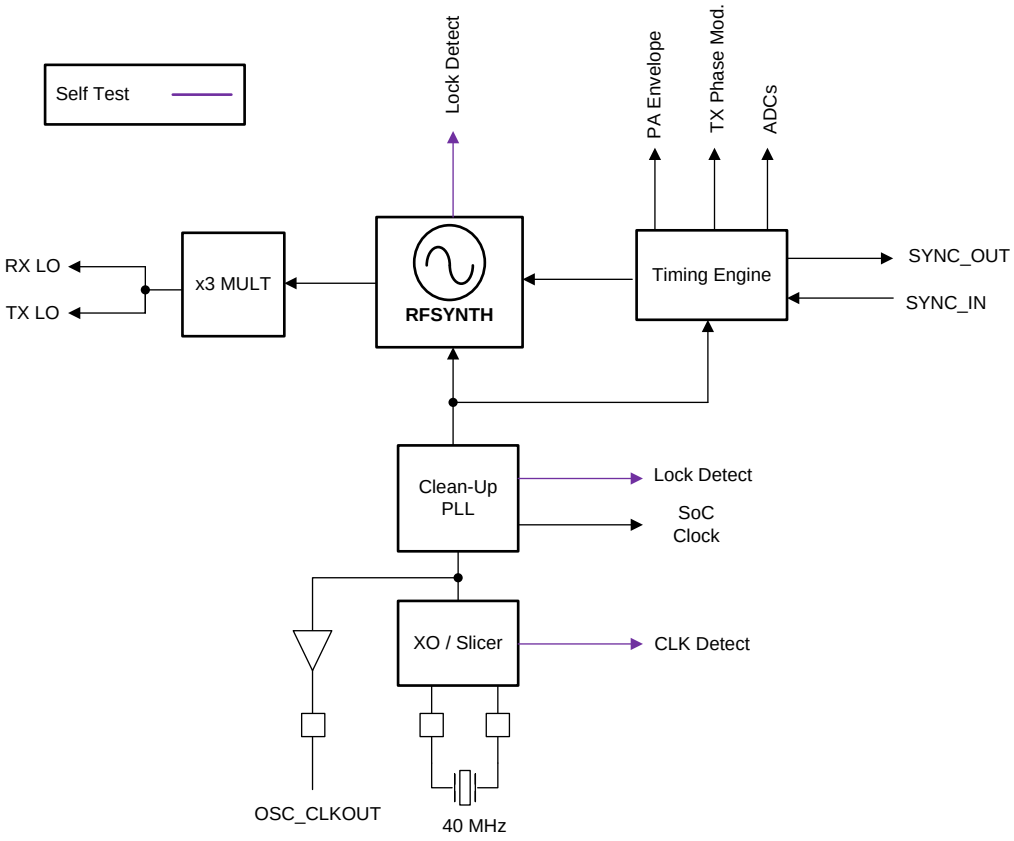



**Figure 6-2. Clock Subsystem**

ADVANCE INFORMATION

### 6.3.1.2 Transmit Subsystem

The IWR6843 transmit subsystem consists of three parallel transmit chains, each with independent phase and amplitude control. The device supports 6-bit linear phase modulation for MIMO radar and interference mitigation.

The transmit chains also support programmable backoff for system optimization.

Figure 6-3 describes the transmit subsystem.

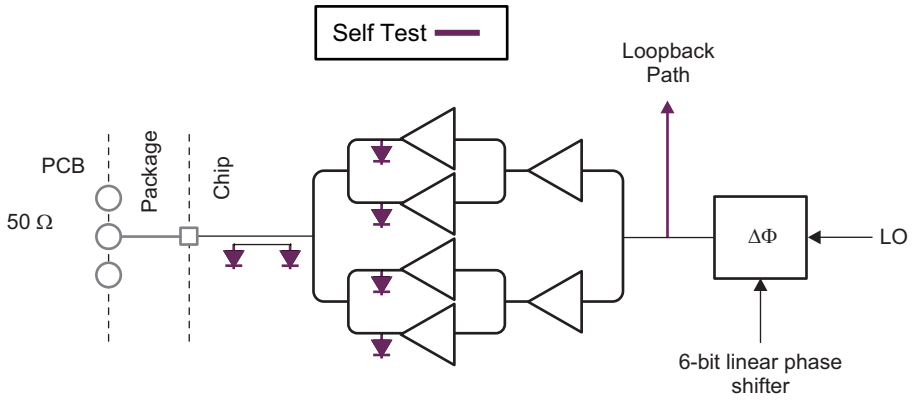



**Figure 6-3. Transmit Subsystem (Per Channel)**

### 6.3.1.3 Receive Subsystem

The IWR6843 receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, A2D conversion, and decimation. All four receive channels can be operational at the same time an individual power-down option is also available for system optimization.

Unlike conventional real-only receivers, the IWR6843 device supports a complex baseband architecture, which uses quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs for each receiver channel. The IWR6843 is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175 kHz and can support bandwidths up to 10 MHz.

Figure 6-4 describes the receive subsystem.

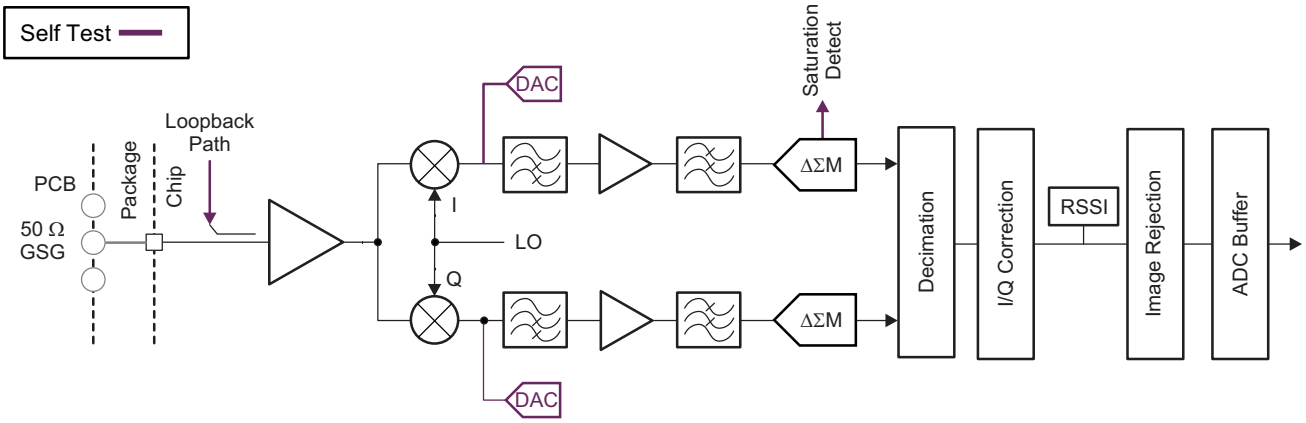



**Figure 6-4. Receive Subsystem (Per Channel)**

### 6.3.2 Processor Subsystem

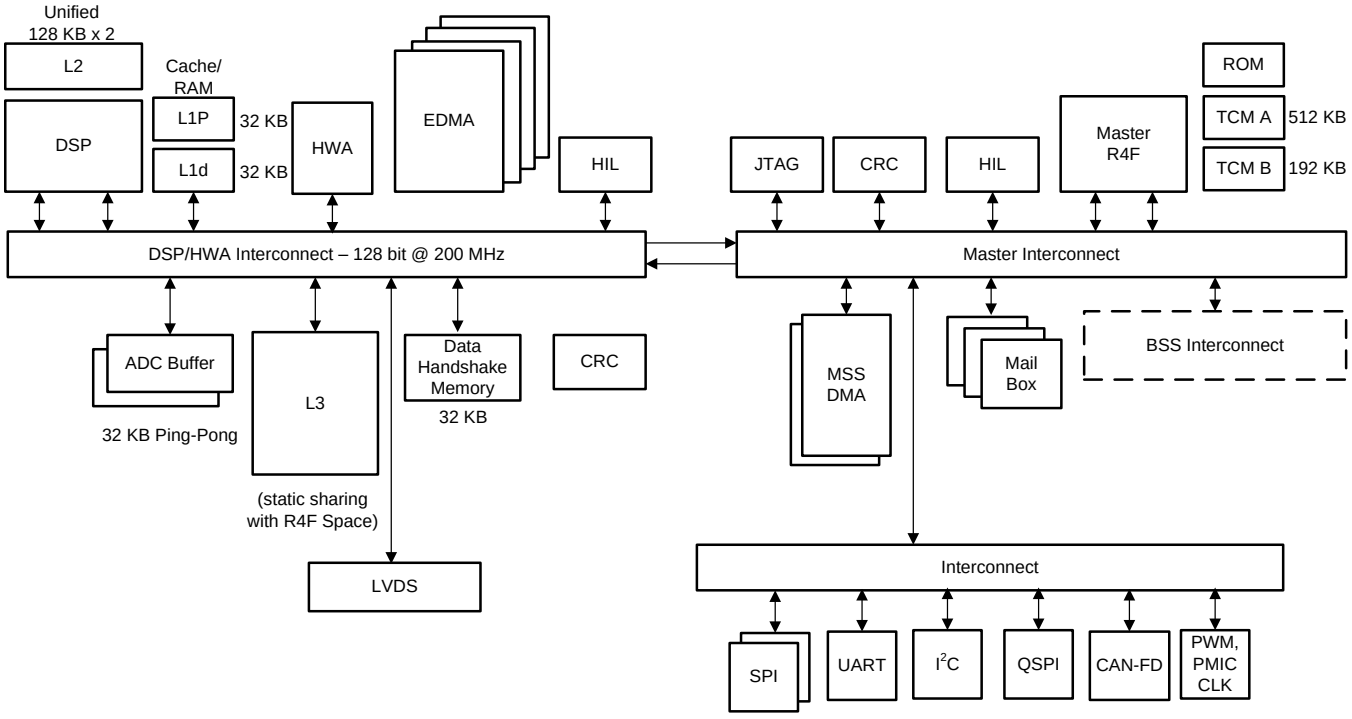



**Figure 6-5. Processor Subsystem**

Figure 6-5 shows the block diagram for customer programmable processor subsystems in the IWR6843 device. At a high level there are two customer programmable subsystems, as shown separated by a dotted line in the diagram. Left hand side shows the DSP Subsystem which contains TI's high-performance C674x DSP, hardware accelerator, a high-bandwidth interconnect for high performance (128-bit, 200MHz) and associated peripherals – four DMAs for data transfer,

LVDS interface for Measurement data output, L3 Radar data cube memory, ADC buffers, CRC engine, and data handshake memory (additional memory provided on interconnect).

The right side of the diagram shows the Master subsystem. Master subsystem as name suggests is the master of the device and controls all the device peripherals and house-keeping activities of the device. Master subsystem contains Cortex-R4F (Master R4F) processor and associated peripherals and house-keeping components such as DMAs, CRC and Peripherals ($I^2C$, UART, SPIs, CAN, PMIC clocking module, PWM, and others) connected to Master Interconnect through Peripheral Central Resource (PCR interconnect).

Details of the DSP CPU core can be found at http://www.ti.com/product/TMS320C6748.

HIL module is shown in both the subsystems and can be used to perform the radar operations feeding the captured data from outside into the device without involving the RF subsystem. HIL on master SS is for controlling the configuration and HIL on DSPSS for high speed ADC data input to the device. Both HIL modules uses the same IOs on the device, one additional IO (DMM_MUX_IN) allows selecting either of the two.

ADVANCE INFORMATION

### 6.3.3 Host Interface

The host interface can be provided through a SPI, UART, or CAN-FD interface. In some cases the serial interface for industrial applications is transcoded to a different serial standard.

The IWR6843 device communicates with the host radar processor over the following main interfaces:

- Reference Clock – Reference clock available for host processor after device wakeup
- Control – 4-port standard SPI (slave) for host control. All radio control commands (and response) flow through this interface.
- Reset – Active-low reset for device wakeup from host
- Host Interrupt - an indication that the mmwave sensor needs host interface
- Error – Used for notifying the host in case the radio controller detects a fault

### 6.3.4 Master Subsystem Cortex-R4F

The master system includes an ARM Cortex R4F processor, clock with a maximum operating frequency of 200 MHz. User applications executing on this processor control the overall operation of the device, including radar control through well-defined API messages, radar signal processing (assisted by the radar hardware accelerator), and peripherals for external interfaces.

See the Technical Reference Manual for a complete description and memory map.

### 6.3.5 DSP Subsystem

The DSP subsystem includes TI's standard TMS320C674x megamodule and several blocks of internal memory (L1P, L1D, and L2). For complete information including memory map, please refer to Technical Reference Manual.

### 6.3.6 Hardware Accelerator

The Radar Hardware Accelerator (HWA) is an IP that enables off-loading the burden of certain frequently used computations in FMCW radar signal processing from the main processor. FMCW radar signal processing involves the use of FFT and Log-Magnitude computations to obtain a radar image across the range, velocity, and angle dimensions. Some of the frequently used functions in FMCW radar signal processing can be done within the radar hardware accelerator, while still retaining the flexibility of implementing other proprietary algorithms in the main processor. See the Radar Hardware Accelerator User's Guide for a functional description and features of this module and see the Technical Reference Manual for a complete list of register and memory map.

## 6.4 Other Subsystems

### 6.4.1 ADC Channels (Service) for User Application

The IWR6843 device includes provision for an ADC service for user application, where the

GPADC engine present inside the device can be used to measure up to six external voltages. The ADC1, ADC2, ADC3, ADC4, ADC5, and ADC6 pins are used for this purpose.

- ADC itself is controlled by TI firmware running inside the BIST subsystem and access to it for customer's external voltage monitoring purpose is via 'monitoring API' calls routed to the BIST subsystem. This API could be linked with the user application running on the Master R4.
- BIST subsystem firmware will internally schedule these measurements along with other RF and Analog monitoring operations. The API allows configuring the settling time (number of ADC samples to skip) and number of consecutive samples to take. At the end of a frame, the minimum, maximum and average of the readings will be reported for each of the monitored voltages.

GPADC Specifications:

- 625 Ksps SAR ADC
- 0 to 1.8V input range
- 10-bit resolution

- For 5 out of the 6 inputs, an optional internal buffer (0.4-1.4V input range) is available. Without the buffer, the ADC has a switched capacitor input load modeled with 5pF of sampling capacitance and 12pF parasitic capacitance (GPADC channel 6, the internal buffer is not available).

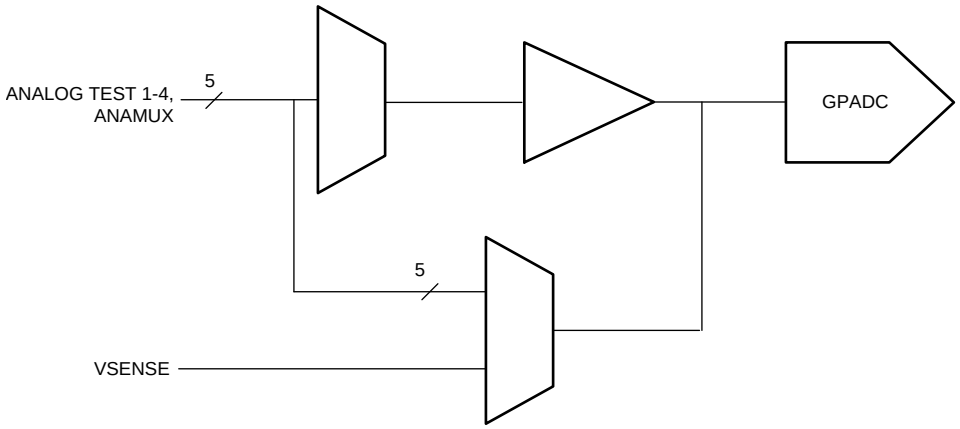



**Figure 6-6. ADC Path**

**Table 6-1. GP-ADC Parameter**

| PARAMETER | TYP | UNIT |
|---|---|---|
| ADC supply | 1.8 | V |
| ADC unbuffered input voltage range | 0 – 1.8 | V |
| ADC buffered input voltage range (1) | 0.4 – 1.3 | V |
| ADC resolution | 10 | bits |
| ADC offset error | ±5 | LSB |
| ADC gain error | ±5 | LSB |
| ADC DNL | –1/+2.5 | LSB |
| ADC INL | ±2.5 | LSB |
| ADC sample rate (2) | 625 | Ksps |
| ADC sampling time (2) | 400 | ns |
| ADC internal cap | 10 | pF |
| ADC buffer input capacitance | 2 | pF |
| ADC input leakage current | 3 | uA |

(1) Outside of given range, the buffer output will become nonlinear.
(2) ADC itself is controlled by TI firmware running inside the BIST subsystem. For more details please refer to the API calls.

ADVANCE INFORMATION

# 7 Applications, Implementation, and Layout

**NOTE**

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 7.1 Application Information

Application information can be found on IWR Application web page.

## 7.2 Reference Schematic

The reference schematic and power supply information can be found in the IWR6843 EVM Documentation.

## 7.3 Layout

### 7.3.1 Layout Guidelines

General layout guidelines can be found in the IWR6843 EVM Documentation and IWR6843 Checklist for Schematic Review, Layout Review, Bringup/Wakeup.

### 7.3.2 Layout Example

The IWR6843 EVM, RF layout can be found in the IWR6843BOOST Layout and Design Files, and IWR6843BOOST Schematics, Assembly Files, and BOM.

### 7.3.3 Stackup Details

Layout Stackup details can be found in the IWR6843BOOST Layout and Design Files.

There are specific RF guidelines for the RF Tx and Rx. There are additional layout guidelines for other sections in the IWR6843 Checklist for Schematic Review, Layout Review, Bringup/Wakeup.

# 8 器件和文档支持

TI 提供大量的开发工具。下面是用于评估器件性能、生成代码和开发解决方案的工具和软件。

## 8.1 器件命名规则

为了指出产品开发周期所处的阶段，TI 为所有微处理器 (MPU) 和支持工具的产品型号分配了前缀。每个器件都具有以下三种前缀之一：X、P 或无（无前缀）（例如 *IWR6843*）。德州仪器 (TI) 建议为其支持的工具使用三个可用前缀指示符中的两个：TMDX 和 TMDS。这些前缀代表了产品开发的发展阶段，即从工程原型 (TMDX) 直到完全合格的生产器件和工具 (TMDS)。

器件开发进化流程：

**X** 试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。

**P** 原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。

无 完全合格的芯片模型的生产版本。

支持工具开发进化流程：

**TMDX** 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品.

**TMDS** 完全合格的开发支持产品。

X 和 P 器件和 TMDX 开发支持工具在供货时附带如下免责条款：

“开发的产品用于内部评估用途。”

生产器件和 TMDS 开发支持工具已进行完全特性描述，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件（X 或者 P）的故障率大于标准生产器件。由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。只有合格的产品器件将被使用。

TI 器件的命名规则还包括一个带有器件系列名称的后缀。此后缀表示封装类型（例如 ABL0161ALB0161）、温度范围（例如，无后缀表示默认的商业级温度范围）。图 8-1 提供了一个图例，用于解读 *IWR6843* 器件的完整器件名称。

如需获取 *IWR6843* 器件（采用 ABL0161 封装类型）的可订购器件号，请参阅此文档的“封装选项附录”、TI 网站 (www.ti.com.cn) 或联系您的 TI 销售代表。

有关裸片器件命名规则标记的其他 说明 ，请参阅 *《IWR6843 器件勘误表》*。

ADVANCE INFORMATION

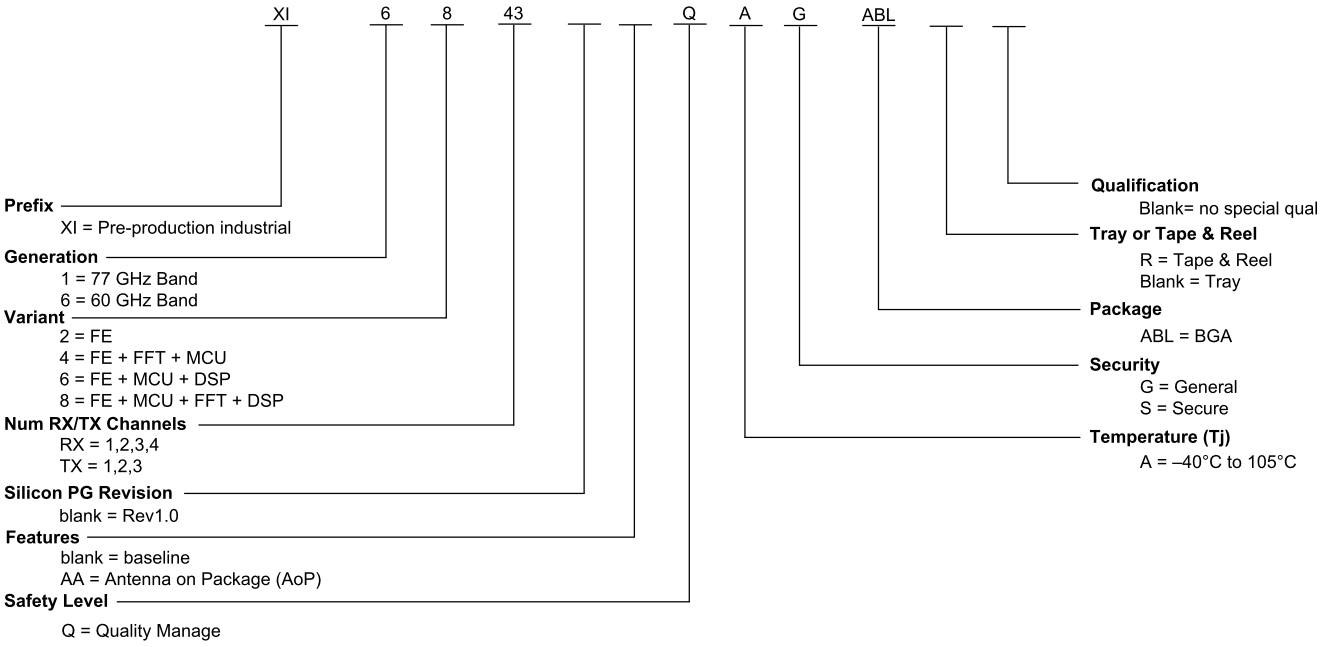



图 **8-1.** 器件命名规则

## 8.2 工具和软件

### 模型

**IWR6843 BSDL 模型** 符合专用器件 IEEE 1149.1 标准的可测试输入和输出引脚的边界扫描数据库。

**IWR6843 IBIS 模型** 适用于器件的 IO 缓冲器的 IO 缓冲器信息模型。有关电路板仿真的信息，请查看 IBIS 开放论坛。

**用于原理图审阅、布局审阅、启动/唤醒的 IWR6843 检查清单** 以电子表格的格式列出了一系列步骤，用于选择系统功能和 PinMux 选项。提供专用 EVM 原理图和布局手册，以应用于客户工程设计。为客户推荐了启动检查清单。

## 8.3 文档支持

要接收文档更新（包括器件勘误表）通知，请访问 ti.com.cn (IWR6843) 上相关器件的产品文件夹。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

下面列出了介绍 DSP、相关外设以及其他配套技术资料的最新文档。

### 勘误表

**IWR6843 器件勘误表** 介绍了器件的已知问题、限制和注意事项并提供了权变措施。

ADVANCE INFORMATION

## 8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 8.5 商标

E2E is a trademark of Texas Instruments.
基于 ARM, Cortex are registered trademarks of ARM Limited.
All other trademarks are the property of their respective owners.

## 8.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 8.7 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

## 8.8 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

# 9 机械、封装和可订购信息

## 9.1 封装信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

**CAUTION**

以下封装信息如有变更，恕不另行通知。

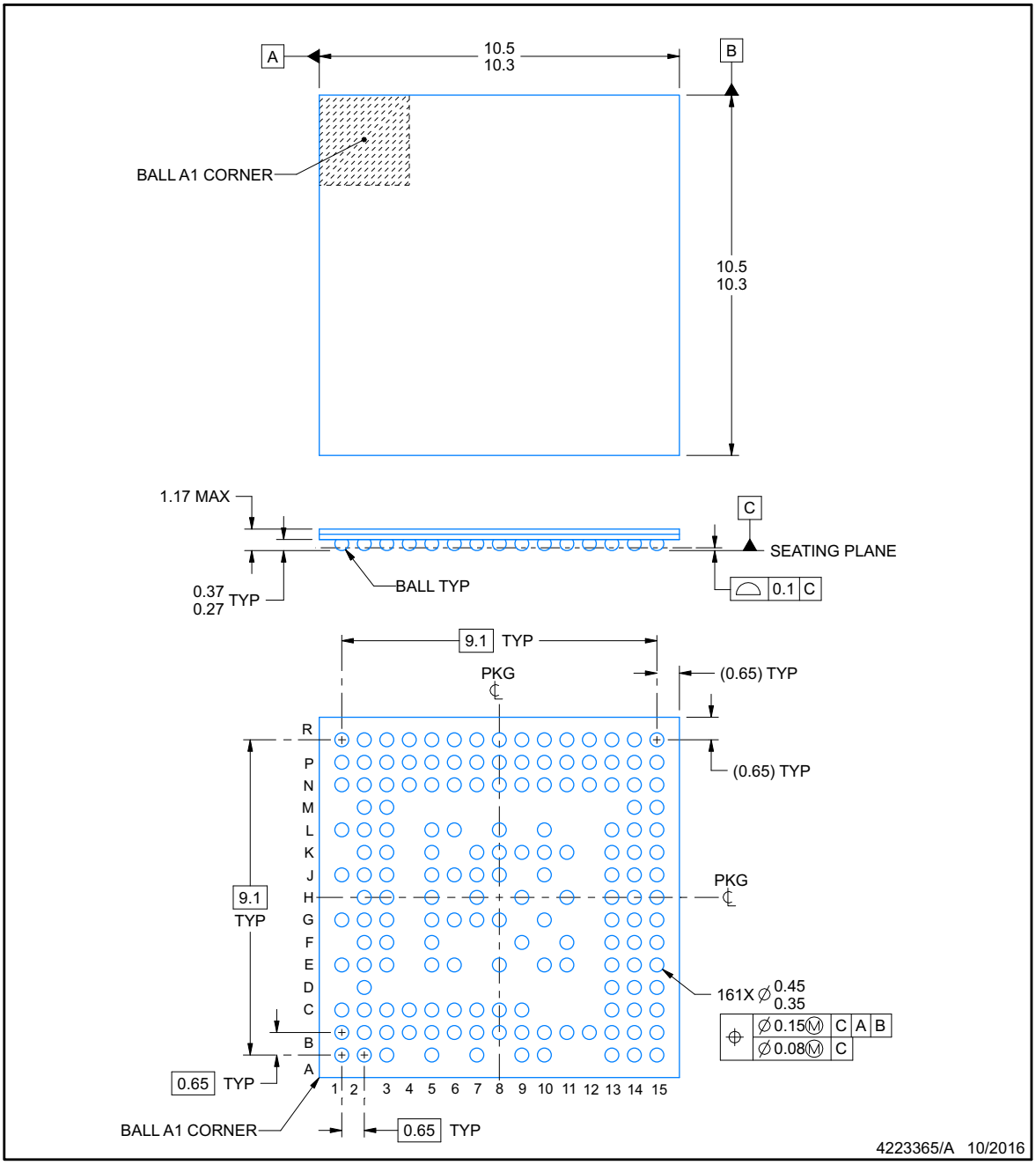
ADVANCE INFORMATION

# PACKAGE OUTLINE

## ABL0161B

## FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY




NOTES:

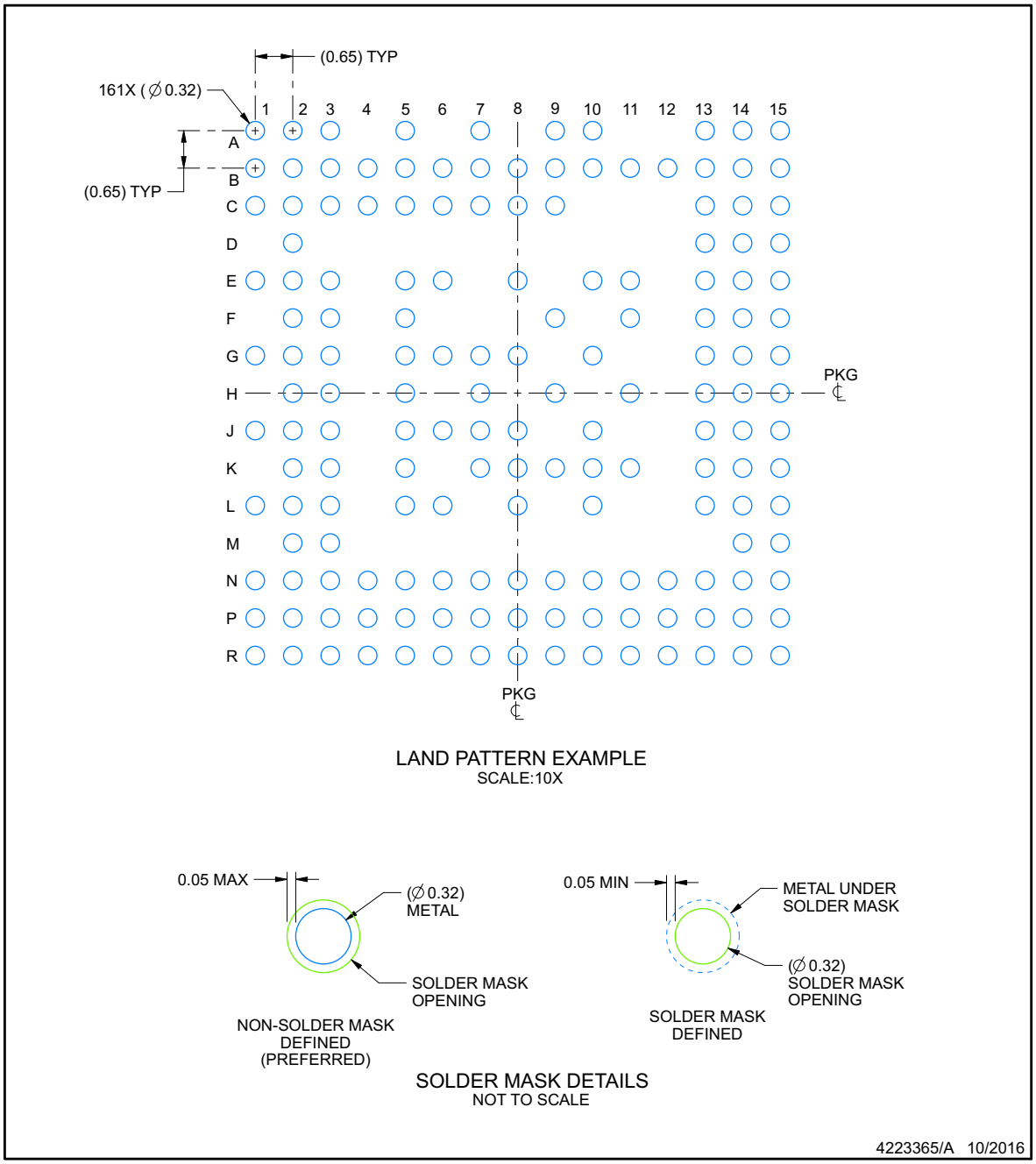
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

## ABL0161B

### FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY




NOTES: (continued)

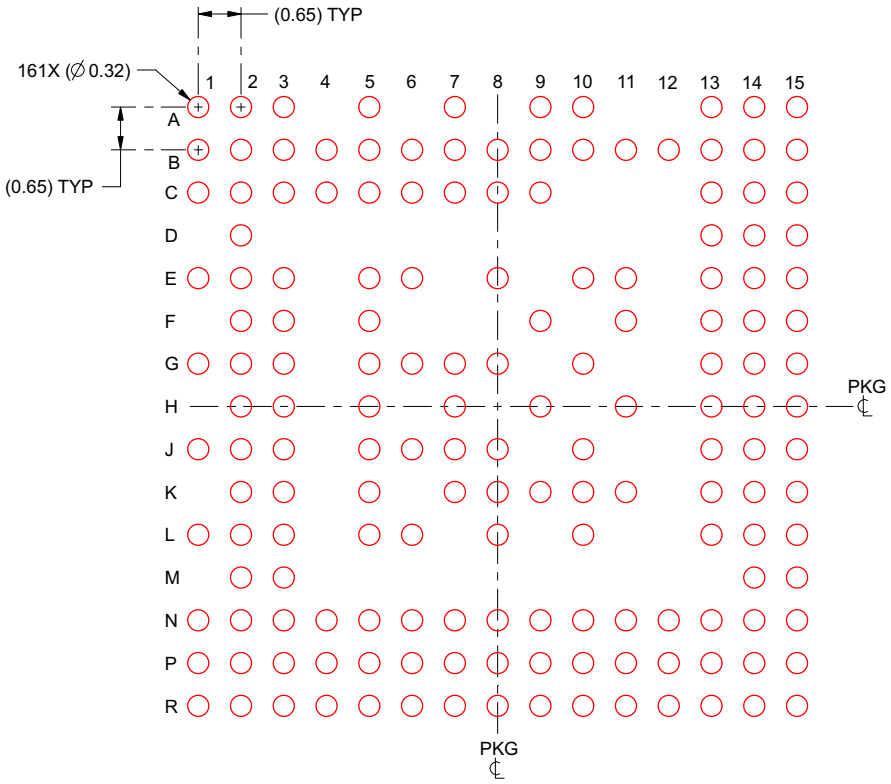
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

ADVANCE INFORMATION

## EXAMPLE STENCIL DESIGN

**ABL0161B** — **FCBGA - 1.17 mm max height**

PLASTIC BALL GRID ARRAY




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4223365/A 10/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

ADVANCE INFORMATION

# 重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| XI6843AAQGALB | ACTIVE | FCBGA | ALA | 209 | 1 | TBD | Call TI | Call TI | -40 to 105 | | Samples |
| XI6843AQGABL | ACTIVE | FC/CSP | ABL | 161 | 1 | TBD | Call TI | Call TI | -40 to 105 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

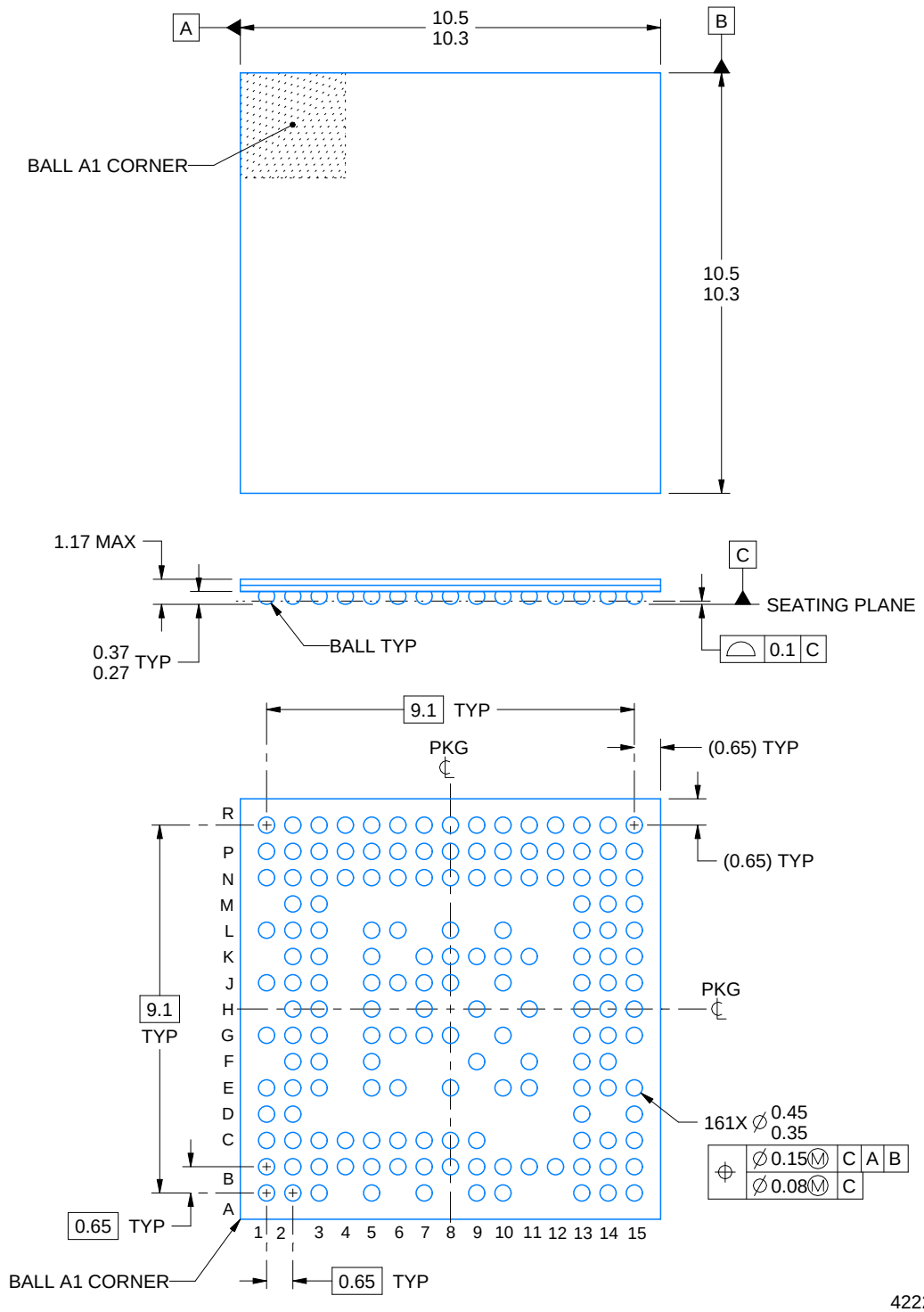
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

# PACKAGE OUTLINE

## ABL0161A

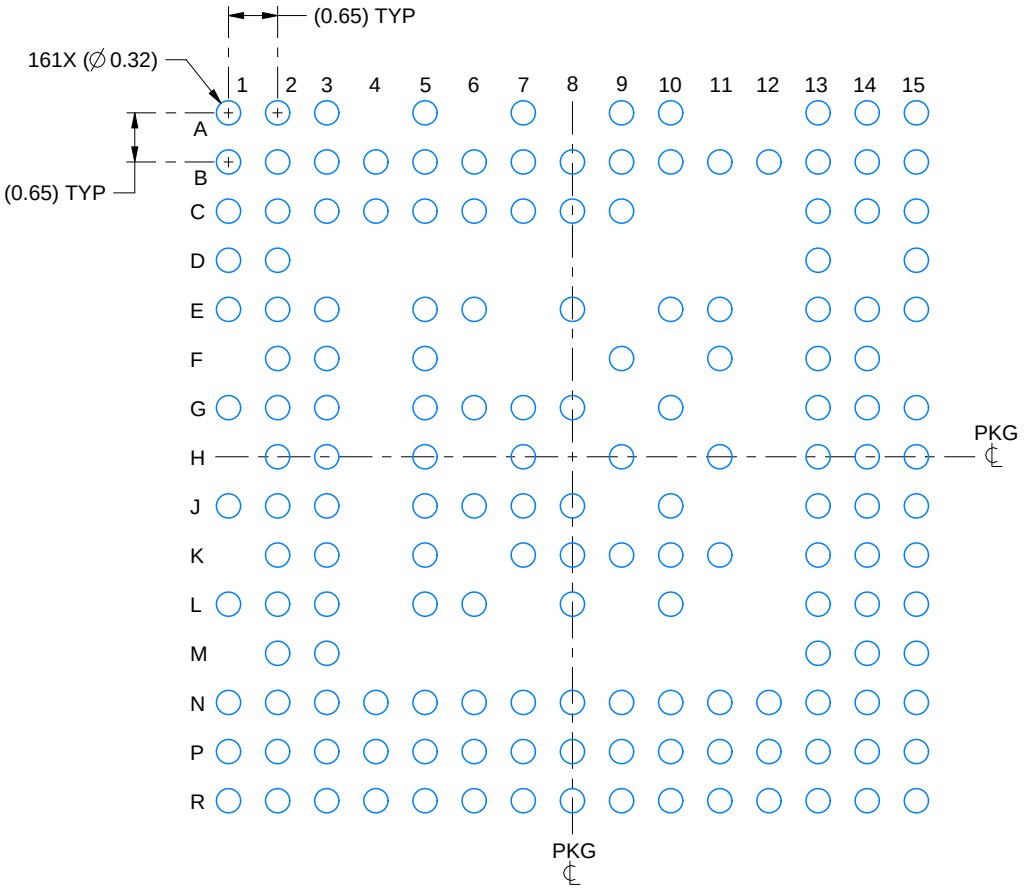
## FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY

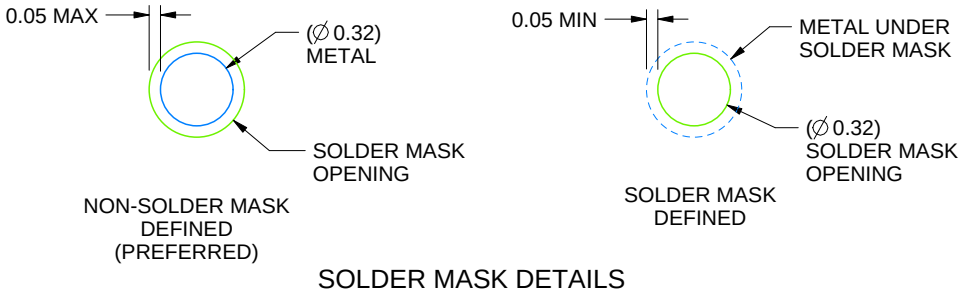



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:10X




SOLDER MASK DETAILS
NOT TO SCALE

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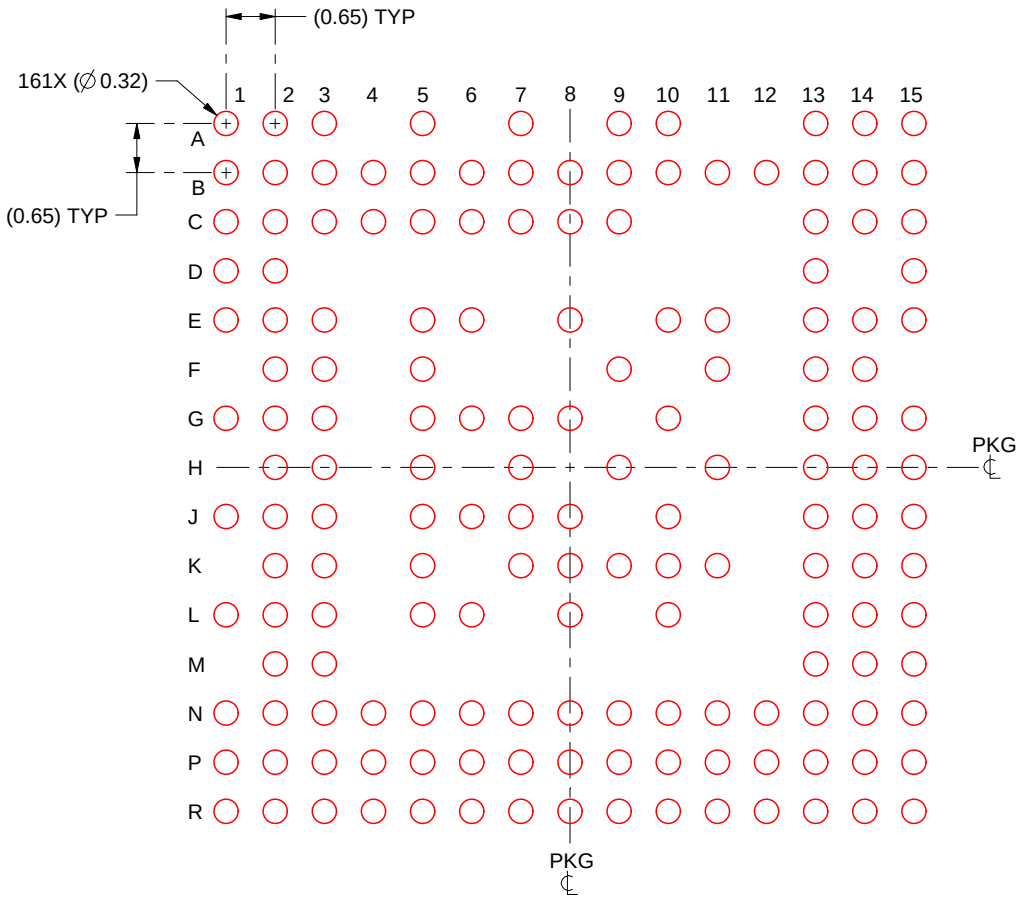
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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