bq21040 0.8A、单输入、单节锂离子和锂聚合物电池充电器

1 特性

- 充电中
  - 充电电压精度为 1%
  - 10% 充电电流精度
  - 低电池泄漏电流 (1μA)
  - 可通过外部电阻编程设定的充电电流最高可达 800mA
  - 4.2V 锂离子和锂聚合物充电器
- 保护
  - 30V 额定输入电压；具有 6.6V 输入过压保护
  - 输入电压动态电源管理
  - 125°C 热调节；150°C 热关断保护
  - OUT 短路保护和 ISET 短路检测
  - 通过负温度系数 (NTC) 实现过热感测保护
  - 10 小时固定安全定时器
- 系统
  - 状态指示 - 充电/完成
  - 采用小型小外形尺寸晶体管 (SOT)-23 封装

2 应用

- 电子销售点 (EPOS)
- 医疗内窥镜
- BLE 扬声器和耳机
- 低功耗手持器件

3 说明

bq21040 器件是一款面向空间受限类便携式应用的高度集成锂离子和锂聚合物线性 电池充电器中运行。此器件可由一个 USB 端口或交流适配器供电运行。具有输入过压保护的高输入电压范围支持低成本、未稳压的适配器。

bq21040 具有一个可为电池充电的单电源输出。如果在 10 小时的安全定时器期间内平均系统负载无法让电池充满电，则可以使系统负载与电池并联。

电池充电经历以下三个阶段：调节，恒定电流和恒定电压。在所有充电阶段，内部控制环路都会监控 IC 结温，当其超过内部温度阈值时，它会减少充电电流。

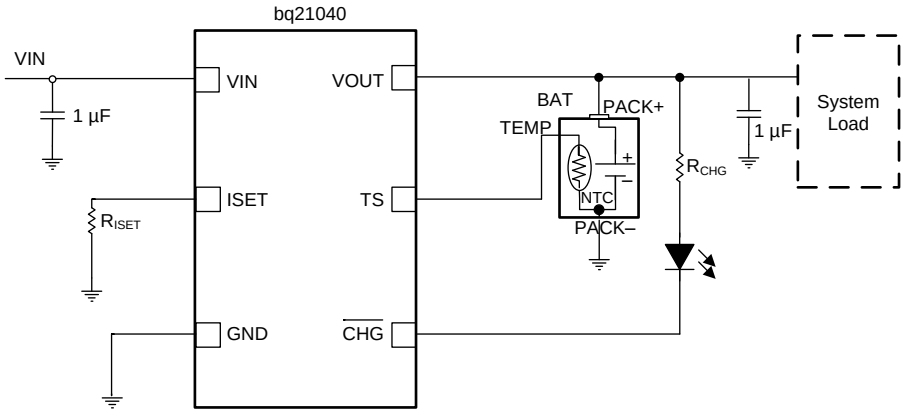
充电器功率级和充电电流感测功能均完全集成。该充电器具有高精度电流和电压调节环路功能、充电状态显示，和充电终止功能。预充电电流阈值和终止电流阈值分别固定为 20% 和 10%。快速充电电流值可通过一个外部电阻进行编程。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
bq21040	SOT-23 (6)	3.00mm x 1.75mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (August 2017) to Revision D — **Page**

- Changed HBM From: ±1000 To: ±2000 in the *ESD Ratings* ... 4
- Changed CDM From: ±250 To: ±500 in the *ESD Ratings* ... 4

Changes from Revision B (May 2017) to Revision C — **Page**

- 已更改 简化原理图 ... 1
- Changed 250 kΩ to 237 kΩ in TS pin description ... 3
- Changed R_{TS} max from 25.8 kΩ to 258 kΩ ... 4
- Changed Low temperature charging to Normal temperature charging in V_{TS-0C} Test Conditions ... 6
- Changed low temperature charging to normal temperature charging in V_{HYS-0C} Test Conditions ... 6
- Changed High temperature charging to Normal temperature charging in V_{TS-45C} Test Conditions ... 6
- Changed high temperature charging to normal temperature charging in $V_{HYS-45C}$ Test Conditions ... 6
- 已删除 Load Regulation graph ... 7
- 已删除 Line Regulation graph ... 7
- 已更改 图 6 ... 11
- 已删除 The bq21040 does not have a safety timer. in Timers ... 15
- 已更改 图 10 ... 17

Changes from Revision A (April 2016) to Revision B — **Page**

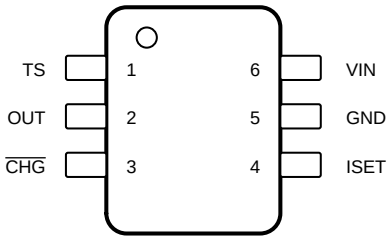
- 更改了*电气特性* 表中的最小值和最大值，更改了快速充电电流系数 KISET 的最小值和最大值 ... 1
- 已添加 *接收文档更新通知* 部分 ... 1

5 Device Comparison

PART NO.	$V_{O(REG)}$	V_{OVP}	TS	PACKAGE
bq21040	4.20 V	6.6 V	TS	3.00 mm × 1.75 mm × 1.45 mm SOT-23

6 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{CHG}$	3	O	Low (FET on) indicates charging and Open Drain (FET off) indicates no Charging or Charge complete.
GND	5	—	Ground terminal
ISET	4	I	Programs the Fast-charge current setting. External resistor from ISET to VSS defines fast charge current value. Range is 10.8kΩ (50mA) to 675Ω (800mA).
OUT	2	O	Battery connection. System load may be connected. Expected range of bypass capacitors 1μF to 10μF.
TS	1	I	Temperature sense terminal connected to bq21040 -10k at 25°C NTC thermistor, in the battery pack. Floating T terminal or pulling High puts part in TTDM "Charger" Mode and disable TS monitoring, Timers and Termination. Pulling terminal Low disables the IC. If NTC sensing is not needed, connect this terminal to VSS through an external 10 kΩ resistor. A 237 kΩ from TS to ground will prevent IC entering TTDM mode when battery with thermistor is removed.
VIN	6	I	Input power, connected to external DC supply (AC adapter or USB port). Expected range of bypass capacitors 1μF to 10μF, connect from IN to V_{SS}.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Input voltage	IN (with respect to VSS)	–0.3	30	V
	OUT (with respect to VSS)	–0.3	7	V
	PRE-TERM, ISET, ISET2, TS, /CHG (with respect to VSS)	–0.3	7	V
Input current	IN		1.25	A
Output current (continuous)	OUT		1.25	A
Output sink current	$\overline{CHG}$		15	mA
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	IN voltage range	3.5		28	V
	IN operating voltage range, restricted by VDPM and VOVP	4.45		6.45	V
I_{IN}	Input current, IN terminal			0.8	A
I_{OUT}	Current, OUT terminal			0.8	A
T_J	Junction temperature	0		125	°C
R_{ISET}	Fast-charge current programming resistor	0.675		10.8	kΩ
R_{TS}	10k NTC thermistor range without entering TTDM	1.66		258	kΩ

7.4 Thermal Information

THERMAL METRIC (1)		bq21040 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
UVLO	Undervoltage lockout exit	V_{IN}: 0 V to 4 V	3.15	3.3	3.45	V
$V_{HYS-UVLO}$	Hysteresis on V_{UVLO_RISE} falling	V_{IN}: 0 V to 4 V, V_{UVLO_FALL} = V_{UVLO_RISE} – $V_{HYS-UVLO}$	175	227	280	mV
V_{IN-DT}	Input power good detection threshold is V_{OUT}+$_{VIN-DT}$	(Input power good if V_{IN} > V_{OUT} + V_{IN-DT}); V_{OUT} = 3.6 V, V_{IN}: 3.5 V to 4 V	30	80	145	mV
$V_{HYS-INDT}$	Hysteresis on V_{IN-DT} falling	V_{OUT} = 3.6 V, VIN: 4 V to 3.5 V		31		mV
V_{OVP}	Input overvoltage protection threshold	V_{IN}: 5 V to 12 V	6.5	6.65	6.8	V
$V_{HYS-OVP}$	Hysteresis on OVP	V_{IN}: 11 V to 5 V		95		mV
V_{IN-DPM}	Adaptor low input voltage protection. Restricts Iout at VIN-DPM	Feature active in adaptor mode; Limit Input Current to 50 mA; V_{OUT} = 3.5 V; R_{ISET} = 825	4.24	4.3	4.46	V
ISET SHORT CIRCUIT TEST						
R_{ISET_SHORT}	Highest resistance considered a fault (short). Monitored for I_{OUT}>90mA	R_{ISET}: 250 Ω to 540 Ω, Iout latches off. Cycle power to reset			500	Ω

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OUT_CL}	Maximum OUT current limit regulation (clamp)	V_{IN} = 5 V, V_{OUT} = 3.6 V, R_{ISET}: 250 Ω to 540 Ω, Iout latches off after $t_{DGL-SHORT}$	1.05		1.4	A
BATTERY SHORT PROTECTION						
$V_{OUT(SC)}$	OUT terminal short-circuit detection threshold/precharge threshold	Vout:3V to 0.5V, no deglitch	0.75	0.8	0.85	V
$V_{OUT(SC-HYS)}$	OUT terminal short hysteresis	Recovery ≥ $V_{OUT(SC)}$ + $V_{OUT(SC-HYS)}$; Rising, no deglitch		77		mV
$I_{OUT(SC)}$	Source current to OUT terminal during short-circuit detection		10	15	20	mA
QUIESCENT CURRENT						
$I_{OUT(PDWN)}$	Battery current into OUT terminal	V_{IN} = 0V			1	µA
$I_{OUT(DONE)}$	OUT pin current, charging terminated	V_{IN} = 6 V, V_{BAT} > $V_{BAT(REG)}$, net current is into OUT pin			6	µA
$I_{IN(STDBY)}$	Standby current into IN pin	TS = Low, V_{IN} ≤ 6 V			125	µA
I_{CC}	Active supply current, IN pin	TS = Low, V_{IN} = 6 V, no load on OUT pin, V_{BAT} > $V_{BAT(REG)}$			1000	µA
BATTERY CHARGER FAST-CHARGE						
$V_{OUT(REG)}$	Battery regulation voltage	V_{REG} = 4.2 V, I_L = 25 mA, V_{IN} = 5.5 V	4.16	4.2	4.23	V
$I_{OUT(RANGE)}$	Programmed output fast charge current range	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}; V_{IN} = 5 V, R_{ISET} = 0.675 to 52 kΩ	10		800	mA
$V_{DO(IN-OUT)}$	Drop-Out, V_{IN} – V_{OUT}	Adjust V_{IN} down until I_{OUT} = 0.5 A, V_{OUT} = 4.15 V, R_{ISET} = 1.08kΩ		325	550	mV
I_{OUT}	Output fast charge formula	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}; V_{IN} = 5 V	KISET/ RISET	KISET/ RISET	KISET/ RISET	A
K_{ISET}	Fast charge current factor	KISET (60mA < I <1000mA)	490	540	590	AΩ
		KISET (25mA < I < 60mA)	470	527	605	
		KISET (10mA < I < 25mA)	340	520	685	
PRECHARGE						
V_{LOWV}	Pre-charge to fast-charge transition threshold		2.4	2.5	2.6	V
Pre-charge	Default pre-charge current	V_{BAT} < V_{LOWV}, I_{CHG} = 50 mA	18	20	22	%ISET
TERMINATION						
%TERM	Termination Threshold Current, default setting	V_{OUT} > V_{RCH}; R_{ISET} = 1 kΩ	9	10	11	%IOUT-CC
RECHARGE OR REFRESH						
V_{RCH}	Recharge detection threshold	V_{IN} = 5 V, V_{TS} = 0.5 V, V_{OUT} = 4.25 V to V_{RCH}	$V_{O(REG)}$ - 120 mV	$V_{O(REG)}$ - 95 mV	$V_{O(REG)}$ - 70 mV	mV
BATT DETECT						
V_{REG-BD}	VOUT Reduced regulation during battery detect	V_{IN} = 5 V, V_{TS} = 0.5 V, battery absent	$V_{O(REG)}$ - 450 mV	$V_{O(REG)}$ - 400 mV	$V_{O(REG)}$ - 350 mV	mV
$I_{BD-SINK}$	Sink current during VREG-BD		7		10	mA
V_{BD-HI}	High battery detection threshold	V_{IN} = 5 V, V_{TS} = 0.5 V, battery absent	$V_{O(REG)}$ - 150 mV	$V_{O(REG)}$ - 100 mV	$V_{O(REG)}$ - 50 mV	V
V_{BD-LO}	Low battery detection threshold		VREG-BD+0.50	VREG-BD+0.1	VREG-BD+0.15	V
BATTERY-PACK NTC MONITOR						
$I_{NTC\ 50µA}$	NTC bias current		48	50	53	µA
$I_{NTC-DIS-10K}$	10K NTC bias current when charging is disabled	V_{TS} = 0 V	27	30	34	µA
$I_{NTC-FLDBK\ -10K}$	INTC is reduced prior to entering TTDM to keep cold thermistor from entering TTDM	V_{TS} = 1.525 V	4	5	6.5	µA

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TTDM(TS)}$	Termination and timer disable mode-Threshold-Enter	V_{TS}: 0.5 V to 1.7 V; timer held in reset	1550	1600	1650	mV
$I_{HYS-TTDM(TS)}$	Hysteresis exiting TTDM	V_{TS}: 1.7 V to 0.5 V; timer enabled		100		mV
$V_{CLAMP(TS)}$	TS maximum voltage clamp	V_{TS} = Open (float)	1800	1950	2000	mV
$V_{TS\_I-FLDBK}$	TS voltage where INTC is reduce to keep thermistor from entering TTDM	INTC adjustment (90 to 10%; 45 to 6.6 µs) takes place near this spec threshold. V_{TS}: 1.425 V to 1.525 V		1475		mV
C_{TS}	Optional capacitance – ESD			0.22		µF
V_{TS-0C}	Low temperature CHG pending	Normal temperature charging to pending; V_{TS}: 1 V to 1.5 V	1220	1250	1280	mV
V_{HYS-0C}	Hysteresis at 0°C	Charge pending to normal temperature charging; V_{TS}: 1.5 V to 1 V		100		mV
V_{TS-45C}	High temperature CHG disable	Normal temperature charging to pending; V_{TS}: 0.5 V to 0.2 V	260	275	290	mV
$V_{HYS-45C}$	Hysteresis at 45°C	Charge pending to normal temperature charging; V_{TS}: 0.2 V to 0.5 V		20		mV
$V_{TS-EN-10K}$	Charge enable threshold (10k NTC)	V_{TS}: 0 V to 0.175 V	80	88	96	mV
$V_{TS-DIS\_HYS-10K}$	HYS below VTS-EN-10k to disable (10k NTC)	V_{TS}: 0.125 V to 0 V		12		mV
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature			155		
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		
CHG INDICATION						
V_{OL}	Output Low Voltage-CHG FET on - first charge after power-up	I_{SINK} = 5 mA			0.4	V
I_{LEAK}	Leakage current into IC	$V_{\overline{CHG}}$ = 5 V			1	µA

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
INPUT						
$t_{DGL(OVP\_SET)}$	Input over-voltage blanking time	V_{IN}: 5 V to 12 V		113		µs
$t_{DGL(OVP\_REC)}$	Deglitch time exiting OVP	Time measured from VIN: 12V to 5V		30		µs
ISET SHORT CIRCUIT TEST						
t_{DGL_SHORT}	Deglitch time transition from ISET short to IOUT disable	Clear fault by disconnecting IN or cycling (high / low) TS		1		ms
PRECHARGE – SET INTERNALLY						
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			70		µs
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			32		ms
TERMINATION						
$t_{DGL(TERM)}$	Deglitch time, termination detected			29		ms
RECHARGE OR REFRESH						
$t_{DGL1(RCHG)}$	Deglitch time, recharge threshold detected	V_{IN} = 5 V, V_{TS} = 0.5 V, VOUT: 4.25 V to 3.5 V in 1 µs; $t_{DGL(RCHG)}$ is time to ISET ramp		29		ms
BATTERY DETECT ROUTINE						
$t_{DGL(HI/LOW\ REG)}$	Regulation time at VREG or VREG-BD			25		ms
BATTERY-PACK NTC MONITOR; TS TERMINAL						
$t_{DGL(TS)}$	Deglitch for TS thresholds: 0/45C.	Battery charging		30		ms

7.7 Typical Operational Characteristics (Protection Circuits Waveforms)

SETUP: bq21040 typical applications schematic; V_{IN} = 5V, V_{BAT} = 3.6V (unless otherwise indicated)

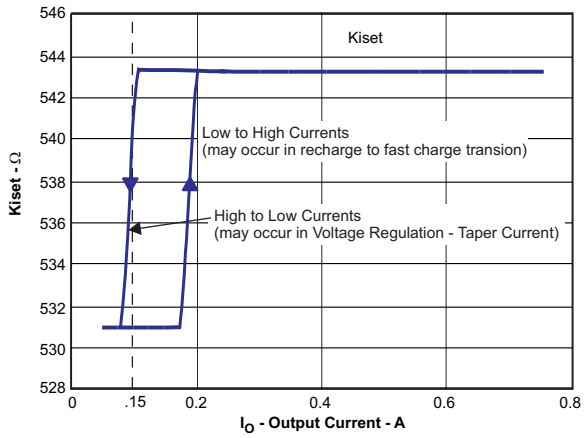


图 1. Kiset for Low and High Currents

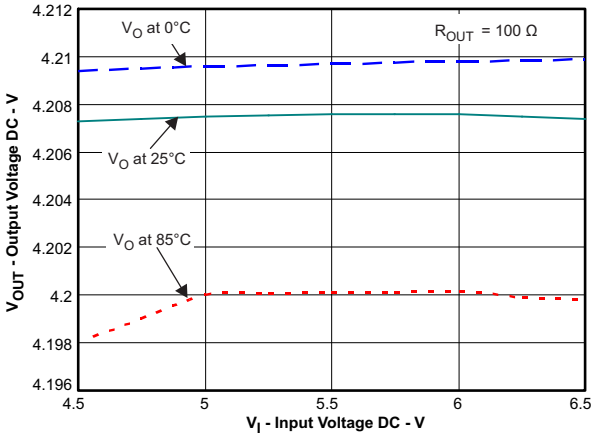


图 2. Line Regulation

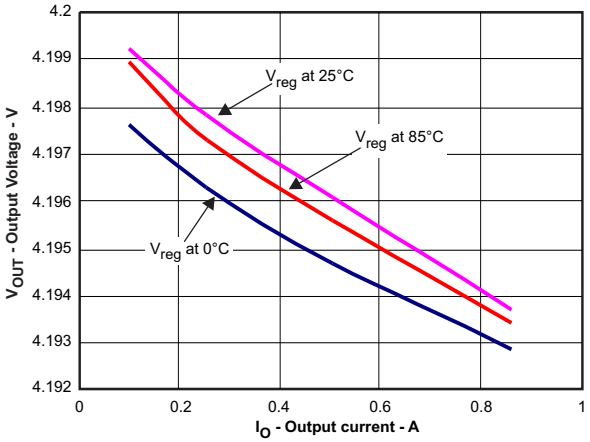


图 3. Load Regulation Over Temperature

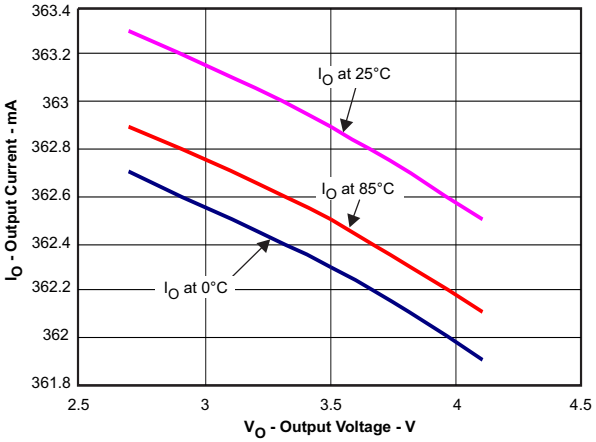


图 4. Current Regulation Over Temperature

8 Detailed Description

8.1 Overview

The bq21040 is a highly integrated single cell Li-Ion and Li-Pol charger. The charger can be used to charge a battery, power a system or both. The charger has three phases of charging: Pre-charge to recover a fully discharged battery, fast-charge constant current to supply the buck charge safely and voltage regulation to safely reach full capacity. The charger is very flexible, allowing programming of the fast-charge current. This charger is designed to work with a USB connection or Adaptor (DC out). The charger also checks to see if a battery is present.

The charger also comes with a full set of safety features: Temperature Sensing Standard, Over-Voltage Protection, DPM-IN, Safety Timers, and ISET short protection. All of these features and more are described in detail below.

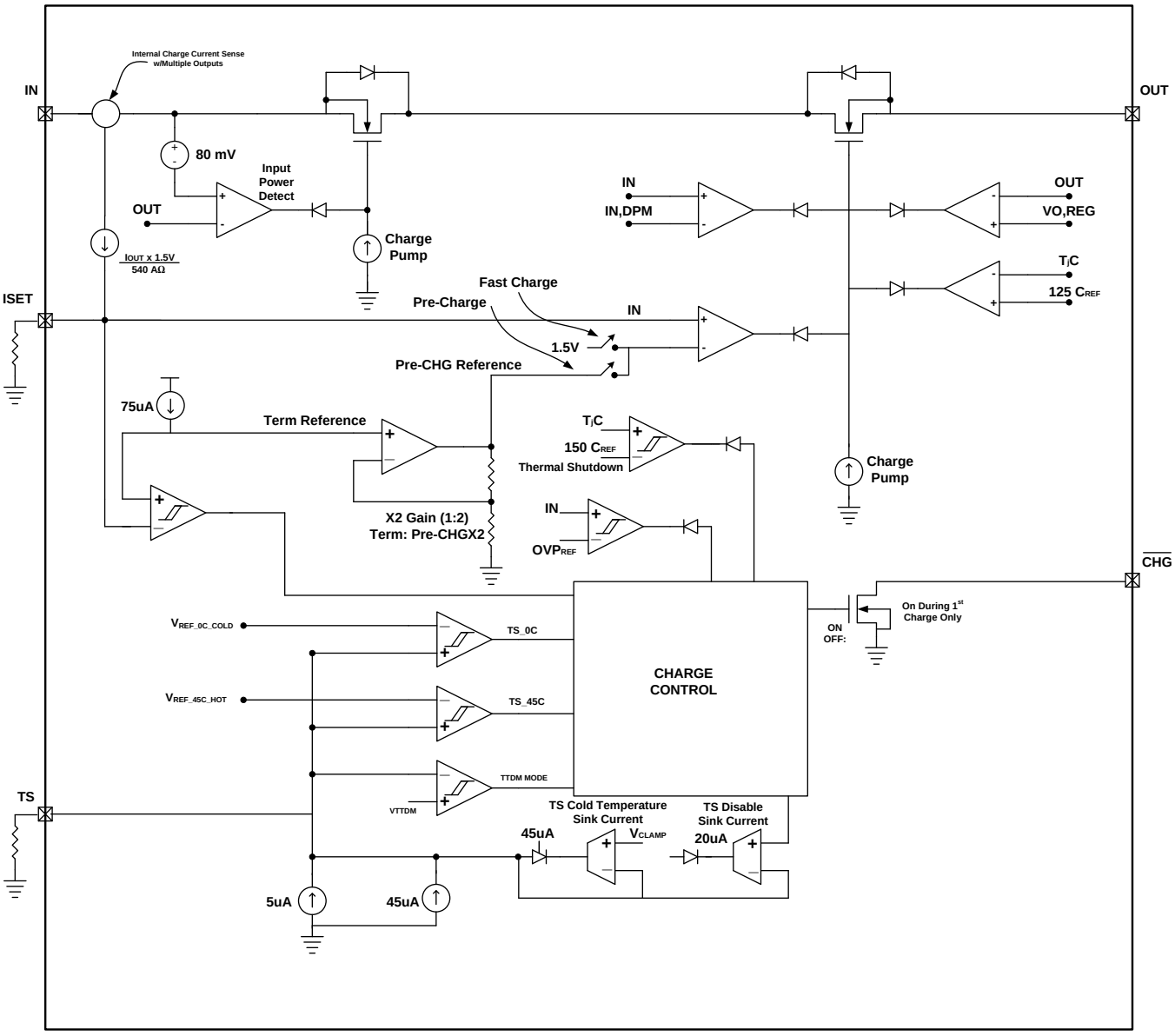
The charger is designed for a single power path from the input to the output to charge a single cell Li-Ion or Li-Pol battery pack. Upon application of a 5VDC power source the ISET and OUT short checks are performed to assure a proper charge cycle.

If the battery voltage is below the LOWV threshold, the battery is considered discharged and a preconditioning cycle begins. The amount of the current goes into the battery during this phase is called pre-charge current. It is fixed to 20% of the fast charge current.

Once the battery voltage has charged to the VLOWV threshold, fast charge is initiated and the fast charge current is applied. The fast charge constant current is programmed using the ISET terminal. The constant current provides the bulk of the charge. Power dissipation in the IC is greatest in fast charge with a lower battery voltage. If the IC reaches 125°C the IC enters thermal regulation, slows the timer clock by half and reduce the charge current as needed to keep the temperature from rising any further. 图 5 shows the charging profile with thermal regulation. Typically under normal operating conditions, the IC's junction temperature is less than 125°C and thermal regulation is not entered.

Once the cell has charged to the regulation voltage the voltage loop takes control and holds the battery at the regulation voltage until the current tapers to the termination threshold. The termination current is set to 10% of the fast charge current. The $\overline{\text{CHG}}$ terminal is low (LED on) during the first charge cycle only and turns off once the termination threshold is reached, regardless if termination, for charge current, is enabled or disabled.

8.2 Functional Block Diagram



8.3 Feature Description

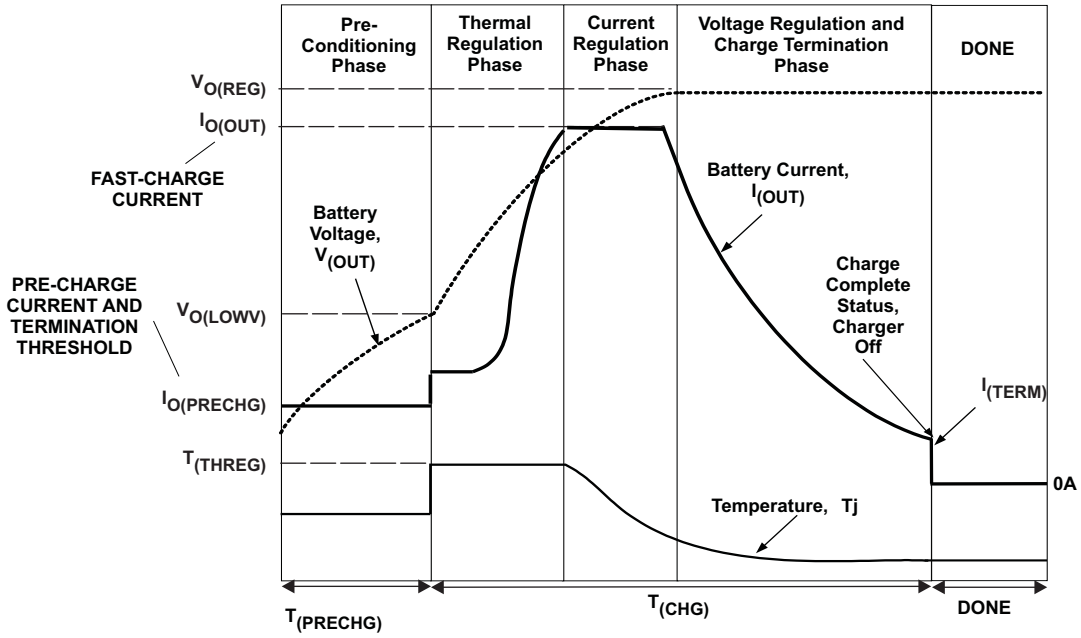


图 5. Charging Profile With Thermal Regulation

8.3.1 Power-Down or Undervoltage Lockout (UVLO)

The bq21040 is in power-down mode if the IN terminal voltage is less than UVLO. The part is considered “dead” and all the terminals are high impedance. Once the IN voltage rises above the UVLO threshold the IC will enter Sleep Mode or Active mode depending on the OUT terminal (battery) voltage.

8.3.2 Power-up

The IC is alive after the IN voltage ramps above UVLO (see sleep mode), resets all logic and timers, and starts to perform many of the continuous monitoring routines. Typically the input voltage quickly rises through the UVLO and sleep states where the IC declares power good, starts the qualification charge at 100mA starts the safety timer and enables the $\overline{CHG}$ terminal. See 图 6.

8.3.3 Sleep Mode

If the IN terminal voltage is between than V_{OUT}+V_{DT} and UVLO, the charge current is disabled, the safety timer counting stops (not reset) and the $\overline{CHG}$ terminal is high impedance. As the input voltage rises and the charger exits sleep mode, the safety timer continues to count, charge is enabled and the $\overline{CHG}$ terminal returns to its previous state. See 图 7.

8.3.4 New Charge Cycle

A new charge cycle is started when a good power source is applied, performing a chip disable/enable (TS terminal), exiting Termination and Timer Disable Mode (TTDM), detecting a battery insertion or the OUT voltage dropping below the VRCH threshold. The $\overline{CHG}$ terminal is active low only during the first charge cycle, therefore exiting TTDM or a dropping below VRCH will not turn on the $\overline{CHG}$ terminal FET, if the $\overline{CHG}$ terminal is already high impedance.

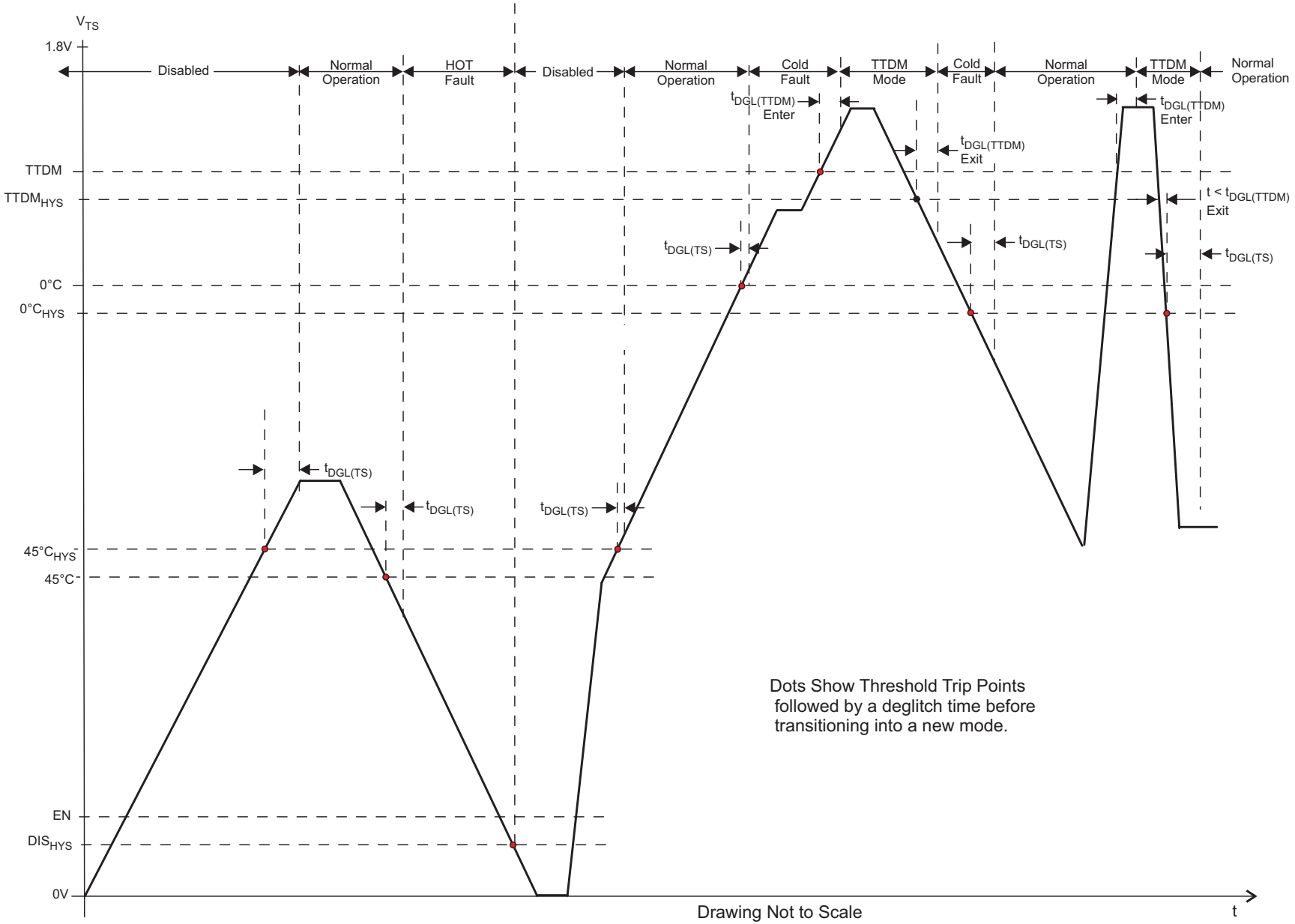


图 6. TS Battery Temperature Bias Threshold and Deglitch Timers

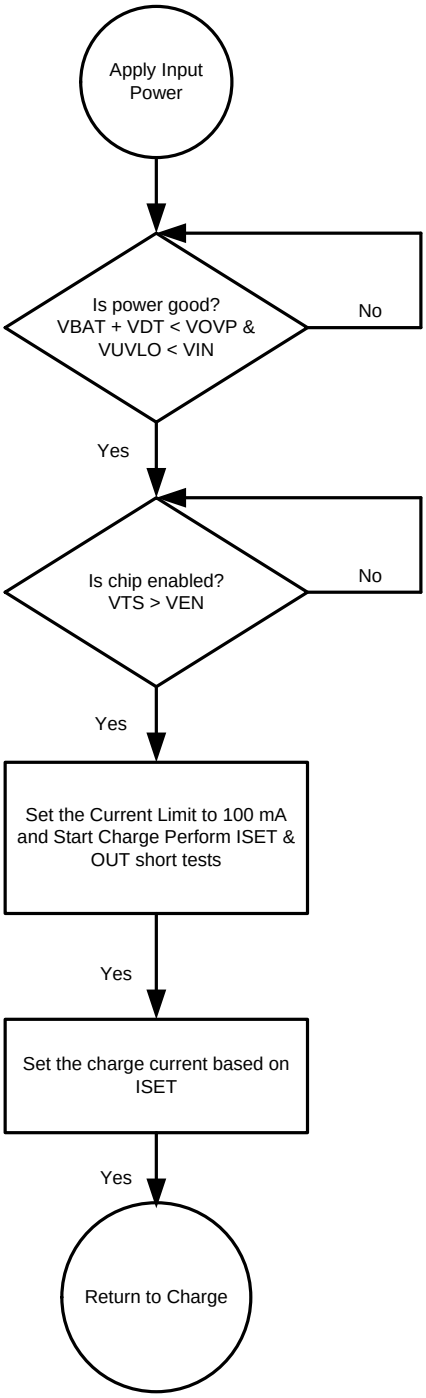


图 7. bq21040 Power-Up Flow Diagram

8.3.5 Overvoltage-Protection (OVP) – Continuously Monitored

If the input source applies an overvoltage, the pass FET, if previously on, turns off after a deglitch, $t_{BLK(OVP)}$. The timer ends and the $\overline{CHG}$ terminal goes to a high impedance state. After the overvoltage returns to a normal voltage, the timer continues, charge continues, and the $\overline{CHG}$ terminal goes low after a 25ms deglitch.

8.3.6 $\overline{\text{CHG}}$ Terminal Indication

The charge terminal has an internal open drain FET which is on (pulls down to V_{SS}) during the first charge only (independent of TTDM) and is turned off once the battery reaches voltage regulation and the charge current tapers to the termination threshold set by the PRE-TERM resistor. The bq21040 does not terminate charge, however, the $\overline{\text{CHG}}$ terminal will turn off once the battery current reaches 10% of the programmed charge current.

The charge terminal is high impedance in sleep mode and OVP and returns to its previous state once the condition is removed.

Cycling input power, pulling the TS terminal low and releasing or entering pre-charge mode causes the $\overline{\text{CHG}}$ terminal to go reset (go low if power is good and a discharged battery is attached) and is considered the start of a first charge.

8.4 Device Functional Modes

8.4.1 $\overline{\text{CHG}}$ LED Pull-up Source

For host monitoring, a pullup resistor is used between the STATUS terminal and the V_{CC} of the host and for a visual indication a resistor in series with an LED is connected between the STATUS terminal and a power source. If the $\overline{\text{CHG}}$ source is capable of exceeding 7 V, a 6.2-V Zener should be used to clamp the voltage. If the source is the OUT terminal, note that as the battery changes voltage, and the brightness of the LEDs vary.

表 1. Charging States and $\overline{\text{CHG}}$ LED

CHARGING STATE	$\overline{\text{CHG}}$ FET/LED
First charge after VIN applied	ON
Refresh charge	OFF
OVP	
SLEEP	
TEMP FAULT	ON for 1st Charge

8.4.2 IN-DPM (V_{IN}-DPM or IN-DPM)

The IN-DPM feature is used to detect an input source voltage that is folding back (voltage dropping), reaching its current limit due to excessive load. When the input voltage drops to the $V_{IN\text{-}DPM}$ threshold the internal pass FET starts to reduce the current until there is no further drop in voltage at the input. This would prevent a source with voltage less than $V_{IN\text{-}DPM}$ to power the out terminal. This works well with current limited adaptors and USB ports as long as the nominal voltage is above 4.3 V. This is an added safety feature that helps protect the source from excessive loads.

8.4.3 OUT

The Charger's OUT terminal provides current to the battery and to the system, if present. This IC can be used to charge the battery plus power the system, charge just the battery or just power the system (TTDM) assuming the loads do not exceed the available current. The OUT terminal is a current limited source and is inherently protected against shorts. If the system load ever exceeds the output programmed current threshold, the output will be discharged unless there is sufficient capacitance or a charged battery present to supplement the excessive load.

8.4.4 ISET

An external resistor is used to Program the Output Current (50 to 800 mA) and can be used as a current monitor.

$$R_{ISET} = K_{ISET} / I_{OUT} \quad (1)$$

where

- I_{OUT} is the desired fast charge current;
- K_{ISET} is a gain factor found in the electrical specification

For greater accuracy at lower currents, part of the sense FET is disabled to give better resolution. 图 1 shows the transition from low current to higher current. Going from higher currents to low currents, there is hysteresis and the transition occurs around 0.15 A.

The ISET resistor is short protected and will detect a resistance lower than ≠340 Ω. The detection requires at least 80mA of output current. If a “short” is detected, then the IC will latch off and can only be reset by cycling the power. The OUT current is internally clamped to a maximum current between 1.05 A and 1.4 A and is independent of the ISET short detection circuitry, as shown in 图 8. Also, see 图 23 and 图 24.

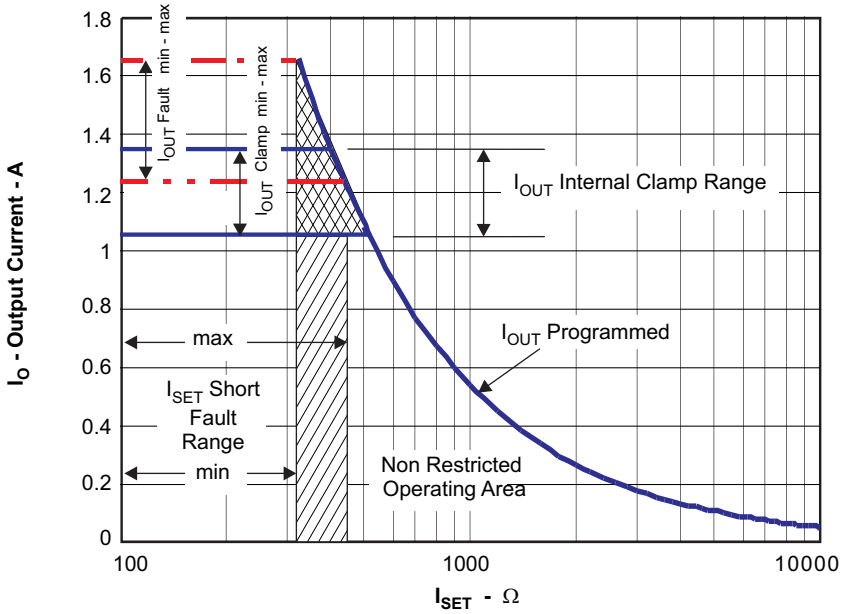


图 8. Programmed/Clamped Out Current

8.4.5 TS

The TS function is designed to follow the temperature sensing standard for Li-Ion and Li-Pol batteries. There are two thresholds, 45°C and 0°C. Normal operation occurs between 0°C and 45°C.

The TS feature is implemented using an internal 50μA current source to bias the thermistor (designed for use with a 10k NTC β = 3370 (SEMITEC 103AT-2 or Mitsubishi TH05-3H103F) connected from the TS terminal to V_{SS}. If this feature is not needed, a fixed 10kΩ can be placed between TS and V_{SS} to allow normal operation. This may be done if the host is monitoring the thermistor and then the host would determine when to pull the TS terminal low to disable charge.

The TS terminal has two additional features, when the TS terminal is pulled low or floated/driven high. A low disables charge (similar to a high on the BAT_EN feature) and a high puts the charger in TTDM.

Above 45°C or below 0°C the charge is disabled. Once the thermistor reaches ≠–10°C the TS current folds back to keep a cold thermistor (between –10°C and –50°C) from placing the IC in the TTDM mode. If the TS terminal is pulled low into disable mode, the current is reduce to ≠30μA, see 图 6. Since the I_{TS} curent is fixed along with the temperature thresholds, it is not possible to use thermistor values other than the 10k NTC (at 25°C).

8.4.6 Termination and Timer Disable Mode (TTDM) - TS Terminal High

The battery charger is in TTDM when the TS terminal goes high from removing the thermistor (removing battery pack/floating the TS terminal) or by pulling the TS terminal up to the TTDM threshold.

When entering TTDM, the 10 hour safety timer is held in reset and termination is disabled. A battery detect routine is run to see if the battery was removed or not. If the battery was removed then the $\overline{CHG}$ terminal will go to its high impedance state if not already there. If a battery is detected the $\overline{CHG}$ terminal does not change states until the current tapers to the termination threshold, where the $\overline{CHG}$ terminal goes to its high impedance state if not already there (the regulated output will remain on).

The charging profile does not change (still has pre-charge, fast-charge constant current and constant voltage modes). This implies the battery is still charged safely and the current is allowed to taper to zero.

When coming out of TTDM, the battery detect routine is run and if a battery is detected, then a new charge cycle begins and the $\overline{CHG}$ LED turns on.

If TTDM is not desired upon removing the battery with the thermistor, one can add a 237k resistor between TS and V_{SS} to disable TTDM. This keeps the current source from driving the TS terminal into TTDM. This creates ≠0.1°C error at hot and a ≠3°C error at cold.

8.4.7 Timers

The pre-charge timer is set to 30 minutes. The pre-charge current, can be programmed to off-set any system load, making sure that the 30 minutes is adequate.

The fast charge timer is fixed at 10 hours and can be increased real time by going into thermal regulation, IN-DPM or if in USB current limit. The timer clock slows by a factor of 2, resulting in a clock than counts half as fast when in these modes. If either the 30 minute or ten hour timer times out, the charging is terminated and the $\overline{CHG}$ terminal goes high impedance if not already in that state. The fast charge timer is reset by disabling the IC, cycling power or going into and out of TTDM.

8.4.8 Termination

Once the OUT terminal goes above VRCH, (reaches voltage regulation) and the current tapers down to the termination threshold (10% of the fast charge current), the $\overline{CHG}$ terminal goes high impedance and a battery detect route is run to determine if the battery was removed or the battery is full. If the battery is present, the charge current will terminate. If the battery was removed along with the thermistor, then the TS terminal is driven high and the charge enters TTDM. If the battery was removed and the TS terminal is held in the active region, then the battery detect routine will continue until a battery is inserted.

8.4.9 Battery Detect Routine

The battery detect routine should check for a missing battery while keeping the OUT terminal at a useable voltage. Whenever the battery is missing the $\overline{CHG}$ terminal should be high impedance.

The battery detect routine is run when entering and exiting TTDM to verify if battery is present, or run all the time if battery is missing and not in TTDM. On power-up, if battery voltage is greater than V_{RCH} threshold, a battery detect routine is run to determine if a battery is present.

The battery detect routine is disabled while the IC is in TTDM, or has a TS fault. See 图 9 for the Battery Detect Flow Diagram.

8.4.10 Refresh Threshold

After termination, if the OUT terminal voltage drops to V_{RCH} (100mV below regulation) then a new charge is initiated, but the $\overline{CHG}$ terminal remains at a high impedance (off).

8.4.11 Starting a Charge on a Full Battery

The termination threshold is raised by ≠14%, for the first minute of a charge cycle so if a full battery is removed and reinserted or a new charge cycle is initiated, that the new charge terminates (less than 1 minute). Batteries that have relaxed many hours may take several minutes to taper to the termination threshold and terminate charge.

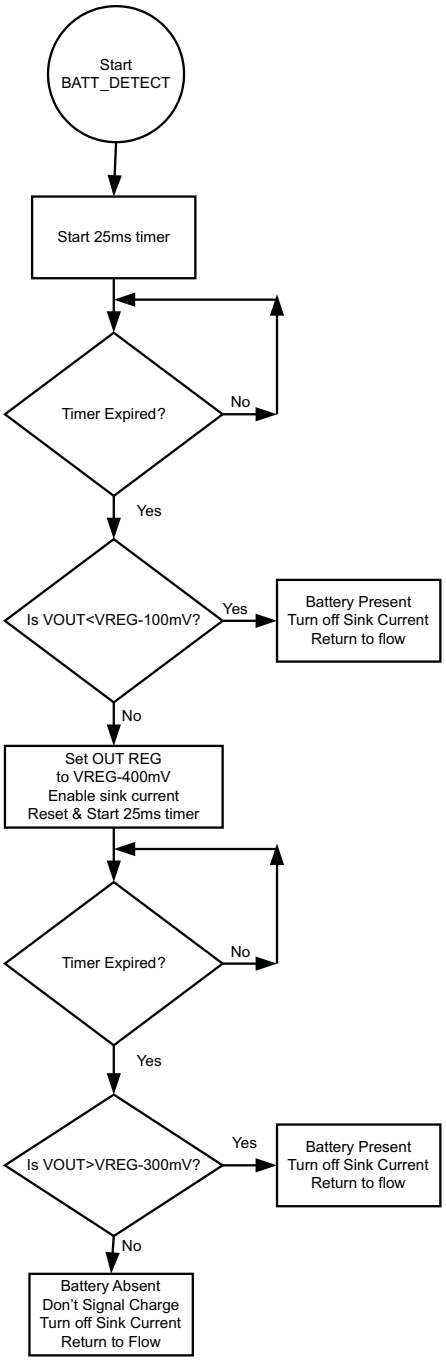


图 9. Battery Detect Routine (bq21040)

9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq21040 device is a highly integrated Li-Ion and Li-Pol linear charger device targeted at space-limited portable applications. The device operates from either a USB port or AC adapter. The high input voltage range with input overvoltage protection supports low-cost unregulated adapters. This device has a single power output that charges the battery. A system load can be placed in parallel with the battery as long as the average system load does not keep the battery from charging fully during the 10 hour safety timer.

9.2 Typical Application

$I_{OUT\_FAST\_CHG}$ = 540mA; $I_{OUT\_PRE\_CHG}$ = 108mA; I_{OUT_TERM} = 54mA

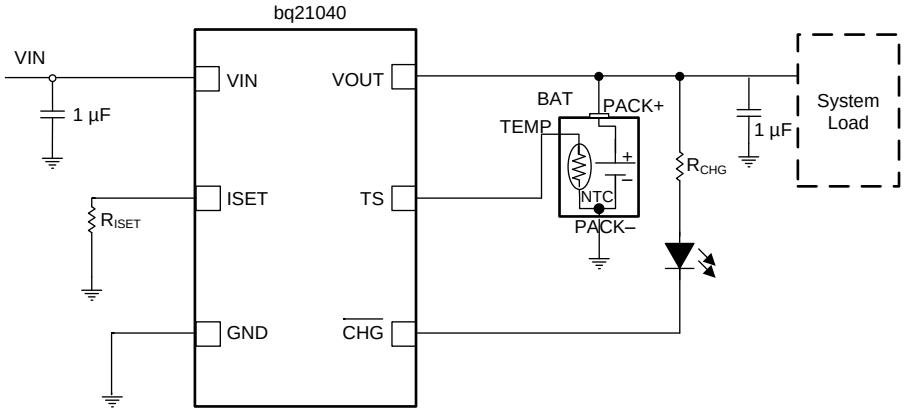

图 10. Typical Application Circuit

9.2.1 Design Requirements

- Supply voltage = 5 V
- Fast charge current: $I_{OUT\text{-}FC}$ = 540 mA; ISET-terminal 2
- Termination Current Threshold: $\%_{IOUT\text{-}FC}$ = 10% of Fast Charge or about 54mA
- Pre-Charge Current by default is twice the termination Current or about 108mA
- TS – Battery Temperature Sense = 10k NTC (103AT)

Typical Application (接下页)

9.2.2 Detailed Design Procedure

9.2.2.1 Calculations

9.2.2.1.1 Program the Fast Charge Current, ISET:

$$R_{ISET} = [K_{(ISET)} / I_{(OUT)}] \quad (2)$$

From the *Electrical Characteristics* table:

- $K_{(SET)}$ = 540AΩ
- R_{ISET} = [540AΩ/0.54A] = 1.0 kΩ

Selecting the closest standard value, use a 1.0 kΩ resistor between ISET (terminal 16) and Vss.

9.2.2.1.2 Pre-Charge and Termination Current Thresholds, ITERM, and PRE-CHG

$$TERM = I_{(OUT)} \times 10\%I_{OUT\text{-}FC} \quad (3)$$

$$TERM = 540mA \times 10\% = 54mA \quad (4)$$

One can calculate the pre-charge current by using 20% of the fast charge current (factor of 2 difference).

$$PRE\text{-}Charge = I_{(OUT)} \times 20\%I_{OUT\text{-}FC} \quad (5)$$

$$PRE\text{-}Charge = 540mA \times 20\% = 108mA \quad (6)$$

9.2.2.1.3 TS Function

Use a 10k NTC thermistor in the battery pack (103AT).

To Disable the temp sense function, use a fixed 10k resistor between the TS (terminal 1) and Vss.

9.2.2.1.4 $\overline{CHG}$

LED Status: connect a 1.5kΩ resistor in series with a LED between the OUT terminal and the $\overline{CHG}$ terminal.

Processor Monitoring: Connect a pull-up resistor between the processor's power rail and the $\overline{CHG}$ terminal.

9.2.2.2 Selecting In and Out Terminal Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power terminal, input and output terminals. Using the values shown on the application diagram, is recommended. After evaluation of these voltage signals with real system operational conditions, one can determine if capacitance values can be adjusted toward the minimum recommended values (DC load application) or higher values for fast high amplitude pulsed load applications. Note if designed for high input voltage sources (bad adaptors or wrong adaptors), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16V capacitor may be adequate for a 30V transient (verify tested rating with capacitor manufacturer).

Typical Application (接下页)

9.2.3 Application Curves

SETUP: bq21040 typical applications schematic; V_{IN} = 5V, V_{BAT} = 3.6V (unless otherwise indicated)

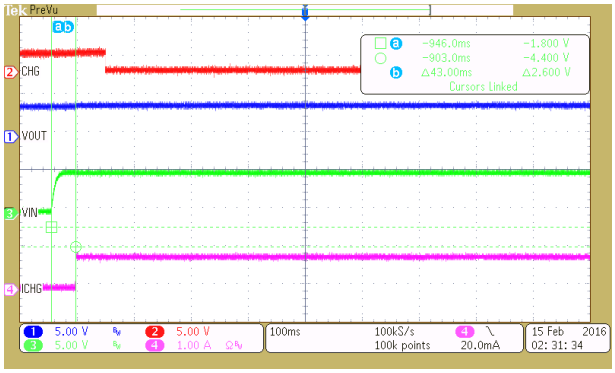

图 11. Power-Up Timing

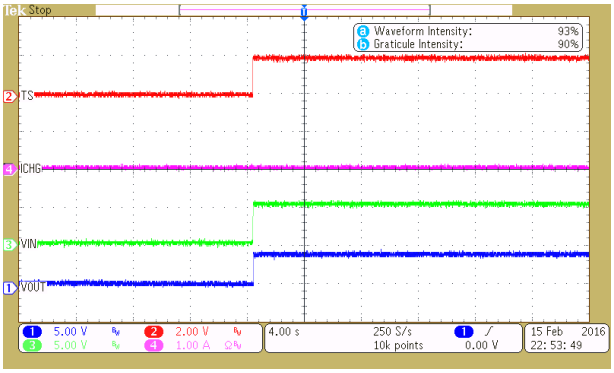

图 12. Power-Up Timing – No Battery or Load in TTDM

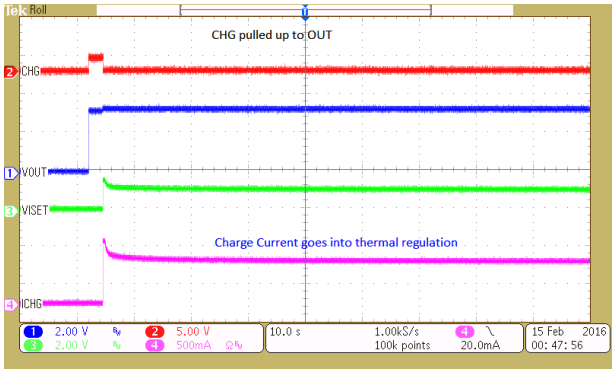

图 13. Start-Up in Thermal Regulation

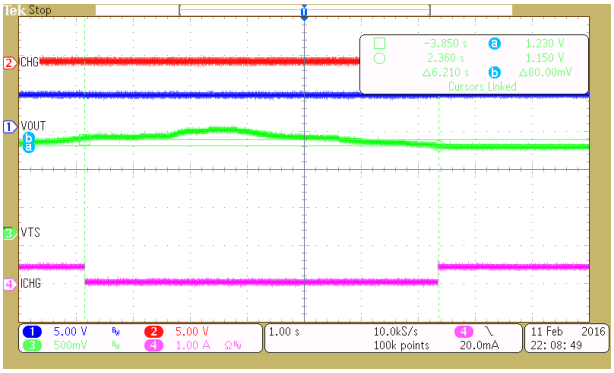

图 14. TS Entering and Leaving Cold Temperature

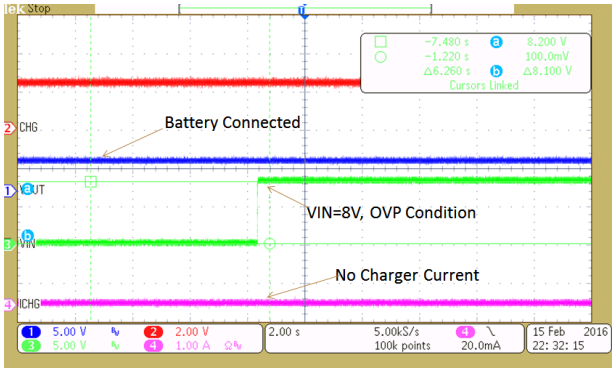

图 15. OVP 8-V Adaptor — Hot Plug

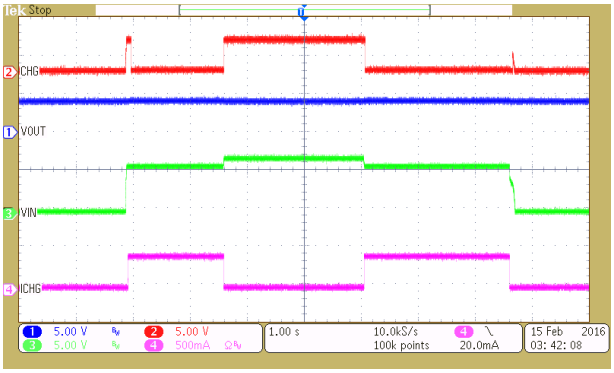

图 16. OVP From Normal Power-Up Operation – V_{IN} 0 V → 6 V → 7 V → 6 V→ 0 V

Typical Application (接下页)

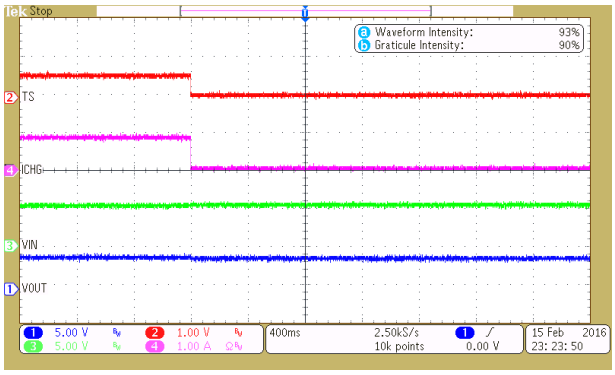

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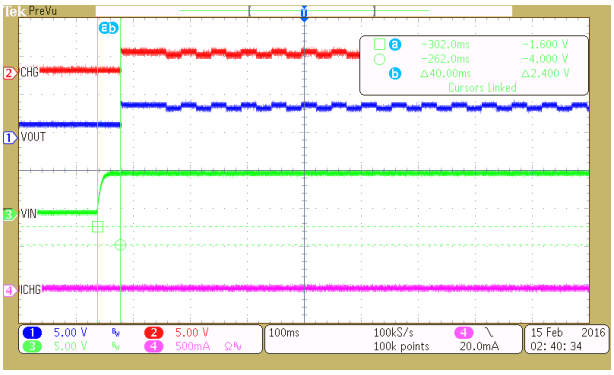
图 17. TS Enable and Disable



Fixed 10kΩ resistor, between TS and GND.

图 18. Power-Up Timing with No Battery and No Load – Battery Detection

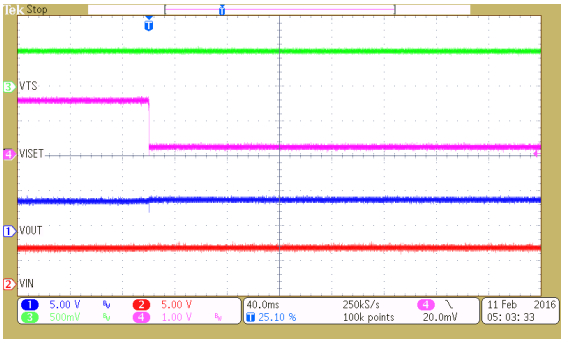


图 19. Battery Removal – GND Removed 1st, 42-Ω Load

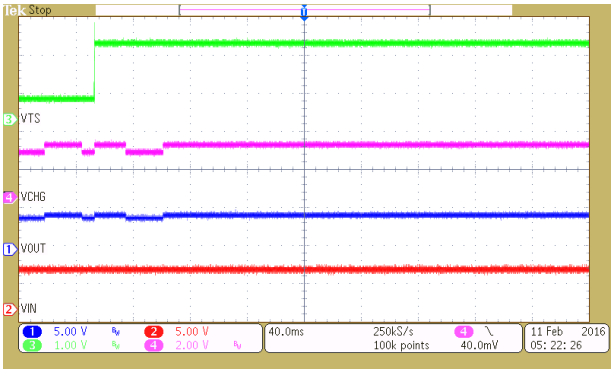
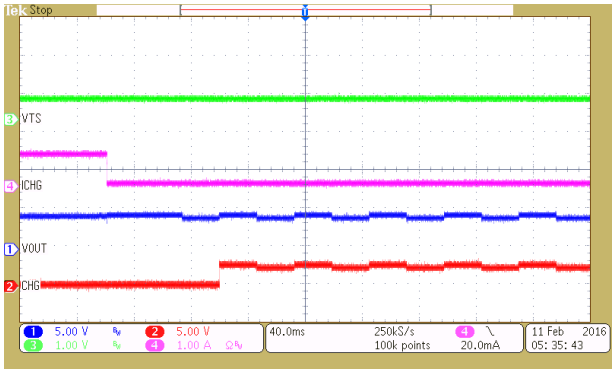
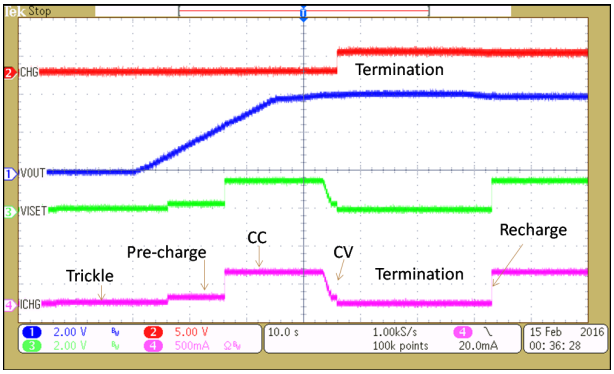


图 20. Battery Removal With OUT and TS Disconnect 1st, With 100-Ω Load



Continuous battery detection when not in TTDM

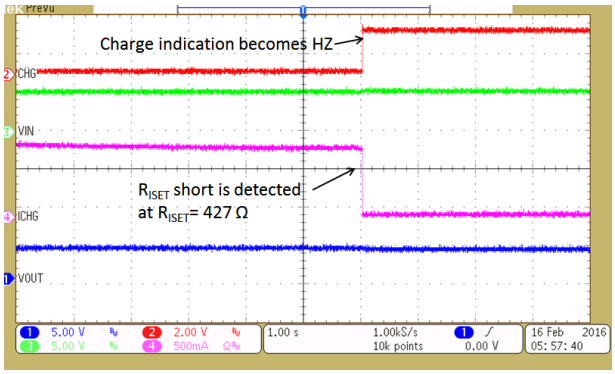
图 21. Battery Removal With Fixed TS = 0.5 V



CH4: I_{OUT} (1A/Div)
Battery voltage swept from 0V to 4.25V to 3.9V.

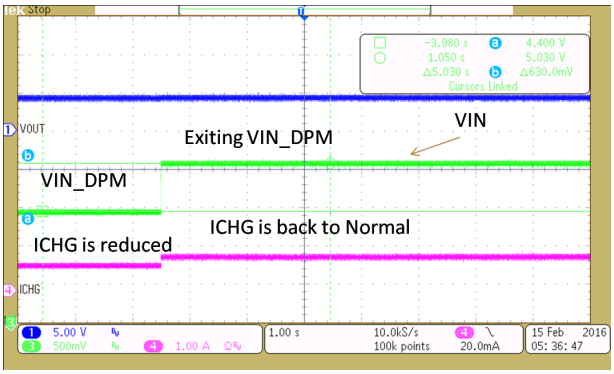
图 22. Battery Charge Profile

Typical Application (接下页)



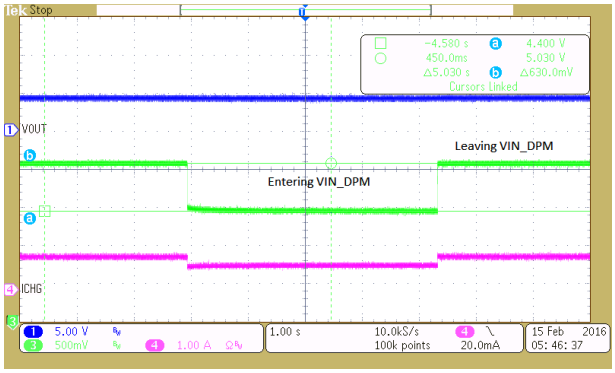
CH4: I_{OUT} (1A/Div)

图 23. ISET Shorted During Normal Operation



CH4: I_{OUT} (0.2A/Div)

图 24. ISET Shorted Prior to USB Power-up



CH4: I_{OUT} (0.2A/Div)

图 25. DPM – Adaptor Current Limits – VIN Regulated

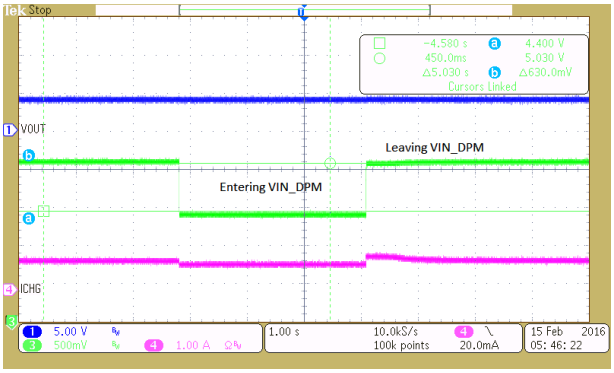
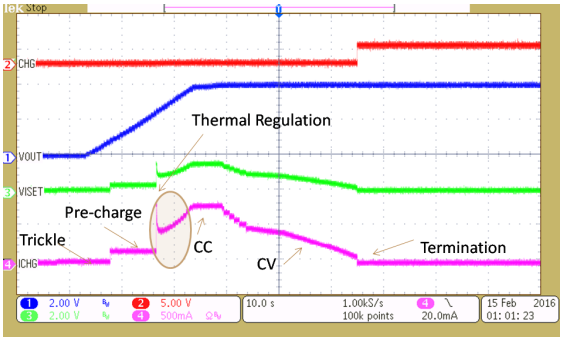


图 26. DPM – USB Current Limits – VIN Regulated to 4.4 V



The IC temperature rises to 125°C and enters thermal regulation. Charge current is reduced to regulate the IC at 125°C. VIN is reduced, the IC temperature drops, the charge current returns to the programmed value

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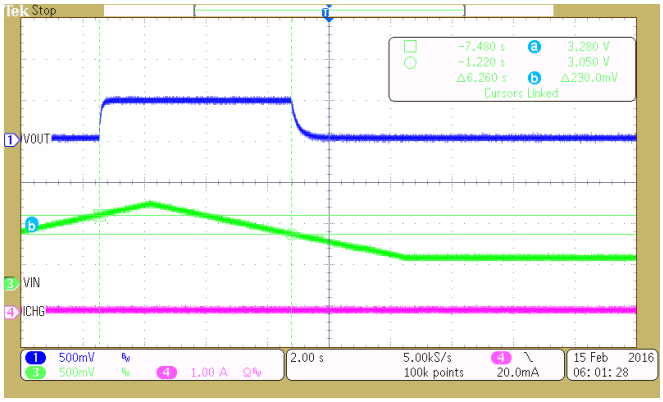
图 27. Charge Cycle With Thermal Regulation



V_{IN} swept from 5 V to 3.9 V to 5 V V_{BAT} = 4 V

图 28. Entering and Exiting UVLO

10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3.5 V and 28 V and current capability of at least the maximum designed charge current. This input supply should be well regulated. If located more than a few inches from the bq21040 IN and GND terminals, a larger capacitor is recommended.

11 Layout

11.1 Layout Guidelines

To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq21040, with short trace runs to both IN, OUT, and GND (thermal pad).

- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN terminal and from the OUT terminal must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces
- The bq21040 is packaged in a thermally-enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. It is best to use multiple 10mil vias in the power pad of the IC and close enough to conduct the heat to the bottom ground plane. The bottom ground place should avoid traces that “cut off” the thermal path. The thinner the PCB the less temperature rise. The EVM PCB has a thickness of 0.031 inches and uses 2 oz. (2.8mil thick) copper on top and bottom, and is a good example of optimal thermal performance.

11.2 Layout Example

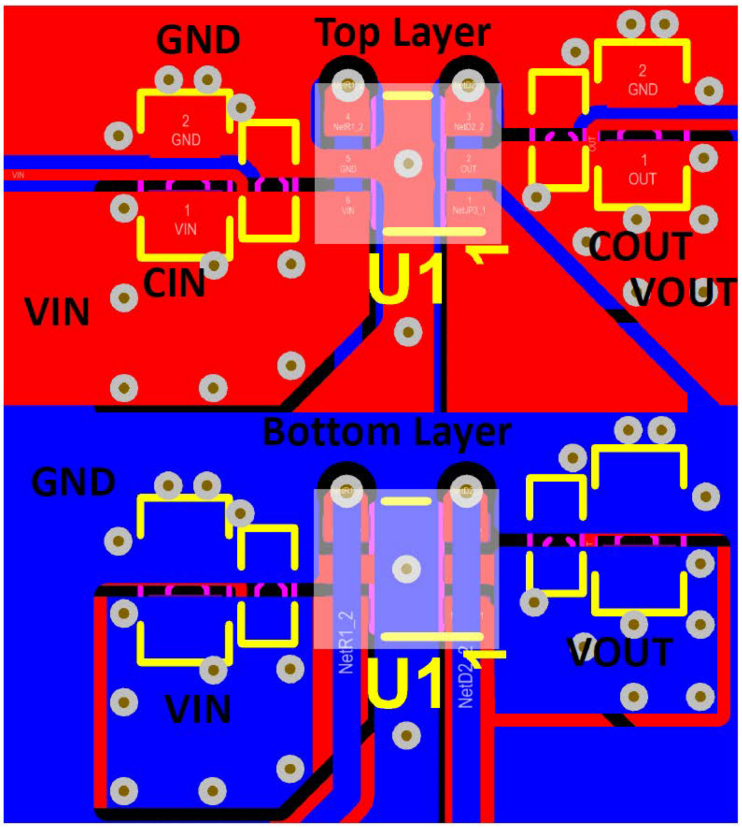


图 29. Board Layout

11.3 Thermal Considerations

The bq21040 is packaged in a thermally-enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). The power pad should be directly connected to the VSS terminal. The most common measure of package thermal performance is thermal impedance ($R_{\theta JA}$) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for ψ_{JT} is:

$$\psi_{JT} = (T_J - T) / P$$

where

- T_J = Chip junction temperature
- P = Device power dissipation
- T = Case temperature (7)

Factors that can influence the measurement and calculation of ψ_{JT} include:

1. Whether or not the device is board mounted
2. Trace size, composition, thickness, and geometry
3. Orientation of the device (horizontal or vertical)
4. Volume of the ambient air surrounding the device under test and airflow
5. Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-Ion and Li-Pol batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically after fast charge begins the pack voltage increases to ≠3.4V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4V is a good minimum voltage to use. This is verified, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad should have multiple vias), the charge current and the battery voltage as a function of time. The fast charge current will start to taper off if the part goes into thermal regulation.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged:

$$P = [V_{(IN)} - V_{(OUT)}] \times I_{(OUT)} + [V_{(OUT)} - V_{(BAT)}] \times I_{(BAT)} \quad (8)$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for non typical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

11.3.1 Leakage Current Effects on Battery Capacity

To determine how fast a leakage current on the battery will discharge the battery is an easy calculation. The time from full to discharge can be calculated by dividing the Amp-Hour Capacity of the battery by the leakage current. For a 0.75AHr battery and a 10μA leakage current (750 mAHr / 0.010 mA = 75000 hours), it would take 75k hours or 8.8 years to discharge. In reality the self discharge of the cell would be much faster so the 10μA leakage would be considered negligible.

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.3 商标

E2E is a trademark of Texas Instruments.
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12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ21040DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	0 to 125	130E	Samples
BQ21040DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	0 to 125	130E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

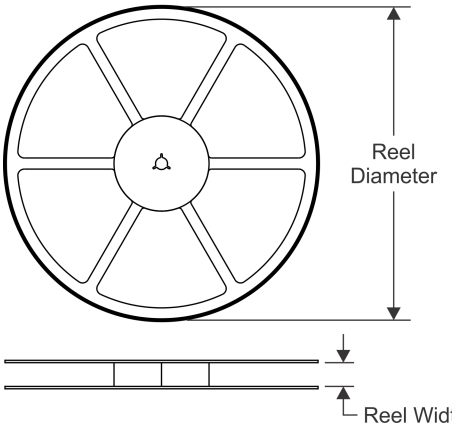
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

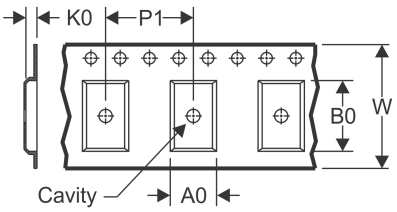
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

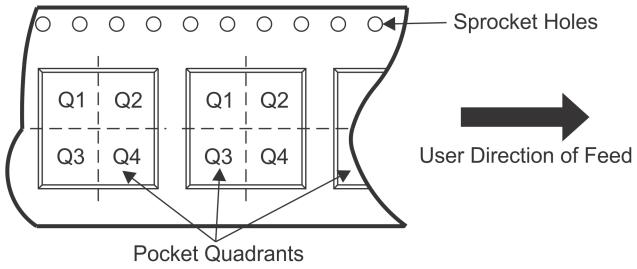


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

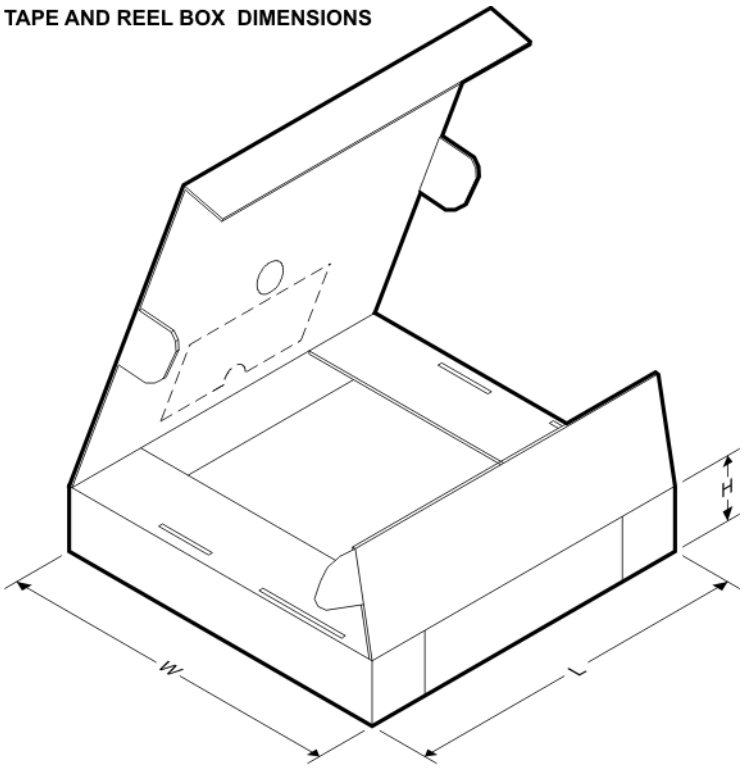
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ21040DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
BQ21040DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

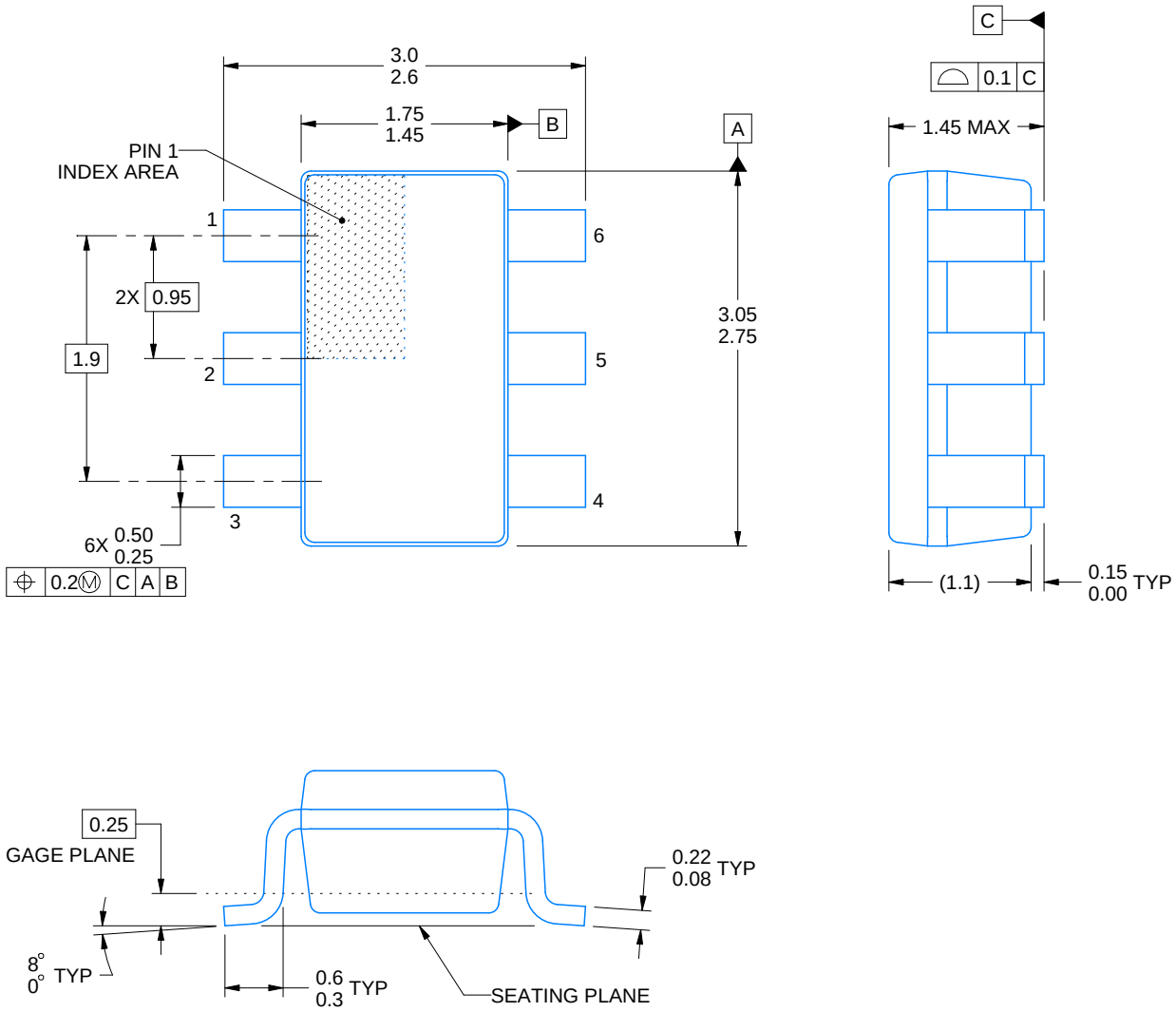
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ21040DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
BQ21040DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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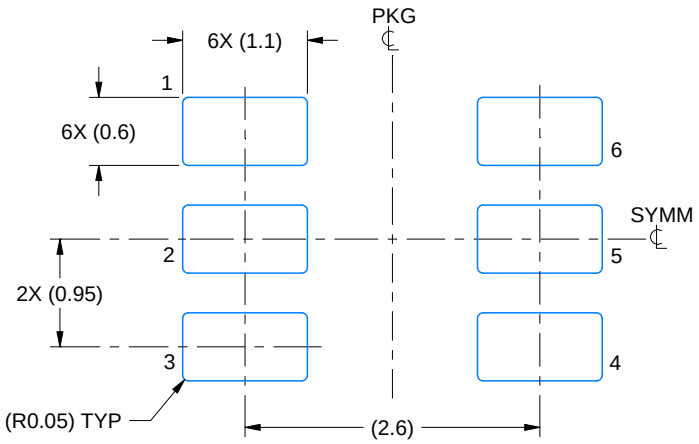
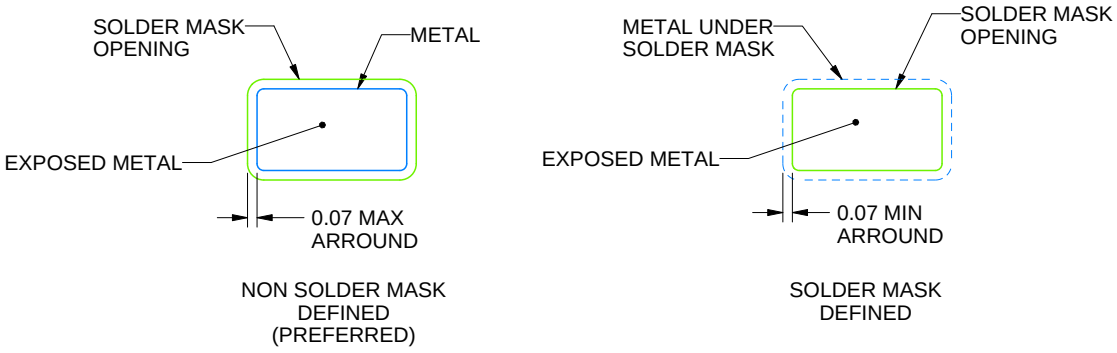
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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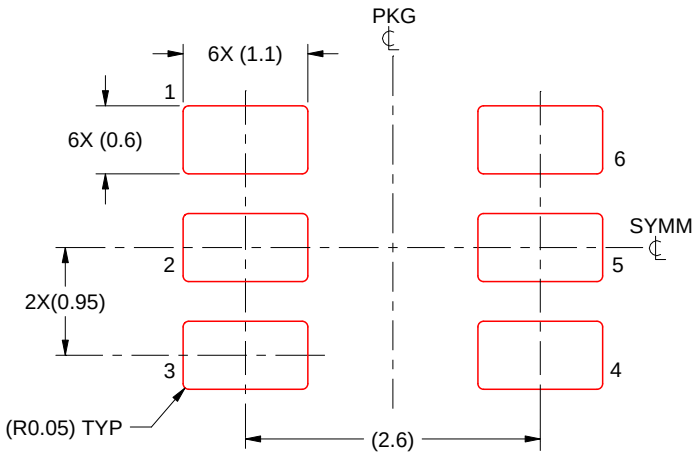
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122