TEXAS INSTRUMENTS

TCAN1046V-Q1 and TCAN1048V-Q1 汽车类高速双路 CAN 收发器

1 特性

- AEC Q100：符合汽车类 应用标准
  - 器件温度等级 1：
    –40°C 至 125°C T_A
- 符合 ISO 11898-2:2016 和 ISO 11898-5:2007 物理层标准的要求
- 高达 5Mbps 的传统 CAN 和 CAN FD 支持
  - 较短的对称传播延迟时间和快速循环次数增加时序余量
  - 在有负载 CAN 网络中实现更快的数据速率
- I/O 电压范围：1.8V 至 5V
- 优化了未上电时的性能
  - 总线和逻辑终端为高阻抗（运行总线或应用上无负载）
  - 支持热插拔：总线和 RXD 输出端加电/断电时的无毛刺脉冲运行
- 符合或超出以下标准要求：
  - SAE J2962-2 (2016) 通信收发器认证
  - GIFT/ICT
  - ISO 16845-2 高速媒介访问单元一致性
- 保护 特性
  - 总线终端的 IEC ESD 保护：±15kV
  - 总线故障保护：±42V
  - 电源终端欠压保护
  - 驱动器显性超时 (TXD DTO)
    - 数据速率低至 9.2kbps
  - 热关断保护 (TSD)
- 结温范围：-40°C 至 150°C
- 可提供 SOIC (14) 封装和无引线 VSON (14) 封装 4.5 mm x 3.0 mm，提高了自动光学检测 (AOI) 能力

2 应用

- 12V 系统 应用
- 汽车和运输
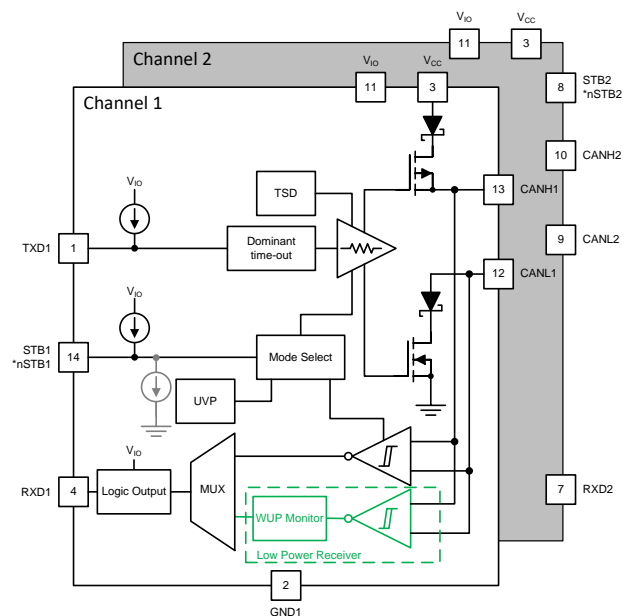 - 车身控制模块
  - 网关
  - 高级驾驶员辅助系统 (ADAS)
  - 信息娱乐系统

3 说明

TCAN1046V-Q1 and TCAN1048V-Q1 器件均为双路高速控制器局域网 (CAN) 收发器，满足 ISO 11898-2:2016 高速 CAN 规范的物理层要求，可提供 CAN 总线和 CAN 协议控制器之间的接口。TCAN1046V-Q1 and TCAN1048V-Q1 器件支持传统 CAN 和 CAN FD 网络，具有最高 5Mbps 的数据速率。器件具有通过 V_{IO} 端子实现的内部逻辑电平转换功能，允许直接连接到 1.8V、3.3V 或 5V 控制器。这些器件具有低功耗待机模式，可通过 ISO 11898-2:2016 定义的唤醒模式 (WUP) 实现远程唤醒。 TCAN1046V-Q1 and TCAN1048V-Q1 器件具有许多保护和诊断 特性，包括热关断 (TSD)、驱动器显性超时 (TXD DTO) 和高达 ±42V 的总线故障保护。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
TCAN1046V-Q1 TCAN1048V-Q1	SOIC (14)	8.95mm x 3.91mm
	VSON (14)	4.50mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化方框图

* TCAN1048V-Q1 通过集成的下拉至接地功能支持 nSTB

ADVANCE INFORMATION

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2018 年 9 月	*	最初发布版本

ADVANCE INFORMATION

5 Pin Configuration and Functions

D Package TCAN1046V-Q1 and TCAN1048V-Q1
14 Pin SOIC
Top View

Not to scale
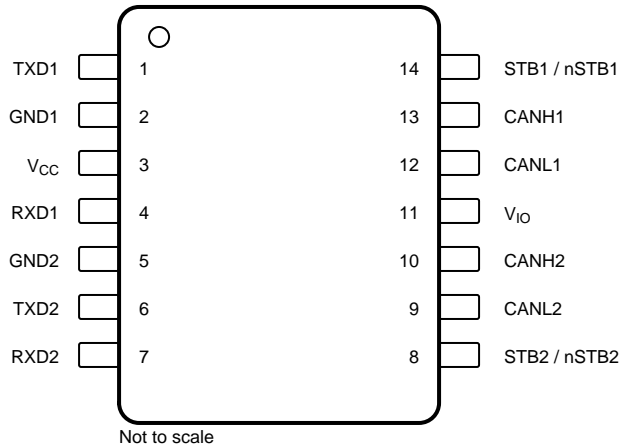
DMT Package TCAN1046V-Q1 and TCAN1048V-Q1
14 Pin VSON
Top View

Not to scale

ADVANCE INFORMATION
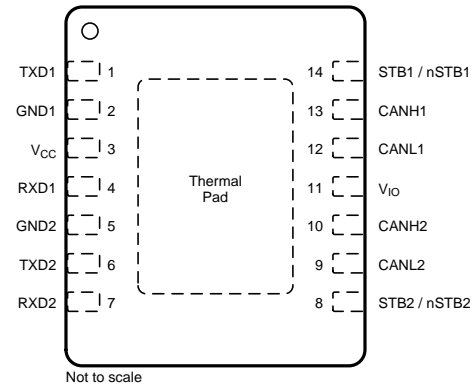
Pin Functions

PINS			Type	Description
Name	D	DMT		
TXD1	1	1	Digital Input	CAN transmit data input 1 (low for dominant and high for recessive bus states)
GND1	2	2	GND	Ground connection one
V_{CC}	3	3	Supply	5-V supply voltage
RXD1	4	4	Digital Output	CAN receive data output 1 (low for dominant and high for recessive bus states), tri-state when powered off
GND2	5	5	GND	Ground connection two
TXD2	6	6	Digital Input	CAN transmit data input 2 (low for dominant and high for recessive bus states)
RXD2	7	7	Digital Output	CAN receive data output 1 (low for dominant and high for recessive bus states), tri-state when powered off
STB2	8	8	Digital Input	Standby input 2 for mode control, integrated pull up (TCAN1046V–Q1)
nSTB2				Standby input 2 for mode control, integrated pull down (TCAN1048V–Q1)
CANL2	9	9	Bus I/O	Low-level CAN bus 2 input/output line
CANH2	10	10	Bus I/O	High-level CAN bus 2 input/output line
V_{IO}	11	11	Supply	I/O supply voltage
CANL1	12	12	Bus I/O	Low-level CAN bus 1 input/output line
CANH1	13	13	Bus I/O	High-level CAN bus 1 input/output line
STB1	14	14	Digital Input	Standby input 1 for mode control, integrated pull up (TCAN1046V–Q1)
nSTB1				Standby input 1 for mode control, integrated pull down (TCAN1048V–Q1)
Thermal Pad	—	—		Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	−0.3	6	V
V_{IO}	Supply voltage I/O level shifter	−0.3	6	V
V_{BUS}	CAN Bus I/O voltage (CANH1, CANL1 & CANH2, CANL2)	−42	42	V
V_{DIFF}	Max differential voltage range between CANH1, CANL1 & CANH2, CANL2	-27	27	V
V_{Logic_Input}	Logic input terminal voltage	−0.3	6	V
V_{RXD}	RXD output terminal voltage range (V_{RXD1}, V_{RXD2})	−0.3	6	V
$I_{O(RXD)}$	RXD output current (I_{ORXD1}, I_{ORXD2})	−8	8	mA
T_J	Operating virtual junction temperature range	−40	150	°C
T_{STG}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	HBM classification level 3A for all pins	±4000	V
			HBM classifification level 3B for global pins CANH & CANL	±10000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings, IEC Specification

				VALUE	UNIT
V_{ESD}	System level electro-static discharge (ESD)[1]	CAN bus terminals (CANH1, CANL1 & CANH2, CANL2) to GND	IEC 61000-4-2 (150pF, 330Ω): Unpowered contact discharge	±15000	V
V_{Tran}	ISO7637 ISO Pulse Transients[2]	CAN bus terminals (CANH1, CANL1 & CANH2, CANL2)	Pulse 1	−100	V
			Pulse 2a	75	V
			Pulse 3a	−150	V
			Pulse 3b	100	V
	ISO7637 Slow transients pulse[3]	CAN bus terminals (CANH1, CANL1 & CNAH2, CANL2) to GND	DCC slow transient pulse	±85	V

(1) Tested according to IEC 62228-3 CAN Transcievers (2018), Section 6.4; DIN EN 61000-4.
(2) Tested according to IEC 62228-3 CAN Transcievers (2018), Section 6.3; standard pulses parameters defined in ISO 7637-2 (2011)
(3) Tested according to ISO 7637-3 (2017); Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{CC}	Supply voltage - VeLIO Compliance	4.75	5	5.25	V
V_{IO}	Supply voltage for I/O level shifter	1.7		5.5	V
$I_{OH(RXD)}$	RXD terminal high level output current – $I_{OH(RXD1)}$ & $I_{OH(RXD2)}$	−2			mA
$I_{OL(RXD)}$	RXD terminal low level output current – $I_{OL(RXD1)}$ & $I_{OL(RXD2)}$			2	mA
T_A	Operational free-air temperature (see thermal characteristics table)	−40		125	°C

6.5 Thermal Characteristics

THERMAL METRIC		TCAN1046V–Q1 TCAN1048V–Q1		UNIT
		D (SOIC)	DMT (VSON)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.6	35.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.4	38.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34	13.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5	1.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	32.6	13.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	3.5	°C/W

6.6 Power Supply Characteristics

Over recomended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current normal mode	Dominant One channel	See 图 6,TXD = 0 V, R_L = 60 Ω, C_L = open			70	mA
I_{CC}	Supply current normal mode	Dominant One channel	See 图 6, TXD = 0 V, R_L = 50 Ω, C_L = open			80	mA
I_{CC}	Supply current normal mode	Dominant Two channels	See 图 6, TXD = 0 V, R_L = 60 Ω, C_L = open			130	mA
	Supply current normal mode	Dominant Two channels	See 图 6, TXD = 0 V, R_L = 50 Ω, C_L = open			140	mA
	Supply current normal mode	Recessive Two channels	See 图 6, TXD = V_{CC}, R_L = 50 Ω, C_L = open, RCM = open			10	mA
I_{CC}	Supply current normal mode	Dominant with bus fault One channel	See 图 6, TXD = 0 V, CANH1 = CANL1 = CANH2 = CANL2 = ±25 V, R_L = open, C_L = open			180	mA
I_{CC}	Supply current normal mode	Dominant with bus fault Two channels	See 图 6, TXD = 0 V, CANH1 = CANL1 = CANH2 = CANL2 = ±25 V, R_L = open, C_L = open			360	mA
I_{CC}	Supply current standby mode[1]		See 图 6, TXD = V_{CC}, R_L = 60 Ω, C_L = open			2	µA
I_{IO}	I/O supply current normal mode	Dominant One channel	RXD floating, TXD = 0 or 5.5 V			300	µA
I_{IO}	I/O supply current normal mode	Dominant Two channels	RXD floating, TXD = 0 V			600	µA
I_{IO}	I/O supply current normal mode	Recessive One channel	RXD floating, TXD = V_{CC}			35	µA
I_{IO}	I/O supply current normal mode	Recessive Two channels	RXD floating, TXD = V_{CC}			70	µA
I_{IO}	I/O supply current standby mode[1]		RXD floating, TXD = V_{CC}			22	µA
UV_{VCC}	Rising under voltage detection on V_{CC} for protected mode				4.2	4.4	V
UV_{VCC}	Falling under voltage detection on V_{CC} for protected mode			3.5	4	4.5	V
UV_{VIO}	Rising under voltage detection on V_{IO}					1.65	V
UV_{VIO}	Falling under voltage detection on V_{IO}			1.4			V

(1) Total supply current in standby mode has a maximum value of 24µA and is typically 17µA (I_{CC} + I_{IO})

ADVANCE INFORMATION

ADVANCE INFORMATION

6.7 Dissipation Ratings

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation one channel Normal mode	V_{CC} = 5 V, V_{IO} = 1.8 V, T_J = 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		V
		V_{CC} = 5 V, V_{IO} = 3.3 V, T_J = 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5 V, V_{IO} = 5 V, T_J = 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5.5 V, V_{IO} = 1.8 V, T_J = 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5.5 V, V_{IO} = 3.3 V, T_J = 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5.5 V, V_{IO} = 3.3 V, T_J = 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5 V, V_{IO} = 1.8 V, T_J = 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5 V, V_{IO} = 3.3 V, T_J = 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5 V, V_{IO} = 5 V, T_J = 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5.5 V, V_{IO} = 1.8 V, T_J = 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5.5 V, V_{IO} = 3.3 V, T_J = 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
		V_{CC} = 5.5 V, V_{IO} = 3.3 V, T_J = 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		TBD		
T_{TSD}	Thermal shutdown temperature			192		°C
T_{TSD_HYS}	Thermal shutdown hysteresis			10		

6.8 Electrical Characteristics

Over recomended operating conditions with T_J = -40°C to 150°C (unless otherwise noted); CAN Electrical Parameters Apply To Both Channels

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{O(D)}$	Dominant output voltage normal mode	CANH	See 图 4 and 图 7, TXD = 0 V, R_L = 60 Ω, C_L = open	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(R)}$	Recessive output voltage normal mode		See 图 4 and 图 7, TXD = V_{CC}, R_L = open	2	0.5 x V_{CC}	3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}		See 图 7 and 图 18, R_{TERM} = 60 Ω, C_L = open, C_{SPLIT} = 4.7 nF	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry (V_{CC} - $V_{O(CANH)}$ - $V_{O(CANL)}$)		See 图 4 and 图 7, R_L = 60 Ω, C_L = open	–400		400	mV

Electrical Characteristics (continued)

Over recomended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted); CAN Electrical Parameters Apply To Both Channels

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(D)}$	Differential output voltage normal mode Dominant	See 图 4 and 图 7, TXD = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open	1.5		3	V
		See 图 4 and 图 7, TXD = 0 V, 45 Ω ≤ R_L ≤ 70 Ω, C_L = open	1.4		3.3	V
		See 图 4 and 图 7, TXD = 0 V, R_L = 2240 Ω, C_L = open	1.5		5	V
$V_{OD(R)}$	Differential output voltage normal mode Recessive	See 图 4 and 图 7, TXD = V_{CC}, R_L = 60 Ω, C_L = open	−120		12	mV
		See 图 4 and 图 7, Normal mode, TXD = V_{CC}, R_L = open, C_L = open	−50		50	mV
$V_{O(STB)}$	Bus output voltage standby mode	CANH, no load	-0.1	0	0.1	V
		CANL, no load	-0.1	0	0.1	V
		CANH - CANL, no load	-0.2	0	0.2	V
$I_{OS(DOM)}$	Short-circuit steady-state output current, Dominant	See 图 4 and 图 13, Normal mode, -15 V ≤ $V_{(CANH)}$ ≤ 40 V, TXD = 0 V	−115			mA
		See 图 4 and 图 13, Normal mode, -15 V ≤ $V_{(CAN\_L)}$ ≤ 40 V, TXD = 0 V			115	mA
$I_{OS(REC)}$	Short-circuit steady-state output current; Recessive	See 图 4 and 图 13, Normal mode, −27 V ≤ V_{BUS} ≤ 32 V, V_{BUS} = CANH = CANL	−5		5	mA
Receiver Electrical Characteristics						
V_{IT}	Input threshold voltage normal mode	See 图 8, 表 1, and 表 5 -12 V ≤ V_{CM} ≤ 12 V	500		900	mV
$V_{IT(STB)}$	Input threshold standby mode	See 图 8, 表 1, and 表 5 -12 V ≤ V_{CM} ≤ 12 V	400		1150	mV
$V_{DIFF(DOM)}$	Normal mode dominant state differential input voltage range	See 图 8, 表 1, and 表 5 -12 V ≤ V_{CM} ≤ 12 V	0.9		9	V
$V_{DIFF(DOM)}$	Standby mode dominant state differential input voltage range	See 图 8, 表 1, and 表 5 -12 V ≤ V_{CM} ≤ 12 V	1.15		9	V
$V_{DIFF(REC)}$	Normal mode recessive state differential input voltage range	See 图 8, 表 1, and 表 5 -12 V ≤ V_{CM} ≤ 12 V	-4		0.5	V
$V_{DIFF(REC)}$	Standby mode recessive state differential input voltage range	See 图 8, 表 1, and 表 5 -12 V ≤ V_{CM} ≤ 12 V	-4		0.4	V
V_{HYS}	Hysteresis voltage for input threshold normal mode	See 图 8, 表 1, and 表 5 -12 V ≤ V_{CM} ≤ 12 V		100		mV
V_{CM}	Common mode range normal and standby modes	See 图 8 and 表 5	−12		12	V
$I_{LKG(IOFF)}$	Unpowered bus input leakage current	CANH = CANL = 5 V, V_{CC} = V_{IO} = GND			5	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{CC} , V_{IO} = V_{CC}			20	pF
C_{ID}	Differential input capacitance	TXD = V_{CC} , V_{IO} = V_{CC}			10	pF
R_{ID}	Differential input resistance	Normal mode, TXD = V_{CC} = V_{IO} = 5 V -12 V ≤ V_{CM} ≤ 12 V	40		90	kΩ
R_{IN}	Single ended input resistance (CANH or CANL)		20		45	kΩ
$R_{IN(M)}$	Input resistance matching [1 − ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	$V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5V	−1%		1%	
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage		0.7 × V_{IO}			V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 × V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5 V	−2.5	0	1	µA

ADVANCE INFORMATION

ADVANCE INFORMATION

Electrical Characteristics (continued)

Over recomended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted); CAN Electrical Parameters Apply To Both Channels

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Low-level input leakage current	TXD = 0 V, V_{CC} = V_{IO} = 5.5 V	−200	-100	−20	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V, V_{CC} = V_{IO} = 0 V	−1	0	1	µA
C_I	Input Capacitance	V_{IN} = 0.4×sin(2×π×2×10^6×t)+2.5 V		5		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level input voltage	See 图 8, I_O = −2 mA	0.8 × V_{IO}			V
V_{OL}	Low-level input voltage	See 图 8, I_O = 2 mA			0.2 × V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5 V, V_{CC} = V_{IO} = 0 V	−1	0	1	µA
STB, nSTB Terminal (Standby Mode Input)						
V_{IH}	High-level input voltage		0.7 × V_{IO}			V
V_{IL}	Low-level input voltage				0.3 × V_{IO}	V
I_{IH}	High-level input leakage current STB	V_{CC} = V_{IO} = STB = 5.5 V	−2		2	µA
I_{IL}	Low-level input leakage current STB	V_{CC} = V_{IO} = 5.5 V, STB = 0 V	−20		−2	µA
I_{IH}	Low-level input leakage current nSTB	V_{CC} = V_{IO} = nSTB = 5.5 V	2		20	µA
I_{IL}	High-level input leakage current nSTB	V_{CC} = V_{IO} = 5.5 V, nSTB = 0 V	−2		2	µA
$I_{LKG(OFF)}$	Unpowered leakage current	STB = 5.5V, nSTB = 0, V_{CC} = V_{IO} = 0 V	−1	0	1	µA

6.9 Switching Characteristics

Over recomended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted); Timing parameters apply to both CAN channels

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	See 图 9 , Normal mode, V_{IO} = 2.8 V to 5 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		100	180	ns
		See 图 9 , Normal mode, V_{IO} = 1.8 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		150	255	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	See 图 9 , Normal mode, V_{IO} = 2.8 V to 5 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		110	180	ns
		See 图 9 , Normal mode, V_{IO} = 1.8 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		150	255	ns
t_{MODE}	Mode change time, from Normal to Standby or from Standby to Normal	See 图 10			20	µs
t_{WK_FILTER}	Filter time for a valid wake-up pattern	See 图 16	0.5		1.8	µs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout value	See 图 16	0.8		5	ms
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	See 图 7 R_L = 60 Ω, C_L = 100 pF, R_{CM} = open		75		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			65		ns
$t_{sk(p)}$	Pulse skew (|tpHR - tpLD|)			20		ns
t_R	Differential output signal rise time			45		ns
t_F	Differential output signal fall time			45		ns
t_{TXD_DTO}	Dominant timeout	See 图 12, R_L = 60 Ω, C_L = 100 pF	1.2		4.0	ms

Switching Characteristics (continued)

Over recomended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted); Timing parameters apply to both CAN channels

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high output (dominant to recessive)	See 图 8 $C_{L(RXD)}$ = 15 pF		65		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (recessive to dominant)			50		ns
t_R	RXD output signal rise time			10		ns
t_F	RXD output signal fall time			10		ns
FD Timing Characteristics						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	See 图 9, STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	435		530	ns
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns		155		210	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns		400		550	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns		120		220	ns
t_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	-65		40	ns
t_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns		-45		15	ns

6.10 Typical Characteristics

图 1. $V_{OD(D)}$ over Temperature

图 2. $V_{OD(D)}$ over V_{CC}

ADVANCE INFORMATION

7 Parameter Measurement Information
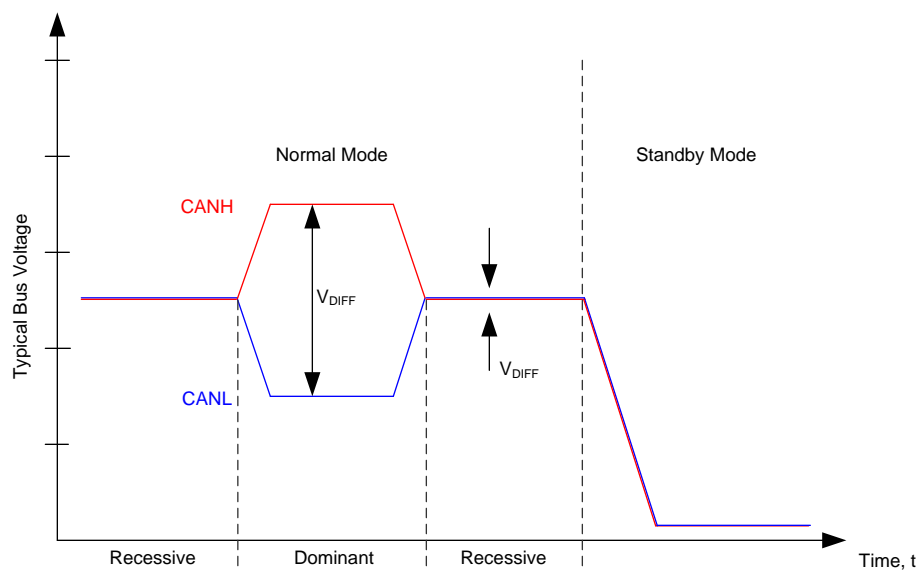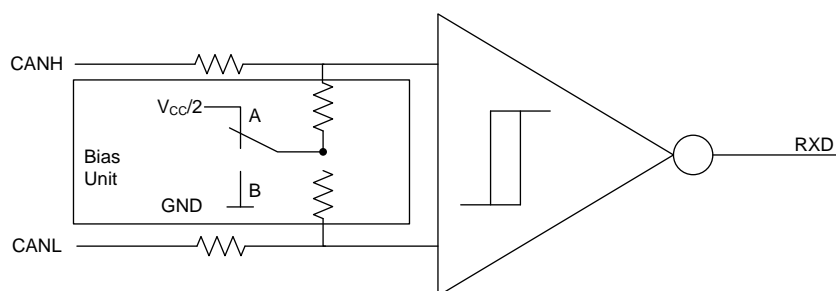

图 3. Bus States

A.   Normal Mode
B.   Standby Mode (Low Power)

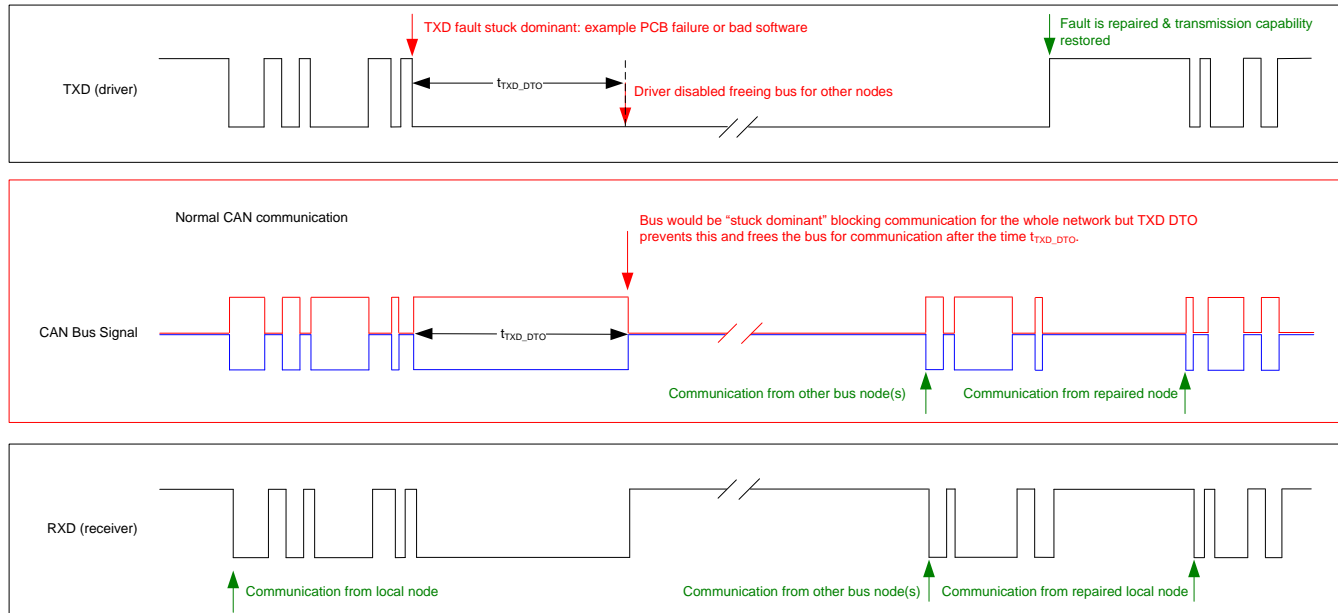图 4. Simplified Recessive Common Mode Bias Unit and Receiver

ADVANCE INFORMATION

Parameter Measurement Information (接下页)

图 5. **Example Timing Diagram for TXD Dominant Timeout**
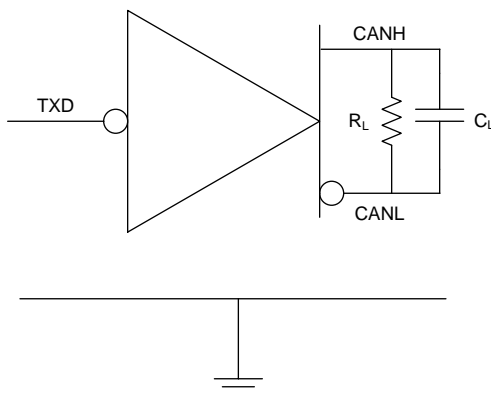
图 6. **I_CC Test Circuit**

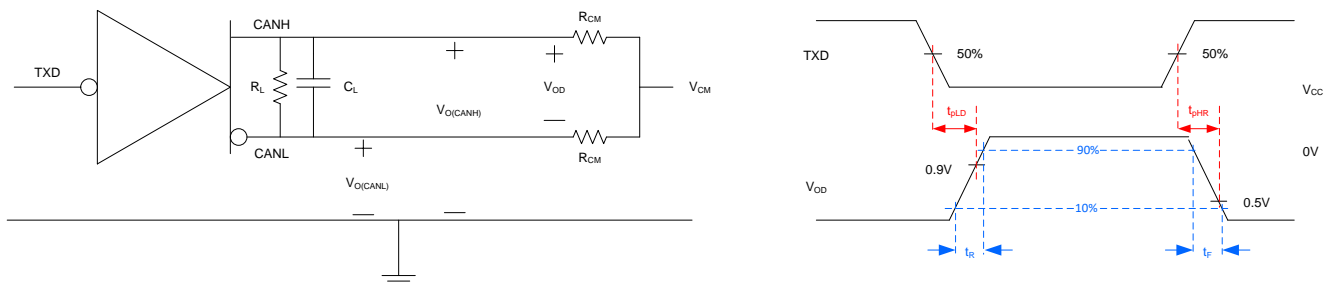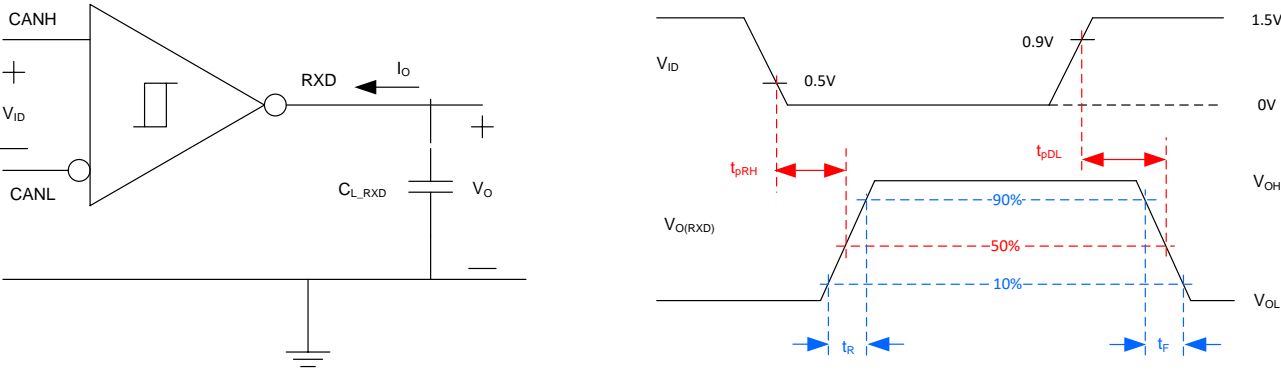图 7. **Driver Test Circuit and Measurement**

ADVANCE INFORMATION

Parameter Measurement Information (接下页)

图 8. Receiver Test Circuit and Measurement

表 1. Receiver Differential Input Voltage Threshold Test (See 图 8)

Input			Output
V_{CANH}	V_{CANL}	$|V_{ID}|$	RXD
-11.5 V	-12.5 V	1000 mV	L
12.5 V	11.5 V	1000 mV	L
-8.55 V	-9.45 V	900 mV	L
9.45 V	8.55 V	900 mV	L
-8.25 V	-9.25 V	500 mV	H
9.25 V	8.25 V	500 mV	H
-11.8 V	-12.2 V	400 mV	H
12.2 V	11.8 V	400 mV	H
Open	Open	X	H

In the Output column: rows with $|V_{ID}|$ of 1000 mV and 900 mV (L) correspond to V_{OL}; rows with 500 mV and 400 mV and Open (H) correspond to V_{OH}.
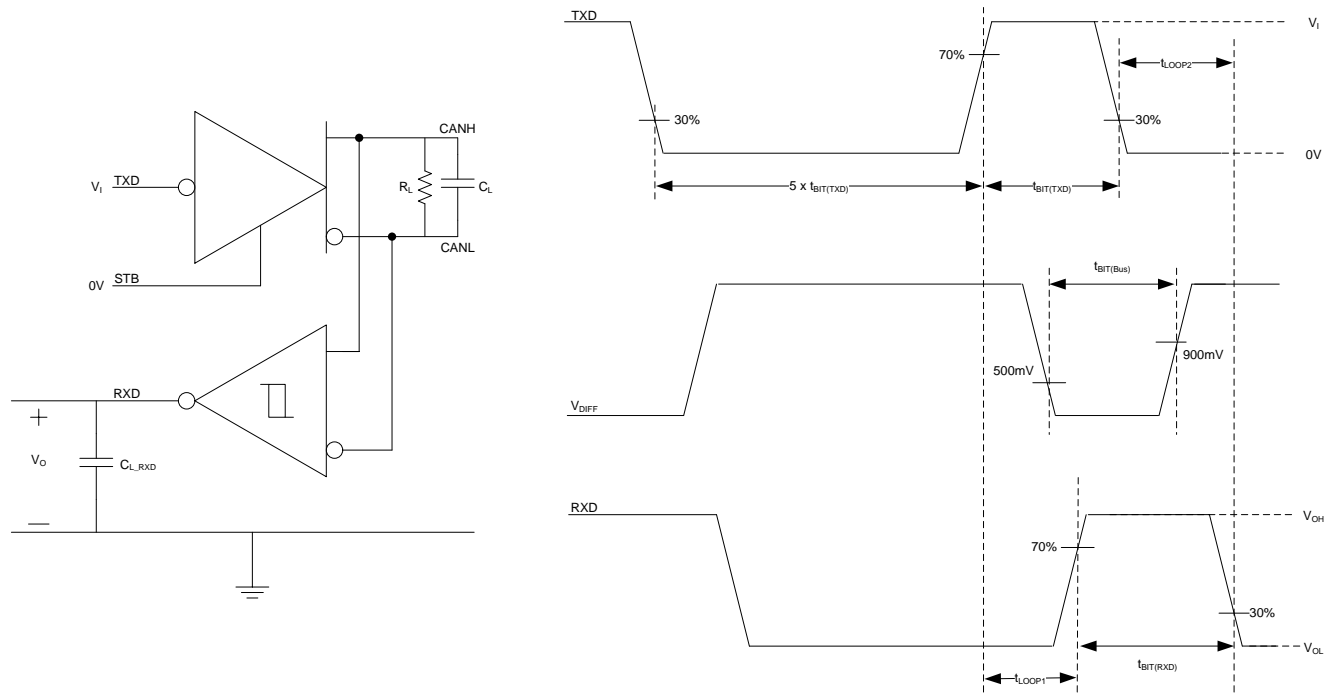
图 9. Transmitter and Receiver Timing Test Circuit and Measurement
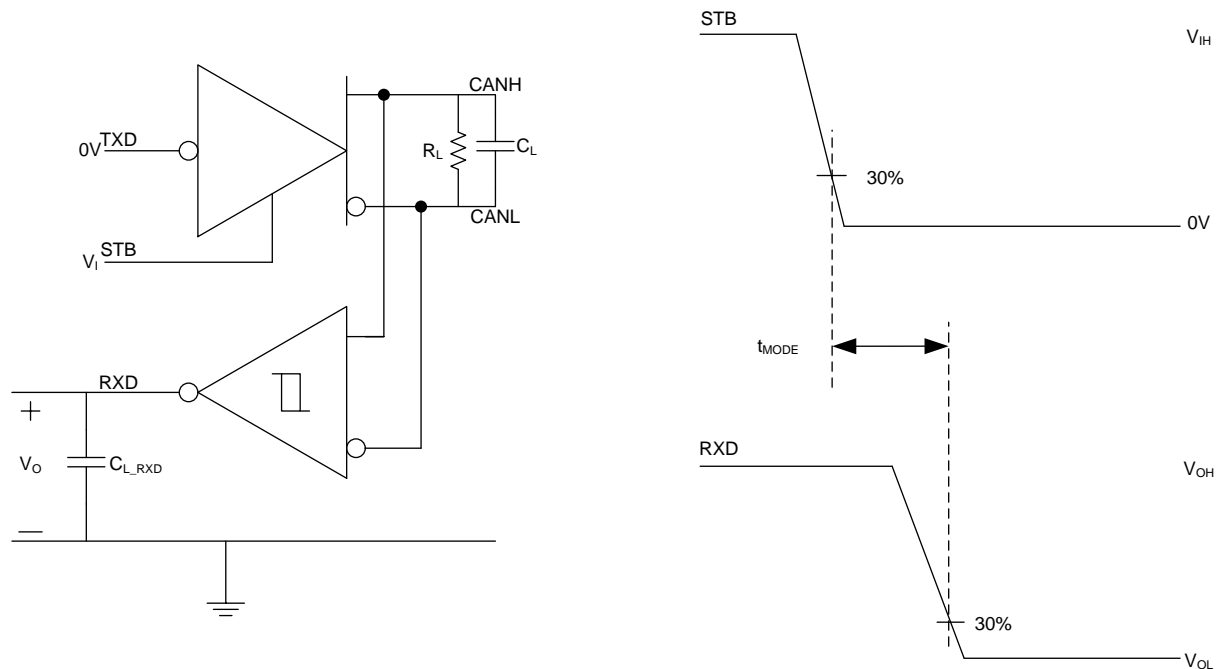
图 10. TCAN1046V-Q1 t_{MODE} Test Circuit and Measurement

ADVANCE INFORMATION
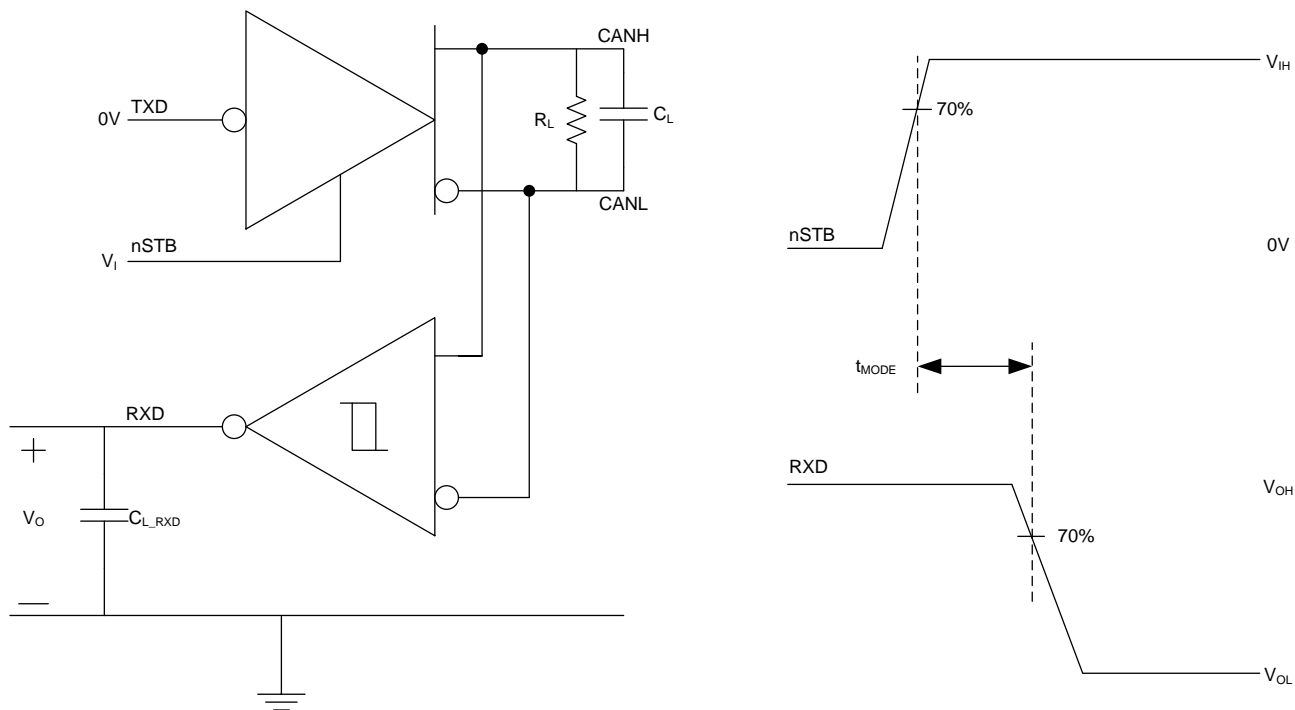
ADVANCE INFORMATION

图 11. TCAN1048V-Q1 t_{MODE} Test Circuit and Measurement
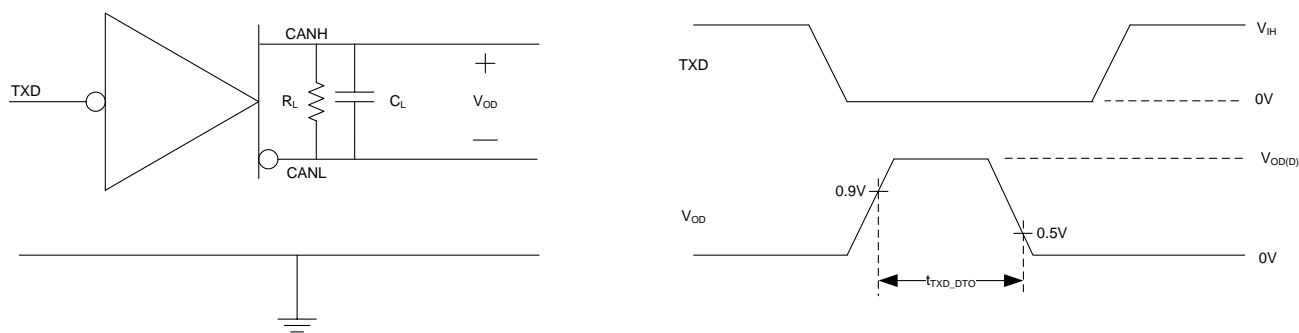
图 12. TXD Dominant Timeout Test Circuit and Measurement
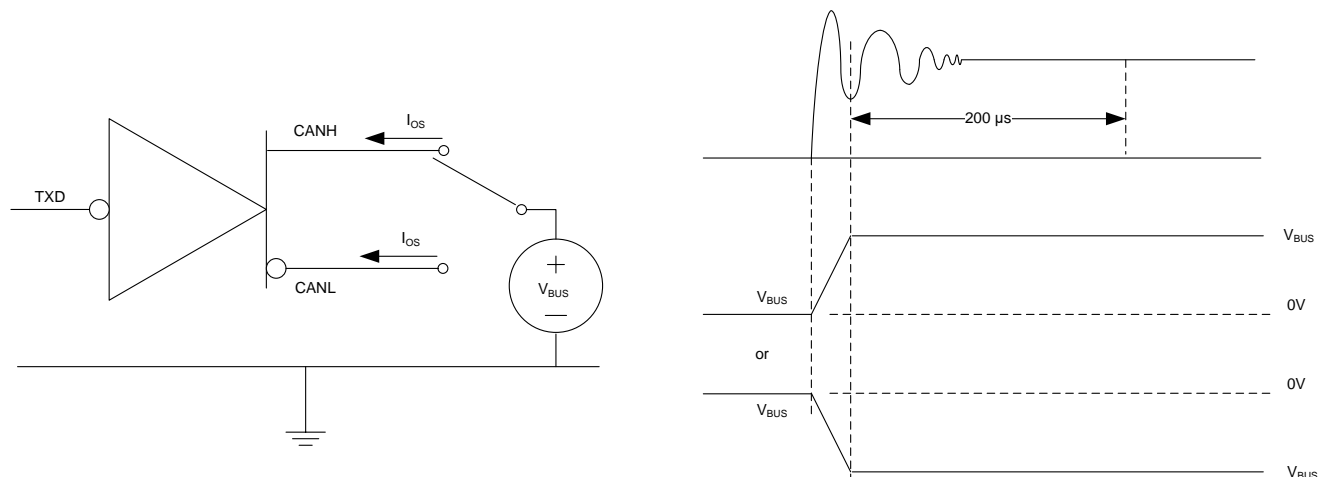
图 **13. Driver Short-Circuit Current Test and Measurement**

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TCAN1046V-Q1 and TCAN1048V-Q1 devices meet or exceed the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. The devices have been certified to the requirements of ISO 11898-2:2016 and ISO 11898-5:2007 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The dual CAN TCAN1046V-Q1 and TCAN1048V-Q1 devices provide differential transmit capability to the CAN bus and differential receive capability from the CAN bus. The devices include many protection features providing device and CAN bus robustness. The TCAN1046V-Q1 and TCAN1048V-Q1 supports CAN and CAN FD (Flexible Data Rate) up to 5 Mbps.
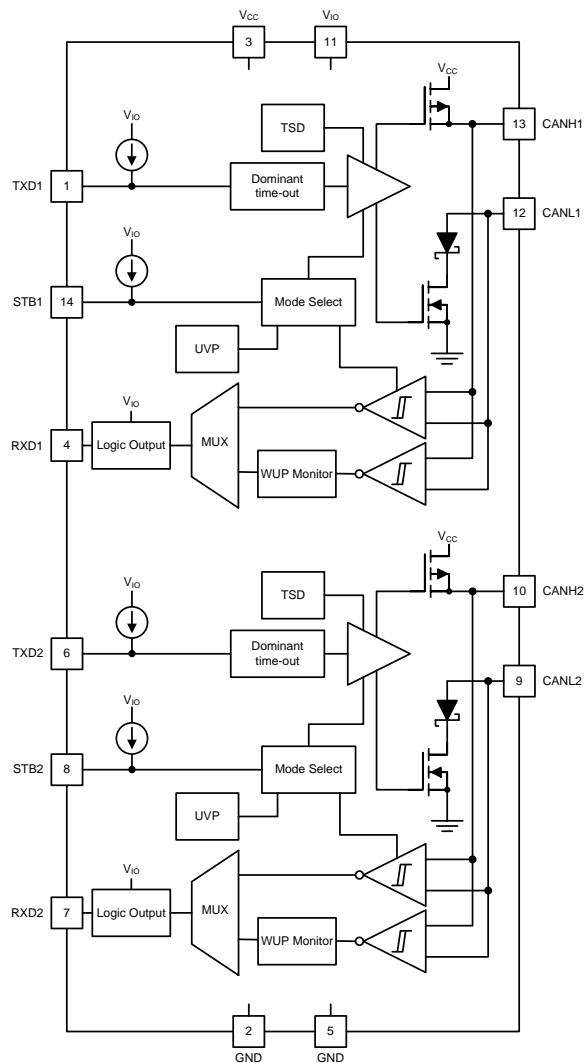
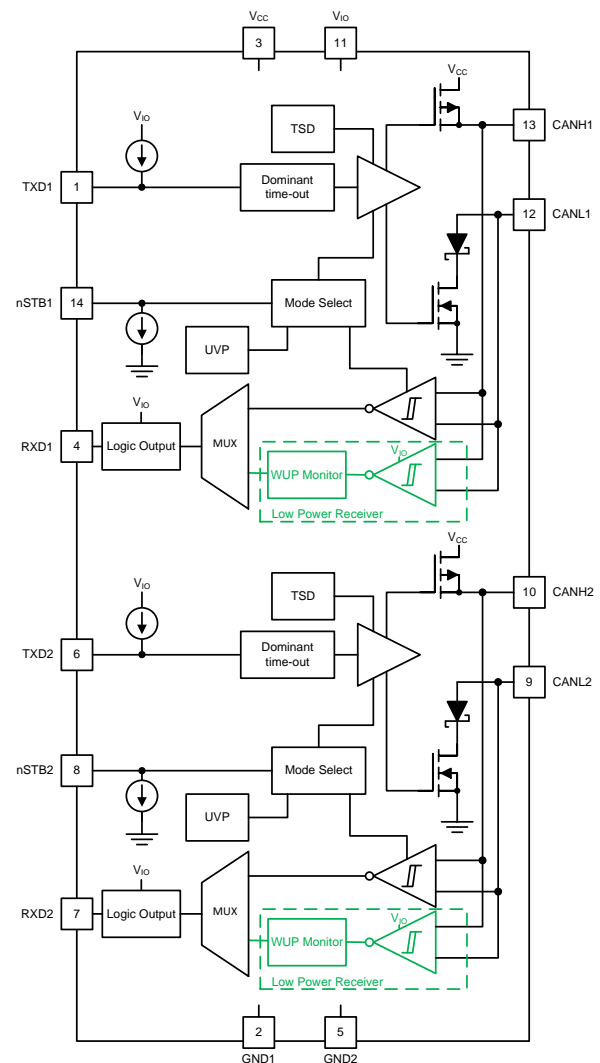### 8.1.1 Functional Block Diagrams

图 14. **TCAN1046V-Q1 Block Diagram**

图 15. **TCAN1048V-Q1 Block Diagram**

8.2 Feature Description

8.2.1 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See 图 3 and 图 4.

A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the TXD and RXD terminals. A recessive bus state is when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors R_{IN} of the receiver, corresponding to a logic high on the TXD and RXD terminals.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, in this case the differential voltage of the bus will be greater than the differential voltage of a single driver.

The host controller of the CAN node uses the TXD terminal to drive the bus and will receive data from the bus on the RXD terminal. Using the TCAN1046V-Q1 and TCAN1048V-Q1 devices allows for the I/O voltage to be level shifted between 1.8 V to 5 V for the host controller via the V_{IO} pin.

The TCAN1046V-Q1 and TCAN1048V-Q1 transceivers possess a low power standby (STB or nSTB) mode which enables a third bus state where the bus terminals are weakly biased to ground via the high resistance internal resistors of the receiver. See 图 3 and 图 4.

8.2.2 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout constant of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on TXD terminal, thus clearing the dominant time out. The receiver remains active and the RXD terminal will reflect the activity on the CAN bus and the bus terminals will be biased to recessive level during a TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using 公式 1

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \tag{1}$$

8.2.3 CAN Bus Short Circuit Current Limiting

The TCAN1046V-Q1 and TCAN1048V-Q1 devices have several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting in dominant and recessive states. The devices have TXD dominant timeout which prevents permanently having the higher short circuit current of dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states, thus the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings the average short circuit current should be used. The percentage dominant is limited by the TXD dominant timeout and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and interframe space. These ensure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using 公式 2.

$$I_{OS(AVG)} = \%\text{Transmit} \times [(\%\text{REC\_Bits} \times I_{OS(SS)\_REC}) + (\%\text{DOM\_Bits} \times I_{OS(SS)\_DOM})] + [\%\text{Receive} \times I_{OS(SS)\_REC}] \tag{2}$$

ADVANCE INFORMATION

Feature Description (接下页)

Where:
- $IO_{S(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current

The short circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance, other network components, and the power supply used to generate V_{CC}.

8.2.4 Thermal Shutdown

If the junction temperature of the devices exceed the thermal shutdown threshold the device turns off the CAN driver circuitry thus blocking the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below the thermal shutdown temperature of the device. The CAN bus terminals will be biased to recessive level during a thermal shutdown fault and the receiver to RXD path will remain operational. If the fault condition that caused the thermal shutdown is still present, the temperature may rise again and the device will enter thermal shutdown again. Prolonged operation with thermal shutdown conditions may affect device reliability. The thermal shutdown circuit includes hysteresis to avoid oscillation of the driver output.

8.2.5 Under Voltage Lockout (UVLO) and Unpowered Device

The V_{CC} supply terminal has under voltage detection circuitry which places the device in a protected mode if an under voltage fault occurs. This protects the bus during an under voltage event on the V_{CC} terminal. If V_{CC} enters an under voltage fault condition, the RXD terminal is tri-stated (high impedance) and the device does not pass any signals from the bus, including any remote wake-up events (WUP). If the device is in normal mode and V_{CC} supply is lost, or has a brown out that triggers the UVLO, the device will transition to a protected mode.

The device is designed to be an "ideal passive" or "no load" to the CAN bus if the device is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered, so they will not load the bus. This is critical if some nodes of the network will be unpowered while the rest of the of network remains operational. Logic terminals also have low leakage currents when the device is unpowered so they will not load other circuits which may remain powered.

Once an under voltage condition is cleared and the V_{CC} supply has returned to a valid level the device will typically need t_{MODE} to transition to normal operation. The host controller should not attempt to send or receive messages until this transition time has expired. If standby mode is enabled and V_{CC} has an under voltage event, the device will go into a protected mode which disables the wake-up receiver and places the RXD output into a high impedance state.

ADVANCE INFORMATION

Feature Description (接下页)

表 2. TCAN1046V-Q1 and TCAN1048V-Q1 Under Voltage Protection

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors Bus
< UV_{VCC}	> UV_{VIO}	Protected	High Impedance	High (Recessive)
> UV_{VCC}	< UV_{VIO}	Protected	Recessive	High Impedance
< UV_{VCC}	< UV_{VIO}	Protected	High Impedance	High Impedance

8.3 Device Functional Modes

8.3.1 Operating Modes

The TCAN1046V-Q1 and TCAN1048V-Q1 has two main operating modes; normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB or nSTB pins on the TCAN1046V-Q1 and TCAN1048V-Q1 device respectively.

表 3. Operating Modes

STB	nSTB	Device Mode	Driver	Receiver	RXD Terminal
High	Low	Low current standby mode with bus wake-up	Disabled	Low power receiver and bus monitor enable	High (Recessive) until wake-up, then filtered mirrors of bus state. See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode
Low	High	Normal Mode	Enabled	Enabled	Mirrors bus state

8.3.2 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD1 and TXD2 inputs to a differential output on the CANH1, CANL1 and CANH2, CANL2 bus pins. The receiver is translating the differential signal from CANH1, CANL1 and CANH2, CANL2 to a digital output on the RXD1 and RXD2 outputs.

8.3.3 Standby Mode

This is the low power mode of the device. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via either of the CAN buses. A wake-up request will be output to RXD1 or RXD2 depending on the channel which received the WUP as shown in 图 16. The local CAN protocol controller should monitor RXD1 and RXD2 for transitions (high to low) and reactivate the device to normal mode by pulling the STB terminal low or the nSTB terminal high. The CAN bus terminals are weakly pulled to GND during this mode, see 图 4.

8.3.4 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN1046V-Q1 and TCAN1048V-Q1 offer a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The devices use the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2016 standard to qualify bus activity. Once a valid WUP has been received, the wake request will be indicated to the controller by a falling edge and low corresponding to a filtered dominant on the RXD1/RXD2 output of the TCAN1046V-Q1 and TCAN1048V-Q1 terminal.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD1/RXD2 output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP and thus no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ will always be detected as part of a WUP and thus a wake request will always be generated. See 图 16 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any CAN or CAN FD message to initiate a wake-up request.

The ISO 11898-2:2016 standard has defined times for a short and long wake up filter time. The t_{WK_FILTER} timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500 kbps, or two back to back bit times at 1 Mbps triggers the filter in either bus state.

For an additional layer of robustness and to prevent false wake ups, the devices implement a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \le t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the part remains in its current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See 图 16 for the timing diagram of the wake up pattern with wake timeout feature.

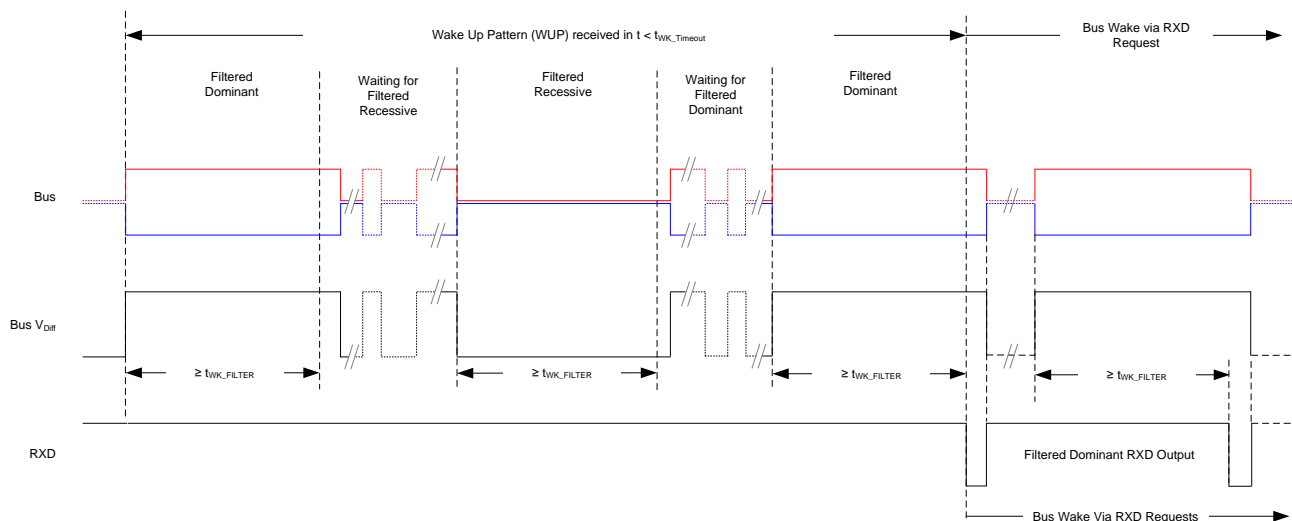图 16. **Wake-Up Pattern (WUP) with $t_{WK\_TIMEOUT}$**

8.3.5 Driver and Receiver Function

The digital logic input and output levels for the TCAN1046V-Q1 and TCAN1048V-Q1 are CMOS levels with respect to V_{IO} for compatibility with protocol controllers having 1.8 V, 3.3 V, or 5 V logic or I/O levels.

表 4. **Driver Function Table**

Device Mode	TXD INPUT[1]	BUS OUTPUTS[2]		DRIVEN BUS STATE[3]
		CANH	**CANL**	
Normal	L	H	L	Dominant
	H or Open	Z	Z	Biased recessive
Standby	X	Z	Z	Weak pull down to ground

(1) H = high level, L = low level, X = irrelevant
(2) H = high level, L = low level, Z = high Z receiver bias
(3) For bus state and bias see 图 3 and 图 4

表 5. Receiver Function Table Normal and Standby Mode

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD TERMINAL[1]
Normal	$V_{ID} \geq 0.9$ V	Dominant	L
	0.5 V $< V_{ID} < 0.9$ V	Undefined	Undefined
	$V_{ID} \leq 0.5$ V	Recessive	H
Standby	$V_{ID} \geq 1.15$ V	Dominant	H
	0.4 V $< V_{ID} < 1.15$ V	Undefined	L if a remote wake event occurred
	$V_{ID} \leq 0.4$ V	Recessive	See Figure
Any	Open ($V_{ID} \approx 0$ V)	Open	H

(1) H = high level, L = low level

8.3.6 Floating Terminals

The TCAN1046V-Q1 and TCAN1048V-Q1 has internal pull-ups or pull-downs on critical terminals to place the device into known states if the terminal floats. See 表 6: Terminal Bias for details on terminal bias conditions.

表 6. Terminal Bias

TERMINAL	PULL UP or PULL DOWN	COMMENT
TXD	Pull-up	Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering
STB	Pull-up	Weakly biases STB terminal towards low power standby mode to prevent excessive system power; TCAN1046V-Q1 only
nSTB	Pull-down	Weakly biases nSTB terminal towards low power standby mode to prevent excessive system power; TCAN1048V-Q1 only

The internal bias should not be relied upon as only termination, especially in noisy environments but should be considered a failsafe protection. Special care needs to be taken when the device is used with MCUs utilizing open drain outputs. TXD is weakly internally pulled up, the pull-up strength and CAN bit timing require special consideration when this device is used with an open drain TXD output on the controller CAN controller. An adequate external pull up resistor must be used to ensure that the TXD output of the CAN controller maintains adequate bit timing input to the CAN transceiver.

ADVANCE INFORMATION

9   Application and Implementation

> 注
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1   Application Information

9.2   Typical Application

The TCAN1046V-Q1 and TCAN1048V-Q1 transceivers are typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. 图 17 shows a typical application configuration for 5 V controller applications. The bus termination is shown for illustrative purposes.
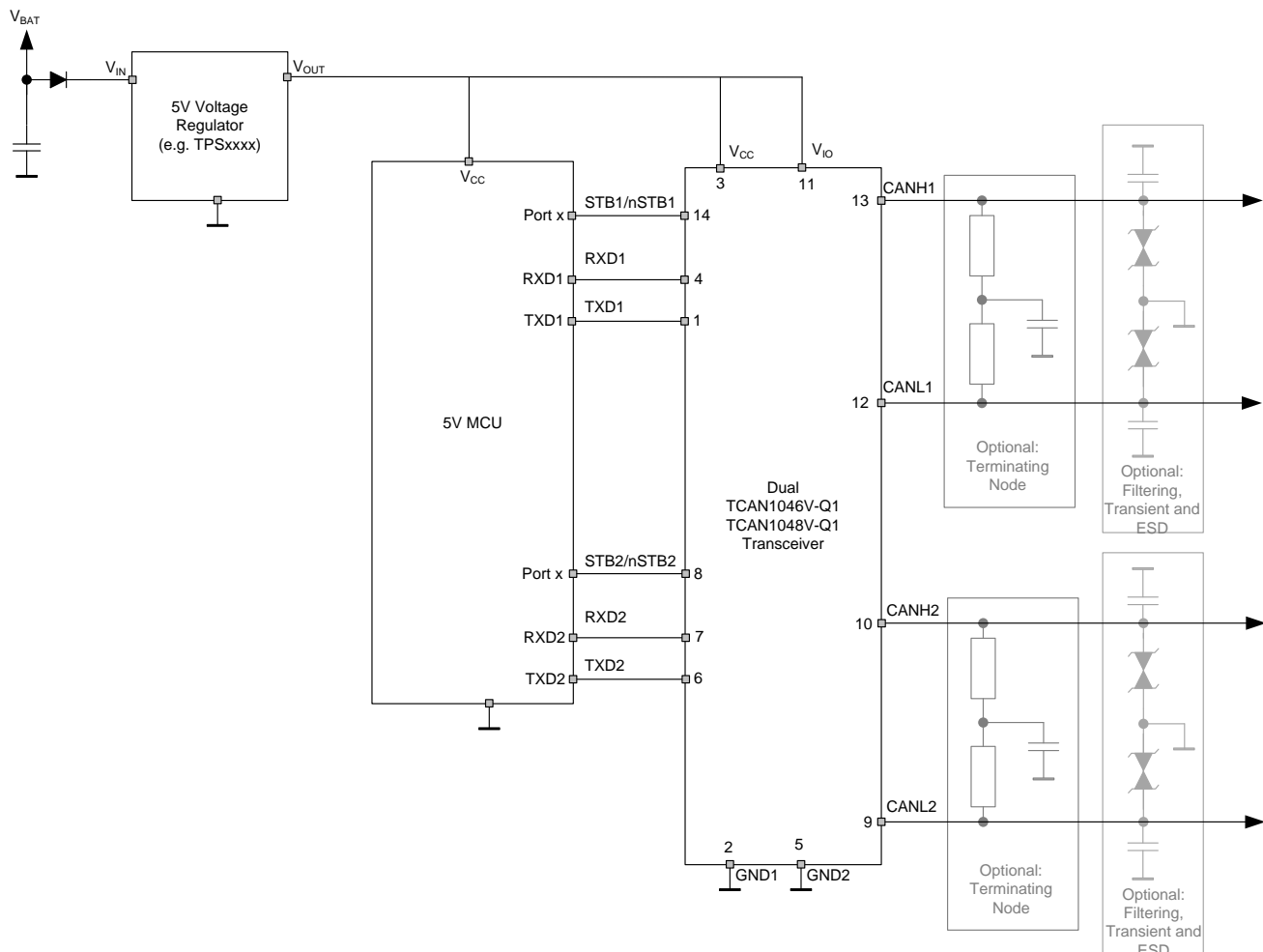
图 17.   Typical TCAN1046V-Q1/TCAN1048V-Q1 Transceiver Application Using 5 V IO Connections

Typical Application (接下页)

9.2.1 Design Requirements

9.2.1.1 CAN Termination

The ISO 11898-2:2016 standard specifies the interconnection to be a single twisted pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be in a node but is generally not recommended, especially if the node may be removed from the bus. Termination must be carefully placed so that it is not removed from the bus. System level CAN implementations such as CANopen allow for different termination and cabling concepts, for example, to add cable length.

Termination may be a single 120-Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired then split termination may be used, see 图 18. Split termination improves the electromagnetic emissions behavior of the network by reducing fluctuations in the bus.
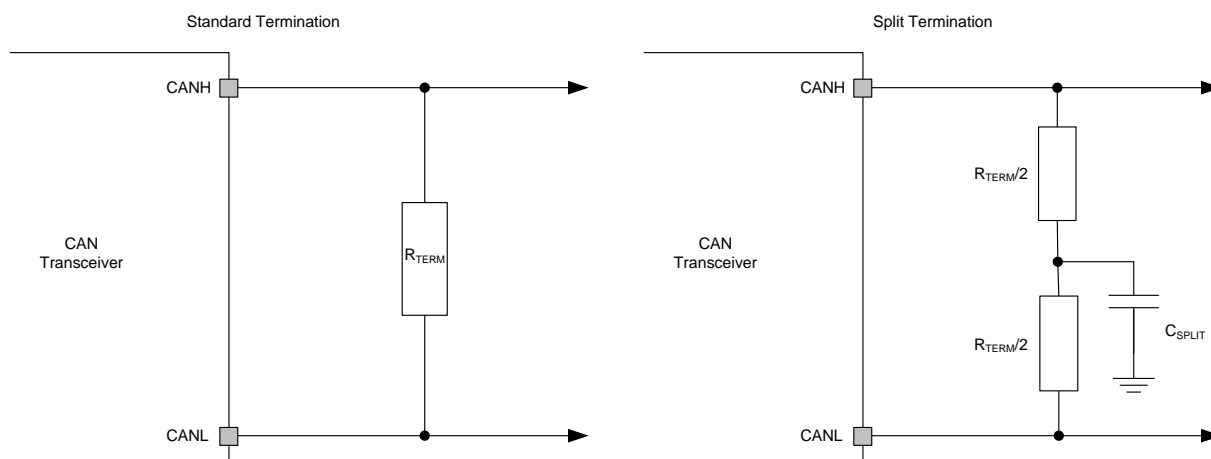

图 18. **CAN Bus Termination Concepts**

ADVANCE INFORMATION

Typical Application (接下页)

9.2.2 Detailed Design Procedures

9.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application can have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1046V-Q1 and TCAN1048V-Q1 family.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from 50 Ω to 65 Ω where the differential output must be greater than 1.5 V. The TCAN1046V-Q1 and TCAN1048V-Q1 family is specified to meet the 1.5-V requirement down to 50 Ω and is specified to meet 1.4-V differential output at 45Ω bus load. The differential input resistance of the TCAN1046V-Q1 and TCAN1048V-Q1 is a minimum of 40 kΩ. If 100 TCAN1046V-Q1 or TCAN1048V-Q1 transceivers are in parallel on a bus, this is equivalent to a 400-Ω differential load in parallel with the nominal 60 Ω bus termination which gives a total bus load of approximately 52 Ω. Therefore, the TCAN1046V-Q1 and TCAN1048V-Q1 family theoretically supports over 100 transceivers on a single bus segment. However for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is much lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design to ensure robust network operation.
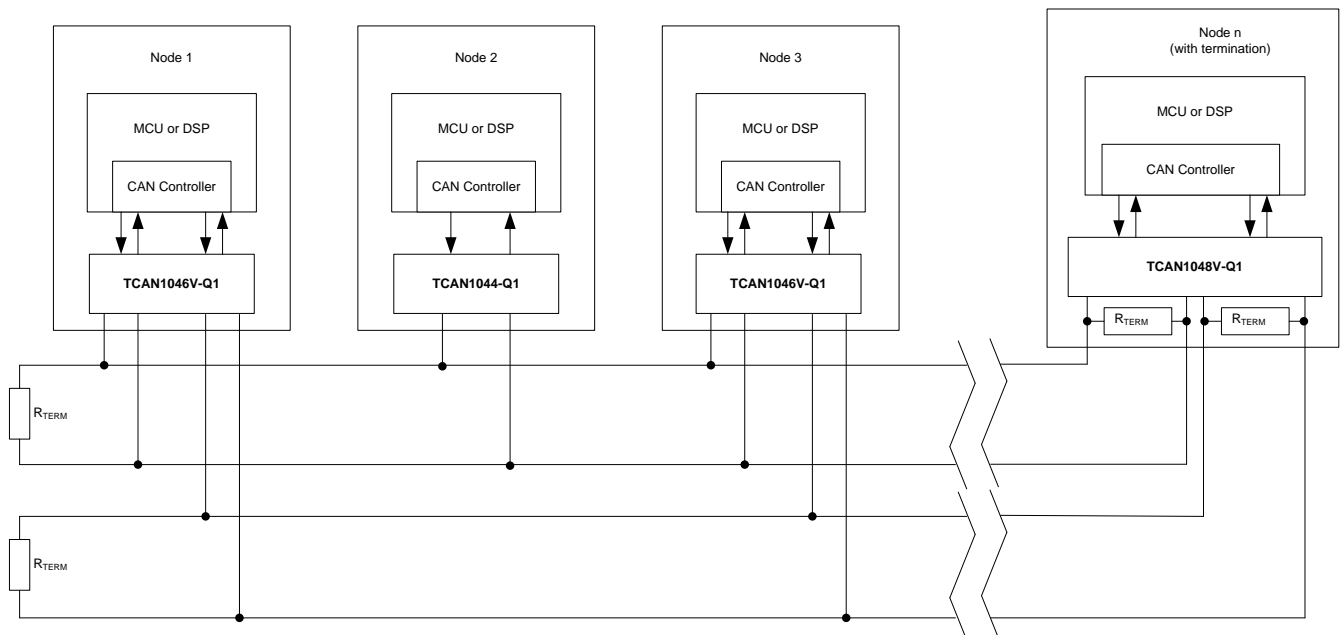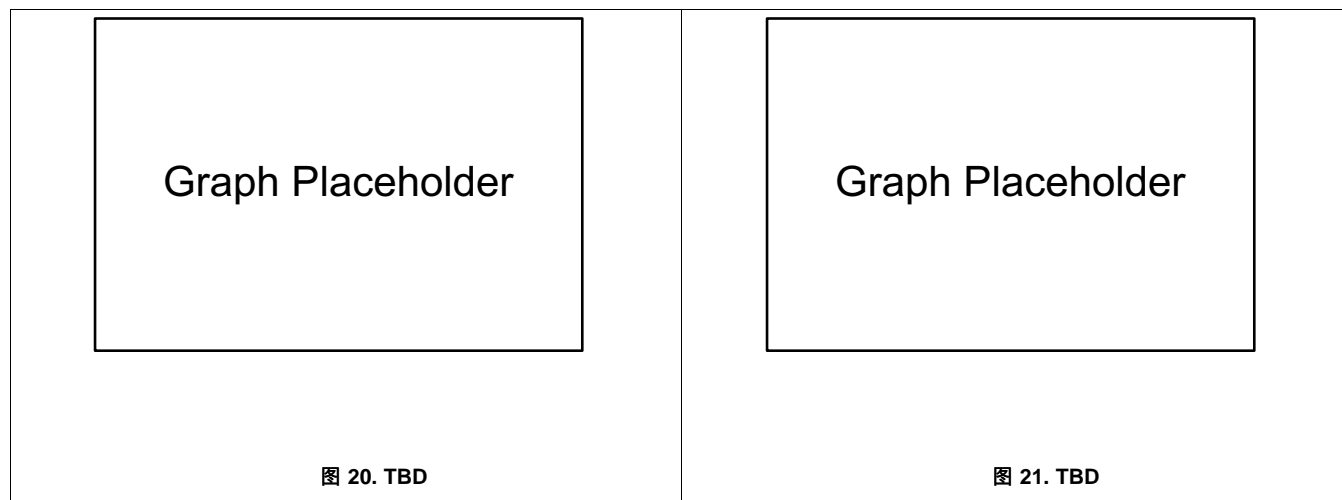
ADVANCE INFORMATION

图 19. TCAN1046V-Q1/TCAN1048V-Q1 Typical CAN Bus

Typical Application (接下页)

9.2.3 Application Curves

<table>
<tr>
<td>

Graph Placeholder

</td>
<td>

Graph Placeholder

</td>
</tr>
<tr>
<td align="center">图 20. TBD</td>
<td align="center">图 21. TBD</td>
</tr>
</table>

9.3 System Examples

The TCAN1046V-Q1 and TCAN1048V-Q1 CAN transceivers are typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. Typical application configuration for 1.8 V to 3.3 V controller applications are shown in 图 22. The bus termination is shown for illustrative purposes.

ADVANCE INFORMATION

System Examples (接下页)
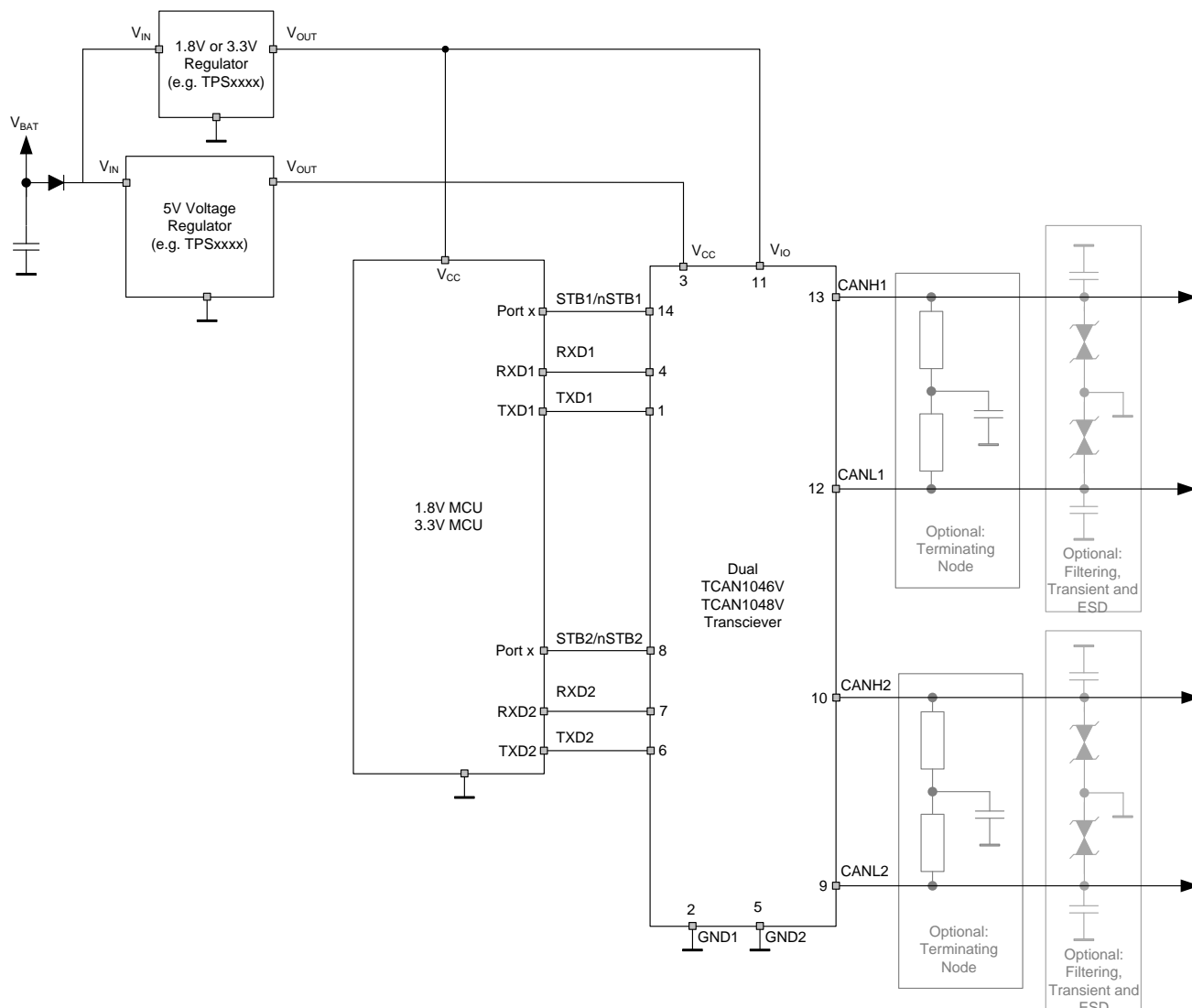
图 22. **TCAN1046V-Q1/TCAN1048V-Q1 Transceiver Application Using 1.8V or 3.3 V IO Connections**

ADVANCE INFORMATION

10 Power Supply Recommendations

The TCAN1046V-Q1 and TCAN1048V-Q1 devices are designed to operate with a main V_{CC} input voltage supply range between 4.5 V and 5.5 V. The devices have an I/O level shifting supply input, V_{IO}, designed for a range between 1.8 V and 5.5 V. Both supply inputs must be well regulated. A decoupling capacitance, typically 100 nF, should be placed near the CAN transceiver's main V_{CC} and V_{IO} supply terminals in addition to bypass capacitors.

11 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

11.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1and J2, to prevent transients, ESD and noise from propagating onto the board. In this layout example for protection transient voltage suppression (TVS) devices, D1 and D2, have been used. The production solution can be either bi-directional TVS diodes or varistors with ratings matching the application requirements. This example also shows optional bus filter capacitors C6, C8, C9, and C11.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use V_{CC} and ground planes to provide low inductance. Note that high frequency current follows the path of least impedance and not the path of least resistance.
- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- This layout example shows how split termination could be implemented on the CAN node. This is where the termination is split into two resistors, R8, R9, R10, and R11, with the center or split tap of the termination connected to ground via capacitors C7 and C10. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to ensure the terminating node is not removed from the bus thus also removing the termination. See CAN Termination, CAN Bus Short Circuit Current Limiting and 公式 2 for information on termination concepts and power ratings needed for the termination resistor(s).
- To limit current of digital lines serial resistors may be used. Examples are R2, R3, R5, R6, R7, R10 and R12.
- Terminal 1 and terminal 6 are shown for the TXD1 and TXD2 inputs of the device with R1 and R4 as optional pull-up resistors. If an open drain host controller is used this is mandatory to ensure the bit timing into the device is met.
- Terminal 8 and 14 are shown assuming the mode terminals STB or nSTB, are used. If the device is only used in normal mode then only a pull-down resistor or pull-up resistor is needed. The TCAN1046V-Q1 will require a pull-down resistor on pins 8 and 14 and the TCAN1048V-Q1 will require a pull-up resistor on pins 8 and 14.

ADVANCE INFORMATION
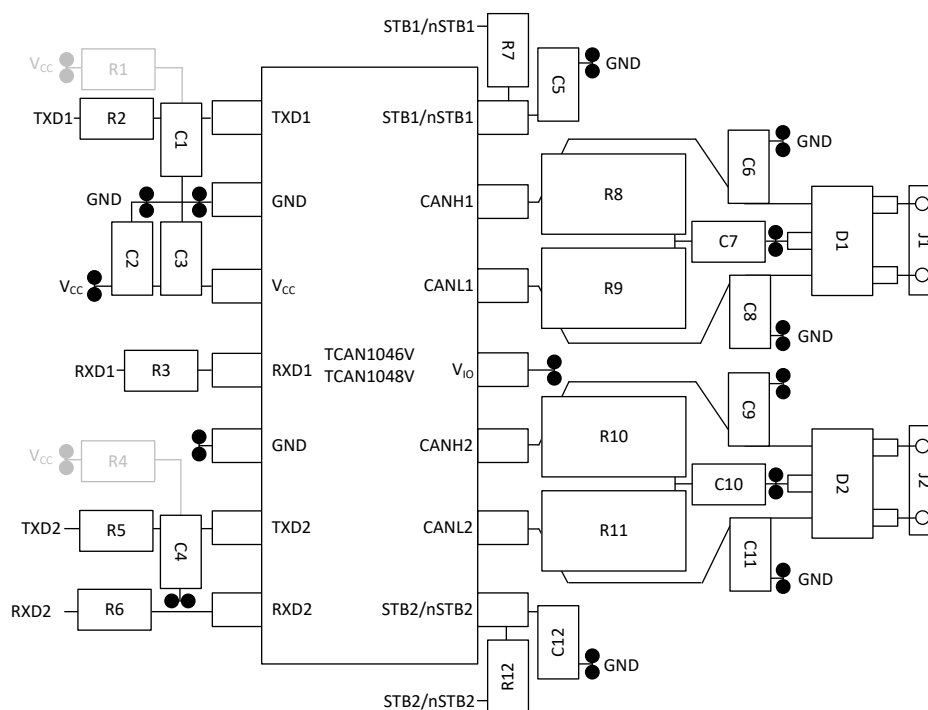
11.2 Layout Example

图 23. **TCAN1046V-Q1 and TCAN1048V-Q1 Example Layout**

ADVANCE INFORMATION

12 器件和文档支持

12.1 文档支持

12.1.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 7. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TCAN1046V-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TCAN1048V-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

TI E2E™ 在线社区 *TI 的工程师对工程师 (E2E) 社区。*此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

　　这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

重要声明和免责声明

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN1046VDMTRQ1	ACTIVE	VSON	DMT	14	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	1046V	Samples
TCAN1048VDRQ1	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
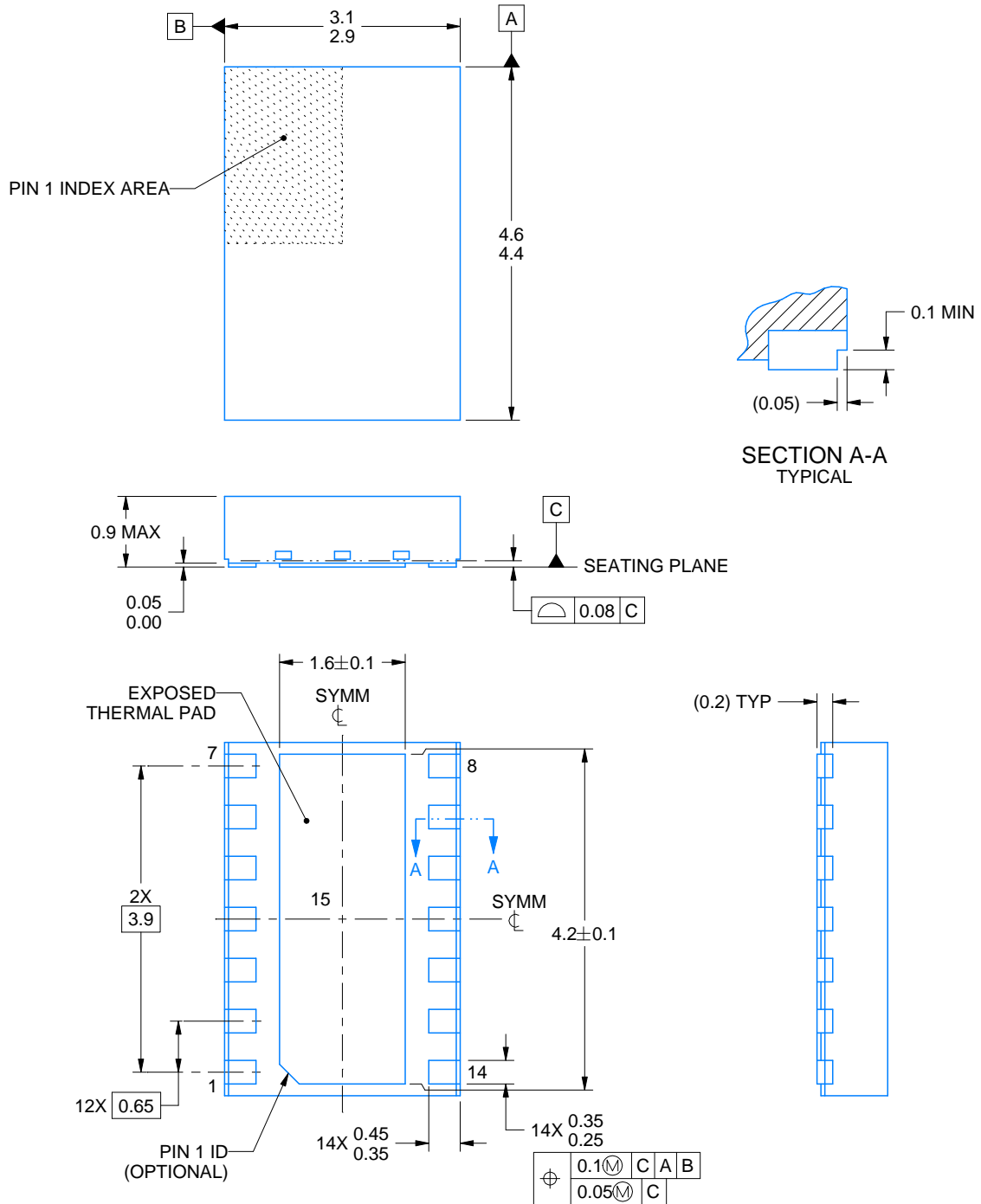
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DMT0014A

PACKAGE OUTLINE
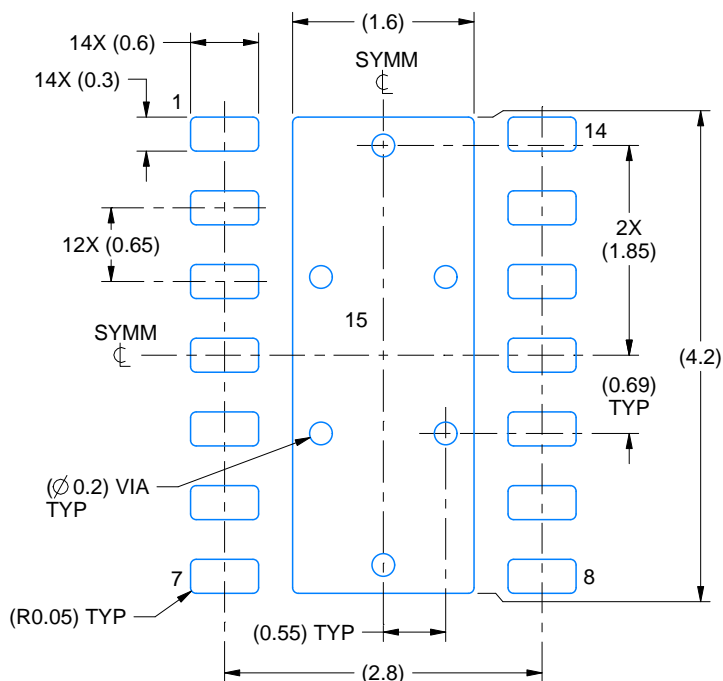
VSON - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

3.1
2.9

PIN 1 INDEX AREA

4.6
4.4

0.1 MIN

(0.05)

SECTION A-A
TYPICAL

0.9 MAX

SEATING PLANE

0.05
0.00

0.08 C

1.6±0.1

SYMM

EXPOSED
THERMAL PAD

(0.2) TYP

7

8

2X 3.9

15

SYMM

4.2±0.1

12X 0.65

1

14

PIN 1 ID
(OPTIONAL)

14X 0.45
0.35

14X 0.35
0.25

0.1 Ⓜ C A B
0.05 Ⓜ C

4223033/B   10/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
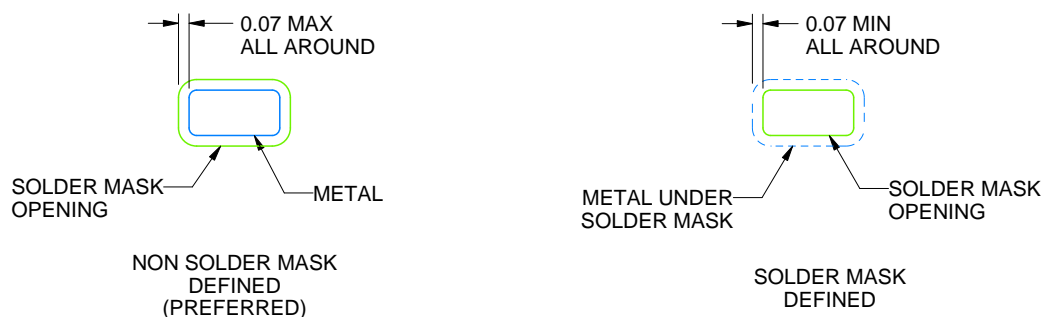
TEXAS
INSTRUMENTS
www.ti.com

14X (0.6)

14X (0.3)

1

(1.6)

SYMM

14

12X (0.65)

2X
(1.85)

SYMM

15

(4.2)

(0.69)
TYP

(⌀ 0.2) VIA
TYP

7

8

(R0.05) TYP

(0.55) TYP

(2.8)

LAND PATTERN EXAMPLE
SCALE:15X

0.07 MAX
ALL AROUND

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4223033/B   10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
   number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown
   on this view. It is recommended that vias under paste be filled, plugged or tented.

DMT0014A

VSON - 0.9 mm max height

14X (0.6)

1

(1.47)

15

14

14X (0.3)

(1.18)

12X (0.65)

SYMM
℄

(R0.05) TYP

(1.38)

METAL
TYP

7

8

SYMM
℄

(2.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4223033/B   10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明