设计指南：*TIDA-010037*
使用独立 *ADC* 的高精度分相 *CT* 电量计参考设计

说明

此参考设计使用高性能、多通道模数转换器 (ADC) 实现 0.1 级分相电能测量。该独立 ADC 对电流互感器 (CT) 在 8kHz 时的输出进行取样，以测量主交流电源各分支的电流和电压。该参考设计在宽输入电流范围下（0.05–100 安培）能达到很高的精度，在必要时还支持高采样频率，以实现独立谐波分析等高级电能质量 功能 。与集成 SoC 和应用特定的专用产品相比，通过使用独立 ADC 对 CT 输出进行采样，可以让设计人员更加灵活地选择计量微控制器。该参考设计使用 SimpleLink™ ARM® Cortex®-M4 主机微控制器来计算电能计量参数。

资源

TIDA-010037	设计文件夹
ADS131M04	产品文件夹
MSP432P4111	产品文件夹
TPS3840	产品文件夹
TPS25921I	产品文件夹
THVD1500	产品文件夹
ISO7731B	产品文件夹
TRS3232E	产品文件夹

TI E2E™ Community

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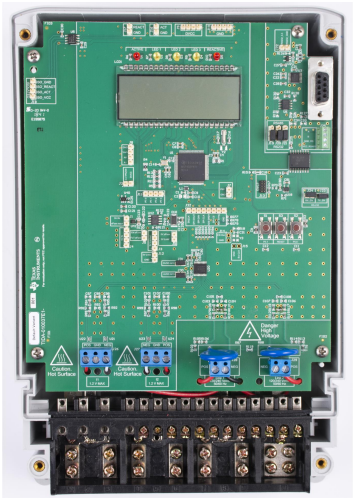
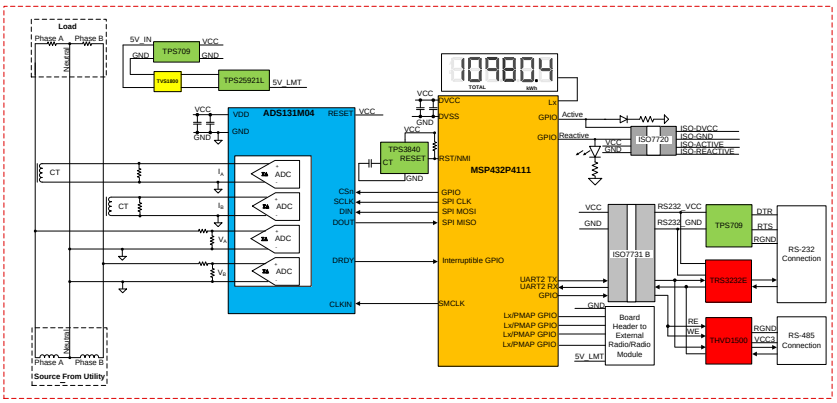
特性

- 电量计分相计量，符合 10000:1 输入范围的 ANSI C12.20 0.1 类有功电能精度要求
- 有功和无功电能和功率、均方根 (RMS) 电流和电压、功率因数以及线路频率计算
- 具有 5kV$_{RMS}$ 隔离的隔离式 RS-232 和 RS-485
- 具有电流限制及过压和欠压保护的通信模块扩展
- 在 50mA 至 100A 输入范围内进行了测试

应用

- 电表
- 电能质量监测仪
- 电能质量分析仪





1 System Description

1.1 End Equipment

1.1.1 Electricity Meter

An increase in utility providers' desired functionality for an electricity meter has driven a need for more features from electricity meters. Advanced features, such as harmonic analysis, are increasingly being required from meters. To meet these requirements, the processing and accuracy requirements often also have to evolve. As an example, adding harmonic analysis capabilities to an electricity meter may require an increase in the sample rate of the meter to capture the desired frequency range. The increase in sample frequency many times has to be done without compromising on accuracy or even while simultaneously increasing accuracy. The high sample rate, in turn, also requires more processing.

As the accuracy and amount of processing expected from electricity meters increases, it becomes more difficult to find a metrology SoC that fulfills both the processing and accuracy requirements of an electricity meter. To address this limitation, a standalone ADC can be used with a host microcontroller (MCU) to simultaneously overcome the processing and accuracy limitations of electricity meter SoCs. Using an accurate standalone ADC typically has the following advantages:

- It enables meeting the most stringent of accuracy requirements
- It enables meeting minimum sample rate requirements(without compromising on accuracy) that may not be obtainable with applications specific products or metrology SoCs
- It enables flexibility in selecting the host microcontroller since you are not limited to selecting host microcontrollers that have accurate ADCs. The host microcontroller can be selected solely based on application requirements, such as processing capability, minimum RAM and Flash storage for logging energy usage, and microcontroller security features for ensuring meter data security.

To properly sense energy consumption, voltage and current sensors translate mains voltage and current to a voltage range that an ADC can sense. To sense the energy consumption when a split-phase distribution system is used, it is necessary for the current sensors to be isolated so they can properly sense the current drawn from the two different lines without damaging the ADC. As a result, current transformers, which inherently have isolation, have historically been used for the current sensors for split-phase, two-phase, and three-phase electricity meters.

In this reference design, Class 0.1 split-phase CT-based energy measurement is implemented by using a standalone ADC device. The standalone ADC senses the Mains voltage and current. When there are new ADC samples available, the host MCU communicates to the standalone ADC via SPI to get the new samples. The host microcontroller uses the new ADC samples from the standalone ADC to calculate metrology parameters. In addition to calculating the metrology parameters, the host MCU also drives the liquid crystal display (LCD) of the board and communicates to a PC GUI through either the isolated RS-232 circuitry or isolated RS-485 circuitry on the board. As an additional safeguard, an external SVS device is added to the design to reset the host MCU when the supplied voltage to power the host MCU is not sufficient. In general, using an external SVS provides more security than the internal SVS on a host microcontroller.

In this design, the test software specifically supports calculation of various metrology parameters for split-phase energy measurement. These parameters can be viewed either from the calibration GUI or LCD. The key parameters calculated during energy measurements are:

- Active, reactive, apparent power and energy
- RMS current and voltage
- Power factor
- Line frequency

The design also enables adding external radio or radio modules for communication. The rail for these external radio modules is current limited in this design to prevent any shorting issues with the communication modules from affecting the metrology.

1.1.2 Power Quality Meter, Power Quality Analyzer

In addition to being used for electricity meters, this standalone ADC architecture can be used for power quality analyzers and power quality meters. Power quality meters and power quality analyzers are used to help utilities and industrial enterprises monitor and control power quality by measuring certain power quality parameters, such as voltage harmonics, current harmonics, supply voltage dips, supply voltage swells, and other parameters as well. For these end equipment, a lot of computation is required for calculating the power quality parameters. Also, accuracy is important to be able to meet the accuracy requirements for the different power quality parameters. The requirement for high accuracy and computation power is something well supported by having a standalone ADC and separate host MCU or processor, as is done in this design.

A couple of the parameters commonly measured by power quality meters and power quality analyzers are voltage and current harmonics. For the most accurate harmonic calculations, coherent sampling should be implemented. One way of implementing coherent sampling is to vary the sampling clock based on the Mains frequency. The standalone ADC in this design has the ability to take in a varying clock so it can support coherent sampling. It should be noted that although the clock to the standalone ADC in this design can be varied, this design cannot support coherent sampling because the sampling clock cannot be varied with the proper resolution; however, this feature can be added in a future design since the standalone ADC can have its clock varied.

1.2 Key System Specifications

表 1. Key System Specifications

FEATURES	DESCRIPTION
Number of phases	1 (split-phase with two voltages measured), 1 (split-phase with one voltage measured), 2 phase
Electricity meter accuracy class	Class 0.1
Current sensor	Current transformer
Tested current range	0.05–100 A
Tested voltage range	15 V–240 V
ADS131M04 CLKIN frequency	8,192,000 Hz
ADS131M04 Delta-sigma modulation clock frequency	4,096,000 Hz (= CLKIN / 2)
SPI Clock	8,192,000 Hz
Oversampling ratio (OSR)	512
Digital filter output sample rate	8,000 samples per second

表 1. Key System Specifications (continued)

FEATURES	DESCRIPTION
Phase compensation implementation	Software
Phase compensation resolution	0.0088° at 50 Hz or 0.0105° at 60 Hz
Selected CPU clock frequency	48 MHz
MCU External SVS voltage	2.0–2.1 V
System nominal frequency	50 or 60 Hz
Measured parameters	• Active, reactive, apparent power and energy • Root mean square (RMS) current and voltage • Power factor • Line frequency
Update rate for measured parameters	Approximately equal to 1 second
Communication options	• LCD • PC GUI via 5 kV_{RMS} isolated RS-232 or isolated RS-485 • External radio, or radio module connected to the Comms header – 5-V rail, current limited to 1.6 A with manual reset after overcurrent thermal shutdown event – Measured power failure detection threshold (VIN Falling) for 5-V rail = 4.05 V – Measured release UVLO (VIN Rising) for 5-V rail = 4.28 V – Measured release overvoltage condition(VIN Falling) for 5-V rail = 5.62 V – Measured overvoltage cutoff threshold(VIN Rising) for 5-V rail = 5.81 V – Custom software must be written for communication)
Utilized LEDs	Total active energy and total reactive energy
Board power supply	Option 1: 3.3 V directly to DVCC rail; Option 2: 5V to J4 header

2 System Overview

2.1 Block Diagram

图 1 and 图 2 depict block diagrams that show the high-level interface used for an ADS131M04-based split-phase energy measurement application. For the two-voltage configuration, the line-to-neutral voltage is directly measured for each line wire. For the one-voltage configuration, in comparison, only the line-to-line voltage is directly measured instead of the line-to-neutral voltages.

图 1. TIDA-010037 Block Diagram, Two-Voltage Configuration

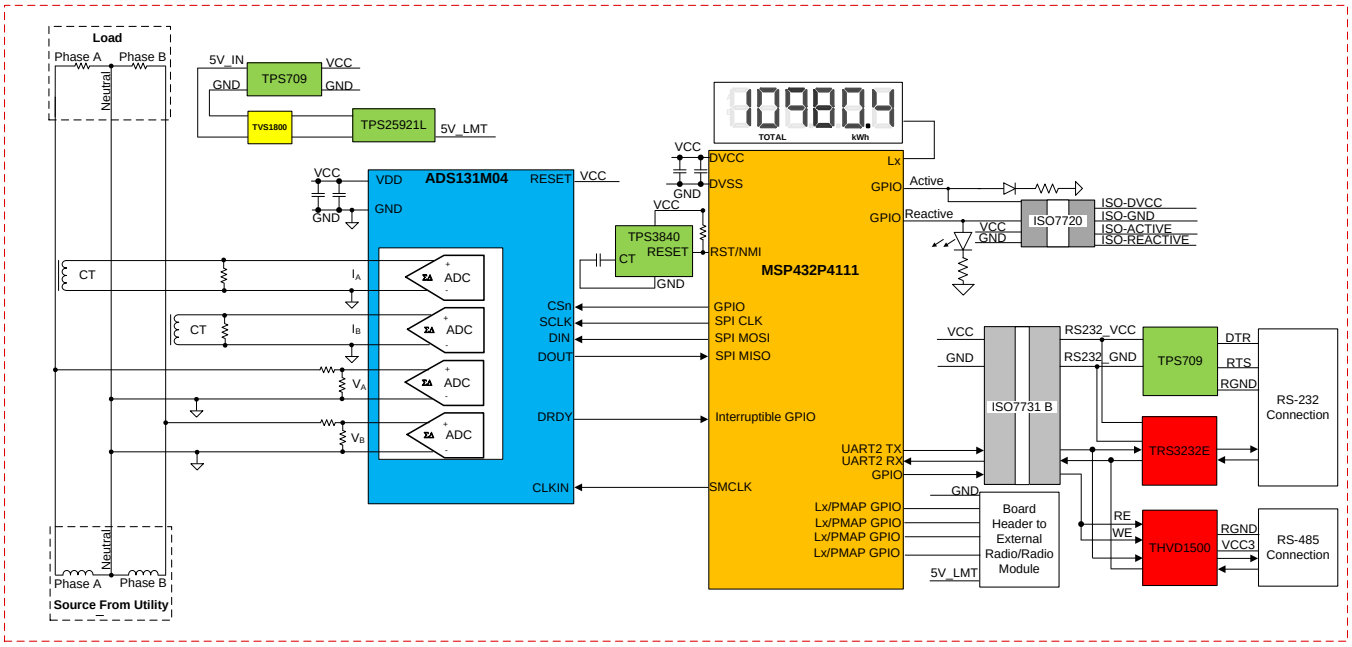
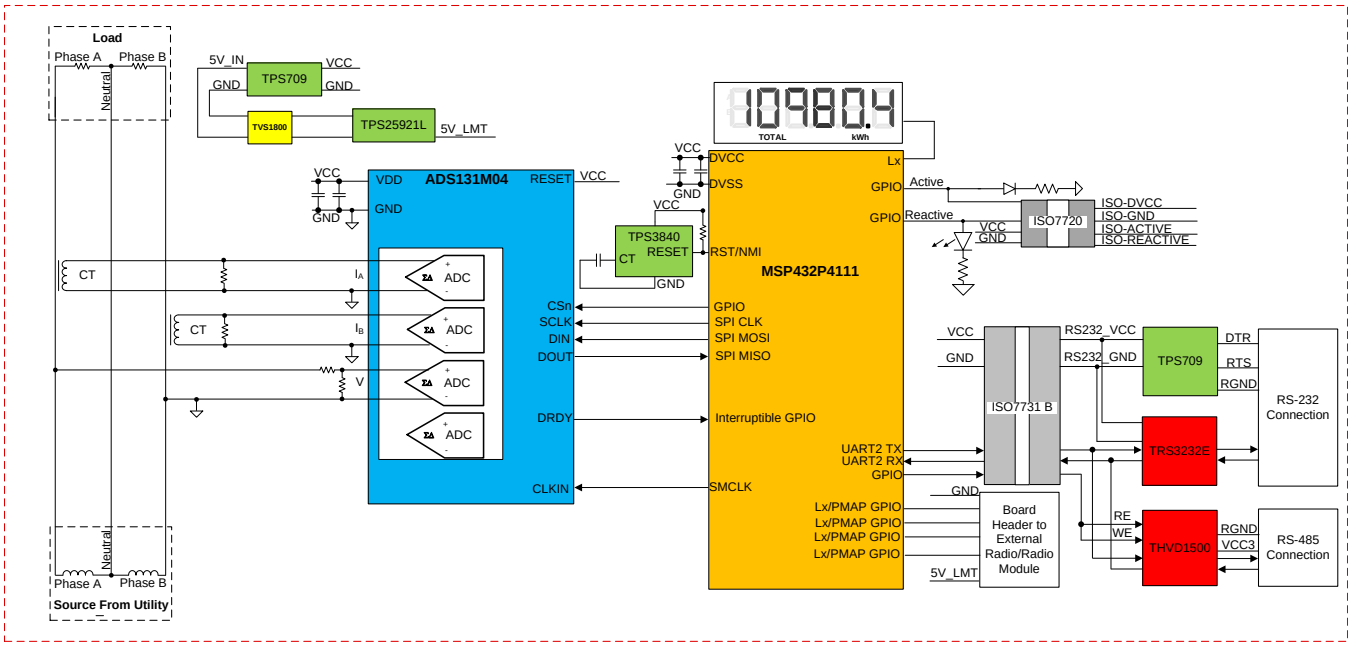


图 2. TIDA-010037 Block Diagram, One-Voltage Configuration



In the diagrams, a current sensor connects to the current channels and a simple voltage divider is used for the corresponding voltage. The CT has an associated burden resistor that must be connected at all times to protect the measuring device. The selection of the CT and the burden resistor is made based on the manufacturer and current range required for energy measurements.

The choice of voltage divider resistors for the voltage channel is selected to ensure the mains voltage is divided down to adhere to the normal input ranges of the ADS131M04 device. Since the ADS131M04 ADCs have a large dynamic range and a large dynamic range is not needed to measure voltage, the voltage front-end circuitry is purposely selected so that the maximum voltage seen at the inputs of the voltage channel ADCs are only a fraction of the full-scale voltage. By reducing the voltage fed to the ADS131M04 voltage ADC, voltage to current crosstalk, which actually affects metrology accuracy more than voltage ADC accuracy, is reduced at the cost of voltage accuracy, thereby resulting in more accurate energy measurements at lower currents.

In this design, the ADS131M04 device interacts with the MSP432™ MCU in the following manner:

1. The CLKIN clock used by the ADS131M04 device is provided from the SMCLK clock signal output of the MSP432 MCU.
2. The ADS131M04 device divides the clock provided on its CLKIN pin by two and uses this divided clock as its delta-sigma modulation clock.
3. When new ADC samples are ready, the ADS131M04 device asserts its $\overline{\text{DRDY}}$ pin, which alerts the MSP432 MCU that new samples are available.
4. After being alerted of new samples, the MSP432 MCU uses one of its SPI interfaces and its DMA to get the voltage and current samples from the ADS131M04 device.

In this design, a TPS3840 device is used as an external SVS for the MSP432 MCU. Although the MSP432 MCU has an internal SVS that suffices for this application, the TPS3840 standalone SVS is used because there is additional security in having a SVS that is independent of the MCU.

Other signals of interest in 图 1 and 图 2 are the active and reactive energy pulses used for accuracy measurement and calibration. The ISO7720 device provides an isolated connection for these pulses for connecting to non-isolated equipment. This is especially needed for the one-voltage configuration since the system is referenced with respect to one of the two high-voltage line voltages for this configuration.

In addition to isolated pulses, the design supports isolated RS-232 communication through the use of the TPS70933, ISO7731B, and TRS3232E devices. The design can be configured to use RS-485 as well instead of RS-232 through the use of the ISO7731B and THVD1500 devices on the board.

The design also supports communication using external radios or radio modules that are connected to the J11 and J12 headers of the board. The J11 header connects the P7.0, P7.1, P7.2, and P7.3 port pins, which can be configured as port mappable GPIO pins, if the LCD is disabled. Software can be added to the MSP432 MCU to communicate to an external radio or radio module by configuring any of these four pins as communication pins(SPI or UART) and appropriately writing and reading packets to and from them. The J12 header is the power rail and GND connection to the radio. The power rail on J12 is the current-limited version of the 5V_IN rail at J4. The J12 power rail is specifically current limited to 1.6 A by the TPS25921L device. If there is a short on the radio module or the current exceeds 1.6 A for some reason, the power to this rail will be limited to prevent the power supply from affecting the power to the metrology-relevant portions of this board. If it is a transient overcurrent event, the module continues to receive power and operate without interruption. However, if there is a persistent fault on the module, the

TPS25921L device will enter thermal shutdown and power is disconnected. After this thermal shutdown event, the power can only be reconnected to the radio module manually by driving the P5.2 GPIO pin. In addition, if the voltage fed to the 5V_IN rail at J4 is below approximately 4.0 V or above 5.8 V, the TPS25921L device is configured to disconnect the power rail on J12. To protect the TPS25921L device from any transients due to switching, a TVS1800 transient protection device is connected to this device.

The design can be powered either by applying 3.3 V at the DVCC header(J9) directly or through the TPS70933 device by applying 5 V at the 5V_IN header(J4). See 表 2 for more details on the proper jumper connections for powering the board for both options.

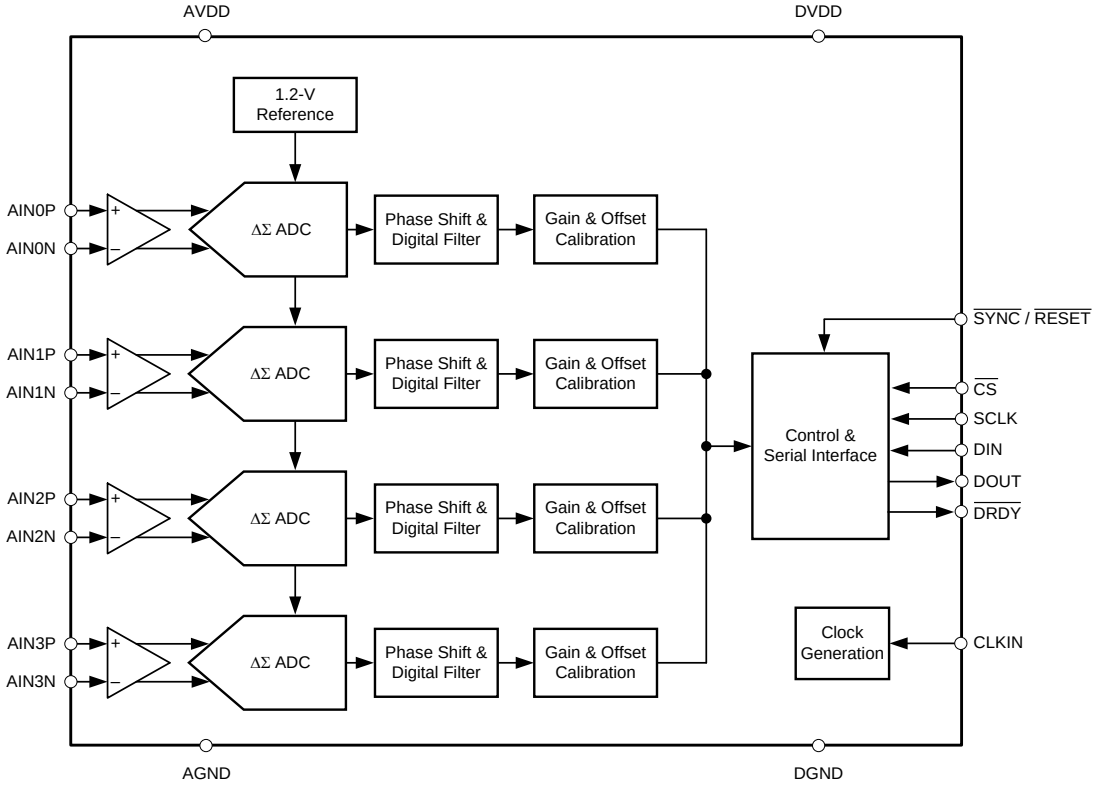
2.2 Highlighted Products

2.2.1 ADS131M04

The ADS131M04 device is a four-channel, simultaneously-sampling, 24-bit, 2nd order delta-sigma (ΔΣ), analog-to-digital converter (ADC) that offers wide dynamic range, and internal calibration features making it well-suited for energy metering, power quality, and protection applications. The ADC inputs can be directly interfaced to a resistor-divider network, a transformer to measure voltage or current, or a Rogowski coil to measure current.

The individual ADC channels can be independently configured depending on the sensor input. A low noise, programmable gain amplifier (PGA) provides gains ranging from 1 to 128 to amplify low-level signals. Additionally, these devices integrate channel to channel phase alignment and offset and gain calibration registers to help remove signal chain errors. A low-drift, 1.2-V reference is integrated into the device reducing printed circuit board (PCB) area. Cyclic redundancy check (CRC) options can be individually enabled on the data input, data output and register map to ensure communication integrity. 图 3 shows a block diagram of this device.

图 3. ADS131M04 Functional Block Diagram



In 图 3, 2.7 V–3.6 V must be fed between AVDD and AGND as well as between DVDD and GND. In addition, an external clock must be connected to CLKIN. When the ADS131M04 device is configured for high-resolution mode, this clock must be between 1 MHz and 8.3 MHz for the ADS131M04 to properly work. The CLKIN clock of the ADS131M04 device can be generated from the SMCLK clock output of the MSP432 MCU. The ADS131M04 divides this clock by two and uses this divided clock for its delta-sigma modulator clock. When new ADC samples are ready, the ADS131M04 asserts its $\overline{\text{DRDY}}$ pin to alert the host MCU that there are new ADC samples that are available. Since the ADS131M04 device can accept a clock with a wide frequency range, the device itself can also be used for applications that require coherent sampling.

2.2.2 MSP432P4111

The SimpleLink™ MSP432P4111 MCUs are optimized MCUs that deliver ultra-low-power performance with FPU and DSP extensions. This device has an Arm® 32-bit Cortex®-M4F CPU with Floating-Point Unit and Memory Protection Unit, a real-time clock, LCD driver, port mappable GPIOs, an AES encryption and decryption accelerator, and multiple serial communication options. The MSP432P4111 device is part of the SimpleLink MCU platform, which consists of Wi-Fi®, *Bluetooth*® low energy, Sub-1 GHz, and host MCUs. All of these devices share a common, easy-to-use development environment with a single-core software development kit (SDK) and rich tool set.

The MSP432 MCU in this design retrieves voltage and current samples from the ADS131M04 device and calculates metrology parameters. In addition, the device also keeps track of time with its RTC module, drives the LCD on the board with its internal LCD driver module, and uses one of its UART interfaces to communicate to a PC GUI using either the isolated RS-232 or isolated RS-485 circuit of the board. The CRC module of the MSP432 MCU is also used to accelerate the CRC calculations that are done to verify the integrity of the ADC packet sent by the ADS131M04 device.

2.2.3 TPS3840

The TPS3840 family of voltage supervisors or reset ICs can operate at high voltage levels while maintaining very low quiescent current across the whole VDD and temperature range. The TPS3840 device offers best combination of low power consumption, high accuracy and low propagation delay.

The reset output signal of the device is asserted when the voltage at VDD drops below the negative voltage threshold (V_{IT-}) or when manual reset is pulled to a low logic ($V_{\overline{MR}\_L}$). The reset signal is cleared when VDD rises above V_{IT-} plus hysteresis (V_{IT+}) and manual reset ($\overline{MR}$) is floating or above $V_{\overline{MR}\_H}$ and the reset time delay (t_D) expires. Reset time delay can be programmed by connecting a capacitor to ground in the CT pin, for a fast reset CT pin can be left floating. Additional features include low power on reset voltage (V_{POR}), built in glitch immunity protection for $\overline{MR}$ and VDD, build in hysteresis and low open drain output leakage current ($I_{LKG(OD)}$).

For electricity meters, some manufacturers prefer to have external SVS devices to reset any microcontrollers in the system, even if the microcontrollers already have an internal SVS. External SVS devices are sometimes preferred over using the SVS within a microcontroller because the external option can be more secure than the internal option, since the external devices function independently of the microcontroller. Although the SVS of the MSP432 MCU suffices for this application, the TPS3840 external SVS device is added to this design for an additional level of security. External SVS devices may sometimes also be used for early detection of a Mains blackout condition by monitoring one of the rails of an AC/DC powered from Mains.

In this design, the TPS3840DL20 variant is specifically used, which has a 2-V threshold and an open drain, active low output.

2.2.4 TPS25921L

The TPS25921 device is a compact, feature-rich eFuse with a full suite of protection functions. The wide operating voltage allows control of many popular DC buses. The precise ±2% current limit, at room temperature, provides excellent accuracy making the TPS25921 device well-suited for many system protection applications. It provides robust protection for all systems and applications powered from 4.5 V to 18 V. For hot-plug-in boards, the device provides in-rush current control and programmable output ramp-rate.

The TPS25921 device integrates overcurrent and short-circuit protection. The precision overcurrent limit helps to minimize over design of the input power supply, while the fast response short circuit protection immediately isolates the load from input when a short circuit is detected. The device allows the user to program the overcurrent limit threshold between 0.4 A and 1.6 A via an external resistor.

The device provides precise monitoring of voltage bus for brown-out and overvoltage conditions and asserts fault for downstream system. Its threshold accuracy of 3% ensures tight supervision of bus, eliminating the need for a separate supply voltage supervisor chip. The TPS25921 device is designed to protect systems such as White Goods, STBs, DTVs, Smart Meters, and Gas Analyzers.

Additional features of the device include:

- Overtemperature protection to safely shutdown in the event of an overcurrent event
- Fault reporting for brown-out and overvoltage faults
- A choice of latched or automatic restart mode

For electricity meters, many manufacturers are using wireless communication to transmit data. These wireless modules may require from hundreds of milliamps to a couple of Amps to operate during the signal emission. If there is a malfunction that causes the current drawn from the module to exceed the current allotted for the wireless module, the power supply could fail, which could affect the metrology side of the meter if it shares the same power supply source as the wireless module without some type of current limiting. To ensure that the metrology is working properly and accurately at any moment, it is important to have a way to control this current spike. The TPS25921 device resolves this issue by limiting the current provided to the wireless communication module.

In this design, the latched version (TPS25921L) of this part is used, which enable the system to choose when the eFuse is reset after a thermal shutdown event. When an overcurrent situation triggers the thermal shutdown event of the TPS25921L device, the current is limited by quickly opening it and triggering the $\overline{\text{FLT}}$ signal. This $\overline{\text{FLT}}$ signal is fed to the MSP432 MCU to let it know that an event happened. After a thermal shutdown event, the MSP432 MCU can pull the ENUV pin low to reset the device and start powering the wireless module again , assuming that the overcurrent condition is no longer present.

2.2.5 THVD1500

The THVD1500 device is a robust half-duplex RS-485 transceiver for industrial applications. The bus pins are immune to high levels of IEC Contact Discharge ESD events eliminating the need of additional system-level protection components.

The device operates from a single 5-V supply. The wide common-mode voltage range and low input leakage on bus pins make THVD1500 suitable for multi-point applications over long cable runs.

The THVD1500 device is available in industry standard 8-pin SOIC package for drop-in compatibility. The device is characterized from –40°C to 125°C. The device also meets or exceeds the requirements of the TIA/EIA-485A Standard and the State Grid Corporation of China (SGCC) Part 11 Serial Communication Protocol RS-485 Standard.

This device is specifically used in this design to convert from UART to RS-485 signals.

2.2.6 ISO7731B

To add isolation to the RS-232 and RS-485 connection to a PC, the isolated RS-232 and isolated RS-485 portion of this reference design uses capacitive galvanic isolation, which has an inherent life span advantage over an opto-isolator. In particular, industrial devices are usually pressed into service for much longer periods of time than consumer electronics; therefore, maintenance of effective isolation over a period of 15 years or longer is important.

The variant of the ISO7731B device used in the RS-232 and RS-485 circuitry of this reference design provides galvanic isolation up to 5 kV_{RMS} for one minute per UL. This digital isolator has three isolated channels where two channels are forward channels and the other is a reverse channel. In this design, two isolation channels are used for the TX and RX. If RS-485 is selected for communication, the third isolation channel is used for the control signal used to enable the receiver or driver. If RS-232 is selected, the third

isolation channel is not needed. If RS-232 is desired in a customer's system instead of RS-485, only two isolation channels are needed, so a two-channel ISO7721B device could be used to reduce cost instead of using the three-channel ISO7731B device (keep in mind that these two devices are not pin-to-pin compatible). Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO2) insulation barrier. This chip supports a signaling rate of 100 Mbps. The chips can operate from a 2.5 V, 3.3-V, and 5-V supply and logic levels.

2.2.7 TRS3232E

To properly interface with the RS-232 standard, a voltage translation system is required to convert between the 3.3-V domain on the board and from the 12 V on the port itself. To facilitate the translation, the design uses a TRS3232E device. The TRS3232E device is capable of driving the higher voltage signals on the RS-232 port from only the 3.3-V DVCC through a charge pump system.

The TRS3232E device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV electrostatic discharge (ESD) protection pin-to-pin (serial-port connection pins, including GND). The device meets the requirements of the Telecommunications Industry Association and Electronic Industries Alliance TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbps and a maximum of 30-V/µs driver output slew rate.

2.2.8 TPS709

To power the data terminal equipment (DTE) side of the isolation boundary and the RS-232 charge pump, there are two choices. The interface can either implement an isolated power supply or harvest power from the RS-232 line. Integrating a power supply adds cost and complexity to the system, which is difficult to justify in low-cost sensing applications.

To implement the second option of harvesting power from the RS-232 port itself, this reference design uses the flow control lines that are ignored in most embedded applications. The RS-232 specification (when properly implemented on a host computer or adapter cable), keeps the request to send (RTS) and data terminal ready (DTR) lines high when the port is active. As long as the host has the COM port open, these two lines retain voltage on them. This voltage can vary from 5 V to 12 V, depending on the driver implementation. The 5 V to 12 V is sufficient for the use requirements in this design.

The voltage is put through a diode arrangement to block signals from entering back into the pins. The voltage charges a capacitor to store energy. The capacitor releases this energy when the barrier and charge pump pull more current than what is instantaneously allowed. The TPS70933 device is used to bring the line voltage down to a working voltage for the charge pump and isolation device.

In addition to being used in the RS-232 circuit, an additional TPS709 device is used to regulate the 5-V input voltage from the 5V_IN rail down to the 3.3 V used to power most of the components on the board.

The TPS70933 linear regulator is an ultra-low quiescent current devices designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy overtemperature. A quiescent current of only 1 µA makes these devices ideal solutions for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety. These regulators can be put into shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150 nA (typical).

2.2.9 TVS1800

The TVS1800 device robustly shunts up to 40 A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes. The device offers a solution to the common industrial signal line EMC requirement to survive up to ±1 kV IEC 61000-4-5 open circuit voltage coupled through a 42-Ω impedance. The TVS1800 device uses a unique feedback mechanism to ensure precise flat clamping during a fault, assuring system exposure below 25 V. The tight voltage regulation allows designers to confidently select system components with a lower voltage tolerance, lowering system costs and complexity without sacrificing robustness. In addition, the TVS1800 device is available in a small 2-mm × 2-mm SON footprint which is ideal for space-constrained applications, offering a 70 percent reduction in size compared to industry standard SMA and SMB packages. The extremely low device leakage and capacitance ensure a minimal effect on the protected line. To ensure robust protection over the lifetime of the product, TI tests the TVS1800 device against 5,000 repetitive surge strikes at high temperature with no shift in device performance. In this design, the TVS1800 device is placed at the input of the TPS25921L device to protect it from any transient voltages that would occur from the TPS25921L disconnecting the load during overcurrent, overvoltage, or undervoltage events.

2.2.10 ISO7720

The ISO772x devices are high-performance, dual-channel digital isolators with 5000 V_{RMS} (DW package) and 3000 V_{RMS} (D package) isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC. The ISO772x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO2) insulation barrier. The ISO7720 device has both channels in the same direction while the ISO7721 device has both channels in the opposite direction. In the event of input power or signal loss, the default output is high for devices without suffix F and low for devices with suffix F. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO772x devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO772x family of devices is available in 16-pin SOIC wide-body (DW) and 8-pin SOIC narrow-body (D) packages.

To test the active energy and reactive energy accuracy of a meter, pulses are output at a rate proportional to the amount of energy consumed. A reference meter can then determine the accuracy of the electricity meter by calculating the error based on these pulses and how much energy is provided to the meter. In this reference design, pulses are output through headers for the cumulative active and reactive energy consumption. Using the ISO7720 device provides an isolated version of these headers for connection to non-isolated equipment, which is especially needed when the design is configured for one-voltage operation since the design is referenced with respect to one of the high-voltage line connections. In this design, the D package of the ISO7720 device is used, which provides an isolation voltage of 3000 V_{RMS} for these signals. These isolated active and reactive signals can be set to have either a 3.3- or 5-V maximum voltage output by applying the selected maximum voltage output between the VCC (ISO_VCC) and GND (ISO_GND) of the isolated side.

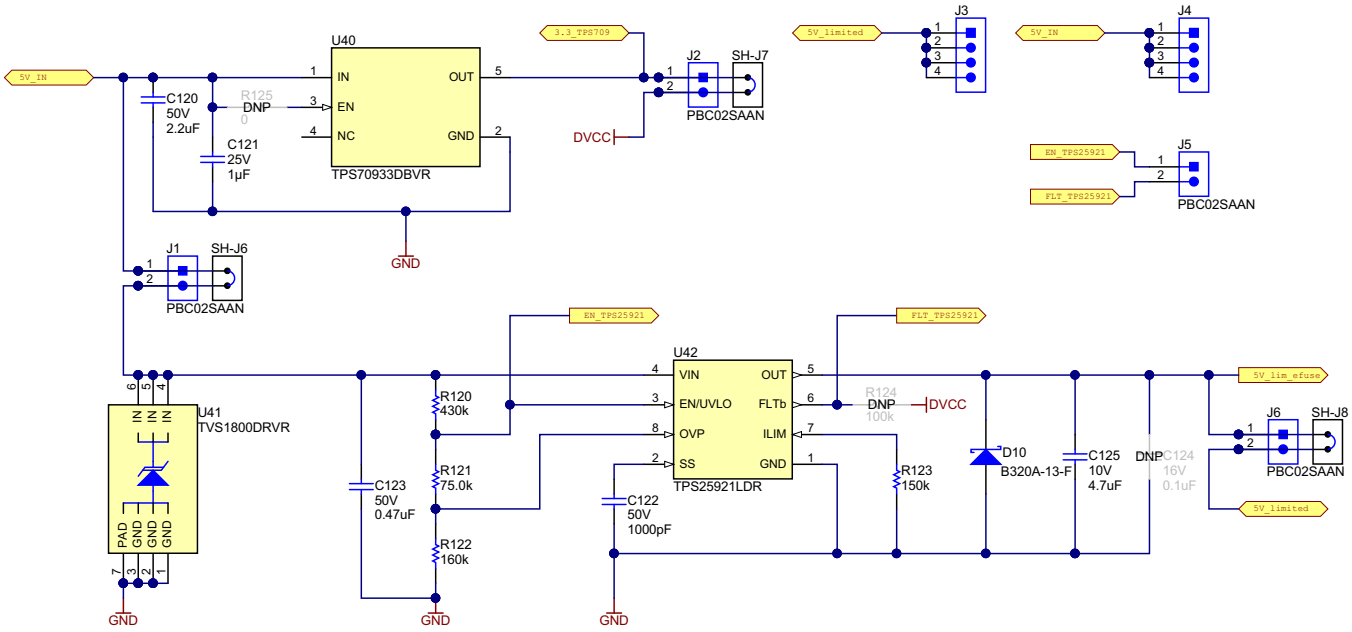
2.3 Design Considerations

2.3.1 Design Hardware Implementation

2.3.1.1 Current Limiter Circuit

For smart meters, it is often desired to limit the current to any communication radios in the system. Limiting the current of the communication devices prevents any issues, whether accidentally induced from unintended shorts or purposely induced by someone for the sake of tampering with the meter, from affecting the metrology. When the design is properly configured, the voltage rail at header J3 is current-limited so that it can be used to power an external radio or radio module while ensuring that any shorts on the radio module would not affect the metrology or any other portions of the system. 图 4 shows the current-limiting circuit used in this design.

图 4. Current Limiting Circuitry



The current-limiting functionality in this design is performed by the TPS25921L e-Fuse device, which powers the load connected to the J3 header from the source connected to the header on J4. For proper operation, use 5 V as the voltage provided by the source connected to J4. There is a TPS70933 LDO that can be used to generate the 3.3-V rail for the ADS131M04 device and MSP432 MCU from the 5 V applied at J4 so that only one input rail is necessary.

If the voltage provided to J4 is below 4.036 V (based on internal undervoltage lockout voltage) or above 5.78 V, the source at J4 will be disconnected from the load at J3. In addition, if the current drawn from the load exceeds 1.6 A, thermal shutdown is eventually triggered and the source is disconnected from the load. During an overvoltage, undervoltage, or thermal shutdown event, the FLT_TPS25921 GPIO pin connected to the FLTb pin on the TPS2591L device is asserted low. During a thermal shutdown event, the TPS25921L device remains off until the EN_TPS25921 GPIO pin is toggled. In the test software, the TPS25921L device is only reset after thermal shutdown by toggling the EN_TPS25921 GPIO pin if the overcurrent condition is immediately addressed and if there were no previous overvoltage, undervoltage, or thermal shutdown events.

In 图 4, R120, R121, and R122 are selected based on the desired overvoltage thresholds. Also, R123 is selected based on the desired current limit. For details on selecting new values of R120, R121, R122, and R123 to change the overvoltage, and current limiting thresholds, see the *TPS25921x 4.5 V - 18 V eFuse with precise current limit and overvoltage protection* data sheet. In this design, the internal undervoltage lockout voltage is used for the undervoltage threshold.

Disconnecting the source from the load could cause transients on the TPS25921L input and output. To protect the TPS25921L device from transient voltages at its input as the result of switching, a TVS1800 surge protection device is used (U41 in 图 4). To protect the load from transient voltages due to switching, a Zener diode is used (D10 in 图 4).

2.3.1.2 TPS3840 SVS

The TPS3840 device is an external supply voltage supervisor (SVS) that is used to externally reset the MSP432 MCU. The TPS3840 maintains very low quiescent current, which enables this device to still be used if there is a power outage and the meter is running from a backup battery. The MSP432 MCU has an internal SVS device that can be used as well, which will suffice for this application; however, using an external SVS instead of the internal SVS of the microcontroller adds an additional layer of security since it is not independent of the microcontroller, and therefore, is less affected by any issues that affect the microcontroller itself.

In this design, the TPS3840DL20 device variant is specifically used, which has a negative-voltage threshold voltage of 2 V. When the voltage rail that powers the MSP432 MCU drops below 2 V, the TPS3840 device resets the MSP432 MCU. When the monitored voltage rises above the undervoltage threshold plus hysteresis voltage value (approximately equal to 2.1 V total) , the RESET pin of the TPS3840 is pulled back high after a user-defined reset delay time, t_D, elapses. t_D is determined based on the value of the capacitor connected to the CT pin of the TPS3840 device. In this design, a 0.33-µF capacitor is connected to the CT pin of the TPS3840 device, which leads to a reset delay time of about 204 ms.

The TPS3840 device is available with both push-pull and open-drain outputs. The open-drain output is specifically selected for this design since a 47-kΩ pullup resistor is recommended in the JTAG circuitry of the MSP432 MCU.

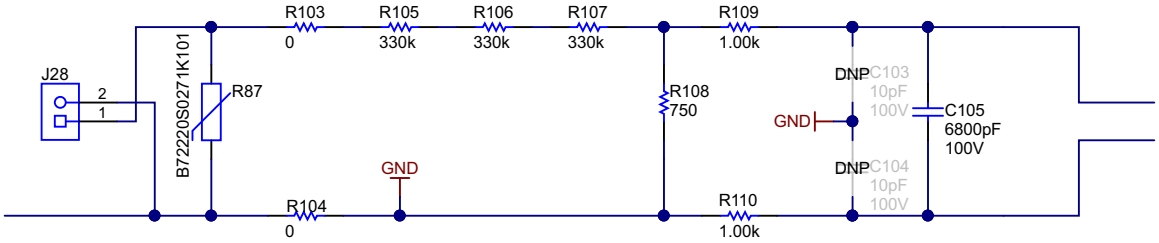
2.3.1.3 Analog Inputs

The analog front end in this design consists of the ADS131M04 delta sigma standalone ADC. Each of the ADS131M04 converters is differential and requires that the input voltages at the pins does not exceed ±1.2 V (gain = 1). To meet this input voltage specification, the current and voltage inputs must be divided down. In addition, the ADS131M04 device can sense voltages down to −1.2 V; therefore, AC signals from mains can be directly interfaced without the need for level shifters. This subsection describes the analog front end used for voltage and current channels.

2.3.1.3.1 Voltage Measurement Analog Front End

The nominal voltage from the mains is from 100 V–240 V so it needs to be scaled down to be sensed by an ADC. 图 5 shows the analog front end used for this voltage scaling. J28 is where the voltage is applied.

图 5. Analog Front End for Voltage Inputs



In the analog front end for voltage, there consists a spike protection varistor (R87), footprints for electromagnetic interference filter beads (resistor footprints R103 and R104) , a voltage divider network (R105, R106, R107, and R108), and an RC low-pass filter (R109, R110, C103, C104, and C105).

At lower currents, voltage-to-current crosstalk affects active energy accuracy much more than voltage accuracy, if power offset calibration is not performed. To maximize the accuracy at these lower currents, in this design the entire ADC range is not used for voltage channels. Since the ADCs of the ADS131M04 device are high-accuracy ADCs, using the reduced ADC range for the voltage channels in this design still provides more than enough accuracy for measuring voltage. 公式 1 shows how to calculate the range of differential voltages fed to the voltage ADC channel for a given Mains voltage and selected voltage divider resistor values.

$$V_{ADC\_Swing,Voltage} = \pm V_{RMS} \times \sqrt{2} \left(\frac{R_{108}}{R_{105} + R_{106} + R_{107} + R_{108}} \right) \quad (1)$$

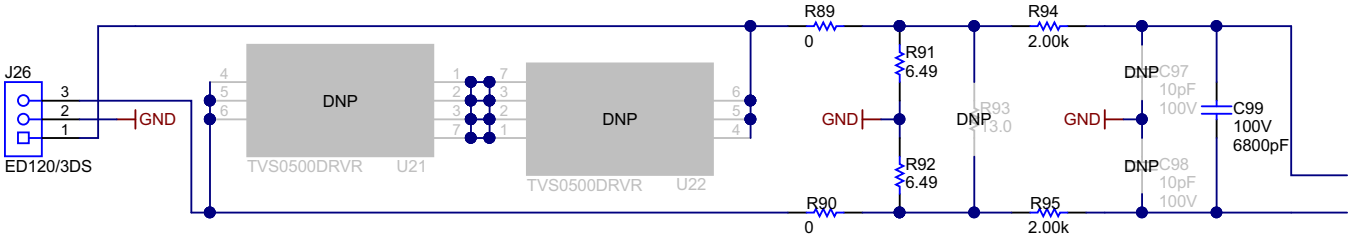
Based on this formula and the selected resistor values in 图 5, for a mains voltage of 120 V (as measured between the line and neutral), the input signal to the voltage ADC has a voltage swing of ±128 mV (91 mV_{RMS}) when using the two-voltage configuration. For the one-voltage configuration, for a mains voltage of 120 V (as measured between the line and neutral), 240 V would be input to the front-end circuit in 图 5 since the line-to-line voltage is measured instead of the line-to-neutral voltage. The 240-V input to the front-end circuit produces a voltage swing of ±257 mV (182 mV_{RMS}). The ±128-mV and the ±257-mV voltage ranges for the two-voltage and one-voltage configurations are both well within the ±1.2-V input voltage that can be sensed by the ADS131M04 device for the selected PGA gain value of 1 that is used for the voltage channels.

Note that the pin order of the AINxP and AINxN pins on the ADS131M04 is swapped when going from one converter to another. As an example, AIN2P is pin 7 and AIN2N is pin 8 but AIN3N is pin 9 and AIN3P is pin 10. The swapped order is why the order of the positive input voltage and negative input voltage is swapped between the J28 voltage input terminal block of Phase A and the J29 voltage input terminal block of Phase B.

2.3.1.3.2 Current Measurement Analog Front End

The analog front end for current inputs is different from the analog front end for the voltage inputs. 图 6 shows the analog front end used for a current channel, where the positive and negative leads from a CT are connected to pins 1 and 3 of header J26.

图 6. Analog Front End for Current Inputs



The analog front end for current consists of footprints for electromagnetic interference filter beads (R89 and R90), burden resistors for current transformers (R91 and R92), and an RC low-pass filter (R94, R95, C97, C98, and C99) that functions as an anti-alias filter. There are also footprints (U21 and U22) that can be replaced with the TVS0500 for supplemental protection from surges, if required.

As 图 6 shows, resistors R91 and R92 are the burden resistors, which are in series with each other. For best THD performance, instead of using one burden resistor, two identical burden resistors in series are used with the common point being connected to GND. This split-burden resistor configuration ensures that the waveforms fed to the positive and negative terminals of the ADC are 180 degrees out of phase with each other, which would provide the best THD results with this ADC. The total burden resistance is selected based on the current range used and the turns ratio specification of the CT (this design uses CTs with a turns ratio of 2000). The total value of the burden resistor for this design is 12.98 Ω.

公式 2 shows how to calculate the range of differential voltages fed to the current ADC channel for a given maximum current, CT turns ratio, and burden resistor value.

$$V_{ADC\_Swing,Current} = \pm \frac{\sqrt{2}\left(R_{91} + R_{92}\right) I_{RMS,max}}{CT_{TURNS\_RATIO}} \quad (2)$$

Based on the maximum current of 100 A, CT turns ratio of 2000, and burden resistor of 12.98 Ω, of this design, the input signal to the current ADC has a voltage swing of ±918 mV maximum (649 mV_{RMS}) when the maximum current rating of the meter (100 A) is applied. This ±918-mV maximum input voltage is well within the ±1.2-V input range of the device for the selected PGA gain of 1 that is used for the current channels.

Note that the pin order of the AINxP and AINxN pins on the ADS131M04 is swapped when going from one converter to another. As an example, AIN0P is pin 3 and AIN0N is pin 4 but AIN1N is pin 5 and AIN1P is pin 6. The swapped order is why the order of the CT positive output terminal and negative output terminal is swapped between the J26 current input terminal block of Phase A and the J27 current input terminal block of Phase B.

2.3.2 How to Implement Software for Metrology Testing

The MSP432 software used for evaluating this design is test software. This section discusses the features of the test software, which should provide insights on how to implement custom software for metrology testing. The first subsection discusses the setup of the ADS131M04 device and various peripherals on the MSP432 MCU. Subsequently, the metrology software is described as two major processes: the foreground process and background process.

2.3.2.1 Setup

2.3.2.1.1 Clock

The MSP432 MCU is configured to have its CPU clock (MCLK) set at 48 MHz and its subsystem master clock (SMCLK) set to 8.192 MHz. The clock source for MCLK is the internal DCO of the MSP432 MCU, which is configured for a frequency of 48 MHz. The clock source for SMCLK is an external 16.384-MHz crystal, which is internally divided by 2 to create the 8.192-MHz SMCLK frequency. An external 32.768-kHz crystal is used as the clock source for the auxiliary clock (ACLK) of the device. This ACLK clock is set to a frequency of 32.768 kHz.

2.3.2.1.2 Port Map

The MSP432 MCU has a port mapping controller that allows a flexible mapping of digital functions to port pins. The set of digital functions that can be ported to other pins is dependent on the device. For the MSP432 device in particular, the SPI clock, SOMI, and SIMO functionality of the EUSCIB0 SPI module are all available options to port to ports P2, P3, and P7. In addition, the SMCLK clock output is also available for output to ports P2, P3, and P7. In the test software, this port mapping feature is used for providing flexibility in the PCB layout.

Using the port mapping controller, the following mappings are used:

- PMAP_SMCLK (SMCLK clock output) → Port P2.0 (connected to the CLKIN pin of the ADS131M04 device so that it can be used to generate the modulator clock of the ADS131M04; however, note that this mapping is not enabled initially and is only enabled after the ADS131M04 is initialized.); this is pin 1 of header J32, which is labeled SMCLK on the board
- PMAP_UCB0SIMO (EUSCIB0 SPI SIMO) → Port P2.1 (connected to the DIN pin of the ADS131M04 device) this is pin 2 of header J32, which is labeled SPI DOUT on the board
- PMAP_UCB0SOMI (EUSCIB0 SPI SOMI) → Port P2.2 (connected to the DOUT pin of the ADS131M04 device) this is pin 3 of header J32, which is labeled SPI DIN on the board
- PMAP_UCB0CLK (EUSCIB0 SPI Clock) → Port P2.3 (connected to the SCK pin of the ADS131M04 device) this is pin 4 of header J32, which is labeled SPI CLK on the board

2.3.2.1.3 UART Setup for GUI Communication

The MSP432 MCU is configured to communicate to the PC GUI through either the RS-232 or RS-485 connection on this reference design. The MSP432 MCU communicates to the PC GUI using a UART module configured for 8N1 at 9600 baud.

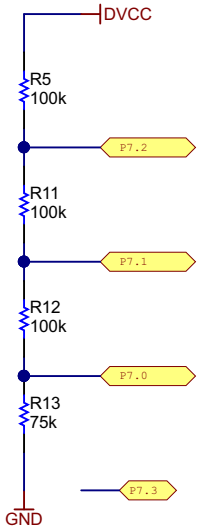
2.3.2.1.4 Real-Time Clock (RTC)

The real-time clock module of the MSP432 MCU is configured to give precise one-second interrupts and update the time and date, as necessary.

2.3.2.1.5 LCD Controller

The LCD controller on the MSP432P4111 MCU can support up to 8-MUX displays and 320 segments or 4-MUX displays and 176 segment displays. In the current design, the LCD controller is configured to work in 4-MUX mode using 144 segments. The eight segment lines not used in the 4-MUX mode of this design are used for the port mapping functionality. In this reference design, the LCD is configured for a refresh rate set to ACLK / 64, which is 512 Hz. For contrast control, external resistors are added between the R23, R13, R03 pins and GND, as 图 7 shows.

图 7. LCD External Resistors



If the LCD is not needed and P7.0, P7.1, or P7.2 is to be used for some other functionality, such as communication to an external radio module, remove the resistors in 图 7 and use software to implement the desired custom functionality.

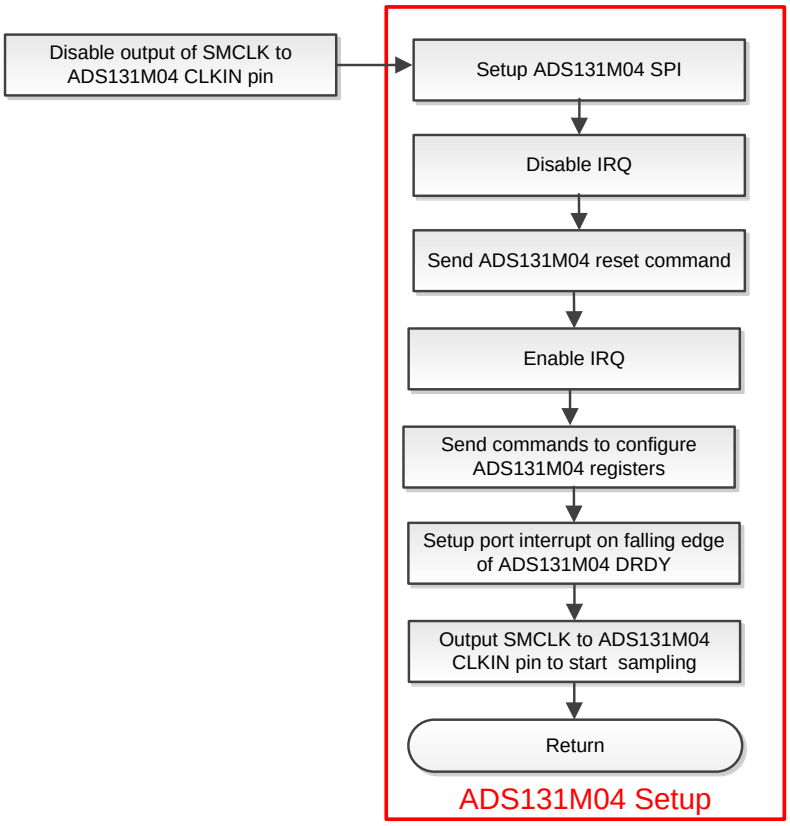
2.3.2.1.6 Direct Memory Access (DMA)

The direct memory access (DMA) module transfers packets between the MSP432 MCU and ADS131M04 device with minimal bandwidth requirements from the MSP432 CPU. Two DMA channels are used for communicating to the ADS131M04. One channel (channel 0) is used to send data to the ADS131M04 and the other channel (channel 1) is used to receive data from the ADS131M04. Once a complete packet has been received from the ADS131M04, an interrupt is generated to complete any necessary post-transfer processing, such as CRC verification and packet assembly. 图 12 shows the packets that are sent and received using the DMA of the MSP432 MCU.

2.3.2.1.7 ADC Setup

图 8 shows the process used to initialize the ADS131M04. This process is followed when the ADS131M04 is being first setup after the MSP432 MCU resets as well as each time calibration is performed.

图 8. ADC Initialization and Synchronization Process



Before setting up the ADS131M04 device, the modulator clock of the ADS131M04 is disabled to prevent the ADS131M04 from generating new samples while trying to set it up. The modulator clock is disabled by disabling the SMCLK output of the MSP432 MCU, which is fed to the CLKIN pin of the ADS131M04. Disabling the SMCLK output only needs to be done after calibration and not after an MSP432 MCU reset event since the SMCLK clock output is automatically not output after the MSP432 MCU resets.

After the SMCLK output is disabled, the EUSCIB0 SPI module of the MSP432 MCU is configured for communication to the ADS131M04 device. The EUSCIB0 SPI module is specifically configured as a master device that uses 3-wire mode (the chip select signal is manually asserted high and low in the test software instead of using the chip select feature of the SPI module) and has an 8.192-MHz SPI clock that is derived from the 8.192-MHz SMCLK clock. After the SPI is setup, all interrupts are disabled and a reset command is sent from the MSP432 MCU to the ADS131M04 via SPI. Interrupts are then re-enabled and the MSP432 MCU sends commands to the ADS131M04 to configure its registers.

At this point, note that the modulation clock is not output by the MSP432 MCU yet, which means that sampling is not started yet. By sending commands to the ADS131M04 to initialize the ADS131M04 registers, the ADS131M04 is configured for the following:

- MODE register settings: 16-bit CCITT CRC used, 24-bit length for each word in the ADS131M04 packet, $\overline{\text{DRDY}}$ signal asserted on most lagging enabled channel, $\overline{\text{DRDY}}$ asserted high when conversion value is not available, $\overline{\text{DRDY}}$ asserted low when conversion values are ready
- GAIN1 register settings: PGA gain of 1 used for all four ADC channels
- CFG register settings: Current detection mode disabled
- CHx_CNG register settings (where x is the channel number)

  - Two-voltage mode: All four ADC channel inputs connected to external ADC pins and channel phase delay set to 0 for each channel (note that software phase compensation is used instead of ADS131M04 hardware phase compensation)
  - One-voltage mode: Channels 0, 1, and 2 inputs connected to external ADC pins and channel phase delay set to 0 for channels 0, 1, and 2 (note that software phase compensation is used instead of ADS131M04 hardware phase compensation); the channel 3 config register is not modified since channel 3 is not used for this configuration.
- CLOCK register settings: 512 OSR, all channels enabled, and high-resolution modulator power mode

After the ADS131M04 registers are properly initialized, the MSP432 MCU is configured to generate a port interrupt whenever a falling edge occurs on the $\overline{\text{DRDY}}$ pin, which would indicate that the ADS131M04 has new current samples that are available. Next, the MSP432 MCU outputs the SMCLK clock to the ADS131M04, which starts the voltage and current sampling.

The ADS131M04 modulator clock is derived from the clock fed to its CLKIN pin, which is output from the SMCLK output of the MSP432 MCU. The clock fed to the CLKIN pin of the ADS131M04 device is internally divided by two, to generate the ADS131M04 modulator clock. The sampling frequency of the ADS131M04 is therefore defined as $f_s = f_M / OSR = f_{CLKIN} / (2 \times OSR)$, where f_s is the sampling rate, f_M is the modulator clock frequency, f_{CLKIN} is the clock fed to the ADS131M04 CLKIN pin, and OSR is the selected oversampling ratio. In this design, the SMCLK clock of the MSP432 MCU that is fed to the ADS131M04 CLKIN pin has a frequency of 8.192 MHz. The oversampling ratio is selected to be 512 . As a result, the ADS131M04 modulator clock is set to 4.096 MHz and the sample rate is set to 8000 samples per second.

For a two-voltage system where each line-to-neutral voltage is measured, at least four ADC channels are necessary to independently measure two voltages and two currents. In this design, the following ADS131M04 channel mappings are used in software for the two-voltage configuration:

- AIN0P and AIN0N ADS131M04 ADC channel pins → Current I1 (Phase A Current)
- AIN1P and AIN1N ADS131M04 ADC channel pins → Current I2 (Phase B Current)
- AIN2P and AIN2N ADS131M04 ADC channel pins → Voltage V1 (Phase A Line-to-Neutral Voltage)
- AIN3P and AIN3N ADS131M04 ADC channel pins → Voltage V2 (Phase B Line-to-Neutral Voltage)

For a balanced split-phase system, each line-to-neutral voltage should be half of the line-to-line voltage. In the one-voltage configuration of this design, only the line-to-line voltage is measured. The line-to-line voltage readings are divided by two (this division is done automatically by following the calibration process) to get the line-to-neutral voltages of each phase. As a result, the same ADC samples are used in the software to calculate the RMS voltage and power for the two phases. This configuration uses three ADC channels: one to measure the line-to-line voltage and the other two for the two currents. In this design, the following ADS131M04 channel mappings are used in software for the one-voltage configuration:

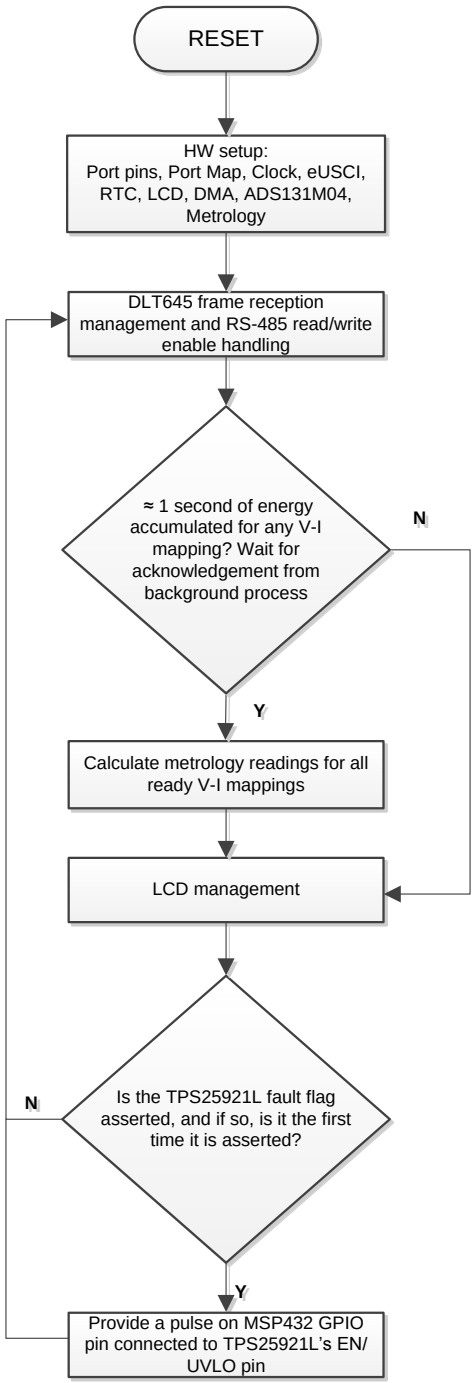
- AIN0P and AIN0N ADS131M04 ADC channel pins → Current I1 (Phase A Current)
- AIN1N and AIN1P ADS131M04 ADC channel pins → Current I2 (Phase B Current)
- AIN2P and AIN2N ADS131M04 ADC channel pins → Line-to-Line Voltage (Phase A line voltage - Phase B line voltage)
- AIN3P and AIN3N ADS131M04 ADC channel pins → Not used in design

Since the line-to-line voltage measured in the one-voltage configuration is the Phase A line voltage - Phase B line voltage and not the Phase B line voltage - Phase A line voltage, the orientation for phase B current should be reversed, which is done by either swapping where the positive and negative output terminals of the current transformers of Phase B are connected, swapping the polarity of the current fed to the Phase B current input in the design, or by using the same input current and CT output terminal polarity at phase A and just negating the current channel ADC channels in software. To prevent having to do any hardware changes when switching from two-voltage to one-voltage modes, this design reverses the polarity of the current channels by choosing the option where the phase B current channel values are negated in the test software.

2.3.2.2 Foreground Process

The foreground process includes the initial setup of the MSP432 hardware and software and the ADS131M04 registers immediately after a device RESET. 图 9 shows the flowchart for this process.

图 9. Foreground Process



The initialization routines involve the setup of the MSP432 general purpose input/output (GPIO) port pins and associated port map controller; MSP432 clock system; MSP432 USCI_A0 for UART functionality; MSP432 RTC module for clock functionality; MSP432 LCD; MSP432 DMA; ADS131M04 registers; and MSP432 metrology variables.

After the hardware is setup, any received frames from the GUI are processed. If RS-485 is selected for communication to the PC GUI, the THVD1500 device must have its RE and DE pins driven to enable the receiver and driver during the proper points in time to receive packets from the PC GUI and send responses back to the GUI. After any packet is sent from the MSP432 MCU to the PC GUI, the foreground process is responsible for asserting the RE and DE pins after the packet has been completely sent out from the MSP432 MCU but before the GUI sends out its next packet.

Subsequently, the foreground process checks whether the background process has notified the foreground process to calculate new metering parameters for any voltage-current mappings. This notification is accomplished through the assertion of the "PHASE_STATUS_NEW_LOG" status flag whenever a frame of data is available for processing. The data frame consists of the processed dot products that were accumulated for approximately one second in the background process. This is equivalent to an accumulation of 50 or 60 cycles of data synchronized to the incoming voltage signal. In addition, a sample counter keeps track of how many samples accumulate over this frame period. This count can vary as the software synchronizes with the incoming mains frequency.

The processed dot products include the V_{RMS}, I_{RMS}, active power, and reactive power. These dot products are used by the foreground process to calculate the corresponding metrology readings in real-world units. Processed voltage dot products, current dot products, active energy dot products, and reactive energy dot products are accumulated in separate 64-bit registers to further process and obtain the RMS and mean values. Using the calculated values of active and reactive power of the foreground process, the apparent power is calculated. The frequency (in Hz) and power factor are also calculated using parameters calculated by the background process using the formulas in 节 2.3.2.2.1.

For the two-voltage configuration, there are two voltage-current mappings, where each voltage-to-current mapping has a different voltage and current channel. Specifically, in the two-voltage mapping, the line-to-neutral voltage measurement for line A and the line A current measurement are associated with each other for one mapping and the line-to-neutral voltage measurement for line B and the line B current measurement are associated with each other for the other mapping. Otherwise, for the one-voltage configuration, each voltage-current mapping has the same voltage for each mapping since only one voltage is measured. In the one-voltage configuration, the line-to-line voltage measurement is associated with the line A current for the first mapping and the same line-to-line voltage measurement is associated with the line B current for the second mapping. For simplicity, note that each voltage-to-current mapping, whether for two-voltage or one-voltage configurations, is referred to as a phase in the rest of this documentation as well as in the PC GUI.

The foreground process also updates the LCD. The LCD display item is changed every two seconds. See 节 3.2.1.3.1 for more information about the different items displayed on the LCD.

In addition, the foreground process also takes action if the $\overline{FLT}$ pin of the TPS25921L device has been asserted low, which would indicate an undervoltage, overvoltage, or thermal shutdown event has occurred. If the $\overline{FLT}$ pin has been asserted low and it is the first time this has happened since the MSP432 MCU has been reset, the MSP432 MCU provides a pulse on the EN/UVLO pin of the TPS25921L device to reset the device. This reset pulse is meant to reconnect the load at the TPS25921L OUT pin with the source at its IN pin since this would be disconnected if the fault source was from a thermal shutdown event. After resetting the TPS25921L, if another thermal shutdown event occurs, the TPS25921L output is disconnected from the input again and the MSP432 MCU does not make any further attempts to provide a reset pulse to the TPS25921L to reconnect the output to the input rail.

2.3.2.2.1 Formulae

This section briefly describes the formulas used for the voltage, current, power, and energy calculations. As previously described, voltage and current samples are obtained at a sampling rate of 8000 Hz. All of the samples that are taken in approximately one second frames are kept and used to obtain the RMS values for voltage and current for each phase. The RMS values are obtained with the following formulas:

$$V_{RMS,ph} = K_{v,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample Count}} v_{ph}(n) \times v_{ph}(n)}{\text{Sample Count}}} - v_{offset,ph} \quad (3)$$

$$I_{RMS,ph} = K_{i,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample Count}} i_{ph}(n) \times i_{ph}(n)}{\text{Sample Count}}} - i_{offset,ph}$$

where

- ph = Phase parameters that are being calculated [that is, Phase A (= 1) or B (= 2)]
- $V_{ph}(n)$ = Voltage sample at a sample instant n
- $V_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the voltage converter
- $I_{ph}(n)$ = Each current sample at a sample instant n
- $I_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the current converter
- Sample count = Number of samples within the present frame
- $K_{v,ph}$ = Scaling factor for voltage
- $K_{i,ph}$ = Scaling factor for current (4)

Power and energy are calculated for active and reactive energy samples of one frame. These samples are phase-corrected and passed on to the foreground process, which uses the number of samples (sample count) to calculate phase active and reactive powers through the following formulas:

$$P_{ACT,ph} = K_{ACT,ph} \frac{\sum_{n=1}^{\text{Sample Count}} v_{ph}(n) \times i_{ph}(n)}{\text{Sample Count}} - P_{ACT\_Offset,ph} \quad (5)$$

$$P_{REACT,ph} = K_{REACT,ph} \frac{\sum_{n=1}^{\text{Sample Count}} V_{90,ph}(n) \times i_{ph}(n)}{\text{Sample Count}} - P_{React\_Offset,ph} \quad (6)$$

$$P_{APP,ph} = \sqrt{P_{ACT,ph}^{2} + P_{REACT,ph}^{2}}$$

where

- $V_{90}(n)$ = Voltage sample at a sample instant ‘n’ shifted by 90°
- $K_{ACT,ph}$ = Scaling factor for active power
- $K_{REACT,ph}$ = Scaling factor for reactive power
- $P_{ACT\_offset,ph}$ = Offset used to subtract effects of crosstalk on the active power measurements from other phases and the neutral
- $P_{REACT\_offset,ph}$ = Offset used to subtract effects of crosstalk on the reactive power measurements from other phases and the neutral (7)

Note that for reactive energy, the 90° phase shift approach is used for two reasons:

1. This approach allows accurate measurement of the reactive power for very small currents
2. This approach conforms to the measurement method specified by IEC and ANSI standards

The calculated mains frequency is used to calculate the 90 degrees-shifted voltage sample. Because the frequency of the mains varies, the mains frequency is first measured accurately to phase shift the voltage samples accordingly.

To get an exact 90° phase shift, interpolation is used between two samples. For these two samples, a voltage sample slightly more than 90 degrees before the current sample and a voltage sample slightly less than 90 degrees before the current sample are used. The phase shift implementation of the application consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap FIR filter. In the test software, a lookup table provides the filter coefficients that are used to create the fractional delays.

In addition to calculating the per-phase active and reactive powers, the cumulative sum of these parameters are also calculated using 公式 8, 公式 9, and 公式 10:

$$P_{ACT,Cumulative} = \sum_{ph=1}^{2} P_{ACT,ph} \quad (8)$$

$$P_{REACT,Cumulative} = \sum_{ph=1}^{2} P_{REACT,ph} \quad (9)$$

$$P_{APP,Cumulative} = \sum_{ph=1}^{2} P_{APP,ph} \quad (10)$$

Using the calculated powers, energies are calculated with the following formulas in 公式 11:

$$E_{ACT,ph} = P_{ACT,ph} \times Samplecount$$
$$E_{REACT,ph} = P_{REACT,ph} \times Samplecount$$
$$E_{APP,ph} = P_{APP,ph} \times Samplecount \quad (11)$$

From there, the energies are also accumulated to calculate the cumulative energies, by the following 公式 12, 公式 13, and 公式 14:

$$E_{ACT,Cumulative} = \sum_{ph=1}^{2} E_{ACT,ph} \quad (12)$$

$$E_{REACT,Cumulative} = \sum_{ph=1}^{2} E_{REACT,ph} \quad (13)$$

$$E_{APP,Cumulative} = \sum_{ph=1}^{2} E_{APP,ph} \quad (14)$$

The calculated energies are then accumulated into buffers that store the total amount of energy consumed since system reset. Note that these energies are different from the working variables used to accumulate energy for outputting energy pulses. There are four sets of buffers that are available: one for each phase and one for the cumulative of the phases. Within each set of buffers, the following energies are accumulated:

1. Active import energy (active energy when active energy ≥ 0)
2. Active export energy (active energy when active energy < 0)
3. React. Quad I energy (reactive energy when reactive energy ≥ 0 and active power ≥ 0; inductive load)
4. React. Quad II energy (reactive energy when reactive energy ≥ 0 and active power < 0; capacitive generator)
5. React. Quad III energy (reactive energy when reactive energy < 0 and active power < 0; inductive

generator)

6. React. Quad IV energy (reactive energy when reactive energy < 0 and active power ≥ 0; capacitive load)
7. App. import energy (apparent energy when active energy ≥ 0)
8. App. export energy (apparent energy when active energy < 0)

The background process also calculates the frequency in terms of samples-per-mains cycle. The foreground process then converts this samples-per-mains cycle to Hertz with 公式 15:

$$\text{Frequency (Hz)} = \frac{\text{Sample Rate (samples / second)}}{\text{Frequency (samples / cycle)}} \tag{15}$$

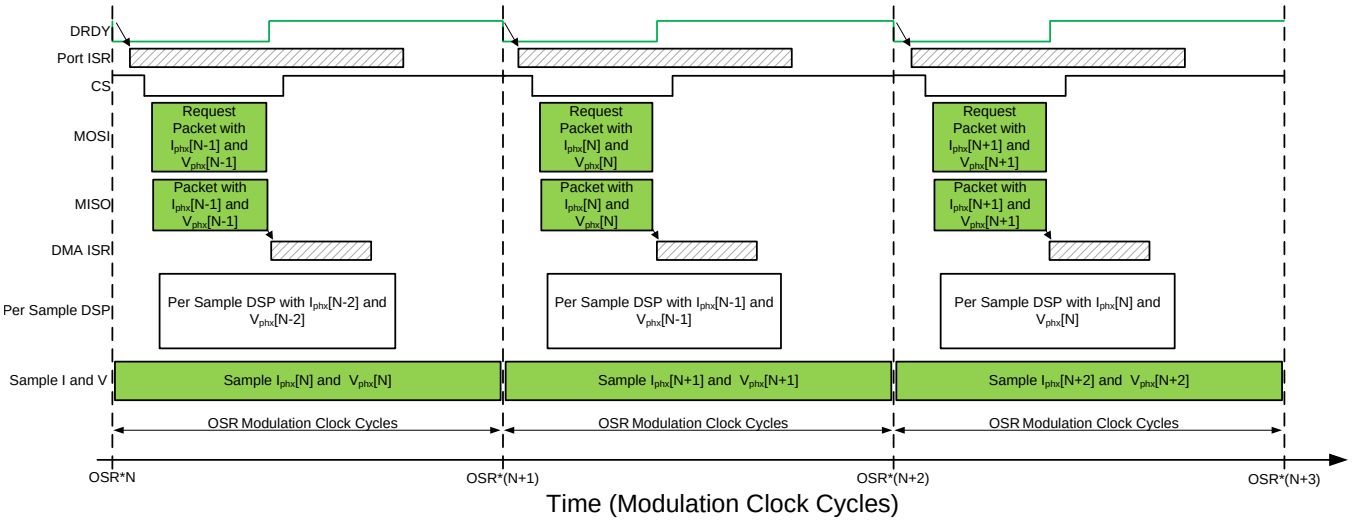
After the active power and apparent power have been calculated, the absolute value of the power factor is calculated. In the internal representation of power factor of the system, a positive power factor corresponds to a capacitive load; a negative power factor corresponds to an inductive load. The sign of the internal representation of power factor is determined by whether the current leads or lags voltage, which is determined in the background process. Therefore, the internal representation of power factor is calculated with 公式 16:

$$\text{Internal Representation of Power Factor} = \begin{cases} \dfrac{P_{Act}}{P_{Apparent}}, \text{ if capacitive load} \\ -\dfrac{P_{Act}}{P_{Apparent}}, \text{ if inductive load} \end{cases} \tag{16}$$

2.3.2.3 Background Process

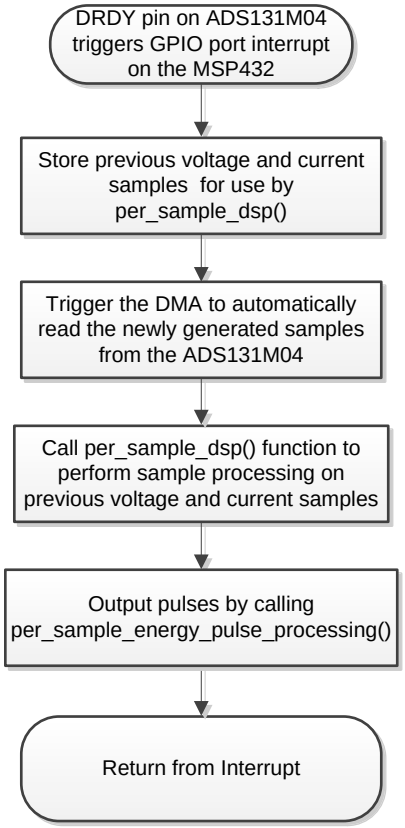
图 10 shows the different events that occur when sampling voltage and current, where the items in olive green are done by the hardware settings and not the test software.

图 10. Voltage and Current Sampling Events



To go over the process mentioned in 图 10, new current samples for each phase are ready every OSR, or 512 for this design, modulation clock cycles. Suppose the most recently ready phase current and voltage samples from the ADS131M04 device corresponds to the N^{th} – 1 current and voltage sample, or $I_{phx}[N - 1]$ and $V_{phx}[N - 1]$. Once new samples are ready, the $\overline{DRDY}$ pin is asserted low by the ADS131M04. The falling edge on the $\overline{DRDY}$ pin on the ADS131M04 causes a GPIO port interrupt on the MSP432 MCU, which triggers the Port ISR on the MSP432 MCU. The background process is run within the Port ISR. 图 11 shows the background process, which mainly deals with timing critical events in the test software.

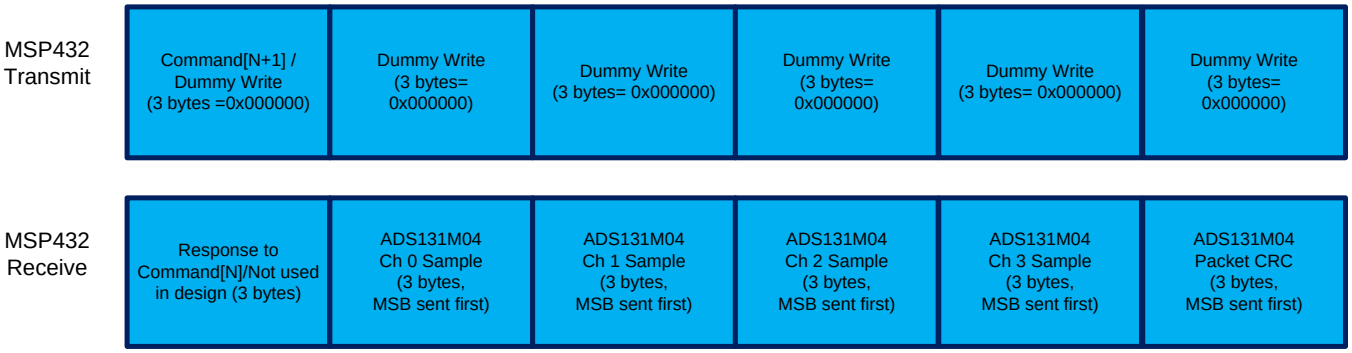
图 11. Background Process



In the background process, the previously-obtained voltage samples ($V_{phx}[N – 2]$) and previously obtained current samples ($I_{phx}[N – 2]$) are stored so that they can be used later by the per_sample_dsp function, which is responsible for updating the intermediate dot product quantities used to calculate metrology parameters. After the previously obtained voltage and current samples are stored, communication to the ADS131M04 is enabled by asserting the chip select signal low. The DMA is then configured to both send a request for the newest current and voltage samples ($I_{phx}[N – 1]$ and $V_{phx}[N – 1]$) of the ADS131M04 device and also to receive the data packet response from the ADS131M04. The request and reception of the current samples is done automatically by the DMA module instead of it being done by the software.

图 12 shows the packet that is transmitted by the DMA of the MSP432 MCU and the response packet from the ADS131M04 that is received and assembled by the DMA as well. The transmission and reception packets contain six words, where each word is three bytes long.

图 12. ADS131M04 ADC Sample Request Packet



When requesting the ADC data from the ADS131M04 device, the first word that has to be sent to the ADS131M04 is the command word. Since the test software does not need to change the settings of the ADS131M04 or read any registers during typical ADC sample readouts, a NULL command is sent to the ADS131M04, which allows you to get the ADC samples from the ADS131M04 without changing the state of the device. The actual size of the null command is 16-bits; however, since 24-bit words are used, the 16-bit command must be padded with an extra value of 0x00 at the end of the command. The NULL command word sent therefore has a value of 0x000000. While the MSP432 MCU is shifting out the command word, the MSP432 is simultaneously shifting in the response word to the command word of the previous packet. The response word to a NULL command is the contents of the STATUS register. The contents of the STATUS register is not used in this design so the first word received from the ADS131M04 is ignored.

After writing the command word, it is necessary for a dummy write to be performed for each byte that is to be read. The dummy byte write is necessary to enable the SPI clock, which is necessary to read a byte from the ADS131M04 device. For each dummy byte write, a value of 0x00 is written to the SPI transmit register for EUSCIB0. Immediately after writing the command byte, writing three dummy bytes allows the MSP432 MCU to receive the 3-byte ADC value from channel 0 of the ADS131M04. Writing the next nine dummy bytes gets the ADC data for channel 1, channel 2, and channel 3, respectively. Finally, writing the next three dummy bytes gets the CRC word. The CRC word is 24-bits; however, note that the actual CRC is only 16-bits, which are placed in the most significant bits of the 24-bit word. As a result, when parsing the CRC word, the last byte is not needed (note though that the dummy write for this zero-padded byte must still be sent though for proper ADS131M04 operation).

图 12 shows that whenever the DMA has received the entire $I_{phx}[N - 1]$ packet, the DMA ISR is automatically called. Within the ISR, the CRC is calculated over the five command and ADC words (15 bytes in total). This CRC calculation uses the CRC module of the MSP432 MCU. Since the CRC module works with an even number of bytes but there are a total of 15 bytes available, the CRC module is used for the first 14 bytes. The final CRC is calculated in software from the CRC module result and the 15th byte. Note that the software CRC calculation on the last byte is only necessary because the word size was selected to be three bytes in this design. If the word size was selected to be two bytes or four bytes instead, the software CRC calculation would not be needed since there would be an even number of bytes. 图 13 shows the code snippet for calculating the CRC over 15 bytes by using the MSP432 CRC module and software.

图 13. Code Snippet for Using the CRC Module of the MSP432 MCU for Calculating CRC Over an Odd Number of Bytes

```
CRC32->INIRES16 = 0xFFFF;                // Init CRC16 HW module
for(i=0; i<CRC_BYTE_START/2; i++) //This for loop uses the MSP432's CRC module for calculating CRC for first 14 bytes of packet
{

    CRC32->DIRB16 = (((uint16_t )packet[i<<1])<<8) | packet[(i<<1) +1];
    __no_operation();
}
CRC16_Result = (unsigned char) (CRC32->INIRES16 >> 8) | (CRC32->INIRES16 << 8); //Stores CRC result for first 14 bytes from CRC module
CRC16_Result ^= packet[CRC_BYTE_START-1]; //packet[CRC_BYTE_START-1] is the last (15th byte) not used by the CRC module's calculation
CRC16_Result ^= (unsigned char) (CRC16_Result & 0xFF) >> 4;
CRC16_Result ^= (CRC16_Result << 8) << 4;
CRC16_Result ^= ((CRC16_Result & 0xFF) << 4) << 1; //The final CRC result over 15 bytes is now stored in CRC16_Result after this line executes.
```

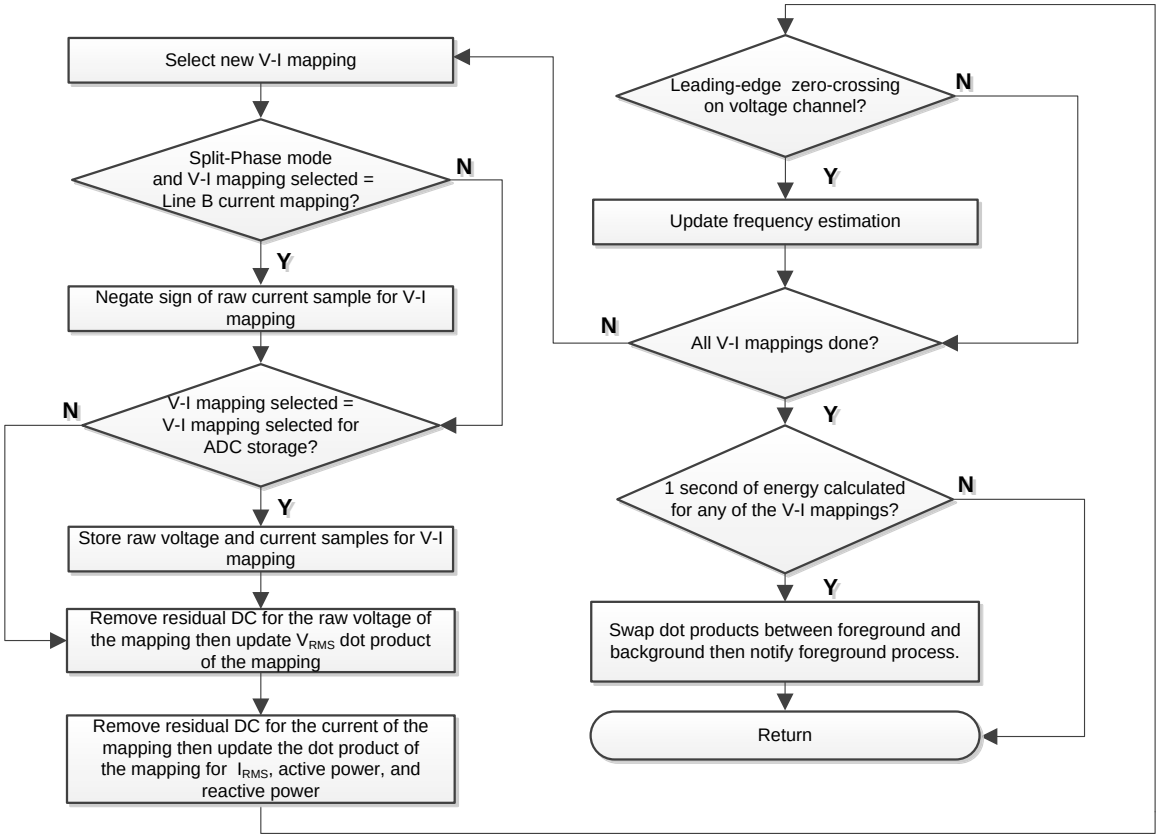
Once the CRC has been calculated over the packet, it is compared to the CRC obtained in the packet sent from the ADS131M04. The sent CRC is parsed from bytes 16 and 17 of the ADS131M04 packet (byte 18, which is part of the CRC word, is zero-padded so it is not used in parsing). If the calculated CRC and the parsed CRC are equal, then the CRC check passes and the ADC data is parsed to get the values of the voltage and current samples at time N – 1. The parsed voltage and current samples are put in temporary buffers so that they are used the next time the per_sample_dsp function is called at the next interrupt. Before the DMA interrupt ends, the chip select line is pulled back high again to properly reset the ADS131M04 communication before the next time current samples are ready from the ADS131M04.

In parallel to receiving the newest current samples from the ADS131M04 using the DMA, the ADS131M04 is currently sampling the next voltage ($V_{phx}[N]$) and current samples ($I_{phx}[N]$) and the test software also performs per-sample processing on the last voltage ($V_{phx}[N – 2]$) and current samples ($I_{phx}[N – 2]$) obtained from the ADS131M04. This per-sample processing is used to update the intermediate dot product quantities that are used to calculate the metrology parameters. After sample processing, the background process uses the "per_sample_energy_pulse_processing" for the calculation and output of energy-proportional pulses. Once the per_sample_energy_pulse_processing is completed, the test software exits from the port ISR.

2.3.2.3.1 per_sample_dsp()

图 14 shows the flowchart for the per_sample_dsp() function. The per_sample_dsp() function is used to calculate intermediate dot product results that are fed into the foreground process for the calculation of metrology readings. Both voltage and current samples are processed and accumulated in dedicated 64-bit registers. Per-phase active power and reactive power are also accumulated in 64-bit registers.

图 14. per_sample_dsp Function



After sufficient samples (of approximately one second) are accumulated, the foreground function is triggered to calculate the final values of V_{RMS}; I_{RMS}; active, reactive, and apparent powers; active, reactive, and apparent energy; frequency; and power factor. In the test software, there are two sets of dot products for a phase: at any given time, one is used by the foreground for calculation and the other used as the working set by the background. After the background process has sufficient samples, it swaps the two dot products so that the foreground uses the newly acquired dot products that the background process just calculated and the background process uses a new empty set to calculate the next set of dot products. Whenever there is a leading-edge zero-crossing (− to + voltage transition) on a voltage channel, the per_sample_dsp() function is also responsible for updating the corresponding frequency (in samples per cycle) of the phase.

The following sections describe the various elements of electricity measurement in the per_sample_dsp() function.

2.3.2.3.1.1 Voltage and Current Signals

For a one-voltage configuration, reverse the orientation for the line B current measurement with respect to the line-to-line voltage measurement for the power readings to have the proper sign. Instead of reversing the CT connections to switch the orientation of the line B current measurement, line B raw current samples are negated for the one-voltage configuration, which allows switching between two-voltage configuration and one-voltage configurations in software without having to rewire the CT to board connections. The test software of the design has support for storing the raw voltage and current ADC values for phase A or phase B, regardless if the one-voltage configuration or two-voltage configuration is selected.

The raw ADS131M04 samples are signed integers and any stray DC or offset value on these converters are removed using a DC tracking filter. A separate DC estimate for all voltages and currents is obtained using the filter, voltage, and current samples, respectively. This estimate is then subtracted from each voltage and current raw ADC sample.

The resulting instantaneous voltage and current samples are used to generate the following intermediate results:

- Accumulated squared values of voltages and currents, which is used for V_{RMS} and I_{RMS} calculations, respectively
- Accumulated energy samples to calculate active energy
- Accumulated energy samples using current and 90° phase-shifted voltage to calculate reactive energy

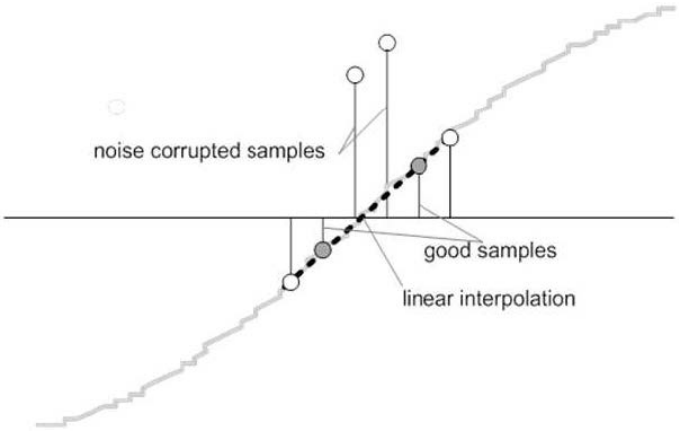
The foreground process processes these accumulated values.

2.3.2.3.1.2 Frequency Measurement and Cycle Tracking

The instantaneous voltages, currents, active powers, and reactive powers are accumulated in 64-bit registers. A cycle tracking counter and sample counter keep track of the number of samples accumulated. When samples of approximately one second have been accumulated, the background process stores these accumulation registers and notifies the foreground process to produce the average results, such as RMS and power values. Cycle boundaries are used to trigger the foreground averaging process because this process produces very stable results.

For frequency measurements, a straight line interpolation is used between the zero crossing voltage samples. 图 15 shows the samples near a zero cross and the process of linear interpolation.

图 15. Frequency Measurement



Because noise spikes can also cause errors, the application uses a rate-of-change check to filter out the possible erroneous signals and make sure that the two points are interpolated from genuine zero crossing points. For example, with two negative samples, a noise spike can make one of the samples positive, thereby making the negative and positive pair appear as if there is a zero crossing.

The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out any cycle-to-cycle variations. This filtering results in a stable and accurate frequency measurement that is tolerant of noise.

2.3.2.3.2 LED Pulse Generation

In electricity meters, the energy consumption of the load is normally measured in a fraction of kilowatt-hour (kWh) pulses. This information can be used to accurately calibrate any meter for accuracy measurement. Typically, the measuring element (the MSP432 microcontroller) is responsible for generating pulses proportional to the energy consumed. To serve both these tasks efficiently, the pulse generation must be accurate with relatively little jitter. Although time jitters are not an indication of bad accuracy, time jitters give a negative indication of the overall accuracy of the meter. The jitter must be averaged out due to this negative indication of accuracy.

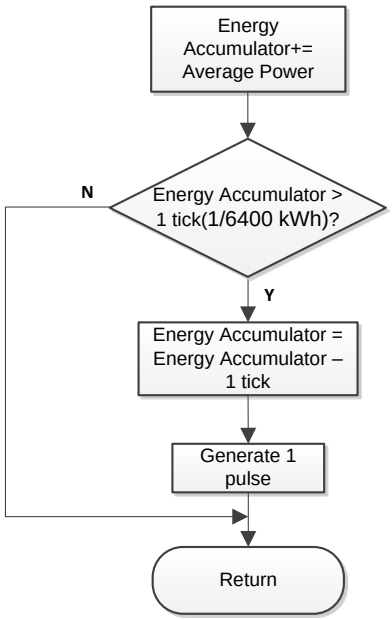
This application uses average power to generate these energy pulses. The average power accumulates at every $\overline{\text{DRDY}}$ port ISR interrupt, thereby spreading the accumulated energy from the previous one-second time frame evenly for each interrupt in the current one-second time frame. This accumulation process is equivalent to converting power to energy. When the accumulated energy crosses a threshold, a pulse is generated. The amount of energy above this threshold is kept and a new energy value is added on top of the threshold in the next interrupt cycle. Because the average power tends to be a stable value, this way of generating energy pulses is very steady and free of jitter.

The threshold determines the energy "tick" specified by meter manufacturers and is a constant. The tick is usually defined in pulses-per-kWh or just in kWh. One pulse must be generated for every energy tick. For example, in this application, the number of pulses generated per kWh is set to 6400 for active and reactive energies. The energy tick in this case is 1 kWh / 6400. Energy pulses are generated and available on a header and also through light-emitting diodes (LEDs) on the board. GPIO pins are used to produce the pulses.

In the reference design, the LED that is labeled "Active" corresponds to the active energy consumption for the two-phase sum. "Reactive" corresponds to the cumulative two-phase reactive energy sum.

图 16 shows the flow diagram for pulse generation.

图 16. Pulse Generation for Energy Indication



The average power is in units of 0.001 W and a 1-kWh threshold is defined as:

1-kWh threshold = 1 / 0.001 × 1 kW × (Number of interrupts per sec) × (Number of seconds in one hour) = 1000000 × 8000 × 3600 = 0x1A3185C50000

2.3.2.3.3 Phase Compensation

When a current transformer (CT) is used as a sensor, it introduces additional phase shift on the current signals. Also, the passive components of the voltage and current input circuit may introduce another phase shift. The user must compensate the relative phase shift between voltage and current samples to ensure accurate measurements. The implementation of the phase shift compensation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap finite impulse response (FIR) filter that interpolates between two samples, similar to the FIR filter used for providing 90°-shifted voltage samples for reactive energy measurements. In the test software, a lookup table provides the filter coefficients that are used to create the fractional delays. The lookup table provides fractional phase shifts as small as 1/256th of a sample. The 8000-Hz sample rate used in this application corresponds to a 0.0088° degree resolution at 50 Hz. In addition to the filter coefficients, the lookup table also has an associated gain variable for each set of filter coefficients. This gain variable is used to cancel out the resulting gain from using a certain set of filter coefficients.

An alternative option to the software phase compensation used in this design is to use the phase compensation feature on the ADS131M04 device. If this hardware phase compensation scheme is used, filter coefficients are not necessary so it is not needed to divide by the gain of the filter coefficients.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Cautions and Warnings

At high currents, the terminal block can get warm. In addition, note that the phase voltages are fed to the board so take the proper precautions.

WARNING

Hot Surface! Contact can cause burns. Do not touch. Take the proper precautions when operating.

CAUTION

High Voltage! Electric shocks are possible when connecting the board to live wires. The board must be handled with care by a professional. For safety, use of isolated test equipment with overvoltage or overcurrent protection is highly recommended.

3.1.2 Hardware

The following figures of the reference design best describe the hardware: 图 17 is the top view of the energy measurement system, and 图 18 shows the location of various pieces of the reference design based on functionality.

图 17. Top View of TIDA-010037 Design

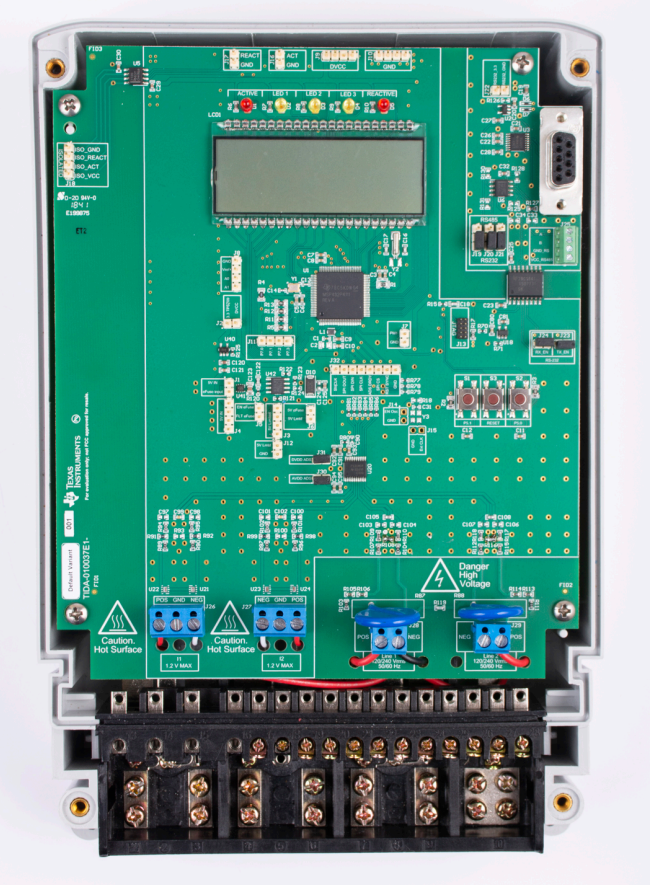
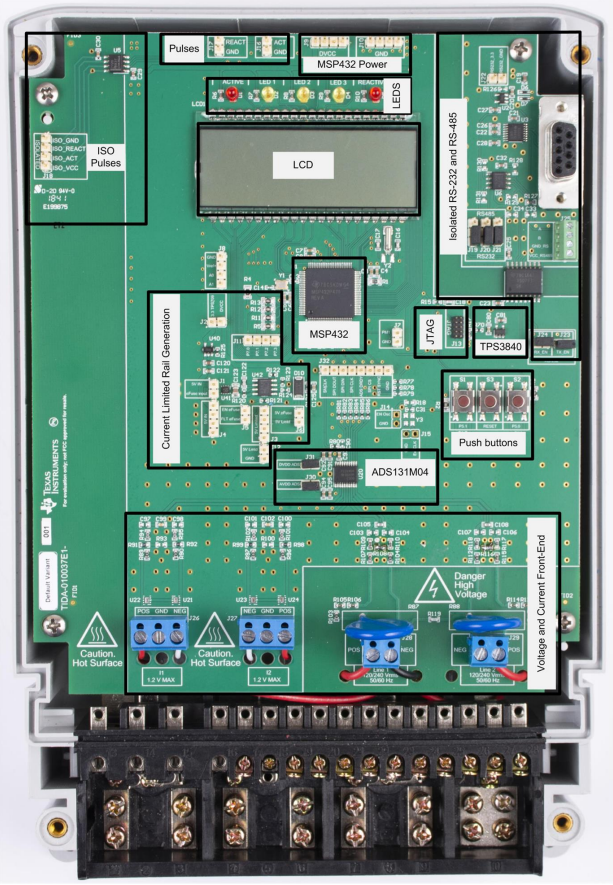


图 18. Top View of TIDA-010037 Design With Components Highlighted



The design has support for two-voltage and one-voltage configurations. The hardware connections depend on which of these two configurations is selected.

3.1.2.1 Connections to the Test Setup

3.1.2.1.1 Two-Voltage Connections

AC voltages and currents can be applied to the board for testing purposes at these points:

- Terminal block "J28" corresponds to the line voltage connection for phase A. This terminal block is a two-position terminal block that has connections for phase A line voltage as well as the neutral. The terminal block position on the left, which is labeled "POS", is where the line connection for phase A is made. The terminal block position on the right, which is labeled "NEG", is where the neutral connection is made. The neutral connection at this terminal block cover is shorted with the neutral connection on "J29" so the neutral only needs to be connected to one of these two positions. Note that the order of the phase line and neutral is reversed here compared to the order on J29.
- Terminal block "J29" corresponds to the line voltage connection for phase B. This terminal block is a

two-position terminal block that has connections for phase B line voltage as well as the neutral. The terminal block position on the right, which is labeled "POS", is where the line connection for phase A is made. The terminal block position on the left, which is labeled "NEG", is where the neutral connection is made. The neutral connection at this terminal block cover is shorted with the neutral connection on "J28" so the neutral only needs to be connected to one of these two positions. Note that the order of the phase line input and neutral is reversed here compared to the order on J28.

- Terminal block "J26" corresponds to the current inputs after the sensors for phase A. This terminal block is a three-position terminal block but only the leftmost and rightmost positions are used. The center position, which is connected to GND, is not connected to the CT. The terminal block position on the most left, which is labeled "POS", is where the positive terminal of the CT should be connected. The terminal block position on the most right, which is labeled "NEG", is where the negative terminal of the CT should be connected. Select the applied current to the input of the CT so that it does not exceed 100 A. **In addition, before performing any test, verify that this terminal block is securely connected to both output leads of the CT.** Note that the order of the CT leads is reversed here compared to the order on "J27".
- Terminal block "J27" corresponds to the current inputs after the sensors for phase B. This terminal block is a three-position terminal block but only the leftmost and rightmost positions are used. The center position, which is connected to GND, is not connected to the CT. The terminal block position on the most right, which is labeled "POS", is where the positive terminal of the CT should be connected. The terminal block position on the most left, which is labeled "NEG", is where the negative terminal of the CT should be connected. Select the applied current to the input of the CT so that it does not exceed 100 A. **In addition, before performing any test, verify that this terminal block is securely connected to both output leads of the CT**. Note that the order of the CT leads is reversed here compared to the order on "J26".

图 19 and 图 20 show the various test setup connections required for the reference design to function properly for the two-voltage configuration.

图 19. Top View of Reference Design With Test Setup Connections, Two-Voltage Configuration

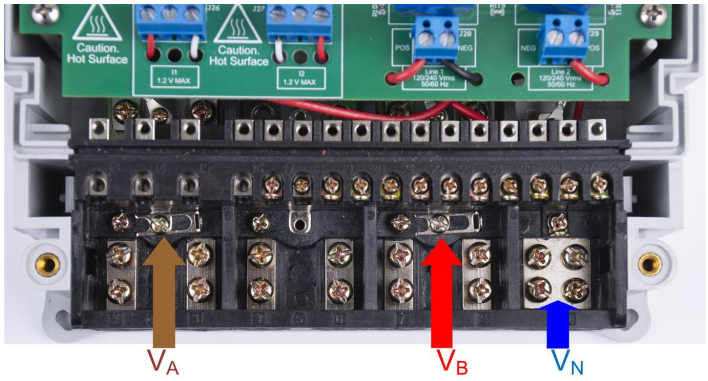


图 20 shows the connections from the front view. V_A and V_B, correspond to the lines for phases A and B. V_N corresponds to the neutral voltage from the test AC source. I_A+ and I_A− correspond to the current inputs for phase A while I_B+, and I_B− correspond to the current inputs for phase B.

图 20. Front View of Reference Design With Test Setup Connections, Two-Voltage Configuration

3.1.2.1.2 One-Voltage Connections

AC voltages and currents can be applied to the board for testing purposes at these points:

- Terminal block "J28" corresponds to the line voltage connection. This terminal block is a two-position terminal block that has connections for line A and line B. The terminal block position on the left, which is labeled "POS", is where line A is connected. The terminal block position on the right, which is labeled "NEG", is where line B is connected.
- Terminal block "J29" does not need to be used for this one-voltage configuration.
- Terminal block "J26" corresponds to the current inputs after the sensors for line A. This terminal block is a three-position terminal block but only the leftmost and rightmost positions are used. The center position, which is connected to GND, is not connected to the CT. Connect the positive terminal of the CT to the terminal block position on the most left, which is labeled "POS". Connect the negative terminal of the CT to the terminal block position on the most right, which is labeled "NEG". Select the applied current to the input of the CT so that it does not exceed 100 A. **In addition, before performing any test, verify that this terminal block is securely connected to both output leads of the CT.** Note that the order of the CT leads is reversed here compared to the order on "J27".
- Terminal block "J27" corresponds to the current inputs after the sensors for line B. This terminal block is a three-position terminal block but only the leftmost and rightmost positions are used. The center position, which is connected to GND, is not connected to the CT. The terminal block position on the most right, which is labeled "POS", is where the positive terminal of the CT should be connected. Connect the negative terminal of the CT to the terminal block position on the most left, which is labeled "NEG". Select the applied current to the input of the CT so that it does not exceed 100 A. **In addition, before performing any test, verify that this terminal block is securely connected to both output leads of the CT.** Note that the order of the CT leads is reversed here compared to the order on "J26".

图 21 and 图 22 show the various test setup connections required for the reference design to function properly for the one-voltage configuration.

图 21. Top View of Reference Design With Test Setup Connections, One-Voltage Configuration

图 22 shows the connections from the front view. V_A and V_B correspond to line A and line B. I_A+ and I_A− correspond to the current inputs for line A while I_B+, and I_B− correspond to the current inputs for line B.

图 22. Front View of Reference Design With Test Setup Connections, One-Voltage Configuration

3.1.2.2 Power Supply Options and Jumper Settings

The MSP432 MCU and ADS131M04 portion of this design is powered from a single voltage rail (DVCC), which can be derived from two potential methods. In the first method, DVCC can be powered directly by connecting a 3.3-V external power supply at the DVCC header J9 and GND. To support this direct way of driving DVCC, a jumper should not be placed on jumper header J2.

In the second method of driving DVCC, the DVCC voltage is produced from the 3.3-V output of a TPS70933 LDO. In this second method, place a jumper at jumper header J2 and apply 5 V between J4 and GND to provide the necessary input voltage to the TPS70933. If a jumper is placed both at jumper headers J1 and J2, the 5-V rail applied at header J4 is used to power DVCC as well as the current-limited rail produced by the TPS25921L.

Various jumper headers and jumper settings are present to add to the flexibility to the board. Some of these headers require that jumpers be placed appropriately for the board to correctly function. 表 2 indicates the functionality of each jumper on the board.

注: The headers with **(WARNING)** text in the *MAIN FUNCTIONALITY* column are not isolated, so measuring equipment should not be used there (especially for the one-voltage configuration, which has the system ground connected to a line voltage) when running off the Mains. This applies, unless either isolators external to the board of the design are used to connect at the headers, if the equipment is battery powered and does not connect to Mains, or if AC mains is isolated.

表 2. Header Names and Jumper Settings

HEADER OR HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
J1	2-pin jumper header	TPS25921L input rail selection **(WARNING)**	Place a jumper at this header to use the voltage applied at the J4 header as the TPS2591L input voltage. A current-limited version of this input voltage is provided at the output of the TPS25921L. To use a different voltage than what is applied at J4, apply an external voltage at this header and do not place a jumper here.	If a jumper is placed at J1 and another jumper is at J2, the TPS25921L input voltage and DVCC is supplied from the same source (header J4) so only one external power supply is necessary. If it is desired to use a separate power supply for DVCC and the TPS25921L, then the jumper at J1 can be removed and the desired TPS25921L can be applied directly at pin 2 of the J1 header. Alternatively, instead of removing the jumper at J1, the jumper at J2 can be removed and 3.3 V can be applied directly at the DVCC header instead of using the voltage at the J4 header and the TPS70933 LDO to generate the 3.3-V rail for DVCC.
J2	2-pin jumper header	TPS70933 DVCC output selection **(WARNING)**	Place a jumper at this header to generate the 3.3-V rail for DVCC from the TPS70933 LDO and the voltage applied at J4. Apply 3.3 V directly at the DVCC header J9 and do not place a jumper here to bypass using the TPS70933.	If a jumper is placed at J1 and another jumper is at J2, the TPS25921L input voltage and DVCC is supplied from the same source (header J4) so only one external power supply is necessary. If it is desired to use a separate power supply for DVCC and the TPS25921L, then the jumper at J1 can be removed and the desired TPS25921L can be applied directly at pin 2 of the J1 header. Alternatively, instead of removing the jumper at J1, the jumper at J2 can be removed and 3.3 V can be applied directly at the DVCC header instead of using the voltage at the J4 header and the TPS70933 LDO to generate the 3.3-V rail for DVCC.
J3	4-pin header	Current-limited, 5-V rail **(WARNING)**	Connect this header and GND to any radios or radio modules that you want to current-limit.	If a jumper is placed at J1, this is the current-limited version of the voltage applied at header J4. This current-limited voltage also appears at pin 1 of header J12.
J4	4-pin header	5-V input **(WARNING)**	Apply 5 V between here and GND to create the 5-V current-limited output at J3 and to create a 3.3-V output that can be connected to DVCC.	To create the current-limited output at J3 from J4, place a jumper at J1. To create the 3.3 V at DVCC from J4, place a jumper at J2.
J5	2-pin header	Header connected to TPS25921 FLTb, and EN/UVLO pins **(WARNING)**	Probe at pin 2 of this header to determine if the TPS25921L has asserted its fault flag. Probe at pin 1 for the state of the EN/UVLO pin of the TPS25921L.	During a TPS25921L thermal shutdown event, the load connected to the out pin of the TPS25921L is disconnected from the source connected to the VIN pin. As a result, header J3 will not anymore be a current-limited version of the voltage applied to J4. The EN/UVLO can be driven low by the microcontroller to try to reconnect the source of the TPS25921L device at its input pin to the load at its output pin. In the test software, a maximum of one retry attempt is made after a thermal shutdown event.
J6	2-pin jumper header	TPS25921L output connection **(WARNING)**	Place a jumper here to connect the TPS25921L out pin to header J3, thereby creating a current-limited version of the rail applied at the VIN pin of the TPS2591L device.	Place a jumper here.

表 2. Header Names and Jumper Settings (continued)

HEADER OR HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
J7	2-pin header	THVD1500 RE and DE pin **(WARNING)**	Probe at this header to view the signal fed to the RE and DE pins of the THVD1500 device, which determines when the receiver or driver is enabled.	This header has two pins: GND and PM1, where PM1 is the P2.7 GPIO pin of the MSP432 MCU that drives the RE and DE pins of the THVD1500 device.
J8	4-pin header	MSP432 ADC14 and reference header **(WARNING)**	Probe here to provide inputs to ADC channels A0 and A1 as well as the ADC14 reference input.	The test software does not use this header. This header is added if it is desired to add custom sensing code with the 14-bit SAR ADC of the MSP432 MCU.
J9	4-pin header	DVCC voltage header **(WARNING)**	Probe here for DVCC voltage. Connect the positive terminal of the bench or external power supply when powering the board externally directly through DVCC instead of using the TPS70933 LDO.	If DVCC is powered from the TPS70933 LDO (jumper is placed at header J2), probe between here and J10 to measure the output voltage from the TPS70933. If DVCC is powered externally directly (remove the jumper from header J2), 3.3 V must be applied between here and J10.
J10	4-pin header	Ground voltage header **(WARNING)**	Probe here for GND voltage. Connect negative terminal of bench or external power supply when powering the board externally directly through DVCC instead of using the TPS70933 LDO.	If DVCC is powered from the TPS70933 LDO (jumper is placed at header J2), probe between here and J9 to measure the output voltage from the TPS70933. If DVCC is powered externally directly (remove the jumper from header J2), 3.3 V must be applied between J9 and this header.
J11	4-pin header	Header containing MSP432 P7.0, 7.1, P7.2, and P7.3 pins **(WARNING)**	Probe here for P7.0, P7.1, P7.2, and P7.3 GPIO pins.	The P7.0, P7.1, and P7.2 pins are used for adjusting contrast of the LCD. P7.3 is not used in this design. These pins are all port mappable. If the LCD is not needed, it can be disabled in software and R5, R11, R12, and R13 can be removed so that P7.0, P7.1, and P7.2 can be port mapped for other purposes such as potentially communicating to an external radio or radio module. If these pins are used for communicating to an external radio or radio module, header J12 can be used for powering these external modules and current limiting the power to them so that if there are any external shorts it does not affect powering the metrology.
J12	2-pin header	Current-limited rail **(WARNING)**	Connect this header to an external module to provide a current-limited 5-V rail to an external module.	Pin 1 of this header is the current-limited output rail from the TPS25921L, which is also available at header J3. Pin 2 of this header is the GND connection. For a 5-V, current-limited voltage to appear here, apply 5 V at header J4, and place jumpers on J1 and J6.
J13	10-pin 2-row connector	JTAG: MSP432 programming header **(WARNING)**	Connect the MSP-FET- 432ADPTR adapter to this connector to power the MSP432 MCU.	The MSP-FET-432ADPTR is used to allow the MSP-FET tool to program the MSP432 device. One connector of the MSP-FET-432ADPTR adapter connects to the FET tool and the other connector connects to the JTAG connector of the MSP432 MCU. Note that the MSP432 has to be powered externally to program the MSP432 MCU. Since this header and the FET tool is not isolated, do not connect to this header when running off Mains and Mains is not isolated.
J16	2-pin header	Active energy pulses **(WARNING)**	Probe here for cumulative active energy pulses. This header has two pins: GND and ACT, which is where the active energy pulses is actually output.	This header is not isolated from AC mains, so do not connect measuring equipment here (especially for the one-voltage configuration) See the "ISO_ACT" pin of J18 instead, which is isolated. If it is desired to test the active power pulses, use the "ISO_ACT" pin of J18 instead since it is isolated.
J17	2-pin header	Reactive energy pulses **(WARNING)**	Probe here for cumulative reactive energy pulses. This header has two pins: GND and REACT, which is where the reactive energy pulses is actually output.	This header is not isolated from AC mains, so do not connect measuring equipment here (especially for the one-voltage configuration). If it is desired to test the reactive power pulses, use the "ISO_REACT" pin of J18 instead since it is isolated.
J18	4-pin header	Isolated pulses header	Probe here for the isolated cumulative active energy pulses and the isolated cumulative three-phase reactive energy pulses. Using these header for pulses is recommended, especially for the one-voltage configuration since the system will be referenced with respect to one of the line voltages in this configuration.	This header has four pins: ISO_GND, ISO_REACT, ISO_ACT, and ISO_VCC. ISO_GND is the isolated ground for the energy pulses. ISO_VCC is the VCC connection for the isolated active and reactive energy pulses. ISO_ACT is where the isolated active energy pulses are output. ISO_REACT is where the isolated active energy pulses are output. This header is isolated from AC mains so it is safe to connect to scope or other measuring equipment because isolators are already present. However, either 3.3 V or 5 V must be applied between ISO_GND and ISO_VCC to produce the active energy pulses and reactive energy pulses at this header. The produced pulses have a logical high voltage that is equal to the voltage applied between ISO_GND and ISO_VCC.
J19	3-pin jumper header	RS-232 or RS-485 selection-power	Place a jumper at either the RS-232 or RS-485 positions depending on which of these two communication options are desired.	Put a jumper in the RS-232 position on this header, J20, and J21 to select RS-232 communication. Put a jumper in the RS-485 position on this header, J20, and J21 to select RS-485 communication.
J20	3-pin jumper header	RS-232 or RS-485 selection-TX	Place a jumper at either the RS-232 or RS-485 positions depending on which of these two communication options are desired.	Put a jumper in the RS-232 position on this header, J19, and J21 to select RS-232 communication. Put a jumper in the RS-485 position on this header, J19, and J21 to select RS-485 communication.
J21	3-pin jumper header	RS-232 or RS-485 selection-RX	Place a jumper at either the RS-232 or RS-485 positions depending on which of these two communication options are desired.	Put a jumper in the RS-232 position on this header, J19, and J20 to select RS-232 communication. Put a jumper in the RS-485 position on this header, J19, and J20 to select RS-485 communication.

表 2. Header Names and Jumper Settings (continued)

HEADER OR HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
J22	2-pin header	Header containing RS232_3.3, which is the voltage source harvested from RS-232 line, and RS232_GND, which is the ground connection for the isolated RS-232	Probe here for the isolated 3.3-V supply generated on the side of the isolation barrier with the RS-232.	Note that the 3.3-V rail produced here is derived from the RS-232 port of the PC so it is not applicable when using RS-485 mode. For RS-485 mode, external power must be provided to power the THVD1500 RS-485 transceiver.
J23	2-pin jumper header	TX_EN: RS-232 transmit enable **(WARNING)**	Place a jumper here to enable RS-232 transmissions.	
J24	2-pin jumper header	RX_EN: RS-232 receive enable **(WARNING)**	Place a jumper here to enable receiving characters using RS-232.	
J25	4-pin terminal block	RS-485 connection	Connection point for RS-485	To view the GUI using RS-485, connect the USB to RS-485 adapter here. 5 V must be provided externally on pin 1 of this header. Pin 2 of this header is the RS-485 ground, pin 3 is the B bus I/O line, and pin 4 is the A bus I/O line.
J26	3-pin terminal block	Phase A (two-voltage configuration) or Line A (one-voltage configuration) CT connection **(WARNING)**	Current inputs after the sensors for line A	This terminal block is a three-position terminal block but only the leftmost and rightmost positions are used. The center position, which is connected to GND, is not connected to the CT. Connect the positive terminal of the CT to the terminal block position on the most left, which is labeled "POS". Connect the negative terminal of the CT to the terminal block position on the most right, which is labeled "NEG". Before performing any test, verify that this terminal block is securely connected to both output leads of the CT. Note that the order of the CT leads is reversed here compared to the order on J27
J27	3-pin terminal block	Phase B (two-voltage configuration) or Line B (one-voltage configuration)CT connection **(WARNING)**	Current inputs after the sensors for line B	This terminal block is a three-position terminal block but only the leftmost and rightmost positions are used. The center position, which is connected to GND, is not connected to the CT. Connect the positive terminal of the CT to the terminal block position on the most right, which is labeled "POS". Connect the negative terminal of the CT to the terminal block position on the most left, which is labeled "NEG". Before performing any test, verify that this terminal block is securely connected to both output leads of the CT. Note that the order of the CT leads is reversed here compared to the order on J26.
J28	2-pin terminal block	Phase A voltage **(WARNING)**	Phase A line connection	For the two-voltage configuration, this terminal block is connected to the Neutral voltage and phase A line voltage connections on the reference design case using wires. For the one-voltage configuration, this terminal block is connected to line B instead of neutral. Connect the pin on the terminal block denoted by a "NEG" on the PCB silk screen to neutral (two-voltage configuration) or line B (one-voltage configuration). The pin on the terminal block denoted by a "POS" on the PCB silk screen to the line of Phase A. The neutral connection on J28 and J29 are all connected to each other on the PCB. This is the Phase A line voltage connection, so only probe here if using equipment that could measure the Mains voltage. Note that the order of the phase input and neutral is reversed here compared to the order on J29
J29	2-pin terminal block	Phase B voltage **(WARNING)**	Phase B line connection	For the two-voltage configuration, this terminal block is connected to the Neutral voltage and phase B line voltage connections on the reference design case using wires. For the one-voltage configuration, this terminal block is not used. Connect the pin on the terminal block denoted by a "NEG" on the PCB silk screen to neutral. Connect the pin on the terminal block denoted by a "POS" on the PCB silk screen to the line of Phase B. The neutral connection on J28 and J29 are all connected to each other on the PCB. This is the Phase B line voltage connection so only probe here if using equipment that could measure the Mains voltage. Note that the order of the phase input and neutral is reversed here compared to the order on J28. Also, this terminal block is not used for one-voltage configurations.
J30	2-pin jumper header	ADS131M04 AVDD jumper **(WARNING)**	A short (either through jumper of ammeter) must be present at this jumper header for proper operation of the ADS131M04.	This header along with J31 allow measuring the current consumption of the ADS131M04.
J31	2-pin jumper header	ADS131M04 DVCC jumper **(WARNING)**	A short (either through jumper of ammeter) must be present at this jumper header for proper operation of the ADS131M04.	This header along with J30 allow measuring the current consumption of the ADS131M04.

表 2. Header Names and Jumper Settings (continued)

HEADER OR HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
J32	8-pin header	ADS131M04 MSP432 communication header **(WARNING)**	Probe here for connections to the chip select signal, SPI signals, $\overline{RST}$ signal, CLKIN signal, and $\overline{DRDY}$ signal of the ADS131M04 device.	The $\overline{RST}$ pin of the ADS131M04 device is used to reset the ADS131M04. When initializing the ADS131M04, the MSP432 drives this pin to reset the ADS131M04. The DRDY pin of the ADS131M04 device is used to alert the MSP432 MCU that new current samples are available. The CLKIN pin is fed from the SMCLK clock output of the MSP432 MCU to the ADS131M04 device, which divides the clock down to produce the used modulator clock. This header is not isolated from AC mains, so do not connect measuring equipment when running from Mains unless isolators external to the reference design are available. The pin mappings on this header are as follows: ● Pin 1: SMCLK (ADS131M04 CLKIN pin) ● Pin 2: SPI DOUT (ADS131M04 DIN pin/SIMO) ● Pin 3: SPI DIN (ADS131M04 DOUT/ pinSOMI ● Pin 4: SPI CLK (ADS131M04 SCLK pin) ● Pin 5: ADS DRDY (ADS131M04 $\overline{DRDY}$ pin) ● Pin 6: SPI CS (ADS131M04 $\overline{CS}$ pin) ● Pin 7: RST SYNC (ADS131M04 $\overline{SYNC/RESET}$ pin) ● GND

3.1.3 Software

The MSP432 software used for evaluating this design is test software. 节 2.3.2 discusses the features of the test software, which provides insights on how to implement custom software for metrology testing.

3.2 Testing and Results

3.2.1 Test Setup

3.2.1.1 SVS and eFuse Functionality Testing

In addition to metrology accuracy testing, functionality testing is done on the TPS3840 SVS device and the TPS25921L eFuse device. For the TPS3840 testing, the board is powered by connecting an external power supply directly to DVCC (a jumper should not be placed on J2 to properly power DVCC directly) and the output voltage of the power supply is slowly varied from 3.3 V down to 1.9 V. The threshold voltage at which the MSP432 MCU is reset by the TPS3840 device, which is referred to as the negative voltage threshold, is logged. After the negative voltage threshold is reached, the power supply output voltage is slowly increased from 1.9 V back to 3.3 V. The voltage at which the reset is released, which is equal to the negative voltage threshold plus hysteresis voltage, is logged as well.

For testing the TPS25921L device, the MSP432 MCU is powered through the TPS70933 device by placing a jumper at J2. The TPS70933 is powered from the 5-V rail applied at header J4 by placing a jumper at J1. In addition to the jumpers at J1 and J2, a jumper is also placed at J6 to connect the TPS25921L output to header J12. An external power supply is connected to J4 (positive lead of power supply) and GND (negative lead of power supply). Also, a multimeter is placed at header J12 to measure the output voltage on the TPS25921L OUT pin. For the first test, the undervoltage lockout threshold is measured by slowly varying the external power supply output from 5 V to 4 V. Before the undervoltage threshold is reached, the voltage at the TPS25921L OUT pin should be equal to the voltage supplied by the external power supply. When the undervoltage threshold is reached, the OUT pin is disconnected from its IN pin, which causes the output voltage to read 0 V instead of the external power supply voltage. After the undervoltage voltage is reached, the power supply voltage is slowly increased back to 5 V. The power supply voltage at which the TPS25921L OUT pin is reconnected to its IN pin is, which is evident by the OUT pin voltage being equal to the external power supply voltage again instead of 0 V, is logged.

In addition to testing the undervoltage threshold, the overvoltage threshold is also tested. The overvoltage threshold test is performed by increasing the power supply voltage from 5 V to 6 V and logging at which voltage would the OUT pin of the TPS25921L device get disconnected from the IN pin. After determining the overvoltage threshold, the voltage is decreased back towards 5 V to determine at what voltage from the external power supply would the OUT pin of the TPS25921L device get reconnected to its IN pin.

For testing the current-limiting functionality of the TPS25921L, a similar setup is used as the undervoltage and overvoltage tests with the exception that header J12 is connected to a Chroma DC Electronic Load instead of just a multimeter. The thermal shutdown feature is specifically tested for current limiting by increasing the current consumption of the load connected to the OUT pin of the TPS25921L device and then measuring at what current would the load get disconnected from the voltage applied at the IN pin of the TPS25921L device. After thermal shutdown is reached, the load current was set to a lower value and the software was modified to provide a pulse on the TPS25921L ENUV pin to verify the OUT pin was reconnected to the external power supply.

3.2.1.2 Electricity Meter Metrology Accuracy Testing

To test for metrology accuracy in the electricity meter configuration, a source generator is used to provide the voltages and currents to the system at the proper locations mentioned in 节 3.1.2.1. In this design, a nominal voltage of 120 V between the line and neutral, calibration current of 10 A, and nominal frequency of 60 Hz are used for each phase for the two-voltage configuration. For the one-voltage configuration, the voltage between the two line voltages is 240 V, a calibration current of 10 A is used, and a nominal frequency of 60 Hz is used.

When the voltages and currents are applied to the system, the system outputs the cumulative active energy pulses and cumulative reactive energy pulses at a rate of 6400 pulses/kWh. This pulse output is fed into a reference meter (in the test equipment for this reference design, this pulse output is integrated in the same equipment used for the source generator) that determines the energy % error based on the actual energy provided to the system and the measured energy as determined by the active and reactive energy output pulse of the system. For the two-voltage configuration, cumulative active energy error testing, cumulative reactive energy error testing, individual phase active energy testing, and frequency variation testing are performed after performing the energy gain calibration and phase compensation as described in 节 3.2.1.3.2.2. In addition to the energy error tests, the RMS voltage % error and RMS current % error are measured as well for the two-voltage configuration. For the one-voltage configuration, cumulative active energy error testing and voltage variation tests are also performed. For both one-voltage and two-voltage testing, note that power offset calibration was not performed.

For cumulative active energy error, cumulative reactive energy error testing, and individual phase active energy testing, current is varied from 50 mA to 100 A . For cumulative active energy and individual phase error testing, a phase shift of 0°, 60°, and −60° is applied between the voltage and current waveforms fed to the reference design. Based on the error from the active energy output pulse, a plot of active energy % error versus current is created for 0°, 60°, and –60° phase shifts. For cumulative reactive energy error testing, a similar process is followed except that 30°, 60°, –30°, and –60° phase shifts are used, and cumulative reactive energy error is plotted instead of cumulative active energy error. In the cumulative active and reactive energy testing, the sum of the energy reading of each phase is tested for accuracy. In contrast, the individual phase energy readings (both Phase A and Phase B) are tested for the individual phase active energy testing. When testing the individual energy accuracy of a phase, the other phase is disabled by providing 0 A input for the current of this other phase so that the cumulative active energy reading should ideally be equal to the individual phase voltage, which allows the cumulative energy pulse output to be used for testing individual phase accuracy.

In addition to testing active energy by varying current, active energy was also tested by varying the RMS voltage from 240–15 V and measuring the active energy % error. This voltage variation testing was specifically done for the cumulative two-voltage active energy test, cumulative one-voltage active energy test, and the individual phase active energy tests.

Another set of energy tests performed were frequency variation tests. For this test, the frequency is varied by ±2 Hz from its 60-Hz nominal frequency. This test is conducted at 0.5 A and 10 A at phase shifts of 0°, 60°, and −60°. The resulting active energy error under these conditions are logged.

To test RMS accuracy, the RMS readings were used from the GUI since the pulse output that was used for the energy accuracy tests cannot be used for RMS voltage and current. For the voltage testing, 10-A current is applied for each phase and the voltage is varied from 9–270 V on each phase simultaneously. The voltage was not varied beyond 270 V because of the 275-V varistor present on the board, which could be removed for testing at voltages beyond 275 V. After applying each voltage, the resulting RMS voltage reading from the GUI is logged for each phase after the readings stabilize. Once the measured

RMS voltage readings are obtained from the GUI, the actual RMS voltage readings are obtained from the reference meter, which is necessary because the source generator may not generate the requested values for voltage, especially at small voltages. With the reference meter measured RMS voltage and the RMS voltage value of the GUI, the RMS voltage % error is calculated. A similar process is used to calculate the RMS current % error by using 120 V for each phase and varying current from 50 mA to 100 A.

3.2.1.3 Viewing Metrology Readings and Calibration

This section describes the methods used to verify the results of this design with the test software.

3.2.1.3.1 Viewing Results From LCD

The LCD scrolls between metering parameters every two seconds. For each metering parameter that is displayed on the LCD, three items are usually displayed on the screen: a symbol used to denote the phase of the parameter, text to denote which parameter is being displayed, and the actual value of the parameter. The phase symbol is displayed at the top of the LCD and denoted by a triangle shape. The orientation of the symbol determines the corresponding phase. 图 23 and 图 24 show the mapping between the different orientations of the triangle and the phase descriptor:

图 23. Symbol for Phase A

图 24. Symbol for Phase B

Aggregate results (such as cumulative active and reactive power) and parameters that are independent of phase (such as time and date) are denoted by clearing all of the phase symbols on the LCD.

The bottom line of the LCD is used to denote the value of the parameter being displayed. The text to denote the parameter being shown displays on the top line of the LCD. 表 3 shows the different metering parameters that are displayed on the LCD and the associated units in which they are displayed. The designation column shows which characters correspond to which metering parameter.

表 3. Displayed Parameters

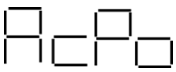
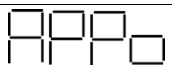
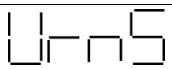
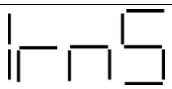
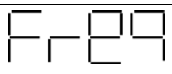
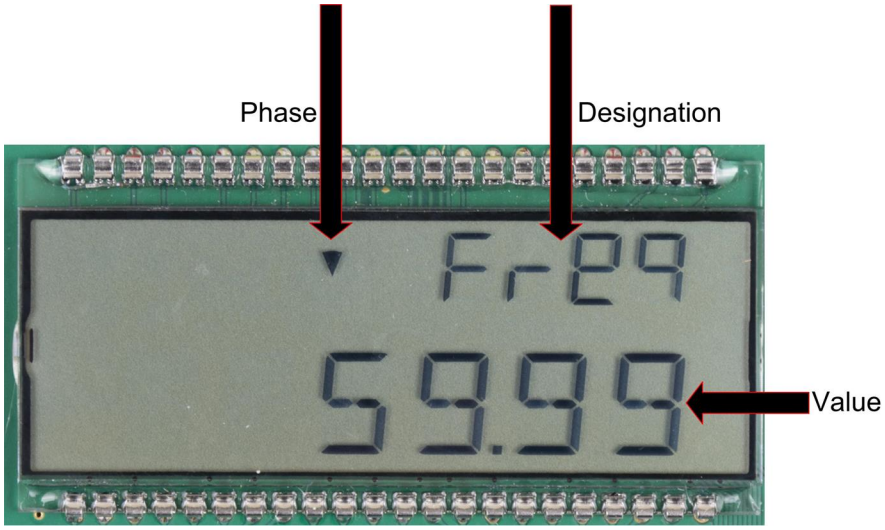
PARAMETER NAME	DESIGNATION	UNITS	COMMENTS
Active power		Watt (W)	This parameter is displayed for each phase. The aggregate active power is also displayed.
Reactive power		Volt-Ampere Reactive (var)	This parameter is displayed for each phase. The aggregate reactive power is also displayed.
Apparent power		Volt-Ampere (VA)	This parameter is displayed for each phase.
Power factor		Constant between 0 and 1	This parameter is displayed for each phase.
Voltage		Volts (V)	This parameter is displayed for each phase.
Current		Amps (A)	This parameter is displayed for each phase.
Frequency		Hertz (Hz)	This parameter is displayed for each phase.

表 3. Displayed Parameters (continued)

PARAMETER NAME	DESIGNATION	UNITS	COMMENTS
Total consumed active energy	AcEn	kWh	This parameter is displayed for each phase.
Total consumed reactive energy	rPEn	kVarh	This parameter is displayed for each phase. This displays the sum of the reactive energy in quadrant 1 and quadrant 4.
Time	t inP	Hour:minute:second	This parameter is only displayed when the sequence of aggregate readings are displayed. This parameter is not displayed once per phase.
Date	dAtP	Year:month:day	This parameter is only displayed when the aggregate readings are displayed. This parameter is not displayed once per phase.

图 25 shows an example of the measured frequency of phase A of 59.99 Hz, displayed on the LCD.

图 25. LCD



3.2.1.3.2 Calibrating and Viewing Results From PC

3.2.1.3.2.1 Viewing Results

To view the metrology parameter values from the GUI, perform the following steps:

1. Select whether to use the RS-485 or RS-232 connection for communication to the PC GUI. This selection is done by placing 3 jumpers on jumper headers J19, J20, and J21. To select the RS-485 communication option, put the jumpers on the top two pins (labeled RS485 on the board) of these three headers. To select the RS-232 communication option, put the jumpers on the bottom two pins (labeled RS232 on the board) of the three headers.
2. Connect the reference design to a PC
   - RS-232 option: Connect the reference design to a PC using a RS-232 cable. If the PC does not have a RS-232 adapter, a serial RS-232 adapter could be used. The RS-232 adapter should create a COM port on the PC when it is plugged in.
   - RS-485 option: A USB to RS-485 adapter can be used to communicate between the PC GUI and the RS-485 port on this design. The USB to RS-485 adapter should create a COM port on the PC when it is plugged in. The other end of the adapter should have wires for the RS-485 Data A and Data B connections as well as a GND connection and a 5-V power connection, which all should be connected to the J25 screw terminal block of the design according to the connection labels next to the terminal block pins. For testing this circuit, the following USB to RS-485 adapter is specifically

used:
http://www.ftdichip.com/Support/Documents/DataSheets/Cables/DS_USB_RS485_CABLES.pdf.
For this specific adapter, the Data A connection is orange, the Data B connection wire is yellow, the GND connection is black, and the 5-V power connection is red.

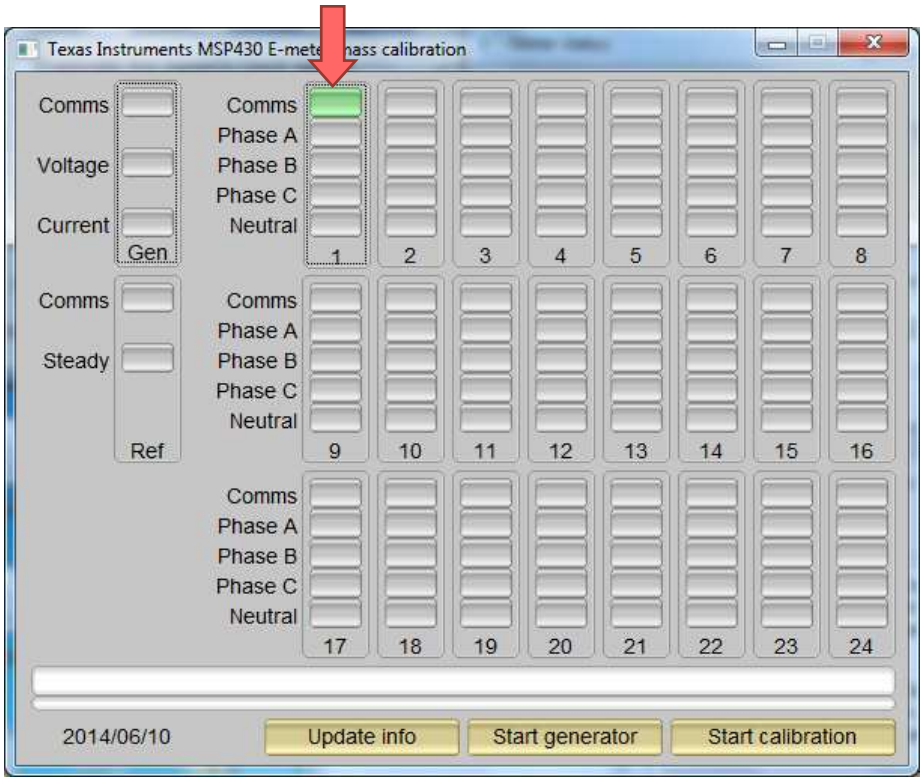
3. Open the GUI folder and open *calibration-config.xml* in a text editor.
4. Change the *port name* field within the *meter* tag to the COM port connected to the system. As 图 26 shows, this field is changed to *COM7*.

图 26. GUI Configuration File Changed to Communicate With Energy Measurement System

```
260       </correction>
261     </phase>
262     <temperature/>
263     <rtc/>
264   </cal-defaults>
265   <meter position="1">
266     <port name="com7" speed="9600"/>
267   </meter>
268   <reference-meter>
269     <port name="USB0::0x0A69::0x0835::A66200101281::INSTR"/>
270     <type id="chroma-66202"/>
271     <log requests="on" responses="on"/>
272     <scaling voltage="1.0" current="1.0"/>
273   </reference-meter>
```

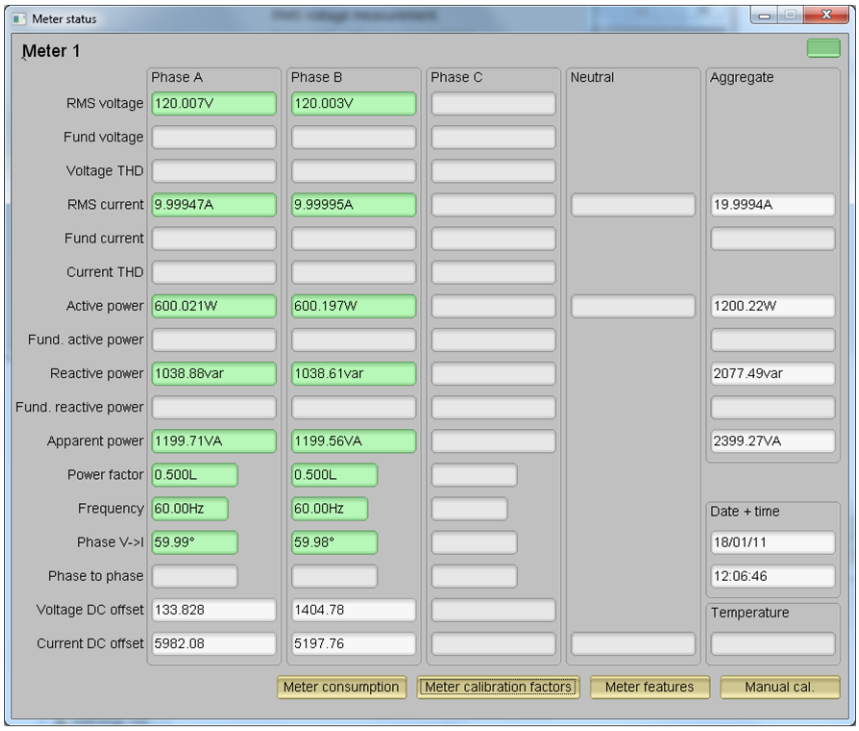
5. Run the *calibrator.exe* file, which is located in the GUI folder. If the COM port in the *calibration-config.xml* was changed in the previous step to the COM port connected to the reference design, the GUI opens (see 图 27). If the GUI connects to the design properly, the top-left button is green. If there are problems with connections or if the code is not configured correctly, the button is red. Click the green button to view the results.

图 27. GUI Startup Window



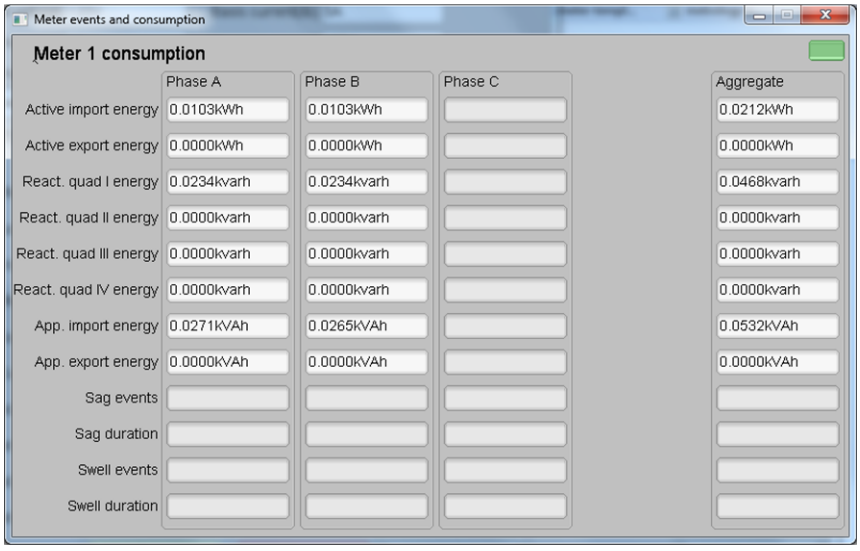
Upon clicking on the green button, the results window opens (see 图 28). In the figure, there is a trailing "L" or "C" on the *Power factor* values to indicate an inductive or capacitive load, respectively.

图 28. GUI Results Window



From the results window, the total-energy consumption readings can be viewed by clicking the *Meter Consumption* button. After the user clicks this button, the *Meter events and consumption* window pops up, as 图 29 shows.

图 29. Meter Events and Consumption Window



From the results window, the user can also view the meter settings by clicking the *Meter features* button, view the system calibration factors by clicking the *Meter calibration factors* button, or open the window used for calibrating the system by clicking the *Manual cal.* button.

3.2.1.3.2.2 Calibration

Calibration is key to any meter performance, and it is absolutely necessary for every meter to go through this process. Initially, every meter exhibits different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify their effects, every meter must be calibrated. To perform calibration accurately, there must be an accurate AC test source and a reference meter available. The source must be able to generate any desired voltage, current, and phase shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section discusses a simple and effective method of calibration of this three-phase design.

The GUI used for viewing results can easily be used to calibrate the design. During calibration, parameters called calibration factors are modified in the test software to give the least error in measurement. For this meter, there are six main calibration factors for each phase: voltage scaling factor, active power offset (erroneously called voltage AC offset in the GUI), current scaling factor, reactive power offset (erroneously called current AC offset in the GUI), power scaling factor, and the phase compensation factor. The voltage, current, and power scaling factors translate measured quantities in metrology software to real-world values represented in volts, amps, and watts, respectively. The power offset is used to subtract voltage to current crosstalk, which appears as a constant power offset and causes greater inaccuracies at lower currents. Note that offset calibration was not used for testing this specific design. The last calibration factor is the phase compensation factor, which is used to compensate any phase shifts introduced by the current sensors and other passives. Note that the voltage, current, and power calibration factors are independent of each other. Therefore, calibrating voltage does not affect the readings for RMS current or power.

When the meter SW is flashed on the MSP432 devices for the first time, default calibration factors are loaded into these calibration factors. These values are modified through the GUI during calibration. The calibration factors are stored in INFO_MEM, and therefore, remain the same if the meter is restarted.

Calibrating any of the scaling factors is referred to as gain correction. Calibrating the phase compensation factors is referred to as phase correction. For the entire calibration process, the AC test source must be ON, meter connections consistent with 节 3.1.2.1, and the energy pulses connected to the reference meter.

3.2.1.3.2.2.1 Gain Calibration

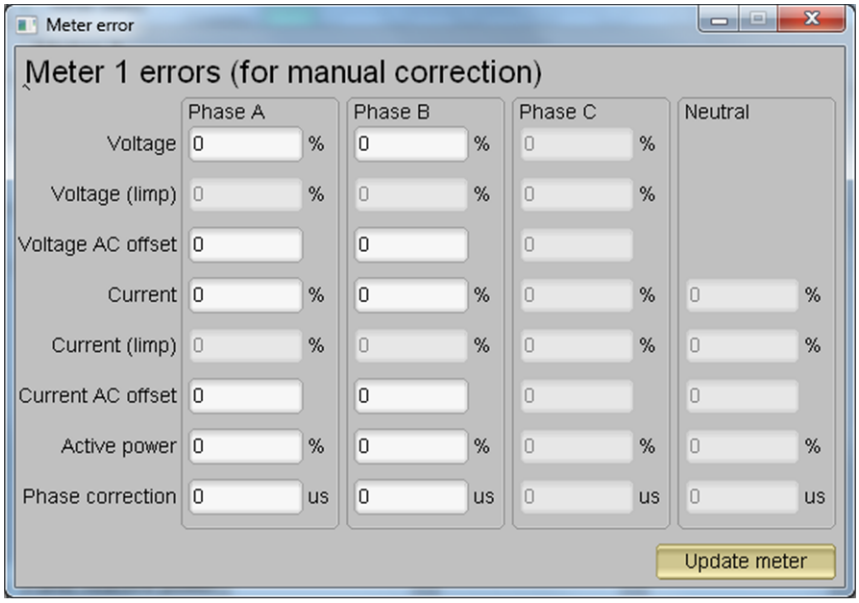
Usually, gain correction for voltage and current can be done simultaneously for all phases. However, energy accuracy (%) from the reference meter for each individual phase is required for gain correction for active power. Also, when performing active power calibration for any given phase, the other phase must be turned OFF by turning off the current but leaving the other voltages still enabled.

3.2.1.3.2.2.2 Voltage and Current Gain Calibration

To calibrate the voltage and current readings, perform the following steps:

1. Connect the GUI to view results for voltage, current, active power, and the other metering parameters.
2. Configure the test source to supply desired voltage and current for all phases. Ensure that these are the voltage and current calibration points with a zero-degree phase shift between each phase voltage and current. For example, for 120 V, 10 A, 0º (PF = 1). Typically, these values are the same for every phase.
3. Click on the *Manual cal.* button that 图 28 shows. The following screen pops up from 图 30:

图 30. Manual Calibration Window



4. Calculate the correction values for each voltage and current. The correction values that must be entered for the voltage and current fields are calculated using 公式 17:

$$\text{Correction (\%)} = \left(\frac{\text{value}_{\text{observed}}}{\text{value}_{\text{desired}}} - 1 \right) \times 100 \quad (17)$$

where

- $\text{value}_{\text{observed}}$ is the value measured by the TI meter
- $\text{value}_{\text{desired}}$ is the calibration point configured in the AC test source

5. After calculating for all voltages and currents, input these values as is (±) for the fields *Voltage and Current* for the corresponding phases.
6. Click on the *Update meter* button and the observed values for the voltages and currents on the GUI settle immediately to the desired voltages and currents.

3.2.1.3.2.2.3 Active Power Gain Calibration

注: This section is an example for one phase. Repeat these steps for the other phase.

After performing gain correction for voltage and current, gain correction for active power must be done. Gain correction for active power is done differently in comparison to voltage and current. Although, conceptually, calculating the active energy % error as is done with voltage and power can be done, this method is not the most accurate and should be avoided.

The best option to get the *Correction (%)* is directly from the reference meters measurement error of the active power. This error is obtained by feeding energy pulses to the reference meter. To perform active power calibration, complete the following steps:

1. Turn off the system and connect the energy pulse output of the system to the reference meter. Configure the reference meter to measure the active power error based on these pulse inputs.
2. Turn on the AC test source.
3. Repeat Step 1 to Step 3 from 节 3.2.1.3.2.2.2 with the identical voltages, currents, and 0º phase shift that were used in the same section.
4. Obtain the % error in measurement from the reference meter. Note that this value may be negative.

5. Enter the error obtained in Step 4 into the *Active Power* field under the corresponding phase in the GUI window. This error is already the value and does not require calculation.
6. Click the *Update meter* button and the error values on the reference meter immediately settle to a value close to zero.

3.2.1.3.2.2.4 Offset Calibration

After performing gain calibration, if the accuracy at low currents is not acceptable, offset calibration could be done. Offset calibration removes any crosstalk, such as the crosstalk to the current channels of a phase from the line voltages.

To perform active power offset calibration for a phase, simply add the offset to be subtracted from the active power reading (in units of mW) to the current value of the active power offset (labeled "voltage AC off" in the meter calibration factors window) and then enter this new value in the *Voltage AC offset* field in the Manual Calibration window. As an example, if the "voltage AC off" has a value of 200 (0.2 W) in the meter calibration window, and it is desired to subtract an additional 0.300 mW, then enter a value of 500 in the *Voltage AC offset* field in the Manual Calibration window. After entering the value in the *Voltage AC offset* field in the Manual Calibration window, press "Update meter".

To perform reactive power offset calibration for a phase, a similar process is followed as the process used to perform active power offset calibration. Add the offset to be subtracted from the reactive power reading (in units of mvar) to the current value of the reactive power offset (labeled "Current AC offset" in the meter calibration factors window) and then enter the value in the *Current AC offset* field in the Manual Calibration window. After entering the value in the *Current AC offset* field in the Manual Calibration window, press "Update meter".

3.2.1.3.2.2.5 Phase Calibration

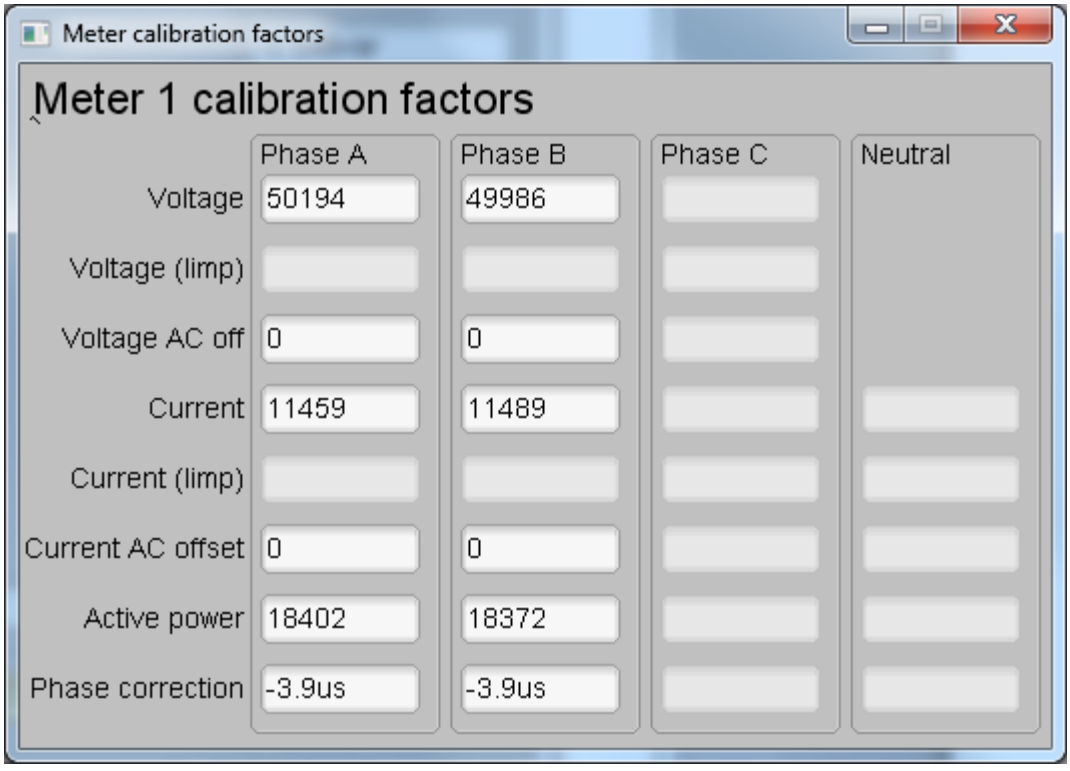
After performing power gain correction, do the phase calibration. Similar to active power gain calibration, to perform phase correction on one phase, the other phase must be disabled. To perform phase correction calibration, complete the following steps:

1. If the AC test source has been turned OFF or reconfigured, perform Step 1 through Step 3 from 节 3.2.1.3.2.2.2 using the identical voltages and currents used in that section.
2. Disable all other phases that are not currently being calibrated by setting the current of these phases to 0 A.
3. Modify only the phase-shift to a non-zero value; typically, +60º is chosen. The reference meter now displays a different % error for active power measurement. Note that this value may be negative.
4. If the error from Step 3 is not close to zero, or is unacceptable, perform phase correction by following these steps:
   a. Enter a value as an update for the *Phase Correction* field for the phase that is being calibrated. Usually, a small ± integer must be entered to bring the error closer to zero. Additionally, for a phase shift greater than 0 (for example: +60º), a positive (negative) error requires a positive (negative) number as correction.
   b. Click on the *Update meter* button and monitor the error values on the reference meter.
   c. If this measurement error (%) is not accurate enough, fine-tune by incrementing or decrementing by a value of 1 based on Step 4a and Step 4b. Note that after a certain point, the fine-tuning only results in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.
   d. Change the phase now to −60° and check if this error is still acceptable. Ideally, errors must be symmetric for same phase shift on lag and lead conditions.

After performing phase calibration, calibration is complete for one phase. Gain calibration, offset calibration, and phase calibration must be performed for the other phases.

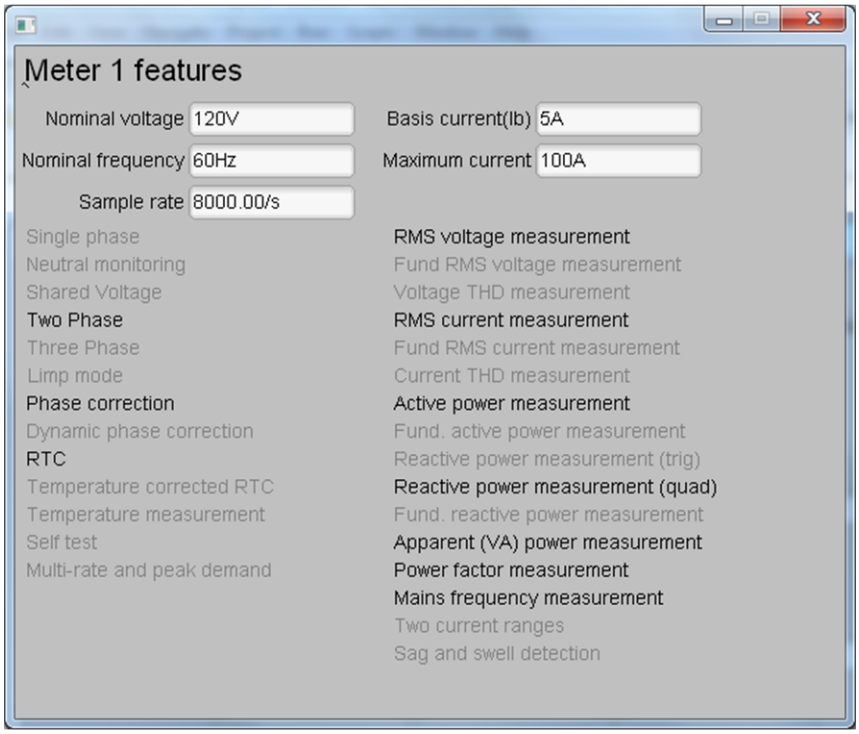
This completes calibration of voltage, current, and power for both phases. View the new calibration factors (see 图 31) by clicking the *Meter calibration factors* button of the GUI metering results window in 图 28. For these displayed calibration factors, note that the "Voltage AC off" parameter actually represents the active power offset (in units of mW) subtracted from each measurement and the "Current AC offset" parameter actually represents the reactive power offset subtracted (in units of mvar) from reactive power readings. Also, this shows example calibration factors for a meter that uses the two-voltage configuration. If the same meter is set for one-voltage configuration, the voltage and active power scaling factors would be approximately half of what it is in 图 28, since the line-to-line voltage measurement is used for the voltage readings of both phases instead of measuring the two line-to-neutral voltages. Under ideal conditions for a split-phase system, the line-to-line voltage measurement has an RMS value that is twice each of the two line to neutral RMS measurements, which means that the voltage fed to the ADC is also twice as much when measuring line-to-line voltage compared to when measuring line-to-neutral voltage. As a result, for one-voltage configurations, the voltage and power readings have to be divided by an additional factor of two, which is automatically done by following the active power and voltage gain calibration steps.

图 31. Calibration Factors Window



View the configuration of the system by clicking on the *Meter features* button in 图 28 to get to the window that 图 32 shows.

图 32. Meter Features Window



3.2.2 Test Results

3.2.2.1 SVS and eFuse Functionality Testing Results

表 4. SVS Test Results

CONDITION	MEASURED VOLTAGE (V)	DATA SHEET TYPICAL VOLTAGE VALUE (V)
Negative voltage threshold, VIT-	2.00 V	2.00 ±1% V
Positive voltage threshold, VIT+ = VIT- + VHYS	2.11 V	2.10 V
Hysteresis voltage, VHYS = VIT+ – VIT-	2.11 – 2.00 = 0.11 V	2.1 – 2.0 = 0.10 V

The measured values of VIT- and VHYS, match closely with the expected values from the data sheet.

表 5. eFuse Test Results

CONDITION	MEASURED VOLTAGE (V)	EXPECTED VOLTAGE VALUE (V)
Power failure detection threshold (VIN Falling)	4.05 V	4.26 – 0.224 = 4.04 V (Based on data sheet typical value for internal UVLO threshold, rising and hysteresis)
Release UVLO (VIN Rising)	4.28 V	4.26 V (Based on data sheet typical value for internal UVLO threshold, rising)
Release overvoltage condition (VIN Falling)	5.62 V	5.57 V (Taken from TPS25921 calculation sheet and selected resistor values)
Overvoltage cutoff threshold (VIN Rising)	5.81 V	5.78 V (Taken from TPS25921 calculation sheet and selected resistor values)

The measured values for the power failure detection threshold and overvoltage cutoff threshold match closely with the expected values. In addition, the overcurrent threshold value that was measured to cause a thermal shutdown was 1.62 A.

3.2.2.2 Electricity Meter Metrology Accuracy Results

For the following test results, gain and phase calibration are applied to the meter. In the following results, the active energy results are within 0.1% at 0° phase shift. At 60° and –60° phase shift, which is allowed to have relaxed accuracy in electricity meter standards, the trend where the results deviate at higher currents is from the CT phase shift varying across current. Additionally, the active energy vs. voltage results and the RMS voltage results show that good accuracy results are able to be obtained despite using only a fraction of the ADC range for the voltage channels.

表 6. Phase A Active Energy % Error Versus Voltage, Two-Voltage Mode

VOLTAGE (V)	% ERROR
240	0.0113
120	–0.0067
60	–0.01
30	–0.012
15	–0.015

表 7. Phase A Active Energy % Error Versus Current, Two-Voltage Mode

CURRENT (A)	0°	60°	–60°
0.05	–0.02	0.007	–0.062
0.10	–0.025	0.017	–0.057
0.25	–0.007	0.031	–0.051
0.50	0.001	0.029	–0.031
1.00	0.0075	0.034	–0.021
2.00	0	0.04	–0.036
5.00	0.003	0.019	–0.019
10.00	0.007	0.009	–0.004
20.00	–0.007	0.006	–0.013
30.00	0.0007	–0.002	0.006
40.00	0.002	–0.007	0.013
50.00	–0.009	–0.04	0.032
60.00	–0.0007	–0.049	0.0445
70.00	0.0003	–0.052	0.058
80.00	0.004	–0.064	0.074
90.00	0.01	–0.065	0.0845
100.00	0.014	–0.07	0.101

图 33. Phase A Active Energy % Error Versus Current, Two-Voltage Mode

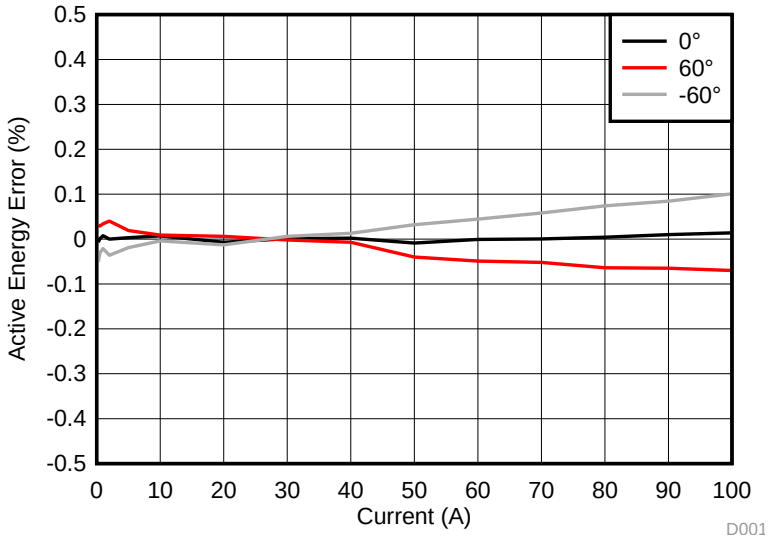


表 8. Phase B Active Energy % Error Versus Voltage, Two-Voltage Mode

VOLTAGE (V)	% ERROR
240	0.011
120	–0.0003
60	–0.004
30	–0.0047
15	–0.0067

表 9. Phase B Active Energy % Error Versus Current, Two-Voltage Mode

CURRENT (A)	0°	60°	–60°
0.05	–0.032	–0.007	–0.122
0.10	–0.019	0.019	–0.083
0.25	–0.019	0.032	–0.058
0.50	–0.007	0.045	–0.062
1.00	–0.007	0.045	–0.045
2.00	–0.015	0.032	–0.06
5.00	–0.007	0.026	–0.036
10.00	–0.0087	0.009	–0.025
20.00	–0.019	–0.019	–0.028
30.00	–0.019	–0.036	–0.011
40.00	-0.023	–0.045	0
50.00	–0.014	–0.06	0.0395
60.00	–0.011	–0.075	0.045
70.00	–0.01	–0.074	0.054
80.00.	–0.0077	–0.08	0.064
90.00	0.003	–0.068	0.066
100.00	0.011	–0.042	0.052

图 34. Phase B Active Energy % Error Versus Current, Two-Voltage Mode

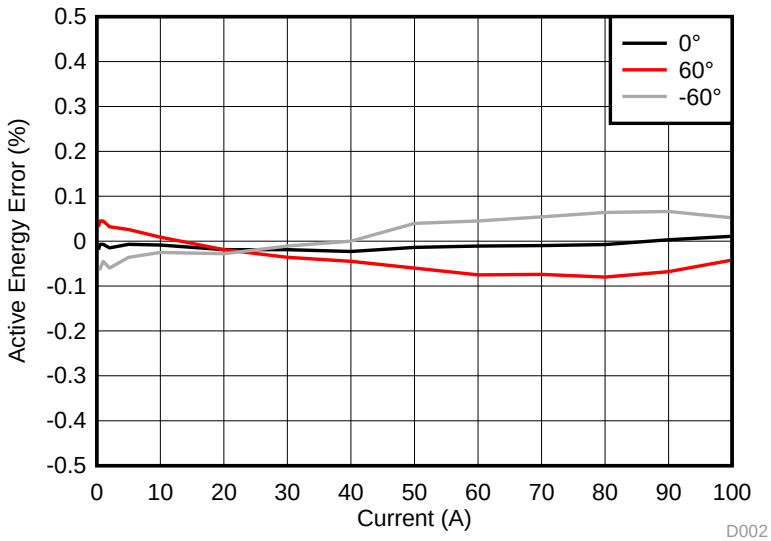


表 10. Cumulative Phase Active Energy % Error Versus Voltage, Two-Voltage Mode

VOLTAGE (V)	% ERROR
240	0.0353
120	0.022
60	0.016
30	0.014
15	0.013

表 11. Cumulative Phase Active Energy % Error Versus Current, Two-Voltage Mode

CURRENT (A)	0°	60°	–60°
0.05	0.019	0.045	–0.032
0.10	0.006	0.058	–0.032
0.25	0.0125	0.045	–0.0385
0.50	0.006	0.032	–0.032
1.00	0.015	0.045	–0.019
2.00	0.003	0.045	–0.039
5.00	0.006	0.024	–0.012
10.00	0.01	0.0165	0
20.00	–0.007	0.002	–0.013
30.00	0.002	–0.007	0.0085
40.00	0	–0.016	0.019
50.00	–0.003	–0.035	0.042
60.00	0.002	–0.047	0.053
70.00	0.009	–0.047	0.063
80.00.	0.007	–0.05	0.067
90.00	0.013	–0.045	0.08
100.00	0.0223	–0.04	0.092

图 35. Cumulative Phase Active Energy % Error Versus Current, Two-Voltage Mode

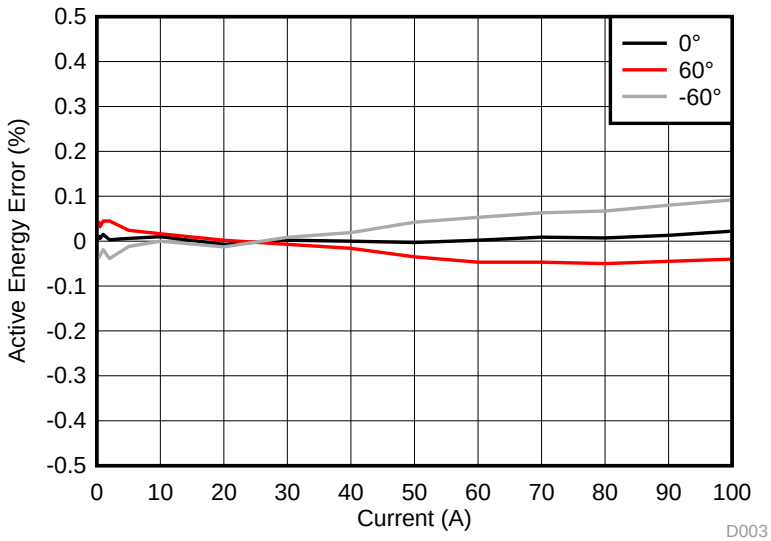


表 12. Cumulative Phase Active Energy % Error Versus Voltage, One-Voltage Mode

VOLTAGE (V)	% ERROR
240	–0.005
120	–0.024
60	–0.031
30	–0.036
15	–0.043

表 13. Cumulative Phase Active Energy % Error Versus Current, One-Voltage Mode

CURRENT (A)	0°	60°	–60°
0.05	–0.058	–0.045	–0.147
0.10	–0.045	–0.007	–0.096
0.25	–0.019	0.019	–0.083
0.50	–0.0255	0.032	–0.07
1.00	–0.011	0.019	–0.058
2.00	–0.017	0.025	–0.07
5.00	–0.0233	0.011	–0.053
10.00	–0.0177	0.005	–0.04
20.00	–0.026	–0.0023	–0.0355
30.00	–0.017	–0.019	–0.0123
40.00	–0.013	–0.0225	–0.01
50.00	–0.031	–0.058	–0.001
60.00	–0.023	–0.06	0.012
70.00	–0.0183	–0.058	0.023
80.00.	–0.005	–0.052	0.027
90.00	–0.009	–0.049	0.036
100.00	0.0013	–0.045	0.045

图 36. Cumulative Phase Active Energy % Error Versus Current, One-Voltage Mode

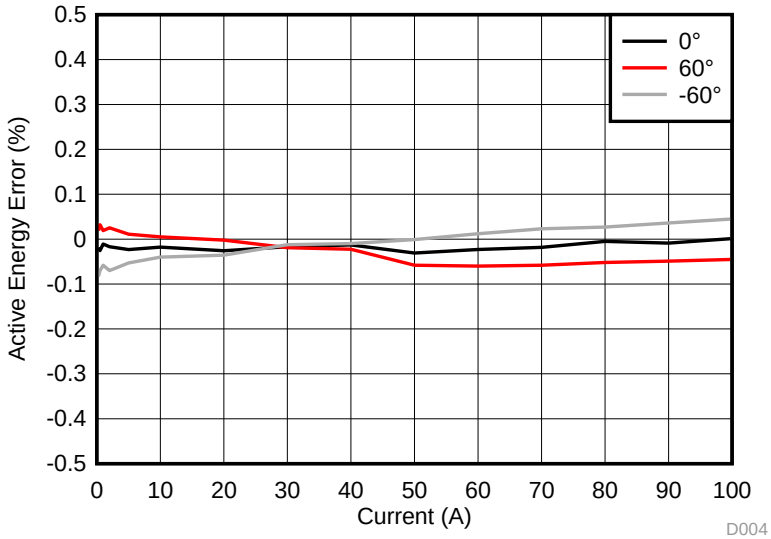


表 14. Cumulative Reactive Energy % Error Versus Current, Two-Voltage Mode

CURRENT (A)	30°	60°	–30°	–60°
0.05	–0.003	0.004	–0.023	–0.027
0.10	–0.037	–0.013	0.011	–0.008
0.25	–0.067	–0.027	0.043	0.002
1.00	–0.044	–0.021	0.0415	0.011
5.00	–0.036	–0.0183	0.022	0.001
10.00	–0.03	–0.012	0.014	–0.003
20.00	–0.041	–0.026	–0.0035	–0.013
40.00	–0.01	–0.016	–0.021	–0.016
60.00	0.025	–0.0007	–0.047	–0.0247
80.00	0.041	0.0085	–0.048	–0.021
100.00	0.054	0.02	–0.044	–0.012

图 37. Cumulative Reactive Energy % Error Versus Current, Two-Voltage Mode

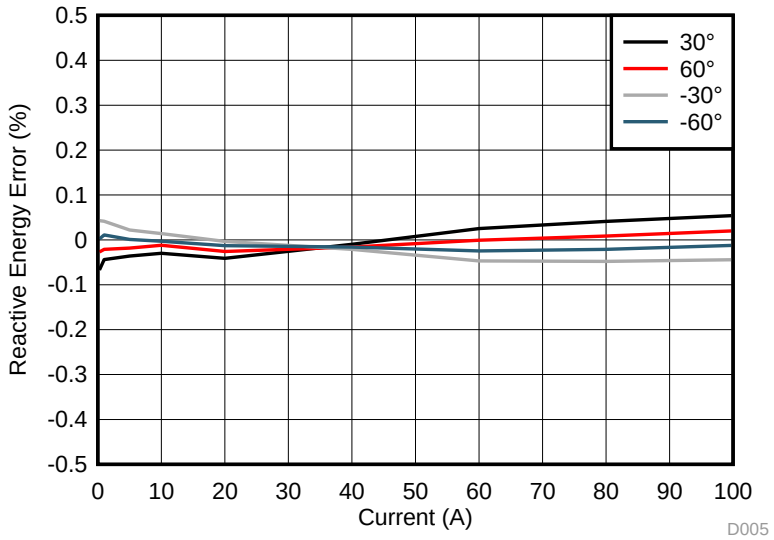


表 15. Cumulative Active Energy Measurement Error Versus Frequency, ±2 Hz From Nominal Frequency

CONDITIONS	58 Hz	60 Hz	62 Hz
0.5 A, 0	0.006	0.0017	–0.007
0.5 A, 60	0.058	0.032	0.032
0.5 A, 300	–0.045	–0.032	–0.032
10 A, 0	0.0047	–0.001	–0.0033
10 A, 60	0.025	0.0073	0.008
10 A, 300	–0.0105	–0.009	–0.013

表 16. Phase A RMS Current % Error, Two-Voltage Mode

CURRENT (A)	GUI CURRENT READING (A)	REFERENCE METER READING (A)	% ERROR
0.05	0.050053	0.050031	0.0440
0.10	0.100039	0.099988	0.0510
0.25	0.250034	0.24997	0.0256
0.50	0.50005	0.49992	0.0260
1.00	1.00017	0.99979	0.0380
2.00	2.00021	1.9996	0.0305
5.00	5.00039	4.9986	0.0358
10.00	10.0013	9.9971	0.0420
20.00	20.0007	19.993	0.0385
30.00	30.0025	29.991	0.0383
40.00	40.0038	39.988	0.0395
50.00	50.0054	49.989	0.0328
60.00	60.0066	59.984	0.0377
70.00	70.0091	69.981	0.0402
80.00.	80.0127	79.981	0.0396
90.00	90.018	89.976	0.0467
100.00	100.024	99.974	0.0500

图 38. Phase A RMS Current % Error, Two-Voltage Mode

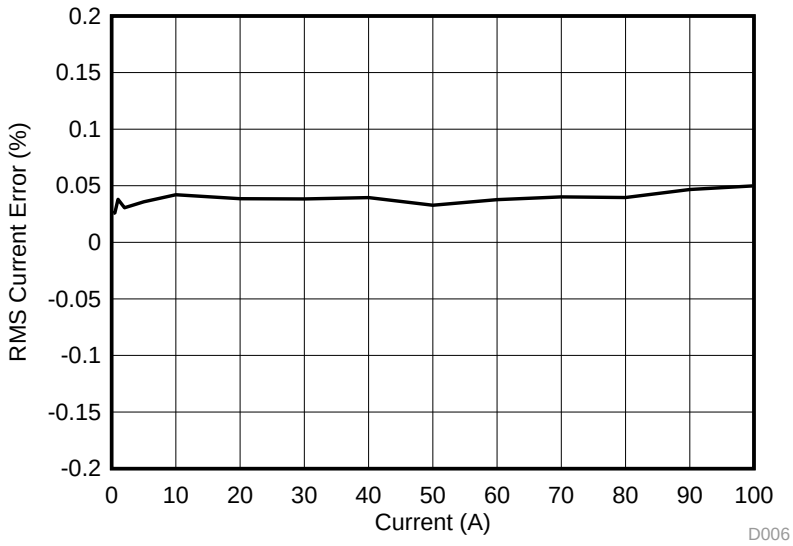


表 17. Phase B RMS Current % Error, Two-Voltage Mode

CURRENT (A)	GUI CURRENT READING (A)	REFERENCE METER READING (A)	% ERROR
0.05	0.050083	0.05005	0.0659
0.10	0.100055	0.10002	0.0350
0.25	0.250019	0.24996	0.0236
0.50	0.500016	0.49989	0.0252
1.00	1.00008	0.99984	0.0240
2.00	2.00016	1.9999	0.0130
5.00	4.99979	4.9987	0.0218
10.00	9.99998	9.9982	0.0178
20.00	19.9986	19.998	0.0030
30.00	29.9948	29.992	0.0093
40.00	39.9936	39.99	0.0090
50.00	49.9918	49.983	0.0176
60.00	59.9906	59.979	0.0193
70.00	69.9921	69.981	0.0159
80.00.	79.9924	79.976	0.0205
90.00	89.9942	89.97	0.0269
100.00	99.9997	99.97	0.0297

图 39. Phase B RMS Current % Error, Two-Voltage Mode

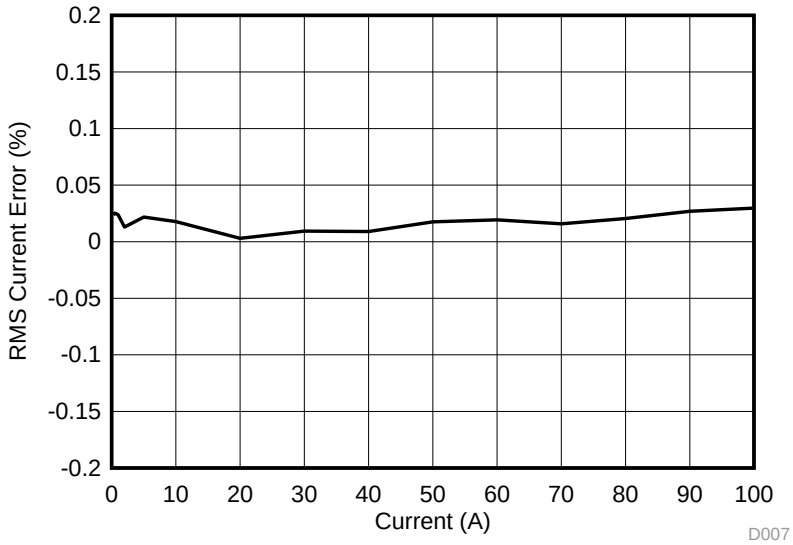


表 18. Phase A RMS Voltage % Error, Two-Voltage Mode

VOLTAGE (V)	GUI VOLTAGE READING (V)	REFERENCE METER READING (V)	% ERROR
9	9.002	9.0034	–0.0155
10	10.003	10.004	–0.0100
30	29.999	30.002	–0.0100
50	50.002	49.999	0.0060
70	70.004	70.001	0.0043
90	90.007	89.999	0.0089
100	100.01	100	0.0100
120	120.016	120	0.0133
140	140.025	140.01	0.0107
160	160.028	160	0.0175
180	180.035	180	0.0194
200	200.049	200	0.0245
220	220.057	220	0.0259
230	230.067	230	0.0291
240.	240.074	240	0.0308
260	260.087	260.02	0.0258
270	270.104	270.03	0.0274

图 40. Phase A RMS Voltage % Error, Two-Voltage Mode

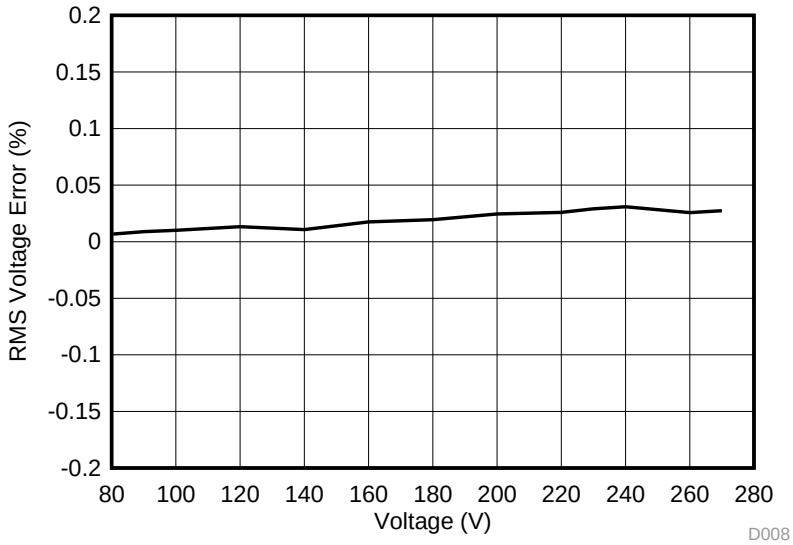
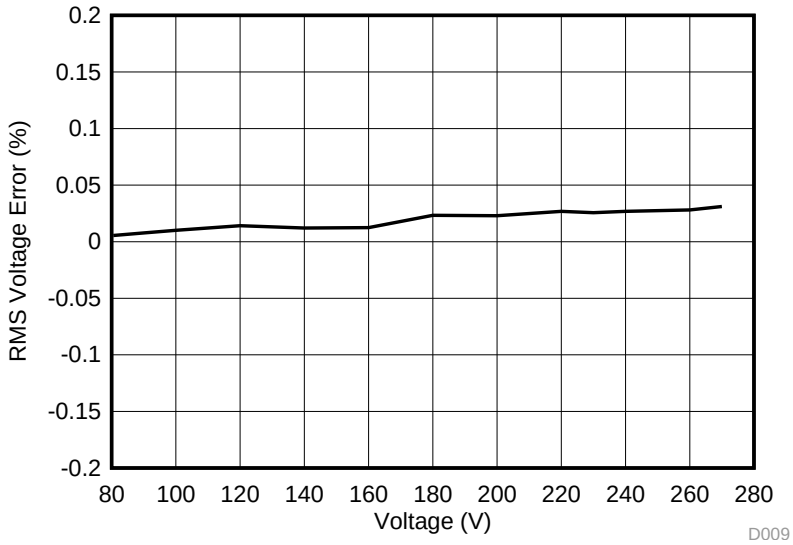


表 19. Phase B RMS Voltage % Error, Two-Voltage Mode

VOLTAGE (V)	GUI VOLTAGE READING (V)	REFERENCE METER READING (V)	% ERROR
9	8.999	9	–0.0111
10	9.99995	9.9995	0.0045
30	29.997	29.997	0.0000
50	49.999	49.995	0.0080
70	70.002	70	0.0029
90	90.009	90.002	0.0078
100	100.01	100	0.0100
120	120.017	120	0.0142
140	140.027	140.01	0.0121
160	160.03	160.01	0.0125
180	180.042	180	0.0233
200	200.056	200.01	0.0230
220	220.069	220.01	0.0268
230	230.079	230.02	0.0256
240.	250.087	250.02	0.0268
260	260.103	260.03	0.0281
270	270.114	270.03	0.0311

图 41. Phase B RMS Voltage % Error, Two-Voltage Mode



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010037.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010037.

4.3 PCB Layout Recommendations

For this design, the following general guidelines must be followed:

- Place decoupling capacitors close to their associated pins.
- Use ground planes instead of ground traces and minimize the cuts in the ground plane, especially near the ADS131M04. In this design, there is a ground plane on both the top and bottom layer; for this situation, ensure that there is good stitching between the planes through the liberal use of vias.
- Keep the two traces to the inputs of an ADC channel symmetrical and as close as possible to each other.
- Crosstalk from the voltage to current channels can reduce accuracy at lower currents if power offset is not performed. To minimize voltage to current crosstalk on the PCB, assign ADC channels 0 and 1 to the current channels and channels 2 and 3 to the voltage channels or assign ADC channels 0 and 1 to the voltage channels and channels 2 and 3 to the current channels.
- For the ADS131M04 device, place the 0.1-μF capacitor closest to the AVDD pin than the 1-μF capacitor. Do the same thing also for the 0.1-μF and 1-μF capacitors connected to DVDD.
- Note that the order of the AINxP and AINxN pins on the ADS131M04 switches when going from one converter to another. This swapped order is dealt with in this design by swapping the connection order of the wires connected to the voltage and current terminals (the order of wires is reversed between J26 and J27 current terminals and it is also reversed between J28 and J29 voltage terminals)
- Minimize the length of the traces used to connect the crystal to the microcontroller. Place guard rings around the leads of the crystal and ground the crystal housing. In addition, there must be clean ground underneath the crystal and placing any traces underneath the crystal must be avoided. Also, keep high-frequency signals away from the crystal.
- Use wide traces for power-supply connections.
- Use a different ground plane for the isolated RS-232 and RS-485. This other ground plane is at the potential of the RS-232 and RS-485 ground and not the GND used elsewhere in the board.
- Ensure that the recommended clearance and creepage spacing are met for the ISO7731B and ISO7720 isolation devices in this design.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010037.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010037.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010037.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010037.

5 Related Documentation

1. Texas Instruments, *ADS131M04 4-channel, simultaneously-sampling, 24-bit, delta-sigma ADC data sheet*
2. Texas Instruments, *MSP432P411x, MSP432P401x SimpleLink™ mixed-signal microcontrollers data sheet*
3. Texas Instruments, *TPS3840 nano power, high input voltage supervisor with $\overline{MR}$ and programmable delay data sheet*
4. Texas Instruments, *TPS25921x 4.5V - 18V eFuse with Precise Current Limit and Over Voltage Protection data sheet*
5. Texas Instruments, *THVD1500 500 kbps RS-485 transceivers with ±8-kV IEC ESD protection data sheet*
6. Texas Instruments, *ISO7731B high-speed, basic insulation triple-channel digital isolator data sheet*
7. Texas Instruments, *TRS3232E 3-V to 5.5-V multichannel RS-232 line driver and receiver with ±15-kV IEC ESD protection data sheet*

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