Application Report
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Common Mode Transient Immunity (CMTI) for UCC2122x Isolated Gate Drivers

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ABSTRACT

Isolated gate drivers are widely used for driving MOSFETs and IGBTs in numerous applications such as solar inverters, telecom & network power and HEV/EV. In addition to switching the MOSFETs or IGBTs on and off, these drivers also provide galvanic isolation. The device's switching rate depends on the application and type of switch being used. Switching frequencies of 10 to 20 kHz are common in MOSFETs and IGBTs, however, silicon carbide (SiC) and gallium-nitride or GaN-based systems can operate at much higher switching frequencies without significant power loss during transition. Some advantages for using a higher switching frequency are smaller filter size, fast control and lower distortion. Common-mode transient immunity (CMTI) is an important parameter of a gate driver to consider when operating it at higher switching frequencies. CMTI is critical for nearly all gate drivers which handle differential voltage between two separate ground references, i.e. isolated gate drivers. This app note will introduce TI's isolated dual-channel gate driver UCC2122x, the CMTI definition, standard requirements, validation and measurement, and design considerations.

Contents

1 Introduction 2
2 What is CMTI? 2
3 How to characterize CMTI for isolated gate drivers on the bench 4
4 Bench Implementation of Common-mode Pulse Generator 4
5 Summary 8

List of Figures

1 Simplified CMTI Test Setup 2
2 Static CMTI Measurement 3
3 Dynamic CMTI Measurement 3
4 Simplified CMTI Test Setup for UCC2122x 4
5 Positive Common-Mode Pulse Generator and typical waveform 5
6 System Diagram for Positive CMTI Characterization 6
7 Negative Common-Mode Pulse Generator and Typical Waveform 6
8 CMTI Measurement Position Across DUT and Below PCB 7
9 CMTI Measurement Position Across DUT and Below PCB 7
10 CMTI Measurement Position Calibration 8
11 UCC2122x CMTI Characterization Results 8

List of Tables

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1 Introduction

With the increasing progress and adoption of new generation power semiconductor devices, such as SiC and GaN, customer end equipment and applications are requiring higher switching frequencies – with more than 2X the dv/dt and over 5X the di/dt during turn on/turn off transients compared to conventional MOSFETs and IGBTs. Common mode transient immunity, known as CMTI and measured in dv/dt (unit: kV/µs or V/ns), is a critical specification that correlates to gate driver robustness for all isolated gate drivers which handle differential voltage between two separate ground references. This paper will start by explaining these challenges with bench waveform measurement comparison, and then, discussing isolated gate drivers and identifying the benefits by addressing key specifications with the related noise immunity. Finally, the dv/dt (CMTI) and di/dt for isolated gate drivers will be summarized with issue definition, standard requirements, bench characterizations and system design solutions using TI's isolated gate driver family.

2 What is CMTI?

Common mode transient immunity (CMTI) is defined as the maximum tolerable rate of rise or fall of the common mode voltage applied between two isolated circuits. The unit is normally in kV/us or V/ns. High CMTI means that the two isolated circuits, both transmitter side and receiver side, function well within the datasheet specifications without error when striking the insulation barrier with very high rise (positive) slew rate, or high fall (negative) slew rate. A simplified CMTI test setup and the typical common-mode pulse waveform are shown in Figure 1. The IN and OUT signal in the simplified block diagram should always follow the appropriate logic as the datasheet truth-table specified when the VCM pulse applies on the insulation barrier. For CMTI testing, the VCM peak voltage should not exceed the allowed maximum peak transient voltage rating between the two isolated circuits. VDE 0884-11 recommends measuring the slew rate of common-mode pulse calculated from 10% to 90% of the final common-mode pulse (|VCM|). For isolated gate drivers with less than 50V/ns, this 10%/90% suggestion is a rule of thumb since it is less dependent on the test setup parasitics. For example, a 1000V |VCM| peak voltage takes 50ns to ramp up/down assuming there is a linear 20V/ns common-mode pulse slew rate, and around 20ns for a typical 400V bus system. However, for isolated gate drivers with over 100V/ns, this 10%/90% measurement guide is not accurate enough and may lead to significant inaccuracy due to the dependency of all the circuit parasitics. For instance, a 200V/ns common-mode slew rate only takes 5ns for a 1000V |VCM| peak voltage, and only 2ns for a 400V |VCM| peak voltage where the parasitics will come into the picture. The popular influences include MOSFET nonlinear capacitances, PCB trace inductances, parasitic coupling capacitance of isolated power supply, the quadrature error of digital oscilloscope and the input capacitance of the high voltage probes.

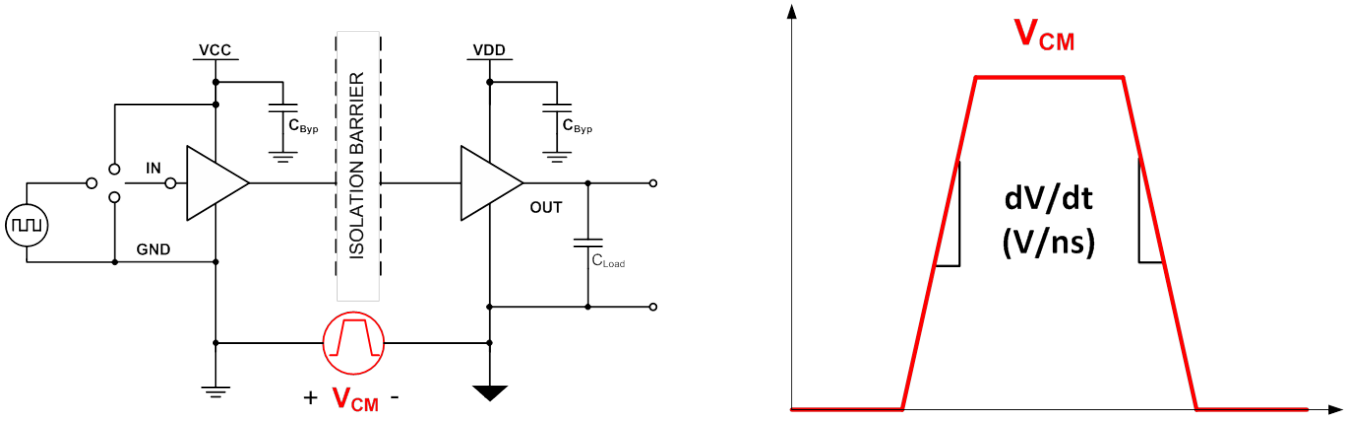

Figure 1. Simplified CMTI Test Setup

Static CMTI is defining a testing condition while the input is tied to either logic high or logic low, and monitors the output state when CMT strike happens. The output should stay in the specified high or low state within the CMTI specifications over the variation of process, voltage and temperature. Figure 2 shows an example of static CMTI measurement, including CMH and CML. For digital isolators which primarily concern the signal integrity, the output should remain at the specified logic-high level or logic-low level. For isolated gate driver applications where the output voltage ties to the power semiconductors, such as MOSFET or GaN, VOH(min) and VOL(max) are typically defined as 80% and 20% of the output VDD power supply. In this case, the power transistor should remain off or on during the common-mode pulse transient.

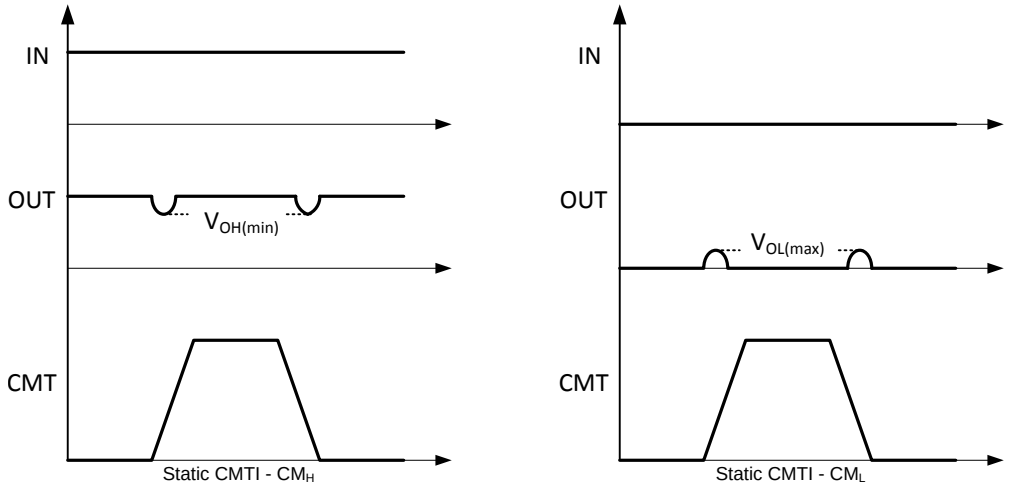

Figure 2. Static CMTI Measurement

While the dynamic CMTI is the maximum slew rate of VCM with switching of the input, either from high to low or low to high, coincident or near to the common mode transient pulse. The criteria are similar to the static CMTI, which means the output should stay in the correct state. Some fault scenarios may include missing pulse, excessive propagation delay, high or low error or output latch, shown in Figure 3. UL and VDE 0884-11 don't specifically discuss the measurement procedure for dynamic CMTI, which is currently an optional specification for digital isolators. However, a customer end power electronics system may test dynamic CMTI of an isolated gate driver by driving a half-bridge for their specified power transistor and then checking the system operation for the possible faults illustrated in .

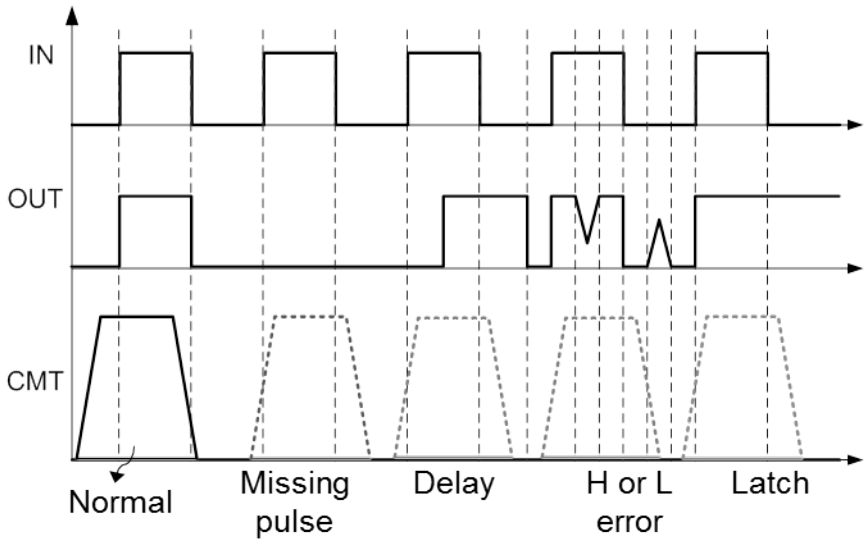

Figure 3. Dynamic CMTI Measurement

3 How to characterize CMTI for isolated gate drivers on the bench

Figure 4 shows a simplified circuit diagram of CMTI characterization for UCC2122x. One way to monitor the output signal in a precise and simple way with a high frequency passive probe is to apply the common-mode pulse in the transmitter side with ground reference in the receiver side, shown as the VSS in green lines in Figure 4. The transmitter side bias is powered from a standalone 28V battery and a programmable LDO voltage adjuster, which is designed to cover the entire VCCI operating range. A high-voltage 1GHz passive probe is used to measure the dv/dt across the two ground references of UCC2122x, GND and VSS. Another way is to apply the common-mode pulse in the receiver side with ground reference in the transmitter side with battery power for VDDA/B. The major challenge of the second solution is that the output signals are floating, which makes it difficult to precisely monitor with a high bandwidth passive probe. High voltage differential probes can be used to measure the output signal in a relatively low bandwidth; however, it would be very difficult to capture the high frequency glitch or logic error.

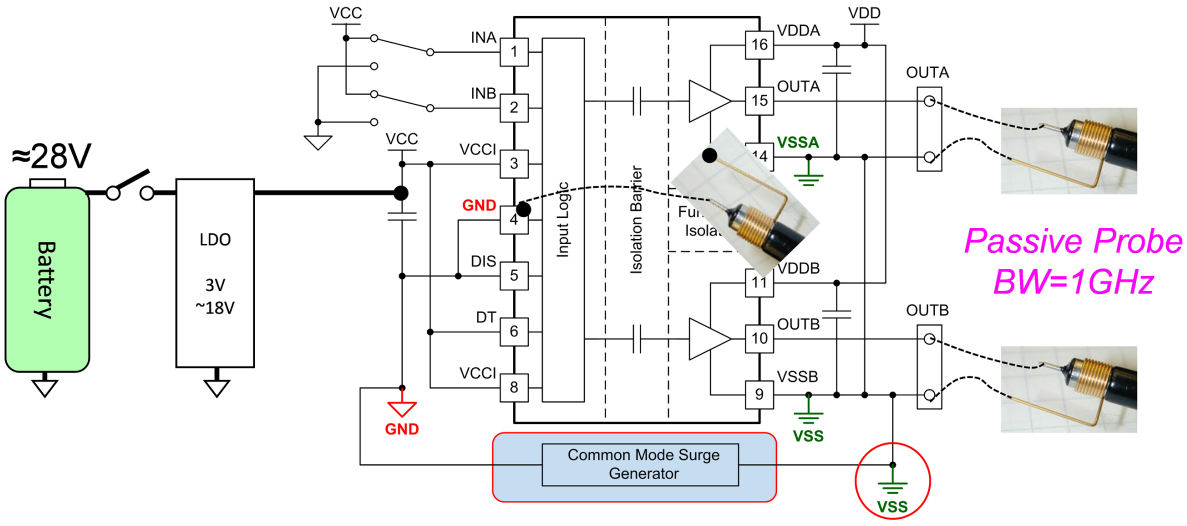

Figure 4. Simplified CMTI Test Setup for UCC2122x

4 Bench Implementation of Common-mode Pulse Generator

Common-mode pulse generators can be implemented in a variety of ways, for example, with an ESD surge generator. However, the common-mode pulse from different setups may not emulate the switching transient that happens in a power electronics system, which is not a perfect textbook waveform as shown in Figure 1. The parasitic inductance and capacitance will introduce fast overshoot, undershoot and high frequency oscillations. Figure 5 shows a positive pulse generator using a boost converter. When the MOSFET is ON, input voltage VChg charges the inductor and builds up the current (1); when the MOSFET is OFF, the inductor current, IL, charges and discharges the output capacitance of the MOSFET and diode (2), COSS and CD. Thus, a rising voltage pulse, VCM, is generated on the switch node. The output voltage of the Boost converter is used to set the |VCM|. Given that time is constant and there is a fixed inductance (3), the dv/dt of VCM is proportional to the input voltage (VChg) (4). Considering the parasitics, a typical experiment common-mode pulse can be found in Figure 5. This waveform is a close match of a practical switching waveform in a power electronics system and is programmable by adjusting a single parameter, VChg. Customers can also add external parasitics, or even replace the power transistor, to adjust the over-/under-shoot.

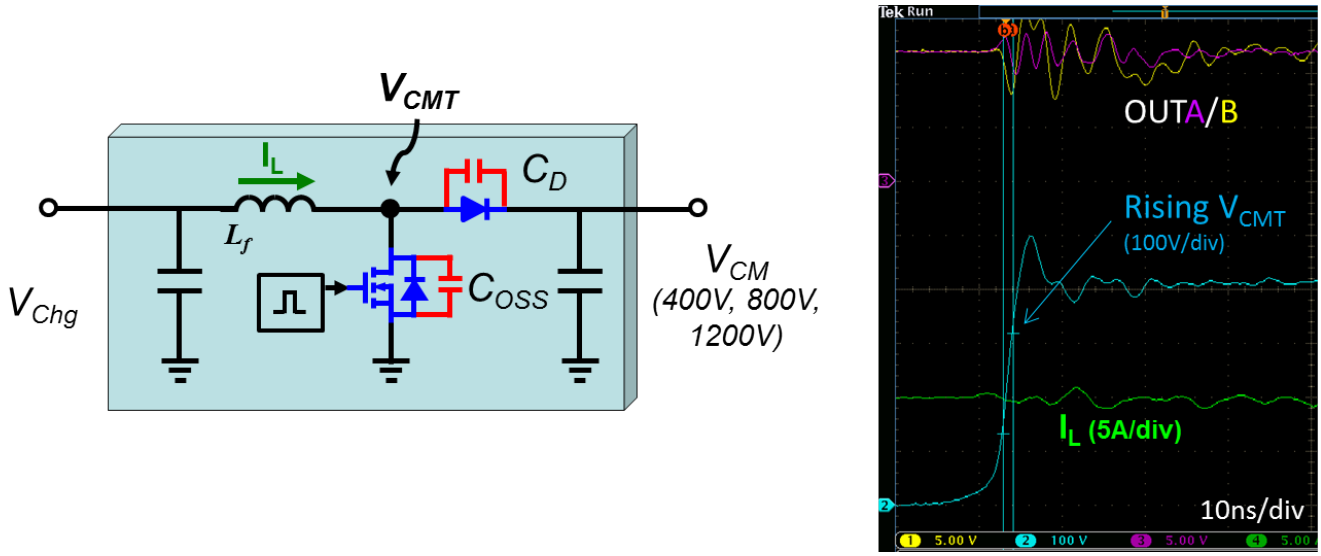

Figure 5. Positive Common-Mode Pulse Generator and typical waveform

$$I_L = \frac{V_{Chg} \cdot T_{ON}}{L_f} \tag{1}$$

$$\frac{dV_{CM}}{dt} = \frac{I_L}{C_{OSS} + C_D} \tag{2}$$

$$\frac{dV_{CM}}{dt} = \frac{V_{Chg} \cdot T_{ON}}{L_f \cdot (C_{OSS} + C_D)} \tag{3}$$

$$\frac{dV_{CM}}{dt} \propto V_{Chg}\big|_{T_{on},\ L_f = Const.} \tag{4}$$

Combining Figure 4 and Figure 5 together, Figure 6 shows a complete positive CMTI test diagram with the switch node tied to the ground reference of the transmitter side. This booster converter can be used as a building block to strike the receiver side if necessary. Following a similar methodology, a buck-boost converter can be used for generating the negative common-mode pulse, shown in Figure 7. The major consideration of this negative pulse generator is that a floating isolated VChg power supply is required, as well as the floating high side MOSFET drive. Here are a few hardware design considerations:

- Select MOSFET, SiC-MOSFET, or GaN with small COSS
- SiC Diode with small CD
- Air core inductor with small parasitic winding capacitance
- Minimization of parasitic capacitive coupling between the two separate ground
- Use floating battery to drive the high side switch for negative CMTI common-pulse generator instead of isolated power supply

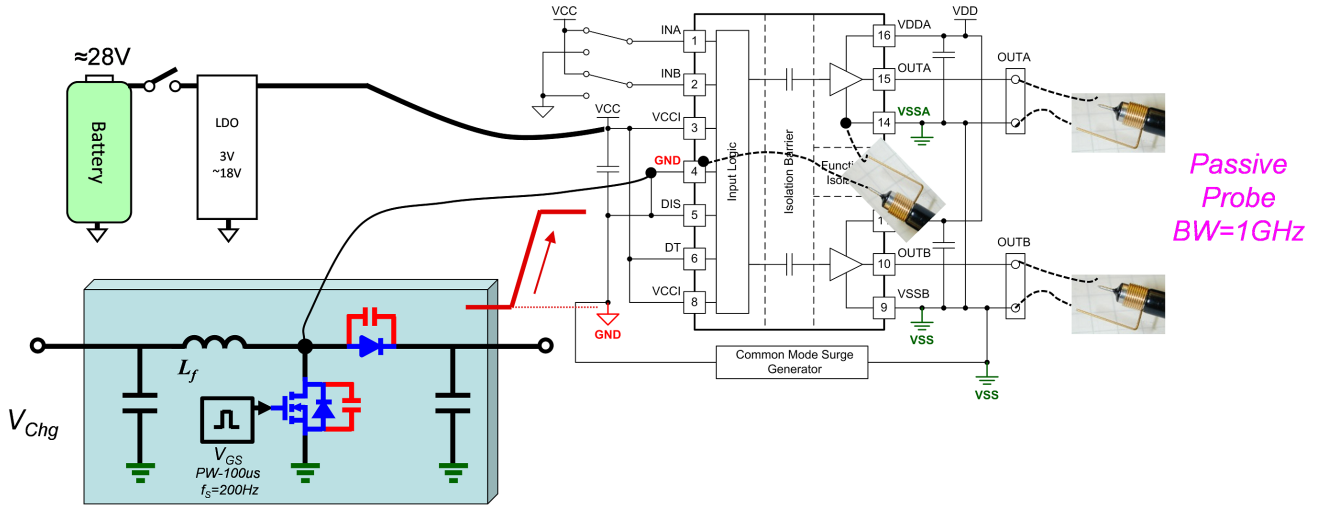

Figure 6. System Diagram for Positive CMTI Characterization

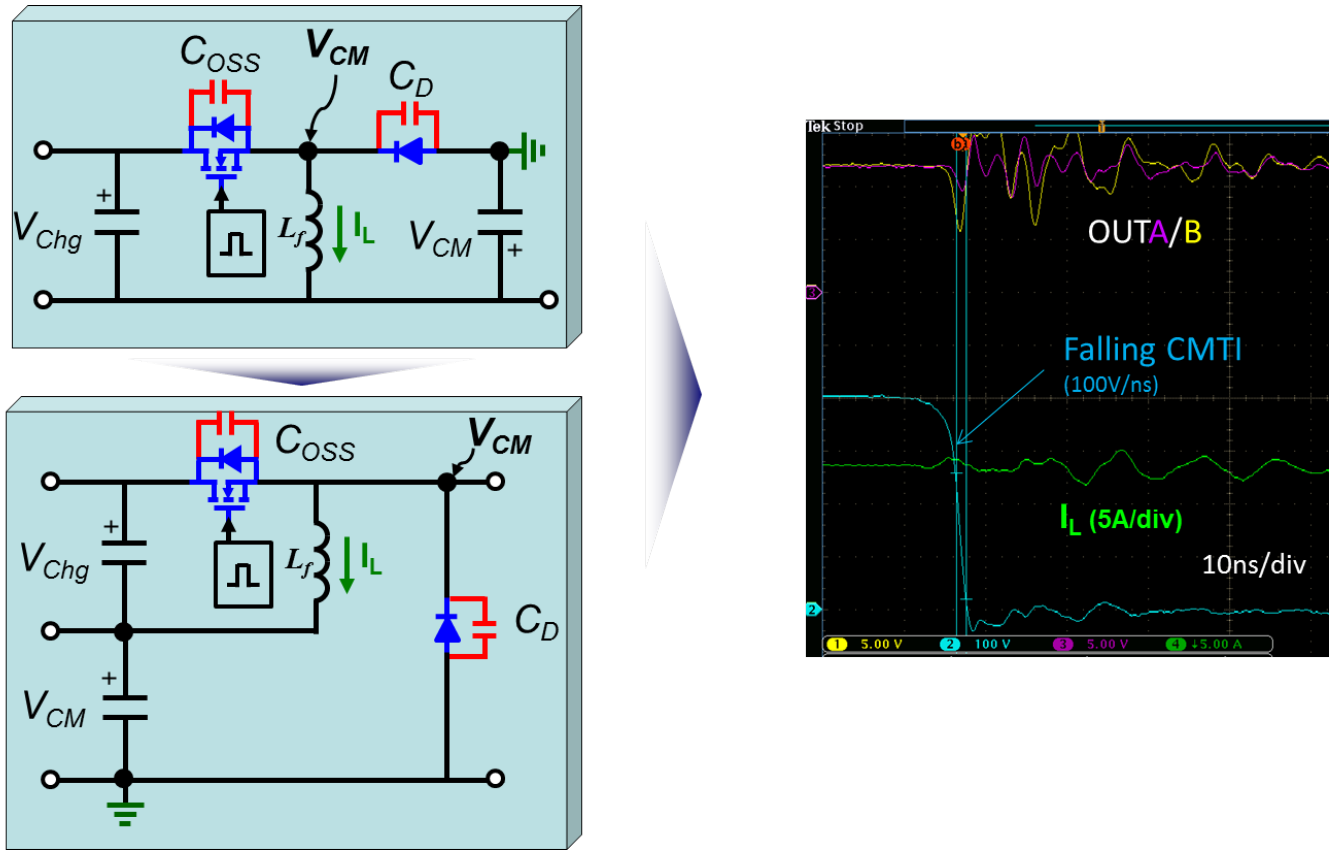

Figure 7. Negative Common-Mode Pulse Generator and Typical Waveform

Another finding during CMTI characterization regards the measurement position. The ideal location would be right across the DUT, at which position it tells the true measurement results and reflects the true silicon performance. However, under temperature characterization, thermal stream is covering the DUT, making it not feasible to probe right on the DUT. To monitor the dv/dt under temperature characterization, another close position is under the mother board, as seen in Figure 8. It is around 1in away from DUT in the final setup. Figure 9 also shows one example of CMTI waveforms measured both across DUT and below the PCB at room temperature at the same common-pulse test condition (pink is measured across DUT which

shows 201V/ns and blue measured below PCB which shows 175V/ns with both probes carefully calibrated). There is a mismatch of 26V/ns, which is caused by the introduced parasitic inductance between DUT and the common-mode pulse generator. Figure 10 summarizes the calibration results for both positive and negative CMTI with vertical axis as CMTI differences, ΔCMTI=CMTIDUT−CMTIPCB, and horizontal axis as the CMTI measured below PCB. The ΔCMTI can be as large as 40V/ns when CMTI is around 200V/ns.

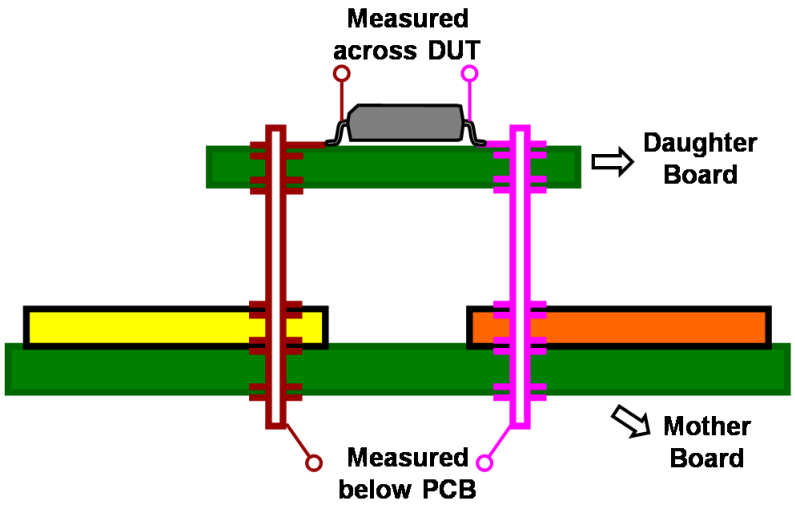

Figure 8. CMTI Measurement Position Across DUT and Below PCB

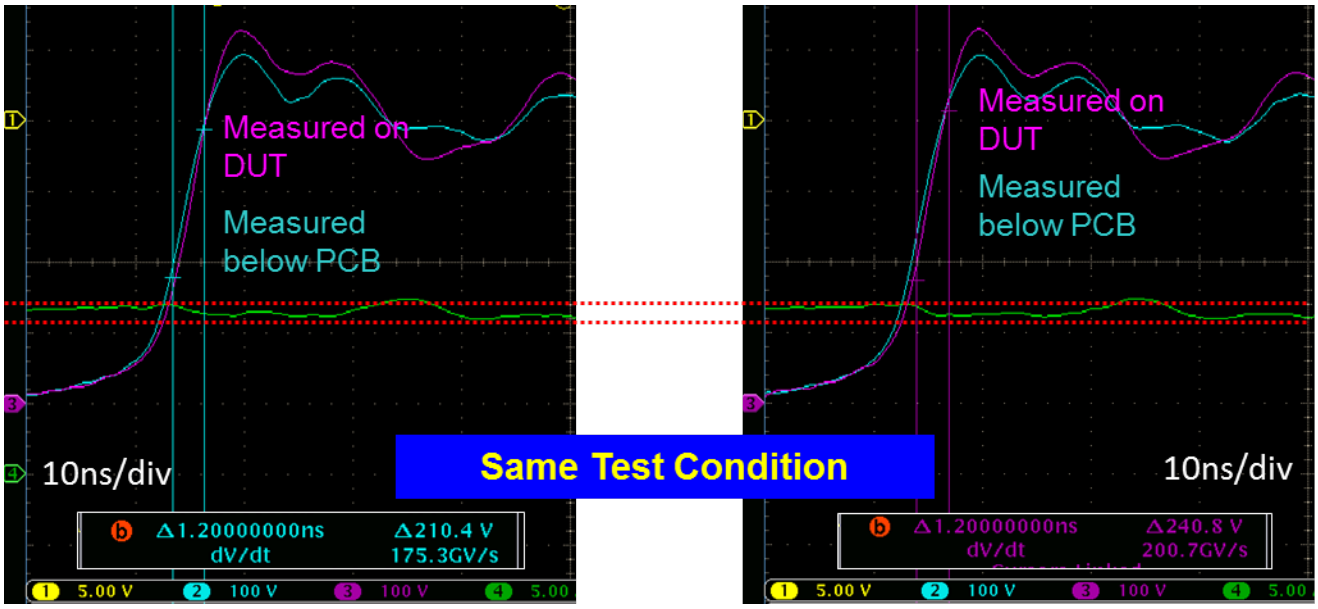

Figure 9. CMTI Measurement Position Across DUT and Below PCB

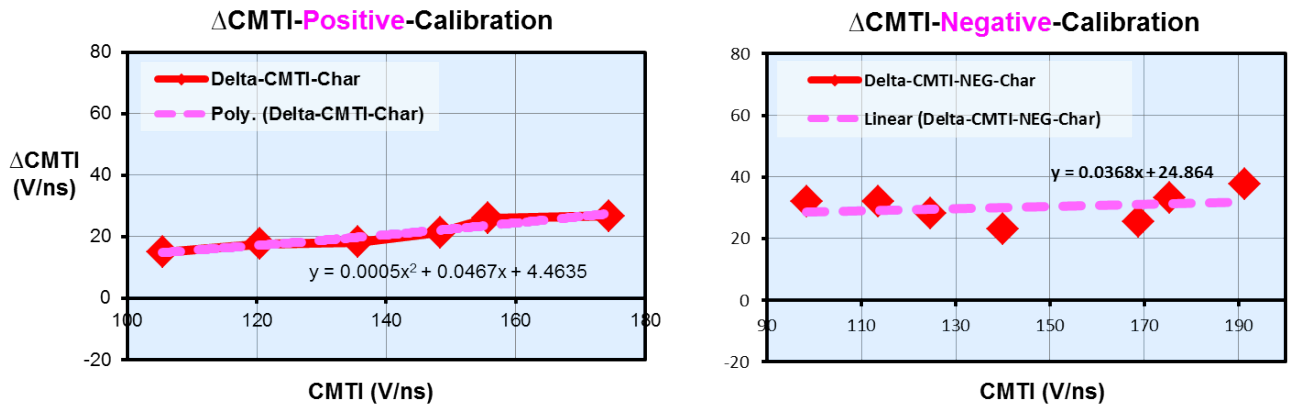

Figure 10. CMTI Measurement Position Calibration

5 Summary

Through the discussion of the definition of CMTI, CMTI system impact, bench implementation of common-mode positive and negative pulse generators, the final CMTI bench setup is able to characterize UCC2122x up to 250V/ns across −40°C~125°C. Figure 11 shows the final test result of CMTI characterization. The lowest CMTI happens at low temperature −40°C, and the highest CMTI is around 250V/ns at 125°C, which demonstrates the robust operation of UCC2122x on a noisy switching environment.

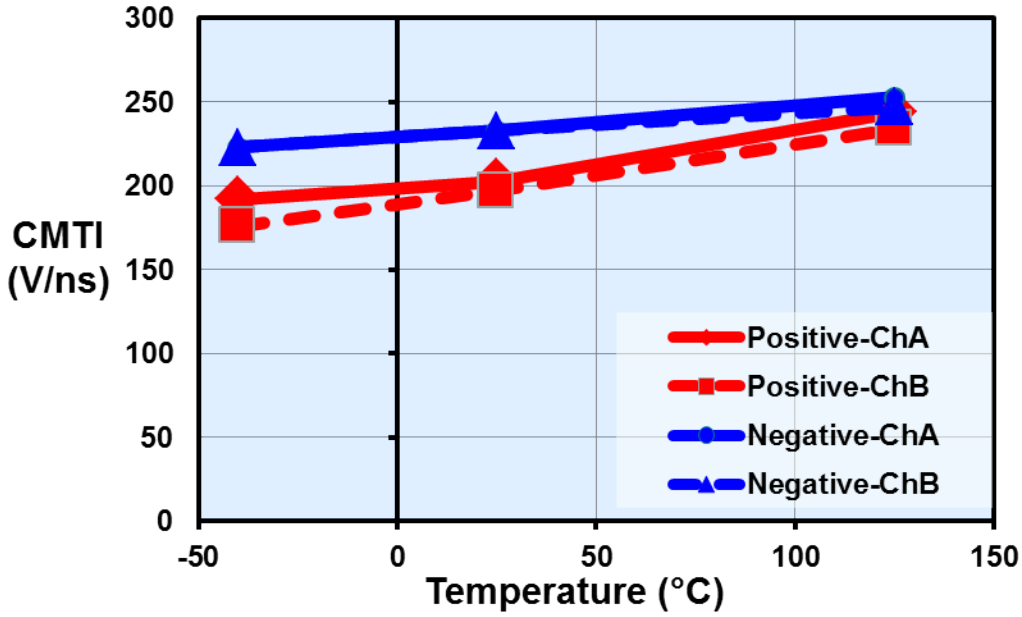

Figure 11. UCC2122x CMTI Characterization Results

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