Application Report
SWRA574B–October 2017–Revised February 2020

AWR2243 Cascade

Anil Kumar K V, Sreekiran, Samala, Karthik Subburaj, Chethan Kumar Y.B.

ABSTRACT

This application report describes TI's cascaded mmWave radar system. This solution is based on TI's AWR2243 radar chip. Using the 20 GHz LO input and output paths, several of these chips are cascaded together and operated synchronously. Each AWR2243 chip supports up to four receive and three transmit antennas. Cascading multiple such chips allows the radar system to operate with more receive and transmit antennas, thereby improving target detection and resolution in comparison with a single AWR2243 radar chip based system. Cascading of two and four AWR2243 chips is illustrated in this application report. This cascaded radar solution is intended to support automotive applications such as Adaptive Cruise Control, Collision Warning, Emergency Braking, and Semi and Fully Autonomous Driving. The system described in this document has been implemented for evaluation in the mmWave cascade imaging radar RF evaluation module (https://www.ti.com/tool/MMWCAS-RF-EVM).

Contents

List of Figures

List of Tables

Trademarks

All trademarks are the property of their respective owners.

1 Cascaded AWR2243 System

Multiple AWR2243 chips may be cascaded on PCB to improve target detection and resolution. In this section, two chip cascading and four chip cascading systems are illustrated as examples. The focus is on connection of various signals that the AWR2243 chips need to share among themselves. Of the multiple AWR2243 chips in the cascaded system, one is referred to as the Master and the others as Slaves. To make the entire cascaded system operate as a single radar system, the Master is designated to generate a common Local Oscillator (LO) signal (19 GHz to 20.25 GHz) shared across all the transmitters and receivers in the entire cascade system. The master also controls the radar chirp/frame timing for all the chips by generating a digital Sync signal and sharing this synchronization signal with the slaves. The master also uses a 40 MHz crystal and generates a 40 MHz oscillator clock (OSC_CLKOUT) and shares it with the slaves (as CLKP), thereby eliminating the need for additional crystals on the slaves and ensuring that the entire system operates from a single clock source.

The master is capable of supplying the shared LO on two different output pins through two different delay matched amplifiers. This can be used in a four chip cascade system to supply the LO signal to the master and three slaves using only passive splitters. This eliminates the need for additional, costly, active components on the PCB. The OSC_CLKOUT pin is used by the master to share the the 40 MHz clock source with the slave devices in the system. In the case of a 2-device system, this can be done with just a passive trace between devices. In the case of more than 2-devices, it is recommended to use a clock fan-out buffer to manage loading and signal integrity issues. Similarly, the DIG_SYNC is conveyed from the master to the slaves and back to itself through delay matched buffers on board.

Other than these connections which are illustrated in the below diagrams and further elaborated in later sections, the cascaded system also has Power Management ICs (PMIC) (each PMIC can handle up to two AWR2243 chips), an optional QSPI Flash (needed for initial software development purpose only) and the mmWave antennas connected to each AWR2243 chip.

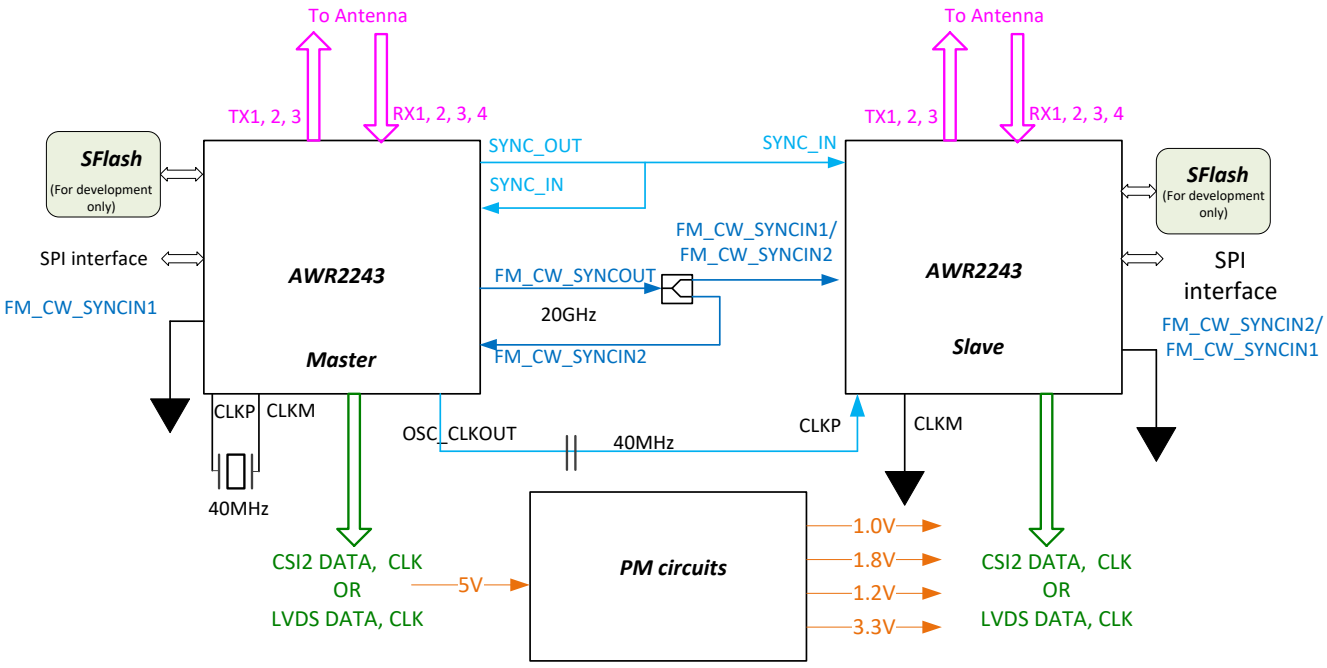


Figure 1. A Two Chip Cascade System

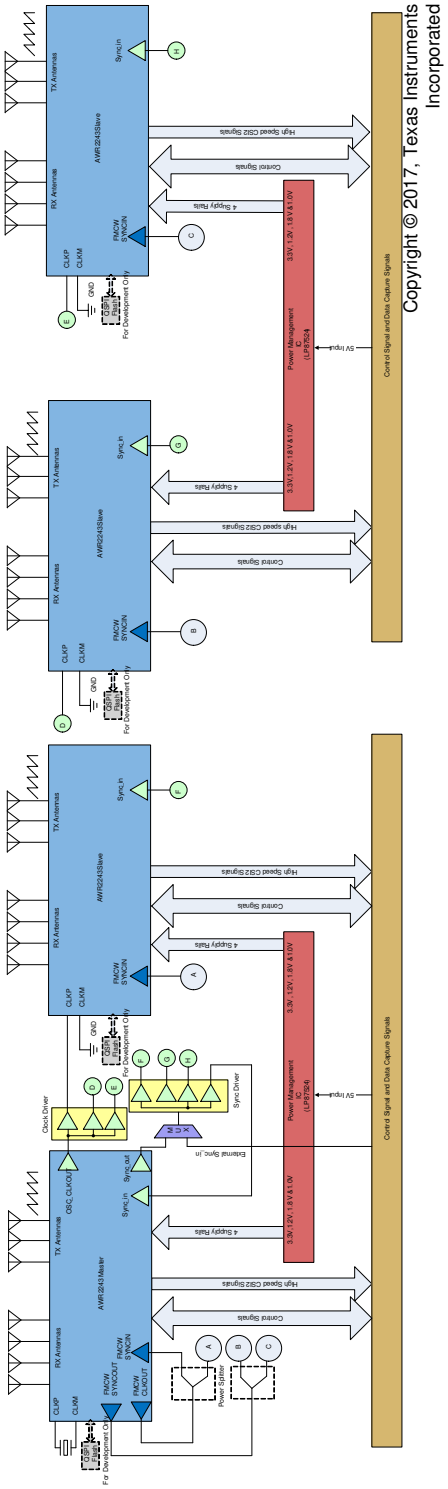


Figure 2. A Four Chip Cascade System

2 Synchronization of AWR2243 Chips

In a cascaded system, there is one Master chip and one or many Slave chips. These cascaded devices are synchronized using the following interfaces:

- 20 GHz (FMCW) RF LO synchronization
- Digital frame timing synchronization
- 40 MHz (System) reference clock synchronization

The 20 GHz (FMCW) RF LO is generated by the master chip and distributed to the slaves and the master. The relevant signals/pins are referred to as FM_CW_SYNCx/CLKx or 20 GHz LO in this document.

The frame timing synchronization is controlled by either the master chip, in the case of software message based frame trigger, or by the host processor, in the case of hardware based frame trigger. The relevant signals/pins are referred to as SYNC_IN/OUT or DIG_SYNC_IN/OUT in this document.

The 40 MHz system clock may be generated by either the master chip or externally supplied. The relevant pins are OSC_CLKOUT, CLKP and CLKM.

Detailed description on syncing is given in the following sections.

2.1 20 GHz (FMCW) RF LO Sync

Figure 3 shows the 20 GHz section of the AWR2243 chip.

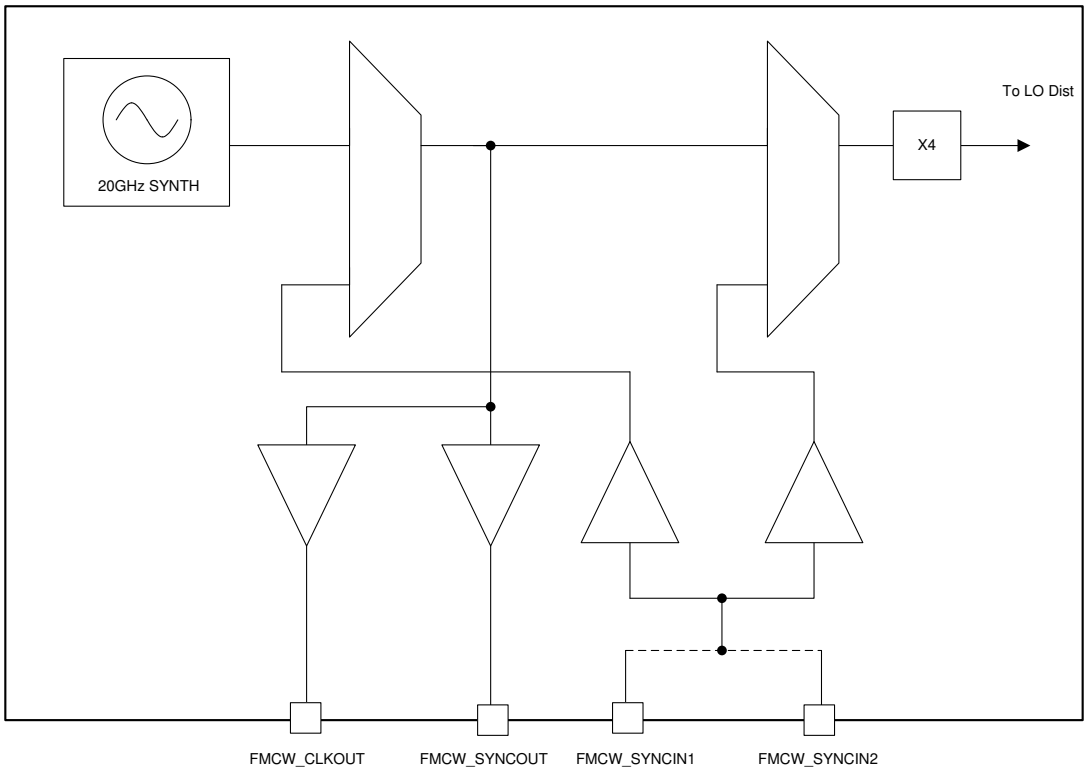


Figure 3. 20 GHz Mux Options in the Chip

All AWR chips should have their RF LO frequencies synchronized. The AWR2243 synthesizer generates LO between 19 GHz and 20.25 GHz, depending on the programmed chirp RF output frequencies. This LO frequency is multiplied by 4 in each chip to generate RF in the 76-81 GHz band. The 20 GHz LO carries the chirp modulation.

The AWR2243 device supports a star LO distribution topology.

In this star distribution topology, the Master LO is divided on the PCB and fed to Slave and Master chips in a star fashion. The LO distribution network is routed on the PCB to produce the same delay for all LO traces. This results in all Slave chips and Master chips receiving the LO with the same delay applied. The Master receives its own LO back from the LO divider so that it can be delay-matched to the Slave chips as well.

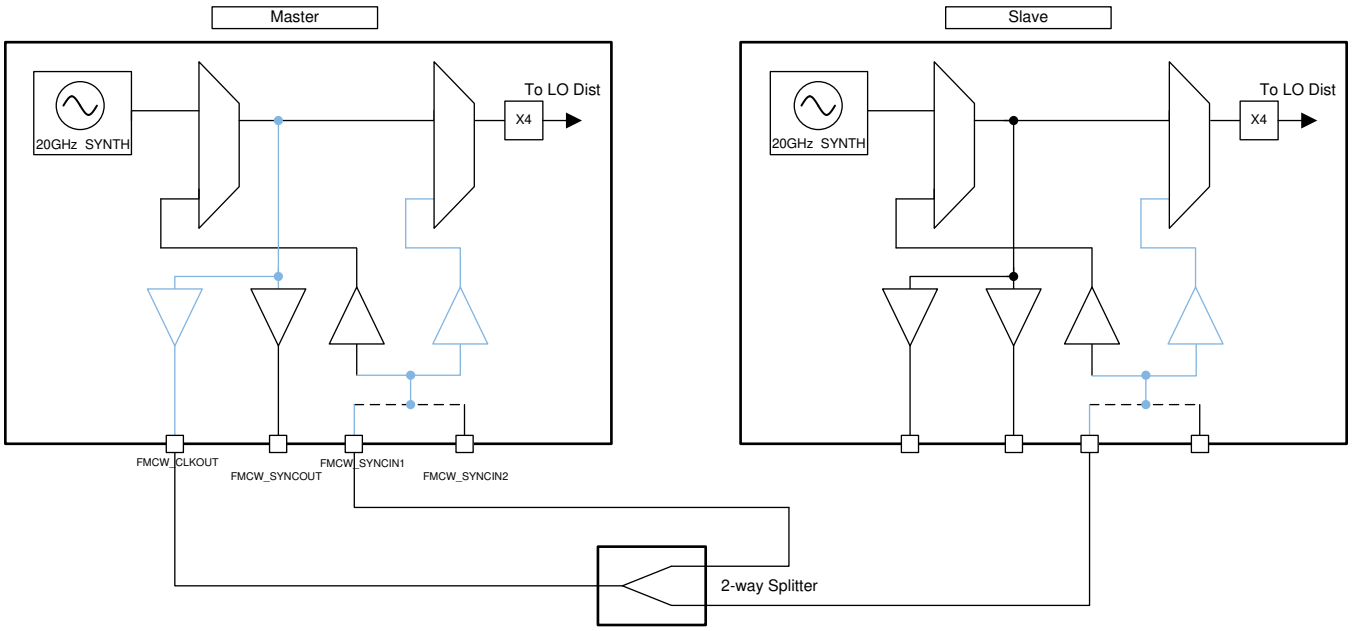


Figure 4. Example of LO Distribution in 2-Chip Star Topology

2.2 Digital Frame Sync

In a cascaded system, it is necessary to synchronize the RX ADC sampling windows between all chips. Frame Sync, described in this section, ensures coherence of ADC samples from all the chips and alignment of the chirp timing signals across the constituent chips.

Note that “Frame (Burst)” in this section refers to frames (as defined in AWR_FRAME_CONF_SB) and bursts (as defined in AWR_ADVANCED_FRAME_CONF_SB).

2.2.1 Frame (Burst) and Chirp Timing in AWR2243

The AWR2243 device includes a frame reference counter (FRC) which maintains timing across frames (bursts). It generates a digital synchronization (labeled "Dig Sync" in Figure 5) signal, also referred to as frame (burst) start signal based on the frame (burst) timing parameters given by the API messages described in the Software Messaging section. The processor firmware also relies on the FRC to schedule calibrations, monitoring and setting up of functional bursts.

The AWR2243 device also includes a high speed synchronizer and clock gator, which starts off the high speed clocks to the RX ADCs and chirp timing engine in synchronism with Dig Sync. The chirp timing engine maintains the timing during and across multiple chirps within each frame (burst) and accounts for the generation of synthesizer ramp and RX ADC valid data picking, and so forth. At the end of each frame (burst), the clocks are stopped by the processor. This is illustrated in the timing and block diagrams below in single chip usage example.

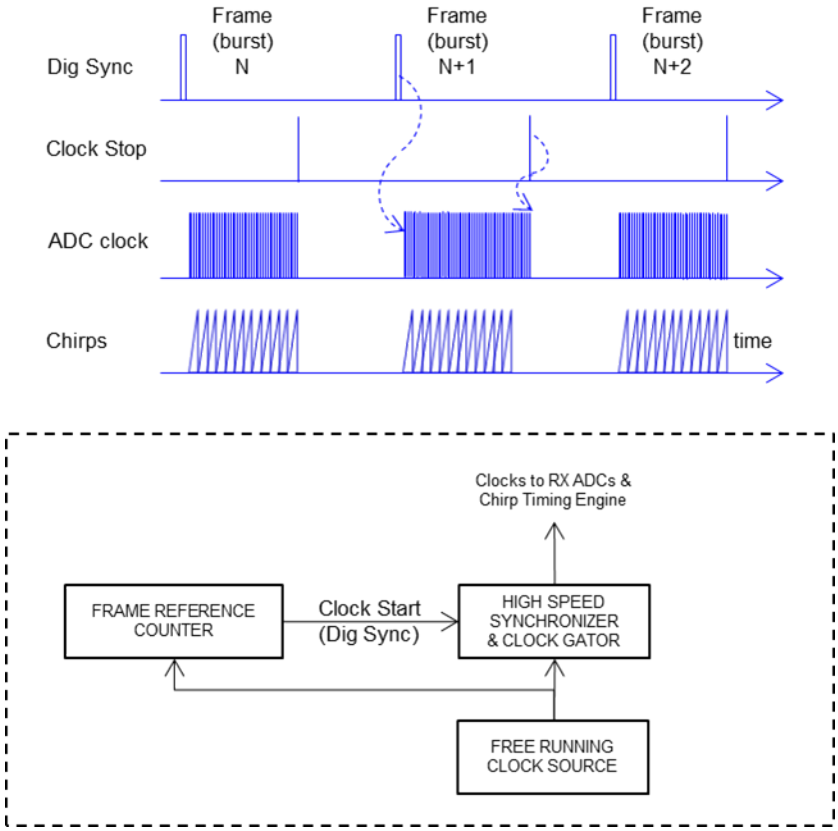


Figure 5. Frame (Burst) Timing and Clock Generation in AWR2243

2.2.2 Frame (Burst) and Chirp Timing in a Cascaded System

In a cascaded system, the FRC and chirp timing engines of the constituent chips are operated in synchronously. The master chip FRC generates the Dig Sync signal. Dig Sync is routed out of the master and fed to the slaves as well as back to the master to match the skew between master and slave chips. As illustrated in Figure 7 (2 chip cascade example), the Dig Sync is synchronized and used to ungated the clocks to all the RX ADC and chirp timing engines in the master and slaves, thereby ensuring timing alignment across chips. It also ensures that the processor firmware in the master and slaves run in (within 5 ns to 10 ns uncertainty). PCB routing of the Dig Sync signal should be delay matched for best alignment between master and slave chips.

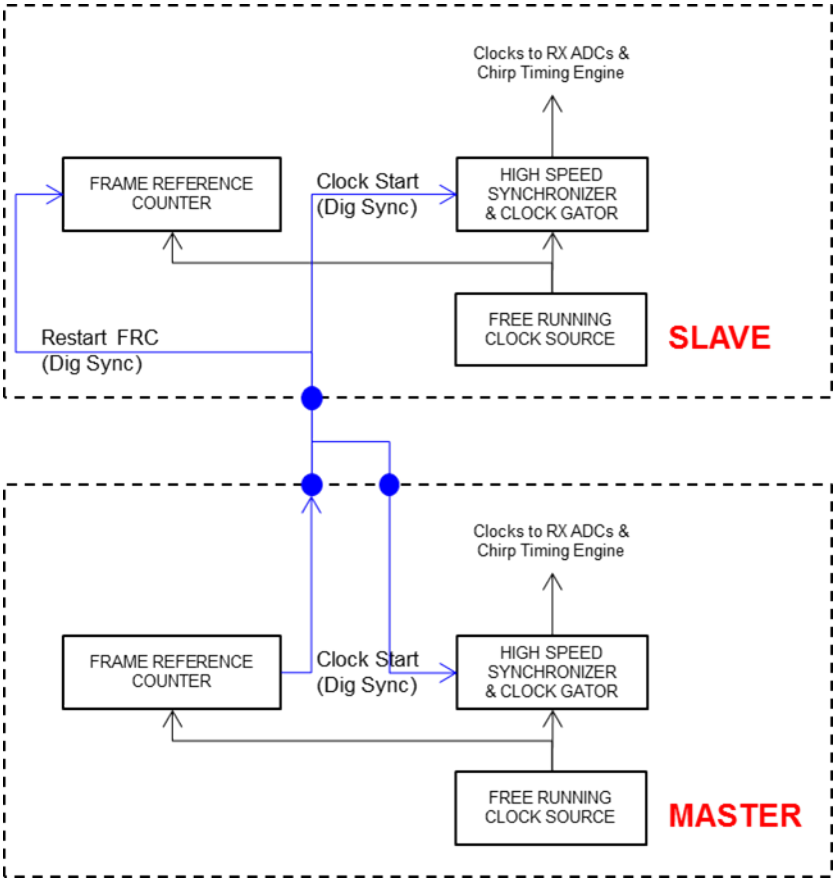


Figure 6. Frame (Burst) Timing Generation in Two Chip Cascade Example

2.2.3 Inter Chip Imbalance of Digital Sync Timing

Ideally, the DIG_SYNC_IN (shown as Dig Sync in Figure 6) reaching the relevant circuits in all chips is balanced in delay, resulting in perfect timing synchronization of chirps. But practically, there are delay imbalances across different AWR2243 devices in a cascaded system. Most of this delay imbalance is due to manufacturing process variation among the AWR2243 devices. Some delay imbalance is due to temperature differences across the devices. Further there is a one clock uncertainty in the synchronizer circuit in each device for each occurrence of the DIG_SYNC_IN pulse. These imbalances are summarized in Table 1.

Table 1. DIG_SYNC_IN Imbalance Summary

DIG_SYNC_IN Inter-Chip Imbalance Type	Total Inter-Chip Imbalance Magnitude
Imbalances due to chip process + voltage differences in a given cascade board	Up to 4 ns approximately
Imbalances due to chip temperature differences in a given cascade board (up to 40°C)	Up to 0.6 ns approximately
Imbalances due to synchronization uncertainty	Either 0 or 0.55 ns (1)

(1) This is variable on each occurrence of the DIG_SYNC_IN pulse. The numbers provided assume that the ADC is operated in regular mode. In low power operation these numbers should be doubled due to the ADC clock frequency being half of the regular mode.

2.3 40 MHz (System) Reference Clock Synchronization

The master reference clock for the system is 40 MHz clock. Typically Master chip generates this clock and distributes to Salve chips. Alternatively, an external source can supply clock to both Master and Slave chips. There is no phase/delay matching requirements on this clock. The Phase Noise requirement is very important when 40 MHz clock is fed externally.

3 Connectivity

3.1 20 GHz LO Sync Pins Connectivity

Table 2 shows the recommended combinations of pins to be used in 20 GHz LO sync on Master chip when the LO feeds back into the same chip.

Table 2. Recommended Combinations of Pins to be Used in 20 GHz LO

Combination	Master LO Output	Master LO Input	Ground
1	FM_CW_SYNCOUT [D1]	FM_CW_SYNCIN2 [D15]	FM_CW_SYNCIN1 [B1]
2	FM_CW_CLKOUT [B15]	FM_CW_SYNCIN1 [B1]	FM_CW_SYNCIN2 [D15]

General guidelines on 20 GHz routing:

- Keep the LO routing distance as small as possible.
- LO Input ports: There are two LO input ports. These are labeled FM_CW_SYNCIN1 and FM_CW_SYNCIN2. These two ports are provided to aid routing of the LO distribution on the PCB. Only one input port can be used at a time. The unused port must be shorted to ground directly at the BGA
- LO Output Ports: There are two LO output ports. Either port can be used or both ports can be used. Unused LO output ports should be left floating at the BGA pad.

3.2 DIG_SYNC Connectivity

The Master chip uses the SYNC_OUT [P11] pin to generate the sync signal. SYNC_OUT feeds into Slaves SYNC_IN [N10]. When more than two chips are cascaded, it is recommended that a clock buffer is used for distribution of SYNC_OUT signal. One of the buffer outputs feeds back into Master chip for delay matching.

3.3 40 MHz (System) Reference Clock Connectivity

In the case when the Master chip sources the reference clock for the other Slave devices, the OSC_CLKOUT [A14] pin of the Master is used. OSC_CLKOUT feeds into the CLKP [E14] pin of the Slave chips. The OSC_CLKOUT signal is an approximately 1.3 V to ground square wave output. It can be dc-coupled or ac-coupled to the CLKP pin of Slave chip. The max input level at CLKP is 1.8 V when dc-coupled and 1.2 Vpp when ac-coupled.

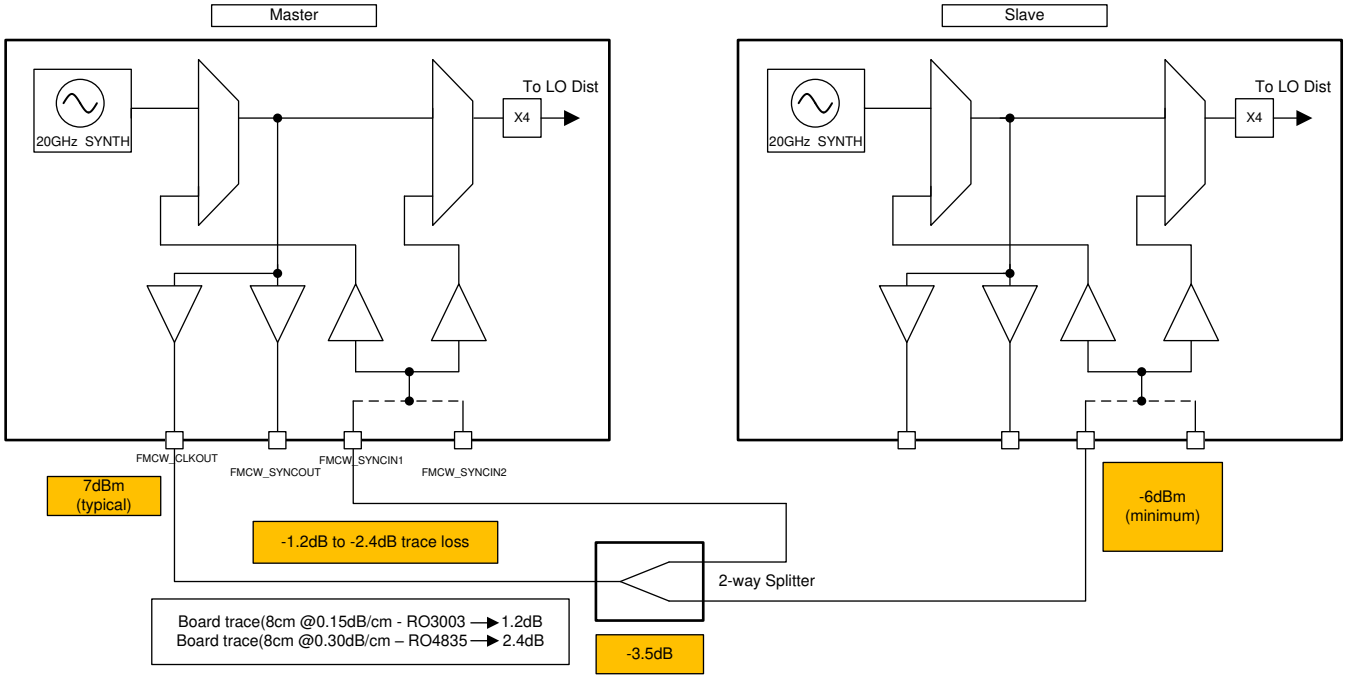
When more than two chips are cascaded, it is recommended to use a clock fan-out buffer to generate the clocks for Slave devices.

4 20 GHz LO Sync Link Budget

Given below is a typical link budget for the 20 GHz LO distribution. Two types of board losses are assumed:

- Rogers RO3003 with rolled copper
- Rogers RO4835 LoPro.

Length of 20 GHz trace is assumed as 8cm.



(1) For more information, see the *AWR2243 Single-Chip 76- to 81-GHz FMCW Transceiver Data Sheet*, RF Specification table, for all LO input and output specifications.

Figure 7. 20 GHz LO - Link Budget

5 Software Messaging

The AWR2243 devices involved in a cascaded system can be controlled through software API messages and that is the focus of this section. The Interface Control Document (ICD) [1] contains the details of the API messages supported by AWR2243. Further, the application report [2], Programming Chirp Parameters in TI Radar Devices explains the typical software configuration in a single chip context. The information provided in it is valid in a cascaded chips system too. This section mainly provides the incremental information applicable to the cascaded chip system, along with brief repetition of some important information covered in the application report [2].

5.1 Configuration of Devices

The AWR2243 devices in a cascaded chip system need to be configured as either MULTICHIP_MASTER or MULTICHIP_SLAVE. This can be done through the message AWR_CHAN_CONF_SET_SB. Note that the message allows a SINGLECHIP option, typically applicable only to single chip systems.

Only one AWR2243 device should be configured as MULTICHIP_MASTER. This AWR2243 device is the master chip and generates FMCW LO and conveys to other MULTICHIP_SLAVE AWR2243 devices in the cascaded chip system.

Typically, the MULTICHIP_MASTER's DIG_SYNC_OUT pin is connected to the DIG_SYNC_IN pins of all the AWR2243 devices in the cascaded chip system. This allows the timing of chirps to be synchronous across the AWR2243 devices.

5.2 Configuration of Frames

The important parameters related to FMCW chirp configuration are explained in the section on Configurable Chirp RAM and Chirp Profiles in the application report [2]. These include the FMCW chirp's start frequency, slope, duration, RX gain, sampling rate, transmitter output power and phase shift. These parameters are programmed to the devices using the messages AWR_PROFILE_CONF_SET_SB (profile configuration), AWR_CHIRP_CONF_SET_SB (chirp configuration) and AWR_FRAME_CONF_SET_SB (frame configuration.

The profile configuration message programs the radar front end parameters for up to four profiles and these parameters are static during the frame. The frame configuration message defines the structure and ordering of a set of chirps constituting a frame, along with frame repetition rate and number of frames requested. The chirps themselves are defined using the chirp configuration message and the definition includes an association of each chirp to one of the defined profiles, the TX channels to be enabled and the TX phase. Further, the chirp configuration message allows incremental but independent chirp to chirp dithering of some parameters even if the chirps are associated with the same profile. The dither-able parameters include idle time, FMCW start frequency and FMCW slope.

Some parameters need to be configured similarly across all the AWR2243 devices in the cascaded system while others can be dissimilar. They are detailed in Section 5.2.1.

5.2.1 Similar Configuration Across AWR2243 Devices

All the timing and frequency parameters are expected to be configured exactly similarly to all AWR2243 devices in the cascaded chip system through the profile configuration message. The timing parameters refer to: Idle Time, Ramp End Time, RX ADC sampling rate, sampling start time and number of ADC samples per chirp. The frequency parameters refer to: Start Frequency and FMCW slope. Further, the timing parameters conveyed through the frame configuration message also need to match across the devices. These include the frame periodicity and number of frames to be generated.

Typically, the incremental dithering of the timing parameters configured through chirp configuration messages are also expected to be similar across the AWR2243 devices. Further, note that the frequency dithering parameters have no meaning in the slave devices as it is only the master which generates the LO signal based on the frequency parameters.

The similarity of timing parameters across AWR2243 devices ensures that the MULTICHIP_SLAVES get ready for each frame in time after completing fully or partially any calibration or monitoring that they may be engaged in during the inter frame times. The similarity of frequency parameters across AWR2243 devices ensures validity of calibration results during actual chirps, given that there may be RF subsystems may have RF frequency dependent performance.

5.2.2 Dissimilar Configuration Across AWR2243 Devices

The TX channel enables, BPM configuration given through chirp configuration messages may differ across the AWR2243 devices during the same chirp. The same is true for TX phase shift setting too if per-chirp phase shift is enabled. Variations in parameters such as RX gain and TX power are also acceptable through dissimilar profile configuration messages across the AWR2243 devices.

5.3 Triggering of Frames

The frames can be triggered using the frame trigger message, AWR_FRAME_TRIG_MSG.

The frame configuration message, briefly introduced in an earlier section, allows configuring frames to be triggered directly using the frame trigger message (SWTRIGGER mode) or through high pulses on the hardware pin, called SYNC_IN or DIG_SYNC, subsequent to the reception of the frame trigger message (HWTRIGGER mode). The SWTRIGGER mode has an associated triggering uncertainty of several tens of microseconds (the frame repetition rate has no uncertainty). The HWTRIGGER mode has much lower triggering uncertainty, detailed in a subsequent section.

In cascaded chip systems, typically, the MULTICHIP_SLAVE devices are configured in HWTRIGGER mode and get triggered by the MULTICHIP_MASTER device. The MULTICHIP_MASTER device is typically triggered in SWTRIGGER mode.

Typically, the host processor needs to issue the frame trigger message to the slave devices to get them ready to receive the DIG_SYNC_IN from the master device. After receiving the acknowledgment, the host processor can issue the frame trigger message to the master device. This starts off a series of frames (as many as programmed in the frame configuration message) and for each such frame, the master device generates a high pulse on its DIG_SYNC_OUT pin, which, through the DIG_SYNC_IN pins, causes all the chips to start the chirp timing, transmission and reception synchronously.

5.4 Example Usage

The important parameters that are configured to AWR2243 devices in a two chip cascade system are tabulated here, to illustrate usage possibilities. Although only two devices are shown here, the example can be expanded to more devices (one of them being a master and others being slaves).

Table 3. Channel Configuration Message

Parameter	Device 1	Device 2
Cascade Configuration	MULTICHIP_MASTER	MULTICHIP_SLAVE

Table 4. Profile Configuration Message

Parameter	Device 1	Device 2
Profile 1 Start Frequency	77 GHz	77 GHz
Profile 1 FMCW Slope	30 MHz/µs	30 MHz/µs
Profile 1 Idle Time	10 µs	10 µs
Profile 1 Ramp End Time	30 µs	30 µs
Profile 1 Sampling Rate, no. of samples	5 MSPS, 128	5 MSPS, 128
Profile 1 TX power (backoff)	0 dB	2 dB
Profile 2 Start Frequency	78 GHz	78 GHz
Profile 2 FMCWC Slope	60 MHz/µs	60 MHz/µs
Profile 2 Idle Time	15 µs	15 µs
Profile 2 Ramp End Time	60 µs	60 µs
Profile 2 Sampling Rate, no. of samples	5 MSPS, 256	5 MSPS, 256
Profile 2 TX power (backoff)	0 dB	2 dB

Table 5. Chirp Configuration Message

	Profile Index		TX_ENABLE (TX1,2,3)		TX (1,2,3) BPM (Degrees)		Idle Time Dither	
Chirp Index	Device 1	Device 2	Device 1	Device 2	Device 1	Device 2	Device 1	Device 2
0	1	1	1,0,0	0,0,0	0,0,0	0,0,0	0 µs	0 µs
1	1	1	0,1,0	0,0,0	0,0,0	0,0,0	2 µs	2 µs
2	1	1	0,0,1	0,0,0	0,0,0	0,0,0	0.5 µs	0.5 µs
3	1	1	0,0,0	1,0,0	0,0,0	0,0,0	1 µs	1 µs
4	1	1	0,0,0	0,1,0	0,0,0	0,0,0	1.5 µs	1.5 µs
5	1	1	0,0,0	0,0,1	0,0,0	0,0,0	0 µs	0 µs
6	1	1	1,0,0	0,0,0	180,0,0	0,0,0	0 µs	0 µs
7	1	1	0,1,0	0,0,0	0,180,0	0,0,0	2 µs	2 µs
8	1	1	0,0,1	0,0,0	0,0,180	0,0,0	0.5 µs	0.5 µs
9	1	1	0,0,0	1,0,0	0,0,0	180,0,0	1 µs	1 µs
10	1	1	0,0,0	0,1,0	0,0,0	0,180,0	1.5 µs	1.5 µs
11	1	1	0,0,0	0,0,1	0,0,0	0,0,180	0 µs	0 µs
12	2	2	1,0,0	0,0,0	0,0,0	0,0,0	0 µs	0 µs
13	2	2	0,1,0	0,0,0	0,0,0	0,0,0	2 µs	2 µs
14	2	2	0,0,1	0,0,0	0,0,0	0,0,0	0.5 µs	0.5 µs
15	2	2	0,0,0	1,0,0	0,0,0	0,0,0	1 µs	1 µs
16	2	2	0,0,0	0,1,0	0,0,0	0,0,0	1.5 µs	1.5 µs
17	2	2	0,0,0	0,0,1	0,0,0	0,0,0	0 µs	0 µs
18	2	2	1,0,0	0,0,0	180,0,0	0,0,0	0 µs	0 µs
19	2	2	0,1,0	0,0,0	0,180,0	0,0,0	2 µs	2 µs
20	2	2	0,0,1	0,0,0	0,0,180	0,0,0	0.5 µs	0.5 µs
21	2	2	0,0,0	1,0,0	0,0,0	180,0,0	1 µs	1 µs
22	2	2	0,0,0	0,1,0	0,0,0	0,180,0	1.5 µs	1.5 µs
23	2	2	0,0,0	0,0,1	0,0,0	0,0,180	0 µs	0 µs

NOTE: The timing dither parameters are different chirp to chirp but similar for both devices.

Table 6. Frame Configuration Message

Parameter	Device 1	Device 2
Start Chirp Index	0	0
End Chirp Index	23	23
Number of loops	8	8
Frame Periodicity	50 ms	50 ms
Number of Frames	100	100
Trigger Mode	SWTRIG	HWTRIG

The frame trigger messages are given in this order:

1. Issue frame trigger message to device 2 (and to other slave devices if more are present)
2. Receive acknowledgment from device 2 (and other slave devices)
3. Issue frame trigger message to device 1 (master)

With this, the desired number of frames gets generated from all AWR2243 devices in the cascaded system in tandem.

5.5 Other Usages

Although only some usages are explained in detail, minor variations are possible. They are briefly described here.

It is possible to trigger all AWR2243 devices (including the master) in HWTRIGGER mode. For this, the host needs to generate DIG_SYNC_IN pulses of the right periodicity and feed to DIG_SYNC_IN pins of all the chips (including the master).

Most of the above note is written using the basic frame configuration message, namely AWR_FRAME_CONF_SB, for easing the explanation. It is possible to use AWR_ADVANCED_FRAME_CONF_SB for achieving more advanced chirp or frame structures. In such a case, the DIG_SYNC_IN pulse occurs at the beginning of each burst (or sub frame or frame – to be determined). If such an advanced frame configuration is used in conjunction with SWTRIGGER of the master too, then the host needs to generate the pulses accordingly.

6 Advantages of AWR2243 Cascading System

The AWR2243 cascaded solution presented in this application report offers many key advantages.

The AWR2243 integrates 20 GHz PA (power amplifier) and LNA (low-noise amplifier) along the LO path that eliminates the need for discrete PA and LNA along the PCB transmission lines. Each AWR2243 device incorporates separate 20 GHz PA for each LO output path (one PA for FMCW_CLKOUT and another for FMCW_SYNCOUT) and separate LNA for each internal branch of the FMCW_SYNCIN1/2 LO input path. The 20 GHz LO routing on the PCB can be minimized through use of the multiple FMCW_CLKOUT/SYNCOUT LO output ports and FMCW_SYNCIN1/2 LO input ports, which are both located on opposite sides of the BGA. Further, the frequency for on board LO routing has been optimally chosen. Routing the 20 GHz LO instead of the 80 GHz mmWave signal on board enables minimizing of board routing loss, noise and cost.

Although only a few topologies of two chip and four chip cascading have been illustrated these examples can be extended to cascaded systems using more than four chips. Overall, the features explained here enable design and manufacturing of a high performance radar system with low cost, size and power consumption.

7 References

1. *AWR2243 Interface Control Document (ICD)*
2. Texas Instruments: *Programming Chirp Parameters in TI Radar Devices*
3. Texas Instruments: *AWR2243 Single-Chip 76- to 81-GHz FMCW Transceiver Data Sheet*
4. MMWCAS-RF-EVM product page

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (December 2017) to B Revision	Page
• Changed AWR1243 to AWR2243 throughout the document.	1
• Update was made in the Abstract of this document.	1
• Updates were made in Section 1.	2
• Update was made in Section 2.2.3.	8
• Updates were made in Section 5.1.	10
• Update was made in Section 5.2.1.	10
• Updates were made in Section 5.2.2.	10
• Update was made in Section 6.	13

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265