LMR33630 SIMPLE SWITCHER® 3.8V 至 36V、 3A 同步降压转换器

1 特性

- 专用于条件严苛的工业 应用
  - 输入电压范围：3.8V 至 36V
  - 输出电压范围：1V 至 24V
  - 输出电流：3A
  - 75mΩ/50mΩ R_{DS-ON} 功率 MOSFET
  - 峰值电流模式控制
  - 最短导通时间很短，只有 68ns
  - 频率：400kHz、1.4MHz、2.1MHz
  - 结温范围为 –40°C 至 +125°C
  - 低 EMI 和低开关噪声
  - 集成补偿网络
- 高效解决方案
  - 峰值效率 > 95%
  - 低至 5µA 的关断静态电流
  - 低至 25µA 的工作静态电流
- 灵活的系统接口
  - 电源正常状态标志和精密使能端
- 使用 LMR33630 并借助 WEBENCH® 电源设计器创建定制设计

2 应用

- 电机驱动系统：无人机、交流逆变器、变频驱动器、伺服系统
- 工厂和楼宇自动化系统：PLC CPU、HVAC 控制、电梯控制
- 通用宽输入电压电源

3 说明

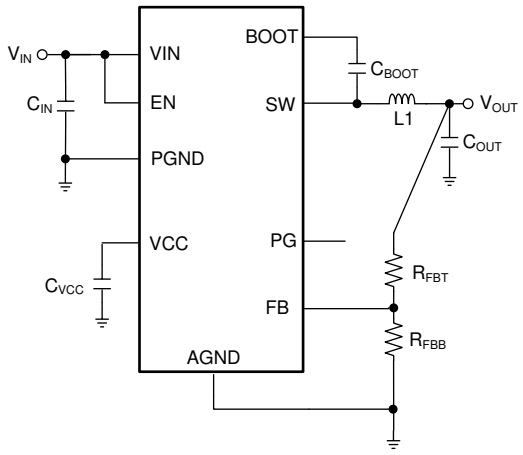
LMR33630 SIMPLE SWITCHER® 稳压器是一款简单易用的同步降压直流/直流转换器，可提供业界一流的效率，适用于条件严苛的工业 应用。 LMR33630 能够使用高达 36V 的输入电压驱动高达 3 A 的负载电流。LMR33630 解决方案以极小的尺寸提供出色的轻负载效率和输出精度。诸如 电源正常状态标志和精密使能端等特性有助于实现灵活而又易用的解决方案 - 适用于广泛的 应用。LMR33630 在轻负载时自动折返频率以提高效率。此器件通过集成技术消除了大多数外部组件，并提供专为实现简单 PCB 布局而设计的引脚排列方式。保护 功能 包括热关断、输入欠压锁定、逐周期电流限制和断续短路保护。LMR33630 采用 8 引脚 HSOIC 封装和具有可湿性侧面的 12 引脚 3mm × 2mm VQFN 封装。该器件还具有符合 AEC-Q100 标准的版本。

器件信息(1)

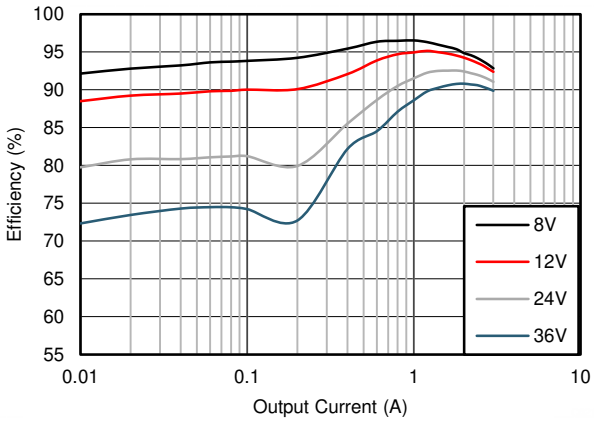
器件型号	封装	封装尺寸（标称值）
LMR33630	HSOIC (8)	5.00mm × 4.00mm
LMR33630	VQFN (12)	3.00mm × 2.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化原理图



效率与输出电流间的关系
V_{OUT} = 5V，400kHz，VQFN



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (June 2018) to Revision D **Page**

- Changed heading to device option ... 3
- Changed Minimum peak current to reflect ATE data. ... 8
- Changed zero cross to reflect ATE data. ... 8
- 已更改 to new current limit equation ... 16
- 已添加 new de-rate curve ... 26

Changes from Revision B (April 2018) to Revision C **Page**

- 已添加 graphs for Typical Switching Frequency in Dropout Mode ... 19

Changes from Revision A (February 2018) to Revision B **Page**

- 已添加 在整个数据表中添加了 WSON 信息 ... 1
- 已更改 block diagram to fix drawing error ... 12
- 已添加 添加了 RNX 封装图 ... 39

Changes from Original (August 2017) to Revision A **Page**

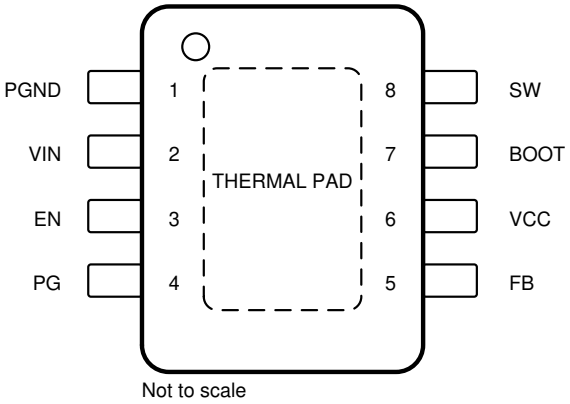
- 第一版生产数据数据表 ... 1

5 Device Comparison Table

DEVICE OPTION	PACKAGE	FREQUENCY	RATED CURRENT	OUTPUT VOLTAGE
LMR33630ADDA	DDA (8-pin HSOIC) 5 × 4 mm	400 kHz	3 A	Adjustable
LMR33630BDDA		1400 kHz	3 A	
LMR33630CDDA		2100 kHz	3 A	
LMR33630ARNX	RNX (12-pin VQFN) 3 × 2 × 0.85 mm	400 kHz	3 A	Adjustable
LMR33630BRNX		1400 kHz	3 A	
LMR33630CRNX		2100 kHz	3 A	

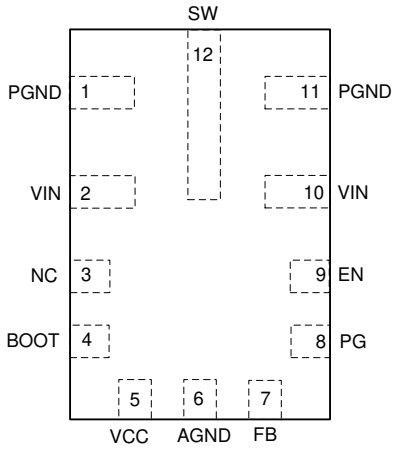
6 Pin Configuration and Functions

DDA Package
8-Pin HSOIC With PowerPAD™
Top View



Not to scale

RNX Package
12-Pin VQFN
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
HSOIC	VQFN	NAME		
1	1,11	PGND	G	Power ground terminal. Connect to system ground and AGND. Connect to bypass capacitor with short wide traces.
2	2,10	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitor(s) directly to this pin and PGND.
3	9	EN	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN; DO NOT FLOAT.
4	8	PG	A	Open drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. Flag pulls low when EN = Low. Can be left open when not used.
5	7	FB	A	Feedback input to regulator. Connect to tap point of feedback voltage divider. DO NOT FLOAT. DO NOT GROUND.
6	5	VCC	P	Internal 5-V LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND.
7	4	BOOT	P	Boot-strap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin. On the VQFN package connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin.
8	12	SW	P	Regulator switch node. Connect to power inductor. On the VQFN package connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin.
THERMAL PAD	6	AGND	G	Analog ground for regulator and system. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB. For the HSOIC package, the pad on the bottom of the device serves as both the AGND connection and a thermal connection to the heat sink ground plane. This pad must be soldered to a ground plane to achieve good electrical and thermal performance.
—	3	NC	—	On the VQFN package the SW pin must be connected to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin. This pin has no internal connection to the regulator.
A = Analog, P = Power, G = Ground				

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range(1)

PARAMETER		MIN	MAX	UNIT
Voltages	VIN to PGND	–0.3	38	V
	EN to AGND(2)	–0.3	V_{IN} + 0.3	
	FB to AGND	–0.3	5.5	
	PG to AGND(2)	0	22	
	AGND to PGND	–0.3	0.3	
	SW to PGND	–0.3	V_{IN} + 0.3	V
	SW to PGND less than 100-ns transients	–3.5	38	
	BOOT to SW	–0.3	5.5	
	VCC to AGND(3)	–0.3	5.5	
T_J	Junction temperature(4)	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V
(3) Under some operating conditions the VCC LDO voltage may increase beyond 5.5V.
(4) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) (1)	±2500	V
		Charged-device model (CDM) (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating temperature range of –40 °C to 125 °C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	3.8	36	V
	EN (2)	0	V_{IN}	
	PG(2)	0	18	
Adjustable output voltage	V_{OUT}(3)	1	24	V
Output current	I_{OUT}	0	3	A

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see *Electrical Characteristics*.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
(3) The maximum output voltage can be extended to 95% of V_{IN}; contact TI for details. Under no conditions should the output voltage be allowed to fall below zero volts.

7.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see *Maximum Ambient Temperature* section.

THERMAL METRIC(1) (2)		LMR336x0		UNIT
		DDA (HSOIC)	RNX (VQFN)	
		8 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.9(2)	72.5(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	35.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.6	23.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.3	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.8	23.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see *Maximum Ambient Temperature* section.

7.5 Electrical Characteristics

Limits apply over the operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Minimum operating input voltage				3.8	V
I_Q	Non-switching input current; measured at VIN pin (1)	V_{FB} = 1.2 V		24	34	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	EN = 0		5	10	µA
ENABLE						
$V_{EN-VCC-H}$	EN input level required to turn on internal LDO	Rising threshold			1	V
$V_{EN-VCC-L}$	EN input level required to turn off internal LDO	Falling threshold	0.3			V
V_{EN-H}	EN input level required to start switching	Rising threshold	1.2	1.231	1.26	V
V_{EN-HYS}	Hysteresis below V_{EN-H}	Hysteresis below V_{EN-H}; falling		100		mV
I_{LKG-EN}	Enable input leakage current	V_{EN} = 3.3 V		0.2		nA
INTERNAL SUPPLIES						
VCC	Internal LDO output voltage appearing at the VCC pin	6 V ≤ V_{IN} ≤ 36 V	4.75	5	5.25	V
$V_{BOOT-UVLO}$	Bootstrap voltage undervoltage lock-out threshold(2)			2.2		V
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage; ADJ option		0.985	1	1.015	V
I_{FB}	Current into FB pin; ADJ option	FB = 1 V		0.2	50	nA
CURRENT LIMITS(3)						
I_{SC}	High-side current limit	LMR33630	3.85	4.5	5.05	A
I_{LIMIT}	Low-side current limit	LMR33630	2.9	3.5	4.1	A

(1) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(2) When the voltage across the C_{BOOT} capacitor falls below this voltage, the low side MOSFET is turned on to recharge C_{BOOT}.
(3) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

Electrical Characteristics (continued)

Limits apply over the operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PEAK-MIN}$	Minimum peak inductor current	LMR33630		0.69		A
I_{ZC}	Zero current detector threshold			-0.106		A
SOFT START						
t_{SS}	Internal soft-start time		2.9	4	6	ms
POWER GOOD (PG PIN)						
$V_{PG-HIGH-UP}$	Power-good upper threshold - rising	% of FB voltage	105%	107%	110%	
$V_{PG-HIGH-DN}$	Power-good upper threshold - falling	% of FB voltage	103%	105%	108%	
$V_{PG-LOW-UP}$	Power-good lower threshold - rising	% of FB voltage	92%	94%	97%	
$V_{PG-LOW-DN}$	Power-good lower threshold - falling	% of FB voltage	90%	92%	95%	
t_{PG}	Power-good glitch filter delay(4)		60		170	µs
R_{PG}	Power-good flag R_{DSON}	V_{IN} = 12 V, V_{EN} = 4 V		76	150	Ω
		V_{EN} = 0 V		35	60	
V_{IN-PG}	Minimum input voltage for proper PG function	50-µA, EN = 0 V			2	V
V_{PG}	PG logic low output	50-µA, EN = 0 V, V_{IN} = 2V			0.2	V
OSCILLATOR						
f_{SW}	Switching frequency	"A" Version	340	400	460	kHz
f_{SW}	Switching frequency	"B" Version	1.2	1.4	1.6	MHz
f_{SW}	Switching frequency	"C" Version, DDA package	1.8	2.1	2.4	MHz
f_{SW}	Switching frequency	"C" Version, RNX package	1.8	2.1	2.3	MHz

(4) See *Power-Good Flag Output* for details.

Electrical Characteristics (continued)

Limits apply over the operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOSFETS						
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	RNX package		75	145	mΩ
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	DDA package		95	160	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	RNX package		50	95	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	DDA package		66	110	mΩ

7.6 Timing Characteristics

Limits apply over the operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

			MIN	NOM	MAX	UNIT
t_{ON-MIN}	Minimum switch on-time	RNX package		68	80	ns
t_{ON-MIN}	Minimum switch on-time	DDA package		75	108	ns
$t_{OFF-MIN}$	Minimum switch off-time	RNX package		52	70	ns
$t_{OFF-MIN}$	Minimum switch off-time	DDA package		50	85	ns
t_{ON-MAX}	Maximum switch on-time			7	9	µs

7.7 System Characteristics

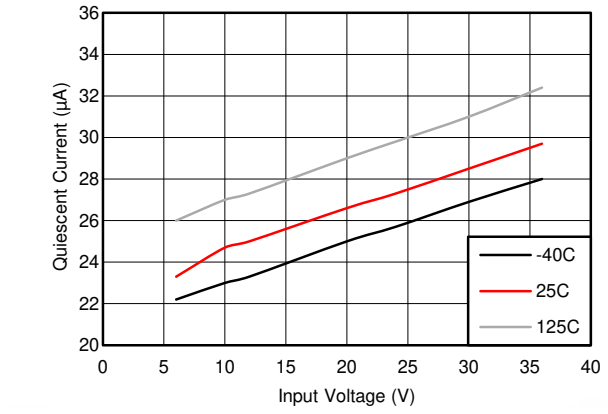
The following specifications apply to a typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 125°C. *These specifications are not ensured by production testing.*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage range	V_{OUT} = 3.3 V, I_{OUT}= 0 A	3.8		36	V
V_{OUT}	Output voltage regulation for V_{OUT} = 5 V(1)	V_{OUT} = 5 V, V_{IN} = 7 V to 36 V, I_{OUT} = 0 A to max. load	–1.5%		2.5%	
		V_{OUT} = 5 V, V_{IN} = 7 V to 36 V, I_{OUT} = 1 A to max. load	–1.5%		1.5%	
	Output voltage regulation for V_{OUT} = 3.3 V(1)	V_{OUT} = 3.3 V, V_{IN} = 3.8 V to 36 V, I_{OUT} = 0 A to max. load	–1.5%		2.5%	
		V_{OUT} = 3.3 V, V_{IN} = 3.8 V to 36 V, I_{OUT} = 1 A to max. load	–1.5%		1.5%	
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A, R_{FBT} = 1 MΩ		25		µA
V_{DROP}	Dropout voltage; (V_{IN} – V_{OUT})	V_{OUT} = 5 V, I_{OUT} = 1A Dropout at –1% of regulation, f_{SW} = 140 kHz		150		mV
D_{MAX}	Maximum switch duty cycle(2)	V_{IN} = V_{OUT} = 12 V, I_{OUT} = 1 A		98%		
V_{HC}	FB pin voltage required to trip short-circuit hiccup mode			0.4		V
t_{HC}	Time between current-limit hiccup burst			94		ms
t_D	Switch voltage dead time			2		ns
T_{SD}	Thermal shutdown temperature	Shutdown temperature		165		°C
		Recovery temperature		148		°C

(1) Deviation is with respect to V_{IN} =12 V, I_{OUT} = 1 A.
(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: f_{MIN} = 1 / (t_{ON-MAX} + $t_{OFF-MIN}$). D_{MAX} = t_{ON-MAX} /(t_{ON-MAX} + $t_{OFF-MIN}$).

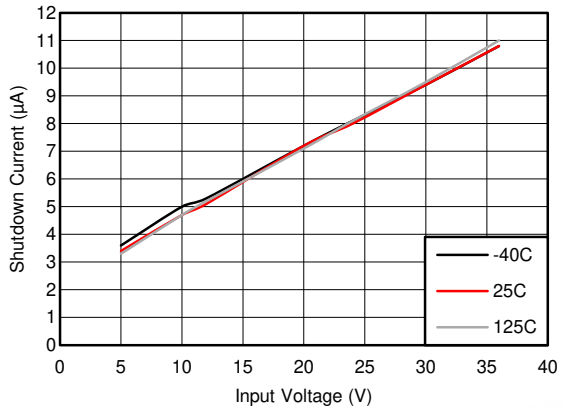
7.8 Typical Characteristics

Unless otherwise specified the following conditions apply: T_A = 25°C and V_{IN} = 12 V



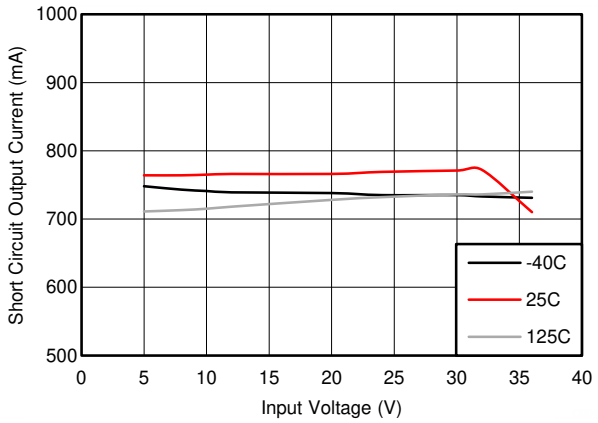
V_{FB} = 1.2 V

图 1. Non-Switching Input Supply Current



EN = 0 V

图 2. Shutdown Supply Current



V_{OUT} = 0 V f_S = 400 kHz See 图 50

图 3. Short-Circuit Output Current

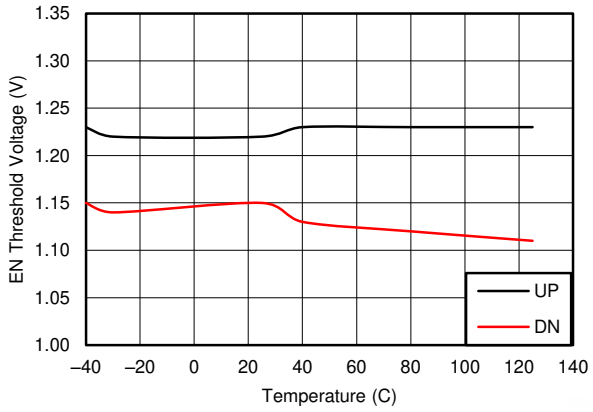
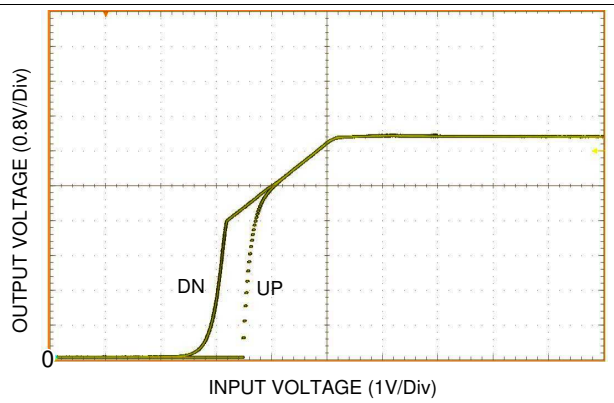
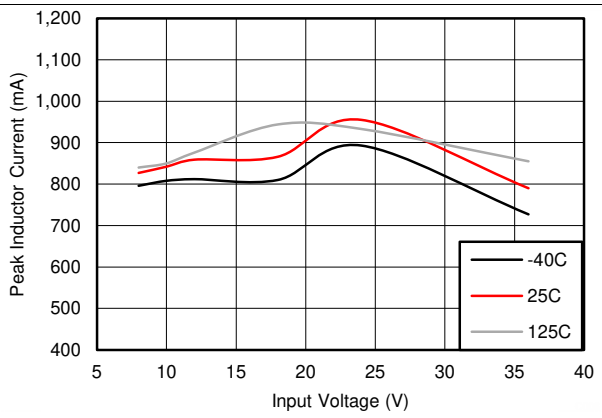


图 4. Precision Enable Thresholds



I_{OUT} = 1 mA See 图 50

图 5. UVLO Thresholds



I_{OUT} = 0 A V_{OUT} = 5 V See 图 50
f_{SW} = 400 kHz

图 6. $I_{PEAK-MIN}$

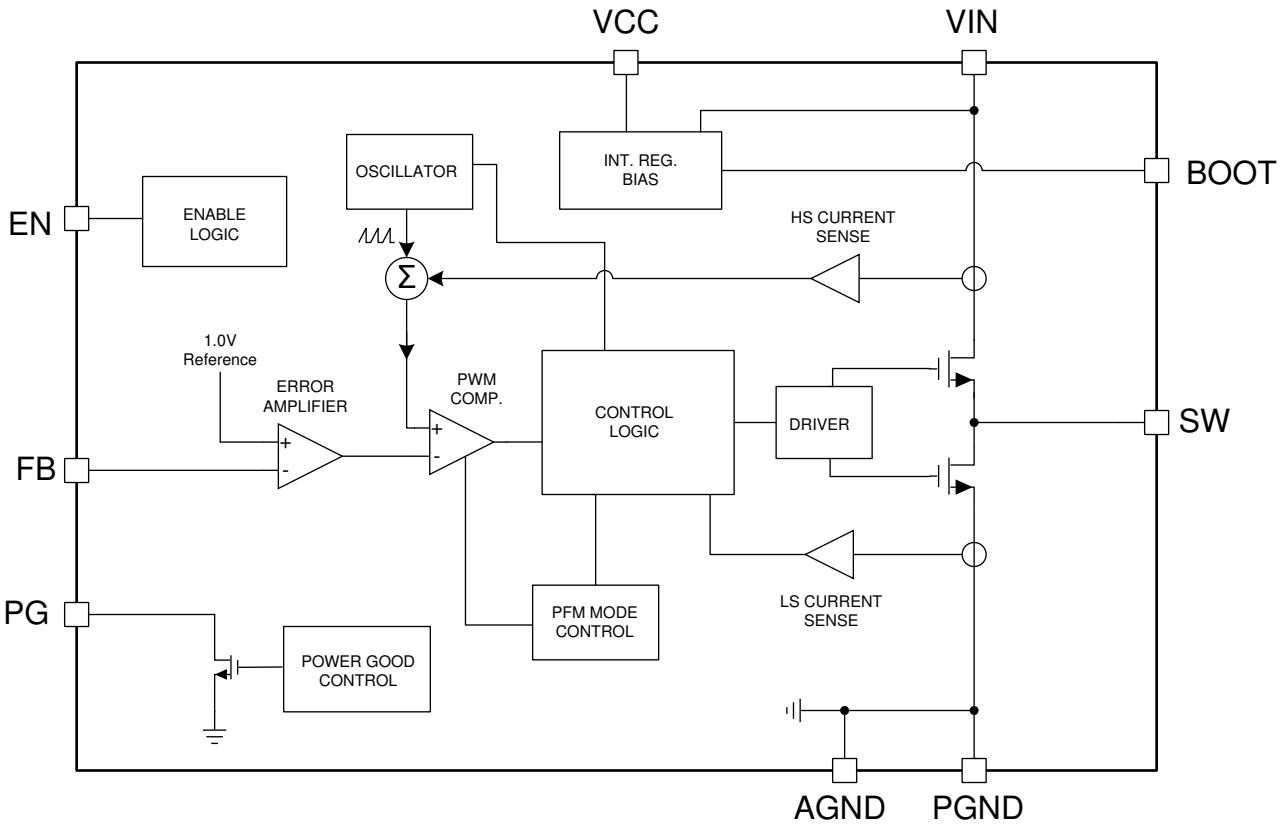
8 Detailed Description

8.1 Overview

The LMR33630 is a synchronous peak-current-mode buck regulator designed for a wide variety of industrial applications. Advanced high speed circuitry allows the device to regulate from an input voltage of 20 V, while providing an output voltage of 3.3 V at a switching frequency of 2.1 MHz. The innovative architecture allows the device to regulate a 3.3 V output from an input of only 3.8 V. The regulator automatically switches modes between PFM and PWM depending on load. At heavy load, the device operates in PWM at a constant switching frequency. At light loads the mode changes to PFM, with diode emulation allowing DCM. This reduces the input supply current and keeps efficiency high. The device features internal loop compensation which reduces design time and requires fewer external components than externally compensated regulators.

The LMR33630 is available in an ultra-miniature VQFN package with wettable flanks. This package features extremely small parasitic inductance and resistance, enabling very high efficiency while minimizing switch node ringing and dramatically reducing EMI. The VIN/PGND pin layout is symmetrical on either side of the VQFN package. This allows the input current magnetic fields to partially cancel, resulting in reduce EMI generation.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power-Good Flag Output

The power-good flag function (PG output pin) of the LMR33630 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output goes low under fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. The timing parameters of the glitch filter are found in the *Electrical Characteristics* table. Output voltage excursions lasting less than t_{PG} do not trip the power-good flag. Power-good operation can best be understood by reference to 图 7 and 图 8. Note that during initial power-up a delay of about 4 ms (typical) is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

The power-good output consists of an open drain NMOS; requiring an external pull up resistor to a suitable logic supply. It can also be pulled up to either VCC or V_{OUT}, through a 100-kΩ resistor, as desired. If this function is not needed, the PG pin should be left floating. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is ≥ 2 V (typical). Limit the current into the power-good flag pin to less than 5 mA D.C. The maximum current is internally limited to about 35 mA when the device is enabled and, about 65 mA when the device is disabled. The internal current limit protects the device from any transient currents that may occur when discharging a filter capacitor connected to this output.

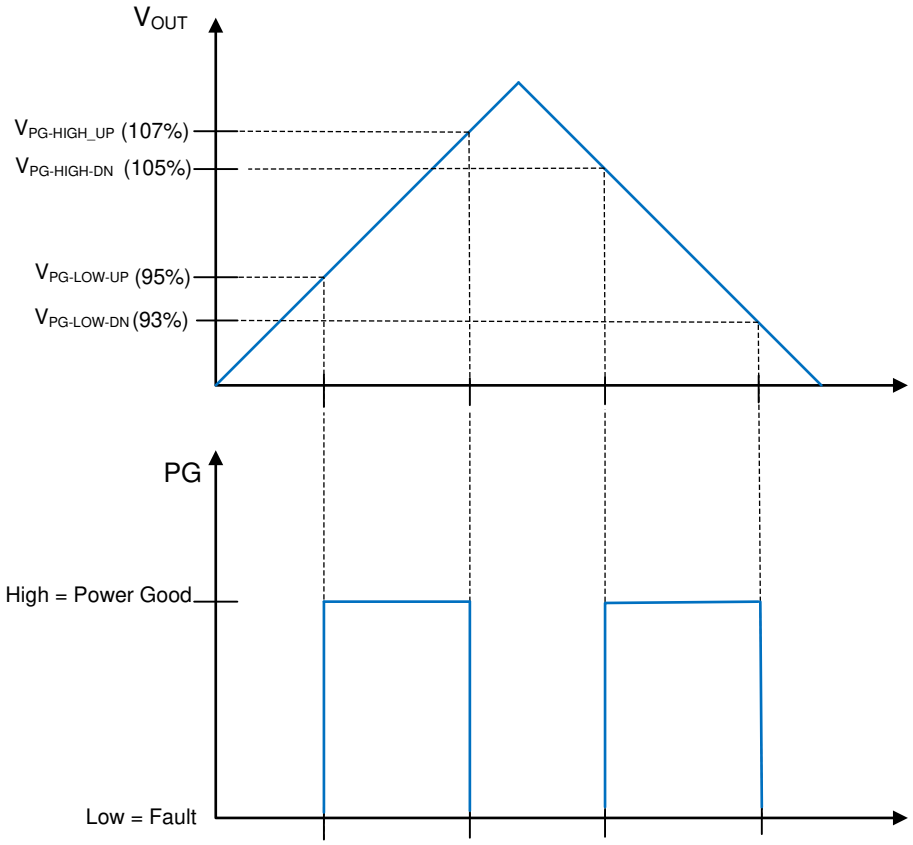


图 7. Static Power-Good Operation

Feature Description (接下页)

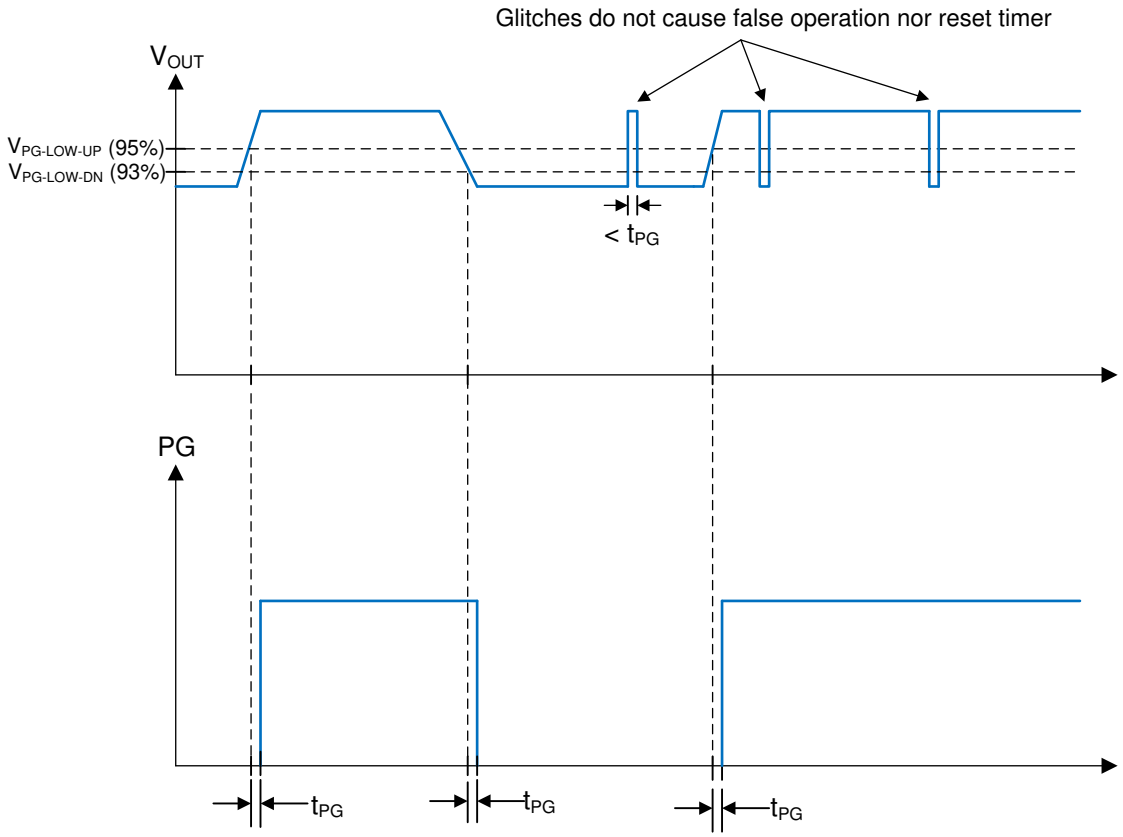


图 8. Power-Good-Timing Behavior

8.3.2 Enable and Start-up

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input UVLO (see the *External UVLO* section). Applying a voltage of ≥ V_{EN-VCC_H} causes the device to enter standby mode, powering the internal VCC, but not producing an output voltage. Increasing the EN voltage to V_{EN-H} fully enables the device, allowing it to enter start-up mode and beginning the soft-start period. When the EN input is brought below V_{EN-H} by V_{EN-HYS}, the regulator stops running and enters standby mode. Further decrease in the EN voltage to below $V_{EN-VCC-L}$ completely shuts down the device. This behavior is shown in 图 9. The EN input may be connected directly to VIN if this feature is not needed. This input must not be allowed to float. The values for the various EN thresholds can be found in the *Electrical Characteristics* table.

The LMR33630 utilizes a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. A typical start-up waveform is shown in 图 10, indicating typical timings. The rise time of the output voltage is about 4 ms (see *Electrical Characteristics*).

Feature Description (接下页)

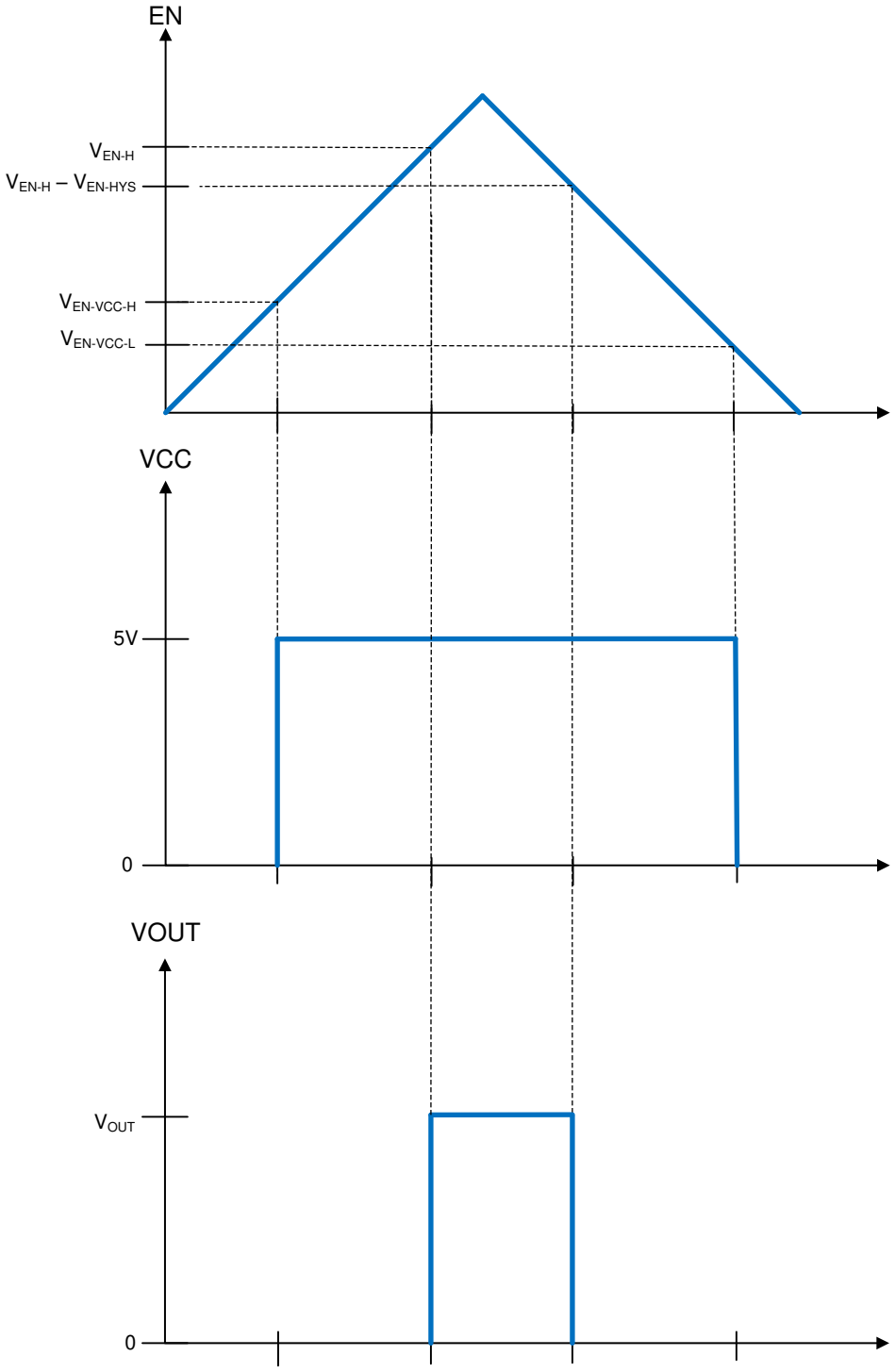


图 9. Precision Enable Behavior

Feature Description (接下页)

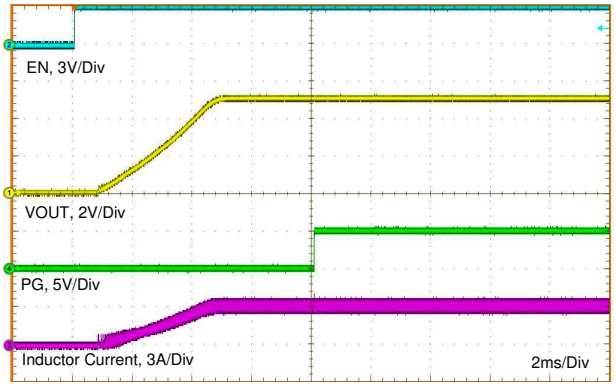


图 10. Typical Start-up Behavior
V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 3 A

8.3.3 Current Limit and Short Circuit

The LMR33630 incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for sustained short circuits. Finally, a zero current detector is used on the low-side power MOSFET to implement DEM at light loads (see *Glossary*). The typical value of this current limit is found under I_{ZC} in the *Electrical Characteristics*.

When the device is overloaded, the valley of the inductor current may not reach below I_{LIMIT}, (see *Electrical Characteristics* table) before the next clock cycle. When this occurs the valley current limit control skips that cycle, causing the switching frequency to drop. Further overload causes the switching frequency to continue to drop, and the inductor ripple current to increase. When the peak of the inductor current reaches the high-side current limit, I_{SC}, (see *Electrical Characteristics* table) the switch duty cycle will be reduced and the output voltage will fall out of regulation. This represents the maximum output current from the converter and is given approximately by 公式 1.

$$I_{OUT}|_{max} = \frac{I_{LIMIT} + I_{SC}}{2} \quad (1)$$

If, during current limit, the voltage on the FB input falls below about 0.4 V, due to a short circuit, the device enters into hiccup mode. In this mode the device stops switching for t_{HC} (see *System Characteristics*), or about 94 ms and then goes through a normal re-start with soft start. If the short-circuit condition remains, the device runs in current limit for about 20 ms (typical) and then shuts down again. This cycle repeats, as shown in 图 11 as long as the short-circuit-condition persists. This mode of operation helps to reduce the temperature rise of the device during a hard short on the output. The output current is greatly reduced during hiccup mode (see *Typical Characteristics*). Once the output short is removed, and the hiccup delay is passed, the output voltage recovers normally as shown in 图 12

Feature Description (接下页)

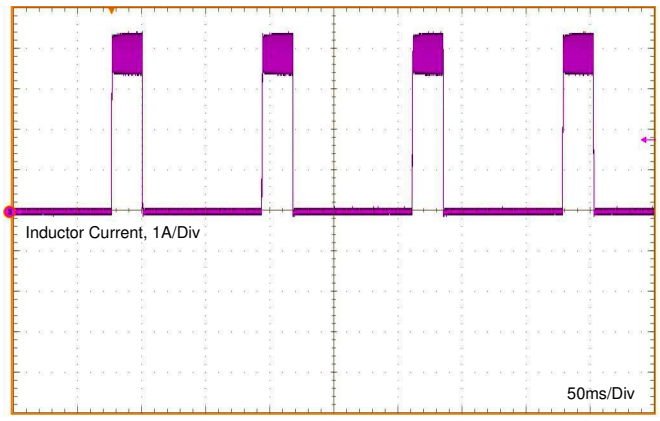


图 11. Inductor Current Burst in Short-Circuit Mode

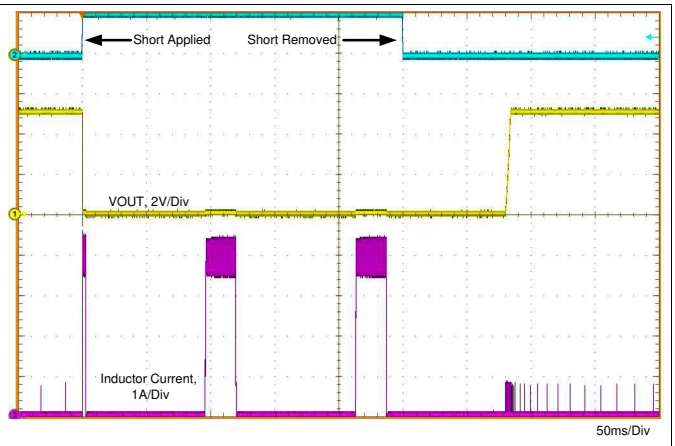


图 12. Short-Circuit Transient and Recovery

8.3.4 Undervoltage Lockout and Thermal Shutdown

The LMR33630 incorporates an undervoltage-lockout feature on the output of the internal LDO (at the VCC pin). When VCC reaches about 3.7 V the device is ready to receive an EN signal and start up. When VCC falls below about 3 V the device shuts down, regardless of EN status. Because the LDO is in dropout during these transitions, the above values roughly represent the input voltage levels during the transitions.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches about 165°C the device shuts down; re-start occurs when the temperature falls to about 148°C.

8.4 Device Functional Modes

8.4.1 Auto Mode

In auto mode the device moves between PWM and PFM as the load changes. At light loads the regulator operates in PFM. At higher loads the mode changes to PWM. The load current for which the device moves from PFM to PWM can be found in the *Application Curves*. The output current at which the device changes modes depends on the input voltage, inductor value and the nominal switching frequency. For output currents above the curve, the device is in PWM mode. For currents below the curve, the device is in PFM. The curves apply for a nominal switching frequency of 400 kHz and the BOM shown in 表 4. At higher switching frequencies the load at which the mode change occurs will be greater. For applications where the switching frequency must be known for a given condition, the transition between PFM and PWM must be carefully tested before the design is finalized.

In PWM mode the regulator operates as a constant frequency converter using PWM to regulate the output voltage. While operating in this mode the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple.

In PFM the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long it takes the inductor current to reach $I_{PEAK-MIN}$. The periodicity of these bursts is adjusted to regulate the output, while diode emulation (DEM) is used to maximize efficiency (see *Glossary*). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at light loads. PFM results in very good light-load efficiency, but also yields larger output voltage ripple and variable switching frequency. Also, a small increase in output voltage occurs at light loads. The actual switching frequency and output voltage ripple depends on the input voltage, output voltage, and load. Typical switching waveforms in PFM and PWM are shown in 图 13 and 图 14. See the *Application Curves* for output voltage variation with load in auto mode.

Device Functional Modes (接下页)

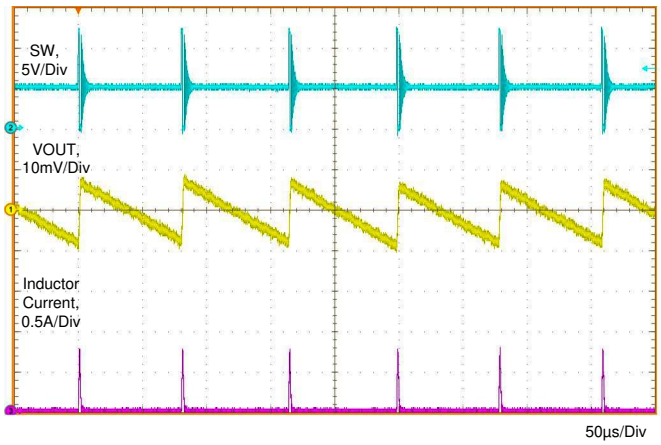


图 13. Typical PFM Switching Waveforms
V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 10 mA

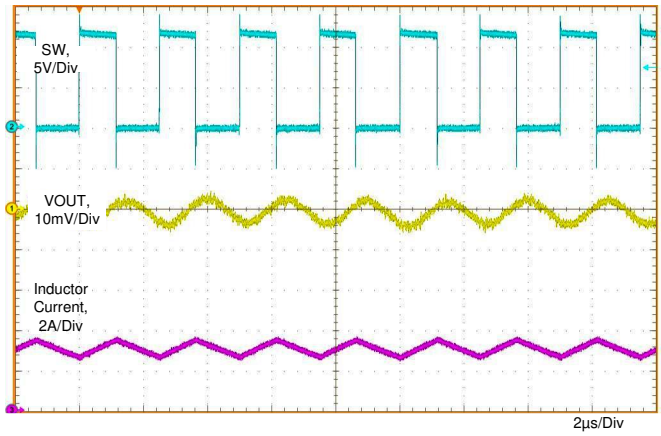


图 14. Typical PWM Switching Waveforms
V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 3 A, f_S = 400 kHz

8.4.2 Dropout

The dropout performance of any buck regulator is affected by the R_{DSON} of the power MOSFETs, the DC resistance of the inductor, and the maximum duty cycle that the controller can achieve. As the input voltage level approaches the output voltage, the off-time of the high side MOSFET starts to approach the minimum value (see *Timing Characteristics*). Beyond this point the switching may become erratic, and/or the output voltage falls out of regulation. To avoid this problem the LMR33630 automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation. In this data sheet the dropout voltage is defined as the difference between the input and output voltage when the output has dropped by 1% of its nominal value. Under this condition the switching frequency has dropped to its minimum value of about 140 kHz. Note that the 0.4 V short circuit detection threshold is not activated when in dropout mode. Typical drop-out characteristics can be found in 图 15, 图 16, 图 17, and 图 18.

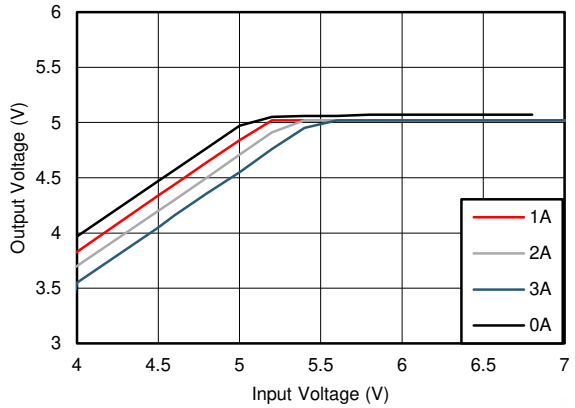


图 15. Overall Dropout Characteristic
V_{OUT} = 5 V

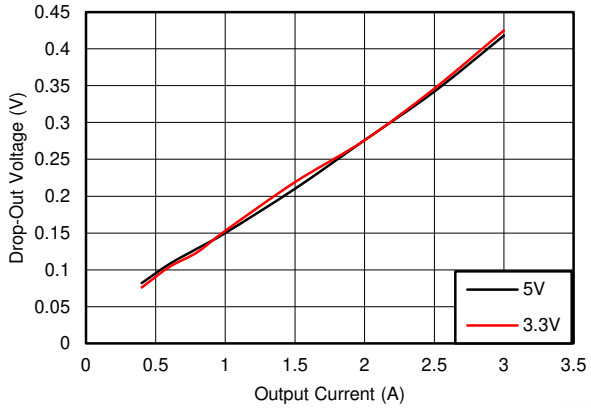


图 16. Typical Dropout Voltage vs Output Current in Frequency Fold-back
f_{SW} = 140 kHz

Device Functional Modes (接下页)

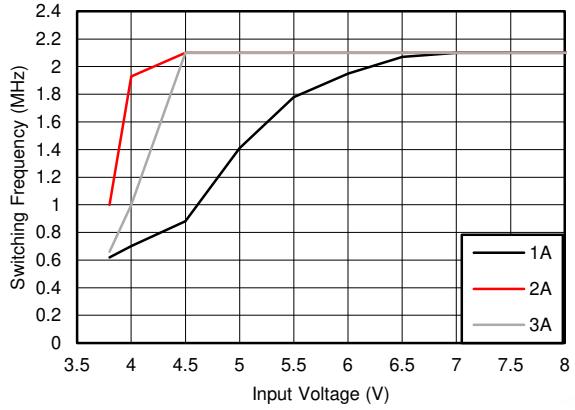


图 17. Typical Switching Frequency in Dropout Mode
V_{OUT} = 3.3 V, f_{SW} = 2.1 MHz

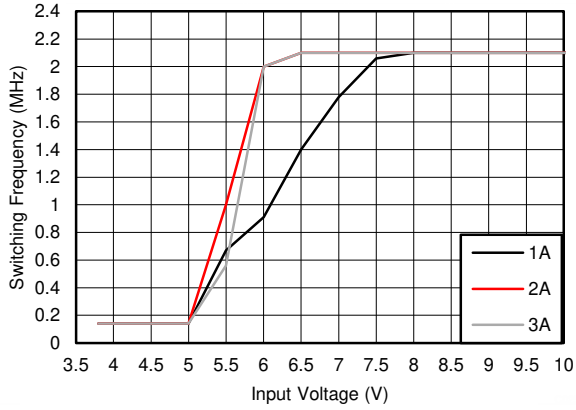


图 18. Typical Switching Frequency in Dropout Mode
V_{OUT} = 5 V, f_{SW} = 2.1 MHz

8.4.3 Minimum Switch On-Time

Every switching regulator has a minimum controllable on-time dictated by the inherent delays and blanking times associated with the control circuits. This imposes a minimum switch duty cycle and therefore a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To help extend the minimum controllable duty cycle, the LMR33630 automatically reduces the switching frequency when the minimum on-time limit is reached. In this way the converter can regulate the lowest programmable output voltage at the maximum input voltage. An estimate for the approximate input voltage, for a given output voltage, before frequency foldback occurs is found in 公式 2. The values of t_{ON} and f_{SW} can be found in the *Electrical Characteristics* table. As the input voltage is increased, the switch on-time (duty-cycle) reduces to regulate the output voltage. When the on-time reaches the limit, the switching frequency drops, while the on-time remains fixed. This relationship is highlighted in 图 19 for a nominal switching frequency of 2.1 MHz.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON} \cdot f_{SW}} \quad (2)$$

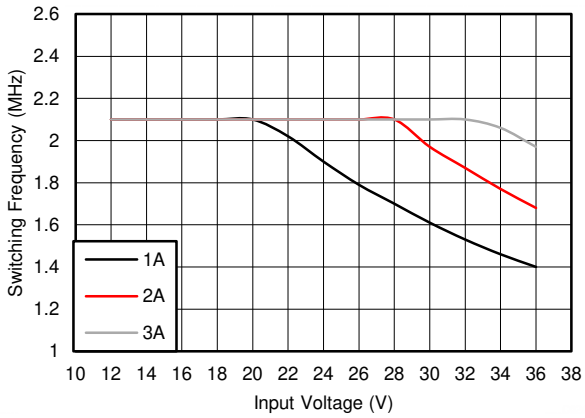


图 19. Switching Frequency vs Input Voltage
V_{OUT} = 3.3 V,

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

注

In this data sheet the *effective* value of capacitance is defined as the actual capacitance under D.C. bias and temperature; not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X5R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under D.C. bias the capacitance drops considerably. Large case sizes and/or higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank should be made in order to ensure that the minimum value of *effective* capacitance is provided.

9.1 Application Information

The LMR33630 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3 A. The following design procedure can be used to select components for the LMR33630. Alternately, the WEBENCH Design Tool may be used to generate a complete design. This tool utilizes an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various options.

9.2 Typical Application

图 20 shows a typical application circuit for the LMR33630. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, *表 2* provides typical component values for a range of the most common output voltages. The values given in the table are typical. Other values may be used to enhance certain performance criterion as required by the application. Note that for the VQFN package, the input capacitors are split and placed on either side of the package; see the *Input Capacitor Selection* section for more details.

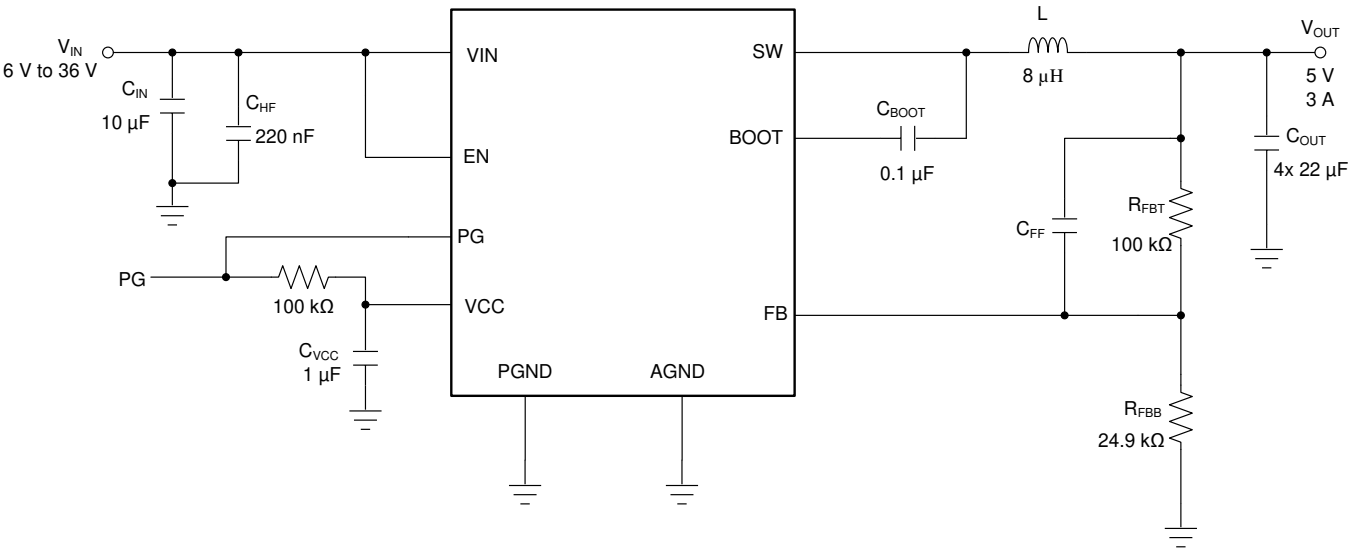


图 20. Example Application Circuit (400 kHz)

Typical Application (接下页)

9.2.1 Design Requirements

表 1 provides the parameters for our detailed design procedure example:

表 1. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V (6 V to 36 V)
Output voltage	5 V
Maximum output current	0 A to 3 A
Switching frequency	400 kHz

表 2. Typical External Component Values

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	C_{OUT} (rated capacitance)	R_{FBT} (Ω)	R_{FBB} (Ω)	C_{IN} + C_{HF}	C_{BOOT}	C_{VCC}	C_{FF}
400	3.3	6.8	4 × 22 µF	100 k	43.2 k	10 µF + 220 nF	100 nF	1 µF	open
1400	3.3	2.2	2 × 22 µF	100 k	43.2 k	10 µF + 220 nF	100 nF	1 µF	open
2100	3.3	1.2	2 × 22 µF	100 k	43.2 k	10 µF + 220 nF	100 nF	1 µF	open
400	5	8	4 × 22 µF	100 k	24.9 k	10 µF + 220 nF	100 nF	1 µF	open
1400	5	2.2	2 × 22 µF	100 k	24.9 k	10 µF + 220 nF	100 nF	1 µF	open
2100	5	1.5	2 × 22 µF	100 k	24.9 k	10 µF + 220 nF	100 nF	1 µF	open
400	12	15	4 × 22 µF	100 k	9.09 k	10 µF + 220 nF	100 nF	1 µF	open
1400	12	4.7	4 × 10 µF	100 k	9.09 k	10 µF + 220 nF	100 nF	1 µF	open
2100	12	3.3	4 × 10 µF	100 k	9.09 k	10 µF + 220 nF	100 nF	1 µF	open

9.2.2 Detailed Design Procedure

The following design procedure applies to 图 20 and 表 1.

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR33630 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, and hence a more compact design. For this example we choose 400 kHz.

9.2.2.3 Setting the Output Voltage

The output voltage of LMR33630 is externally adjustable using a resistor divider network. The range of recommended output voltage is found in the *Recommended Operating Conditions* table. The divider network is comprised of R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF}. The resistance of the divider is a compromise between excessive noise pick-up and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R_{FBT} is 100 kΩ; with a maximum value of 1 MΩ. If a 1 MΩ is selected for R_{FBT}, then a feed-forward capacitor must be used across this resistor to provide adequate loop phase margin (see *C_{FF} Selection*). Once R_{FBT} is selected, 公式 3 is used to select R_{FBB}. V_{REF} is nominally 1 V (see *Electrical Characteristics* for limits).

$$R_{FBB} = \frac{R_{FBT}}{\left[\frac{V_{OUT}}{V_{REF}} - 1\right]} \tag{3}$$

For this 5-V example, R_{FBT} = 100 kΩ and R_{FBB} = 24.9 kΩ are chosen.

9.2.2.4 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current should be used. 公式 4 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example we choose K = 0.3 and find an inductance L = 8.1 µH; we select the next standard value of 8 µH.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \cdot K \cdot I_{OUT\,max}} \cdot \frac{V_{OUT}}{V_{IN}} \tag{4}$$

Ideally, the saturation current rating of the inductor should be at least as large as the high-side switch current limit, I_{SC} (see *Electrical Characteristics*). This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LIMIT}, is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This may lead to component damage; do not allow the inductor to saturate! Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies typically above 1 MHz. In any case the inductor saturation current should not be less than the device low-side current limit, I_{LIMIT} (see *Electrical Characteristics*). In order to avoid sub-harmonic oscillation, the inductance value should not be less than that given in 公式 5. The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current should be no less than about 10% of the device maximum rated current under nominal conditions.

$$L_{MIN} \geq 0.28 \cdot \frac{V_{OUT}}{f_{SW}} \tag{5}$$

9.2.2.5 Output Capacitor Selection

The value of the output capacitor, and its ESR, determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements, rather than the output voltage ripple. 公式 6 can be used to estimate a lower bound on the total output capacitance, and an upper bound on the ESR, required to meet a specified load transient.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \cdot \Delta V_{OUT} \cdot K} \cdot \left[(1-D) \cdot (1+K) + \frac{K^2}{12} \cdot (2-D) \right]$$

$$ESR \leq \frac{(2+K) \cdot \Delta V_{OUT}}{2 \cdot \Delta I_{OUT} \left[1+K+\frac{K^2}{12} \cdot \left(1+\frac{1}{(1-D)} \right) \right]}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

where

- ΔV_{OUT} = output voltage transient
- ΔI_{OUT} = output current transient
- K = Ripple factor from *Inductor Selection*

(6)

Once the output capacitor and ESR have been calculated, 公式 7 can be used to check the peak-to-peak output voltage ripple; V_r.

$$V_r \cong \Delta I_L \cdot \sqrt{ESR^2 + \frac{1}{(8 \cdot f_{SW} \cdot C_{OUT})^2}} \tag{7}$$

The output capacitor and ESR can then be adjusted to meet both the load transient and output ripple requirements.

For this example we require a ΔV_{OUT} of ≤ 250 mV for an output current step of ΔI_{OUT} = 2 A. 公式 6 gives a minimum value of 52 µF and a maximum ESR of 0.11 Ω. Assuming a 20% tolerance and a 10% bias de-rating, we arrive at a minimum capacitance of 72 µF. This can be achieved with a bank of 4 × 22-µF, 16-V, ceramic capacitors in the 1210 case size. More output capacitance can be used to improve the load transient response. Ceramic capacitors can easily meet the minimum ESR requirements. In some cases an aluminum electrolytic capacitor can be placed in parallel with the ceramics to help build up the required value of capacitance. In general use a capacitor of at least 10 V for output voltages of 3.3 V or less, while a capacitor of 16 V or more should be used for output voltages of 5 V and above.

In practice the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and Bode plots are the best way to validate any given design and should always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help to reduce high frequency noise. Small case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing voltage spikes on the output caused by inductor and board parasitics.

The maximum value of total output capacitance should be limited to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

9.2.2.6 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 10 µF of ceramic capacitance is required on the input of the LMR33630. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and/or maintain the input voltage during load transients. In addition a small case size 220-nF ceramic capacitor must be used at the input, as close a possible to the regulator. This provides a high frequency bypass for the control circuits internal to the device. For this example a 10-µF, 50-V, X7R (or better) ceramic capacitor is chosen. The 220 nF must also be rated at 50 V with an X7R dielectric. The VQFN (RNX) package provides two input voltage pins and two power ground pins on opposite sides of the package. This allows the input capacitors to be split, and placed optimally with respect to the internal power MOSFETs, thus improving the effectiveness of the input bypassing. In this example, place two 4.7-µF and two 100-nF ceramic capacitors at each VIN/PGND location. A single 10-µF can also be used on one side of the package.

Many times it is desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor(s). The approximate worst case RMS value of this current can be calculated from 公式 8 and should be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{8}$$

9.2.2.7 C_{BOOT}

The LMR33630 requires a boot-strap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 10 V is required.

9.2.2.8 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general avoid loading this output with any external circuitry. However, this output can be used to supply the pull-up for the power-good function (see *Power-Good Flag Output*). A value of 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 5 V; see *Electrical Characteristics* for limits. Do not short this output to ground or any other external voltage.

9.2.2.9 C_{FF} Selection

In some cases a feed-forward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. This is especially true when values of R_{FBT} > 100 kΩ are used. Large values of R_{FBT}, in combination with the parasitic capacitance at the FB pin, can create a small signal pole that interferes with the loop stability. A C_{FF} can help to mitigate this effect. 公式 9 can be used to estimate the value of C_{FF}. The value found with 公式 9 is a starting point; use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor. The application report *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feed-forward Capacitor* is helpful when experimenting with a feed-forward capacitor.

$$C_{FF} < \frac{V_{OUT} \cdot C_{OUT}}{120 \cdot R_{FBT} \cdot \sqrt{\frac{V_{REF}}{V_{OUT}}}} \tag{9}$$

9.2.2.10 External UVLO

In some cases an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in 图 21. The input voltage at which the device turns on is designated V_{ON}; while the turnoff voltage is V_{OFF}. First a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ and then 公式 10 is used to calculate R_{ENT} and V_{OFF}.

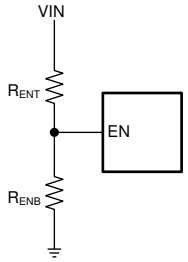


图 21. Set-Up for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-H}} - 1 \right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot \left(1 - \frac{V_{EN-HYS}}{V_{EN-H}} \right)$$

where

- V_{ON} = V_{IN} turnon voltage
- V_{OFF} = V_{IN} turnoff voltage

(10)

9.2.2.11 Maximum Ambient Temperature

As with any power conversion device, the LMR33630 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss and the effective thermal resistance, $R_{\theta JA}$ of the device and PCB combination. The maximum internal die temperature for the LMR33630 must be limited to 125°C. This establishes a limit on the maximum device power dissipation and therefore the load current. 公式 11 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions can not be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in *Semiconductor and IC Package Thermal Metrics*, the value of $R_{\theta JA}$ given in the *Thermal Information* table is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \quad (11)$$

where

- η = Efficiency

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as power dissipation, air temperature/flow, PCB area, copper heat-sink area, number of thermal vias under the package, and adjacent component placement; to mention just a few. The HSOIC (DDA) package utilizes a die attach paddle, or thermal pad (PAD) to provide a place to solder down to the PCB heat-sinking copper. This provides a good heat conduction path from the regulator junction to the heat sink and must be properly soldered to the PCB heat sink copper. Due to the ultra-miniature size of the VQFN (RNX) package, a DAP is not available. This means that this package exhibits a somewhat large value $R_{\theta JA}$. Typical examples of $R_{\theta JA}$ vs copper board area can be found in 图 22 and 图 23. The copper area given in the graph is for each layer; the top and bottom layers are 2 oz. copper each, while the inner layers are 1 oz. Typical curves of maximum output current vs ambient temperature are shown in 图 24 and 图 25. This data was taken with a device/PCB combination giving an $R_{\theta JA}$ as noted in the graph. It must be remembered that the data given in these graphs are for illustration purposes only, and the actual performance in any given application depends on all of the previously mentioned factors.

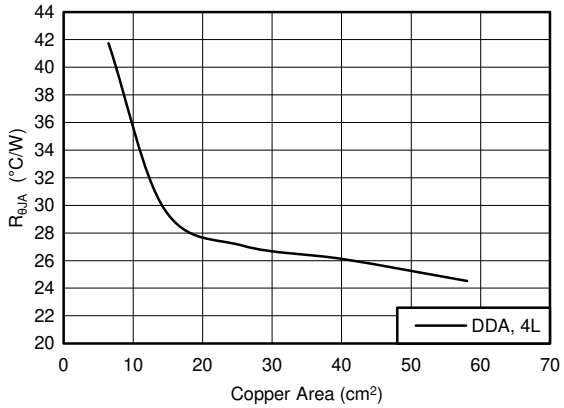


图 22. Typical $R_{\theta JA}$ vs Copper Area for a Four-Layer Board and the HSOIC (DDA) Package

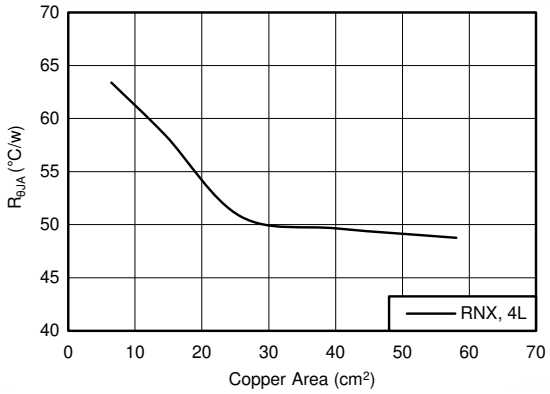


图 23. $R_{\theta JA}$ vs Copper Board Area for the VQFN (RNX) Package

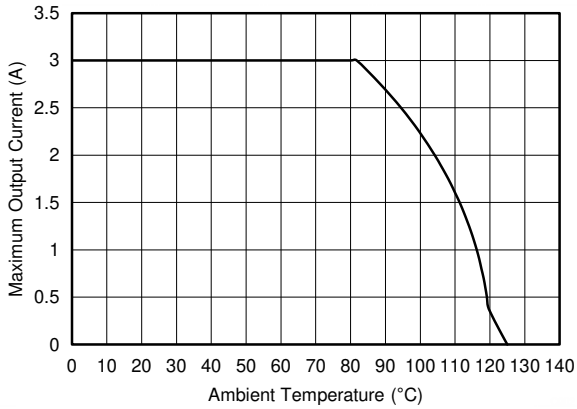


图 24. Maximum Output Current vs Ambient Temperature

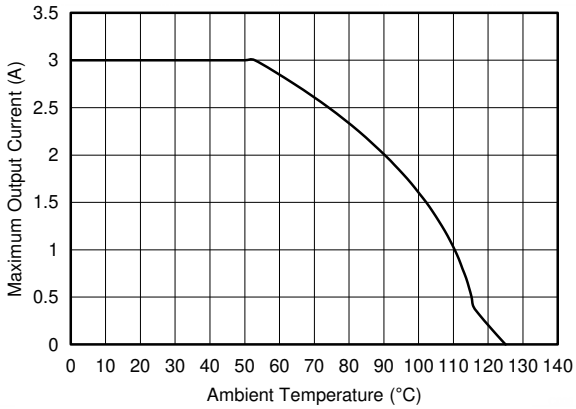


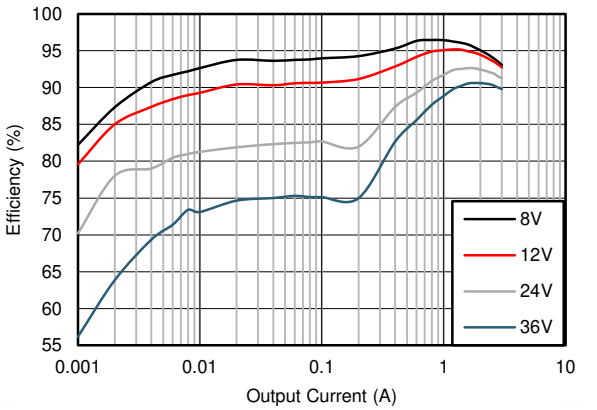
图 25. Maximum Output Current vs Ambient Temperature

Use the following resources as a guide to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
- *Semiconductor and IC Package Thermal Metrics*
- *Thermal Design Made Simple with LM43603 and LM43602*
- *SLMA002 PowerPAD™ Thermally Enhanced Package*
- *PowerPAD™ Made Easy*
- *SBVA025 Using New Thermal Metrics*

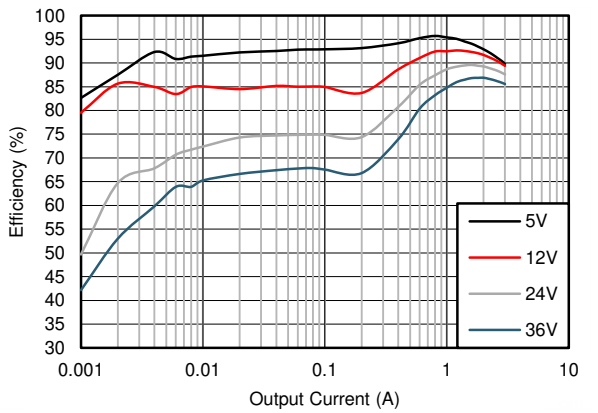
9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, T_A = 25°C. The circuit is shown in 图 50, with the appropriate BOM from 表 3 or 表 4.



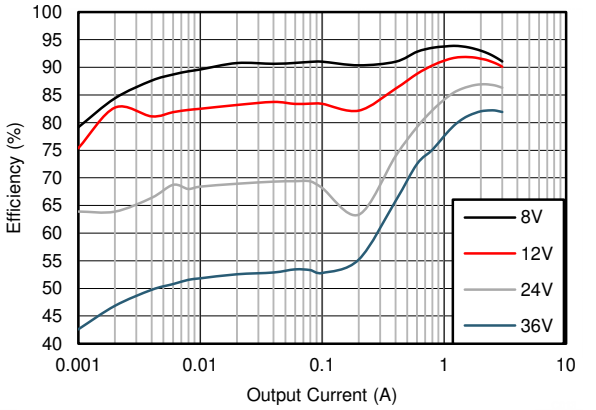
V_{OUT} = 5 V 400 kHz DDA Package

图 26. Efficiency



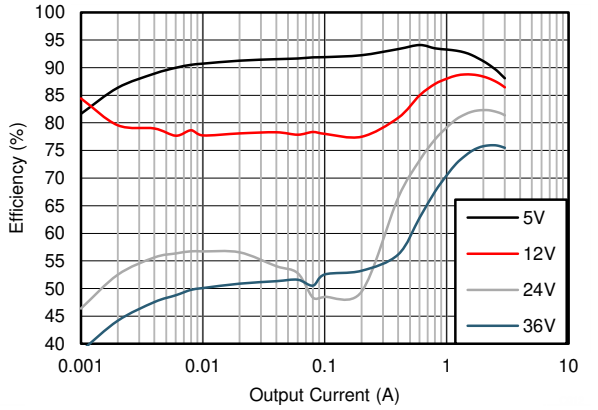
V_{OUT} = 3.3 V 400 kHz DDA Package

图 27. Efficiency



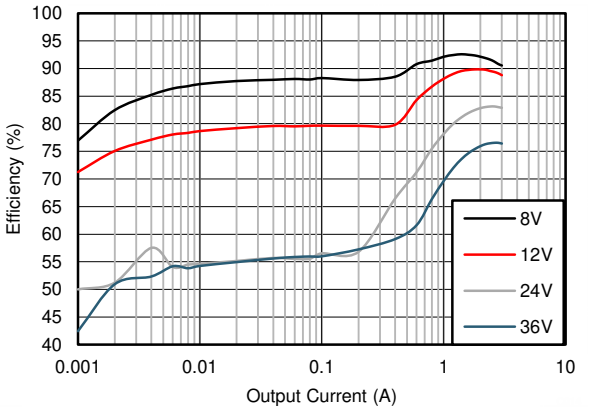
V_{OUT} = 5 V 1.4 MHz DDA Package

图 28. Efficiency



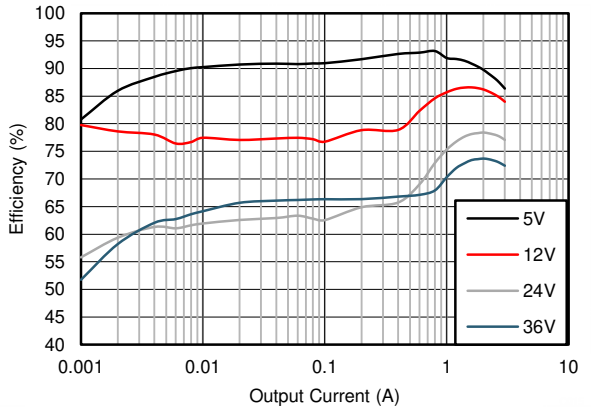
V_{OUT} = 3.3 V 1.4 MHz DDA Package

图 29. Efficiency



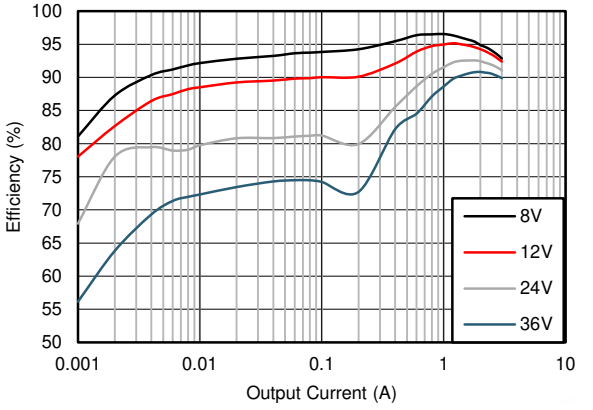
V_{OUT} = 5 V 2.1 MHz DDA Package

图 30. Efficiency



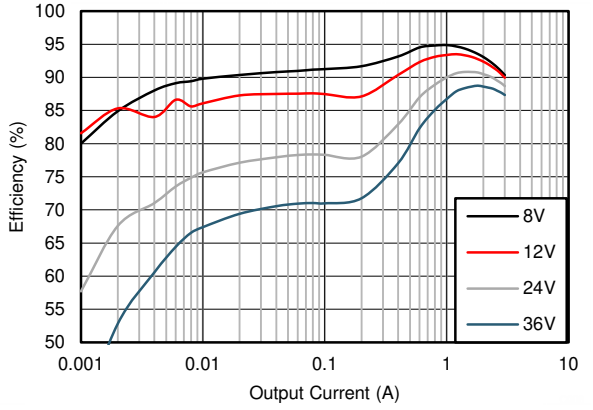
V_{OUT} = 3.3 V 2.1 MHz DDA Package

图 31. Efficiency



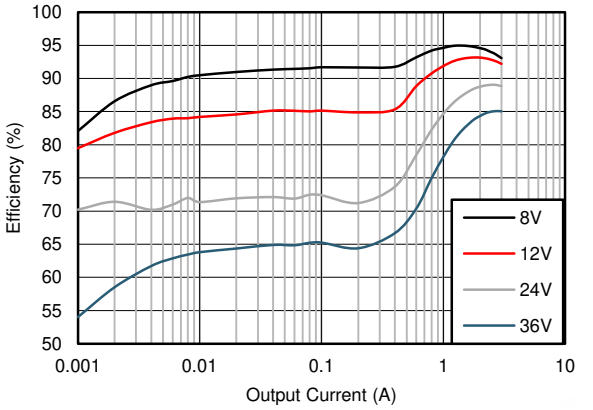
V_{OUT} = 5 V 400 kHz RNX Package

图 32. Efficiency



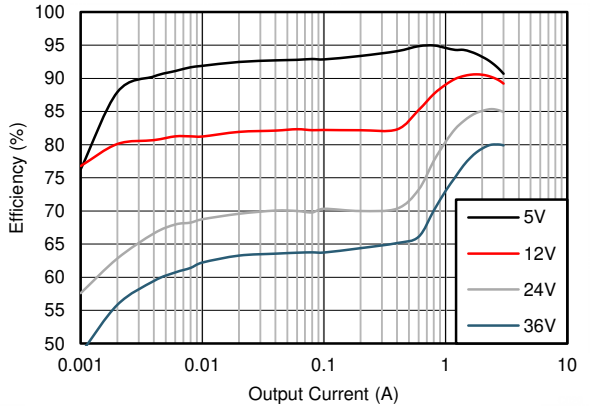
V_{OUT} = 3.3 V 400 kHz RNX Package

图 33. Efficiency



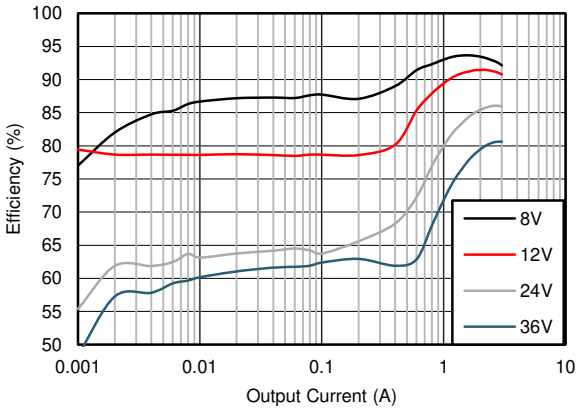
V_{OUT} = 5 V 1.4 MHz RNX Package

图 34. Efficiency



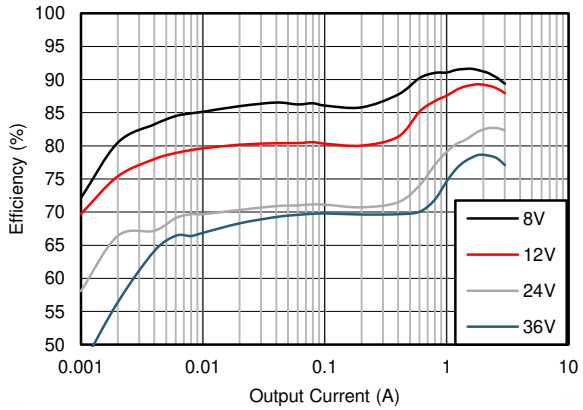
V_{OUT} = 3.3 V 1.4 MHz RNX Package

图 35. Efficiency



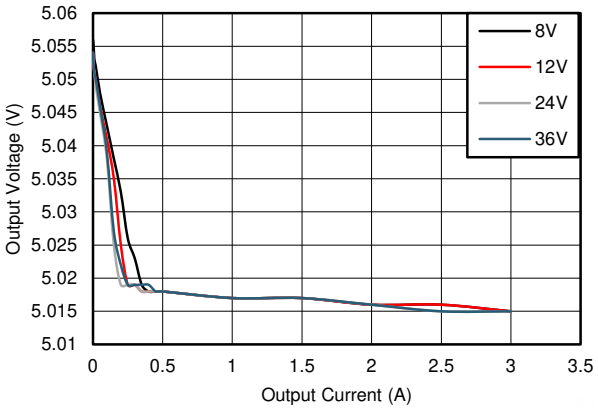
V_{OUT} = 5 V 2.1 MHz RNX Package

图 36. Efficiency



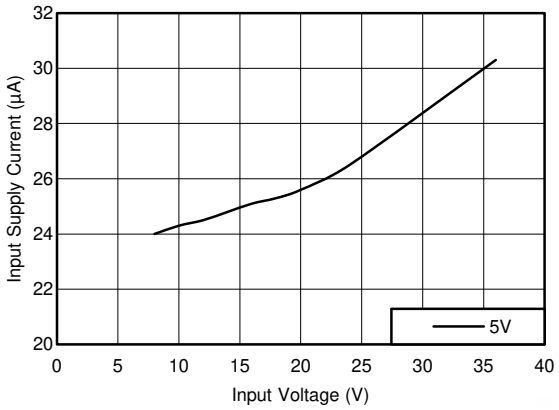
V_{OUT} = 3.3 V 2.1 MHz RNX Package

图 37. Efficiency



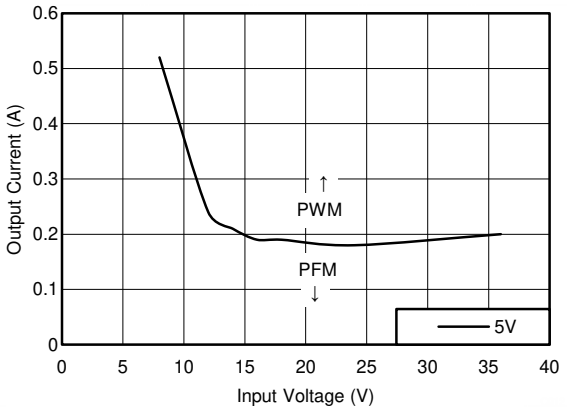
V_{OUT} = 5 V

图 38. Line and Load Regulation



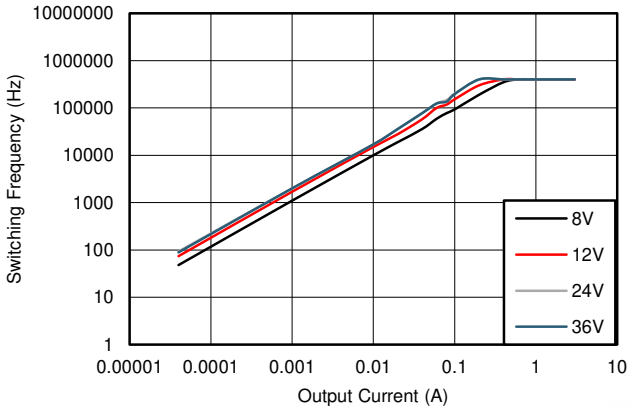
V_{OUT} = 5 V I_{OUT} = 0 A R_{FBT} = 1 MΩ

图 39. Input Supply Current



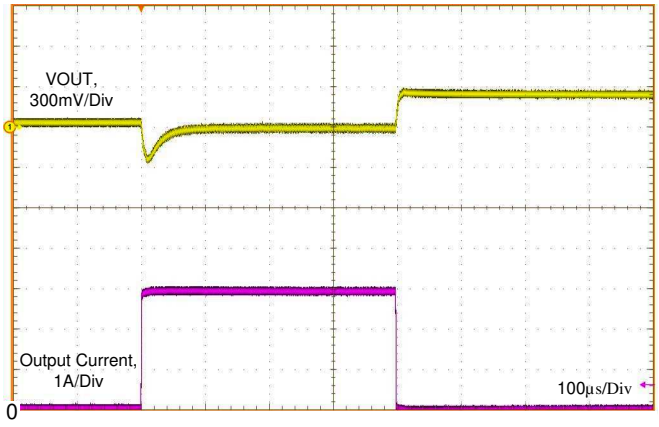
V_{OUT} = 5 V f_{SW} = 400 kHz

图 40. Mode Change Thresholds



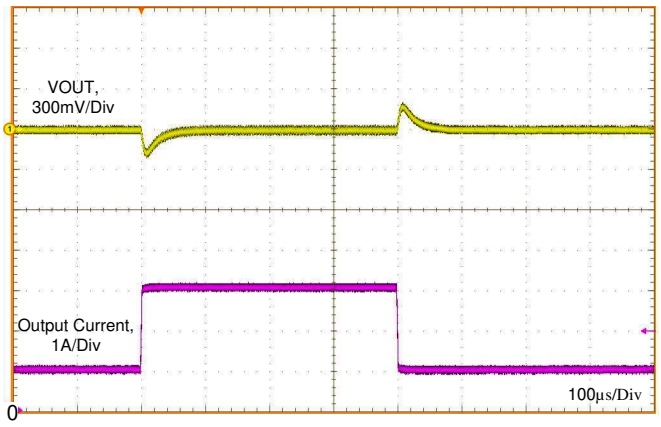
V_{OUT} = 5 V f_{SW} = 400 kHz

图 41. Switching Frequency vs Output Current



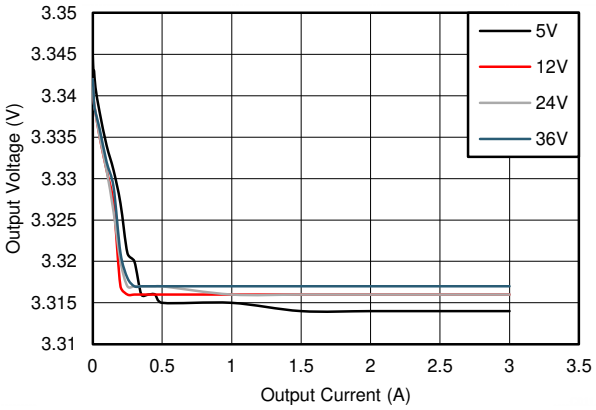
V_{IN} = 12 V
$t_f = t_r$ = 2 µs
V_{OUT} = 5 V
I_{OUT} = 0 A to 3 A

图 42. Load Transient



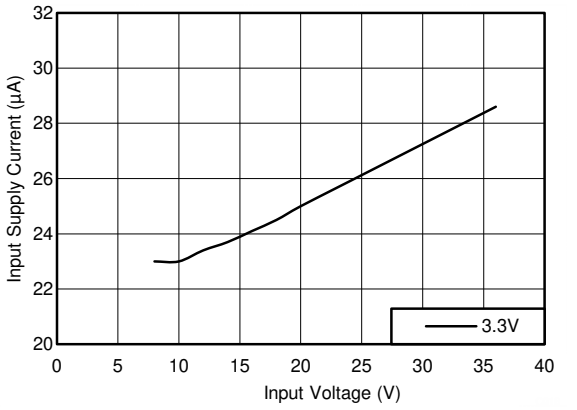
V_{IN} = 12 V
$t_f = t_r$ = 2 µs
V_{OUT} = 5 V
I_{OUT} = 1 A to 3 A

图 43. Load Transient



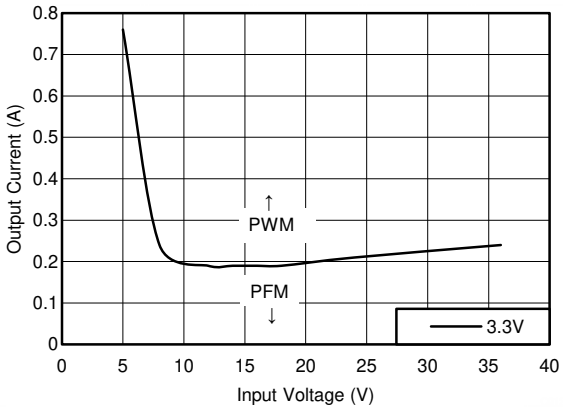
V_{OUT} = 3.3 V

图 44. Line and Load Regulation



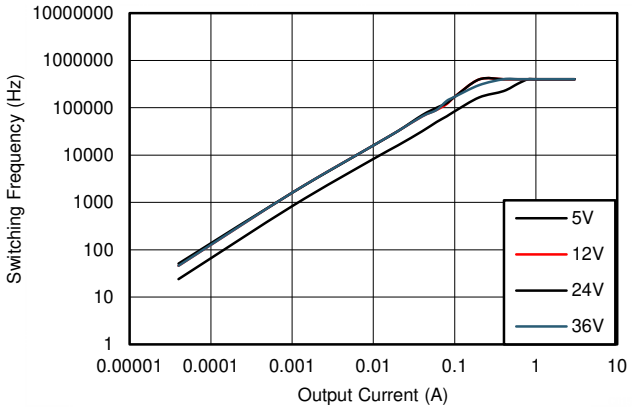
V_{OUT} = 3.3 V I_{OUT} = 0 A R_{FBT} = 1 MΩ

图 45. Input Supply Current



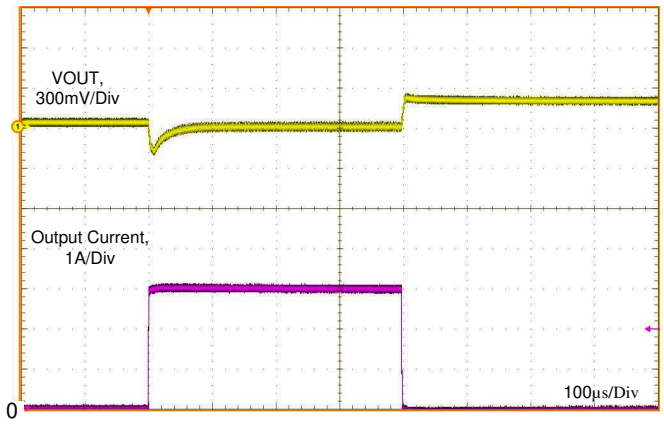
V_{OUT} = 3.3V f_{SW} = 400 kHz

图 46. Mode Change Thresholds



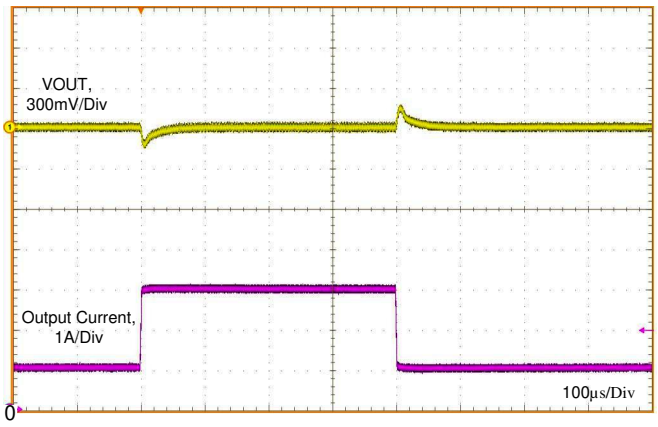
V_{OUT} = 3.3 V f_{SW} = 400 kHz

图 47. Switching Frequency vs Output Current



V_{IN} = 12 V
$t_f = t_r$ = 2 µs
V_{OUT} = 3.3 V
I_{OUT} = 0 A to 3 A

图 48. Load Transient



V_{IN} = 12 V
$t_f = t_r$ = 2 µs
V_{OUT} = 3.3V
I_{OUT} = 1 A to 3 A

图 49. Load Transient

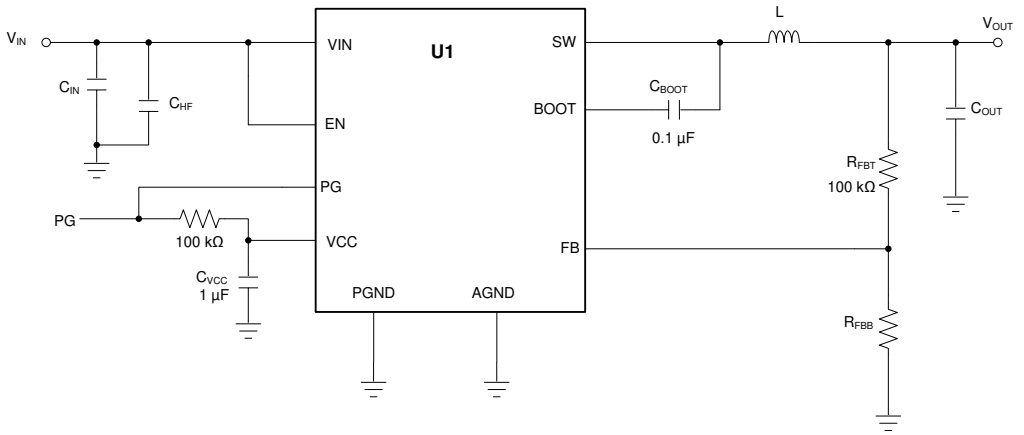


图 50. Circuit for Application Curves

表 3. BOM for Typical Application Curves DDA Package(1)

V_{OUT}	FREQUENCY	R_{FBB}	C_{OUT}	C_{IN} + C_{HF}	L	U1
3.3 V	400 kHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	6.8 µH, 14 mΩ	LMR33630ADDA
3.3 V	1400 KHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	2.2 µH, 11.4 mΩ	LMR33630BDDA
3.3 V	2100 kHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	1.2 µH, 16 mΩ	LMR33630CDDA
5 V	400 kHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	8 µH, 14 mΩ	LMR33630ADDA
5 V	1400 KHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	2.2 µH, 11.4 mΩ	LMR33630BDDA
5 V	2100 kHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	1.5 µH, 8.2 mΩ	LMR33630CDDA

(1) The values in this table were selected to enhance certain performance criteria and may not represent typical values.

表 4. BOM for Typical Application Curves RNX Package(1)

V_{OUT}	FREQUENCY	R_{FBB}	C_{OUT}	C_{IN} + C_{HF}	L	U1
3.3 V	400 kHz	43.3 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	6.8 µH, 14 mΩ	LMR33630ARNX
3.3 V	1400 KHz	43.3 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	2.2 µH, 11.4 mΩ	LMR33630BRNX
3.3 V	2100 kHz	43.3 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	1.2 µH, 7 mΩ	LMR33630CRNX
5 V	400 kHz	24.9 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	8 µH, 25 mΩ	LMR33630ARNX
5 V	1400 KHz	24.9 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	2.2 µH, 11.4 mΩ	LMR33630BRNX
5 V	2100 kHz	24.9 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	1.5 µH, 8.2 mΩ	LMR33630CRNX

(1) The values in this table were selected to enhance certain performance criteria and may not represent typical values.

9.3 Do's and Don'ts

- **Don't:** Exceed the *Absolute Maximum Ratings*
- **Don't:** Exceed the *ESD Ratings*
- **Don't:** Exceed the *Recommended Operating Conditions*
- **Don't:** Allow the EN input to float.
- **Don't:** Allow the output voltage to exceed the input voltage, nor go below ground.
- **Don't:** Use the value of $R_{\theta JA}$ given in the *Thermal Information* table to design your application. Us the information in the Maximum Ambient Temperature section.
- **Do:** Follow all the guidelines and/or suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success (see *社区资源*).

10 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 公式 12, where η is the efficiency.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \quad (12)$$

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under damped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip may cause the regulator to momentarily shutdown and/or reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the regulator and/or use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help to damp the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The user guide *AN-2162 Simple Success With Conducted EMI From DCDC Converters* provides helpful suggestions when designing an input filter for any switching regulator.

In some cases a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow may damage the device.

The input voltage should not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors will discharge through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then a Schottky diode between the input supply and the output should be used.

11 Layout

11.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout, to a great extent. In a buck converter the most critical PCB feature is the loop formed by the input capacitor(s) and power ground, as shown in 图 51. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages will disrupt the proper operation of the converter. Because of this, the traces in this loop should be wide and short, and the loop area as small as possible to reduce the parasitic inductance. 图 52 and 图 53 show recommended layouts for the critical components of the LMR33630 .

1. ***Place the input capacitor(s) as close as possible to the VIN and GND terminals.*** VIN and GND pins are adjacent, simplifying the input capacitor placement. With the VQFN package there are two VIN/PGND pairs on either side of the package. This provides for a symmetrical layout and helps to minimize switching noise and EMI generation. A wide VIN plane should be used on a lower layer to connect both of the VIN pairs together to the input supply; see 图 53.
2. ***Place bypass capacitor for VCC close to the VCC pin.*** This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. ***Use wide traces for the C_{BOOT} capacitor.*** Place C_{BOOT} close to the device with short/wide traces to the BOOT and SW pins. For the VQFN package, it is important to route the SW connection under the device to the NC pin, and use this path to connect the BOOT capacitor to SW.
4. ***Place the feedback divider as close as possible to the FB pin of the device.*** Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
5. ***Use at least one ground plane in one of the middle layers.*** This plane acts as a noise shield and also act as a heat dissipation path.
6. ***Connect the thermal pad to the ground plane.*** The SOIC package has a thermal pad (PAD) connection that must be soldered down to the PCB ground plane. This pad acts as a heat-sink connection and an electrical ground connection for the regulator. The integrity of this solder connection has a direct bearing on the total effective $R_{\theta JA}$ of the application.
7. ***Provide wide paths for VIN, VOUT, and GND.*** Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
8. ***Provide enough PCB area for proper heat sinking.*** As stated in the *Maximum Ambient Temperature* section, enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper; and no less than one ounce. With the SOIC package, use an array of heat-sinking vias to connect the thermal pad (PAD) to the ground plane on the bottom PCB layer. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes.
9. ***Keep switch area small.*** Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time the total area of this node should be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies*
- *Simple Switcher PCB Layout Guidelines*
- *Construction Your Power Supply- Layout Considerations*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x*

Layout Guidelines (接下页)

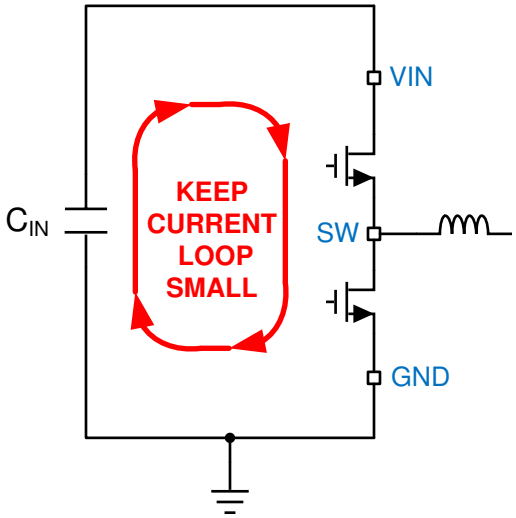


图 51. Current Loops with Fast Edges

11.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins should be connected to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low side MOSFET switch, and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and may bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise and must be used for sensitive routes.

TI recommends providing adequate device heat sinking by utilizing the thermal pad (PAD) of the device as the primary thermal path. Use a minimum 4 × 3 array of 10 mil thermal vias to connect the PAD to the system ground plane heat sink. The vias must be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding and lower thermal resistance.

11.2 Layout Example

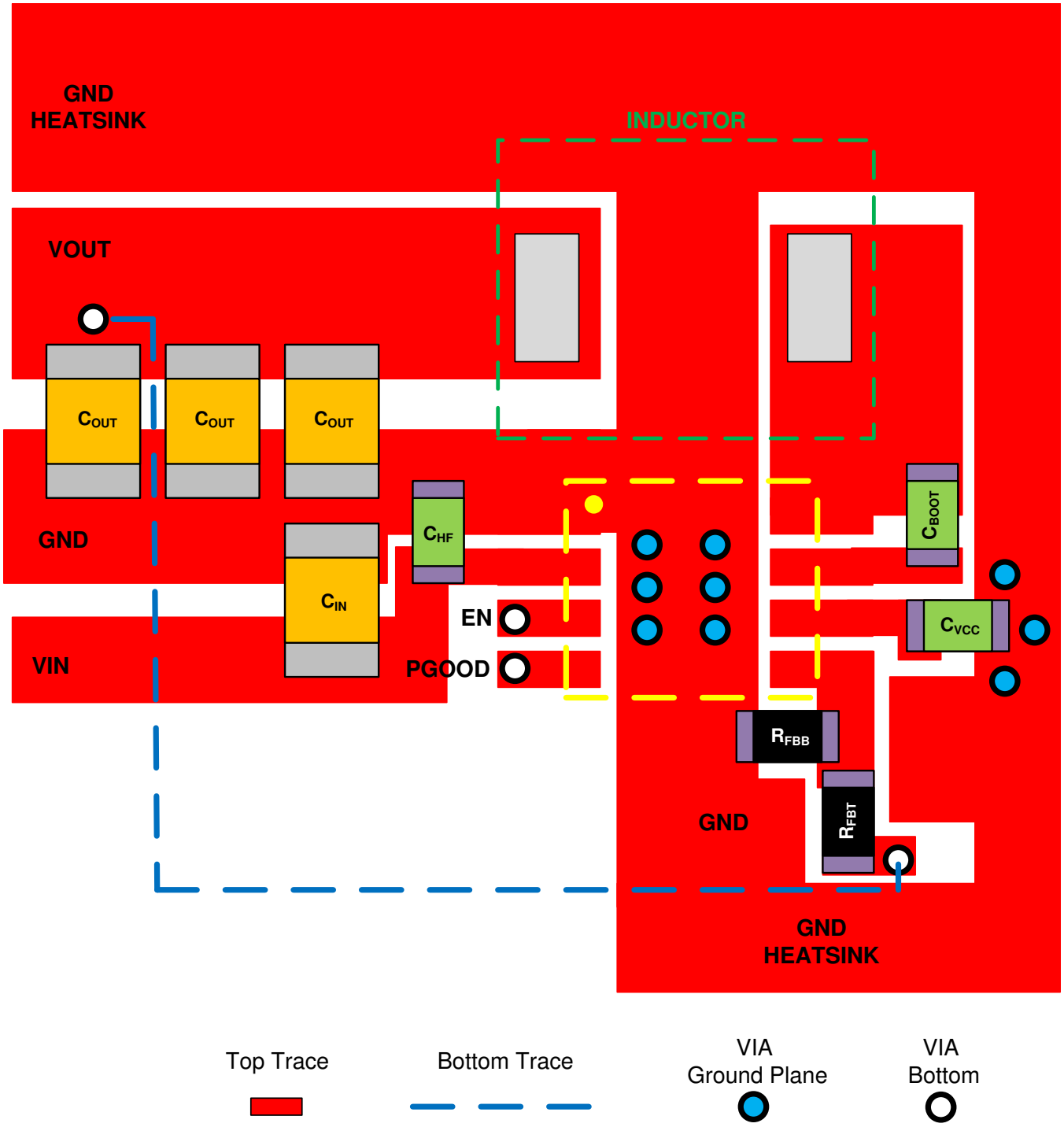


图 52. Example Layout for HSOIC (DDA) Package

Layout Example (接下页)

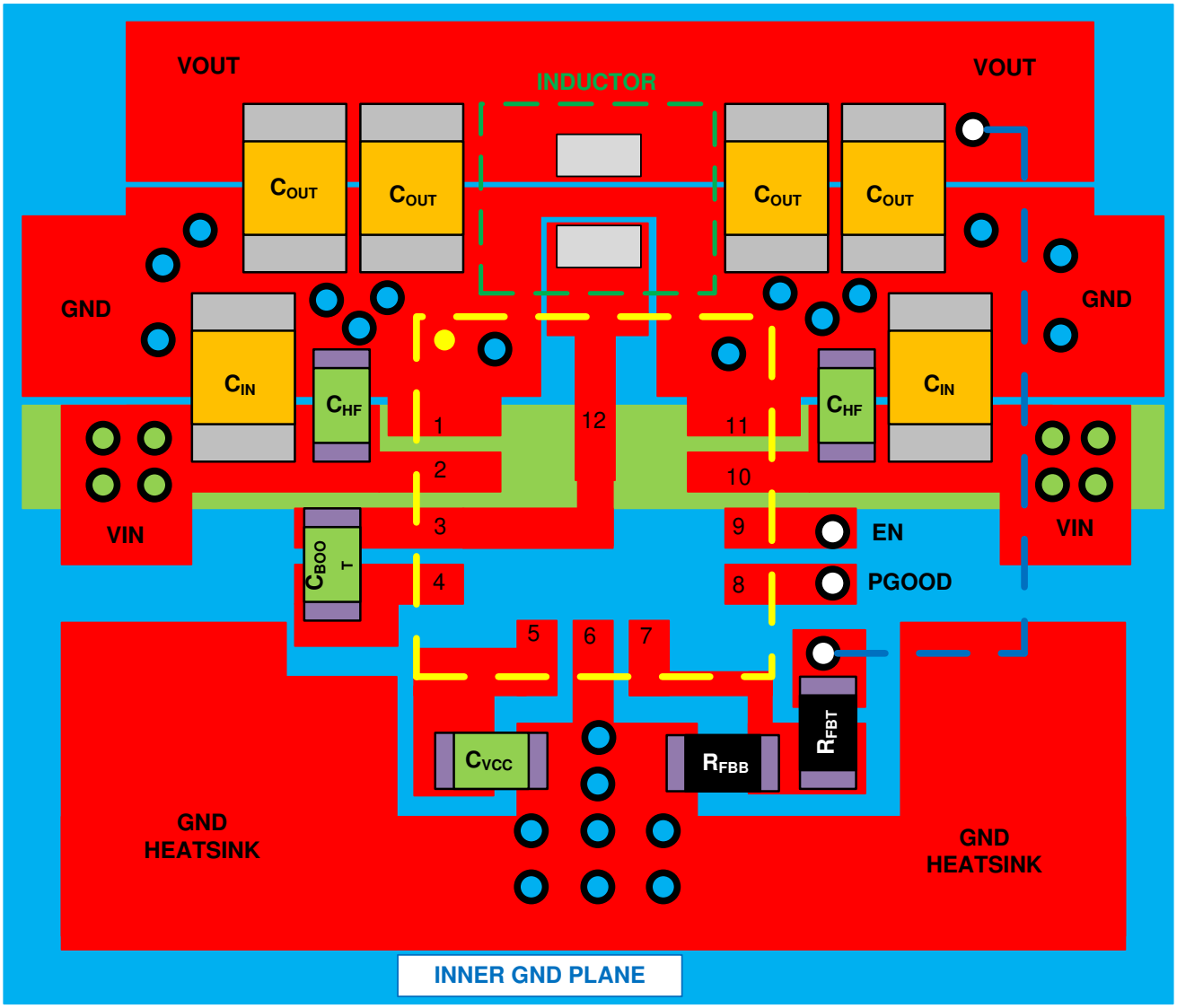


图 53. Example Layout for VQFN Package

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 使用 WEBENCH® 工具创建定制设计

单击此处，使用 LM33630 器件并借助 WEBENCH® 电源设计器创建定制设计。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- *《热设计：学会洞察先机，不做事后诸葛》*
- *《外露焊盘封装实现最佳热阻性的电路板布局指南》*
- *《半导体和 IC 封装热指标》*
- *《使用 LM43603 和 LM43602 简化热设计》*
- *《SLMA002 PowerPAD™ 热增强型封装》*
- *《PowerPAD™ 速成》*
- *《SBVA025 使用新的热指标》*
- *《开关电源布局指南》*
- *《Simple Switcher PCB 布局指南》*
- *《构建电源 - 布局注意事项》*
- *《使用 LM4360x 与 LM4600x 简化低辐射 EMI 布局》*

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

PowerPAD, E2E are trademarks of Texas Instruments.

12.5 商标 (接下页)

SIMPLE SWITCHER, WEBENCH are registered trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR33630ADDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33630A	Samples
LMR33630ADDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33630A	Samples
LMR33630ARNXR	ACTIVE	VQFN-HR	RNX	12	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	33630A	Samples
LMR33630ARNXT	ACTIVE	VQFN-HR	RNX	12	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	33630A	Samples
LMR33630BDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33630B	Samples
LMR33630BDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33630B	Samples
LMR33630BRNXR	ACTIVE	VQFN-HR	RNX	12	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	33630B	Samples
LMR33630BRNXT	ACTIVE	VQFN-HR	RNX	12	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	33630B	Samples
LMR33630CDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33630C	Samples
LMR33630CDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33630C	Samples
LMR33630CRNXR	ACTIVE	VQFN-HR	RNX	12	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	33630C	Samples
LMR33630CRNXT	ACTIVE	VQFN-HR	RNX	12	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	33630C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

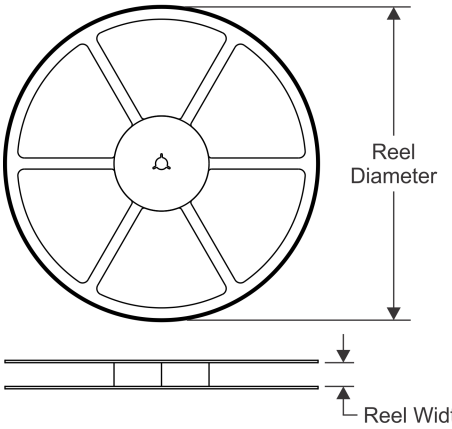
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

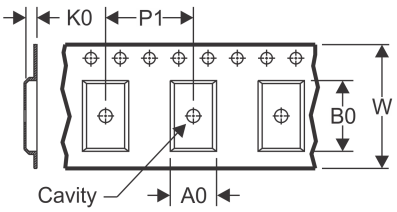
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

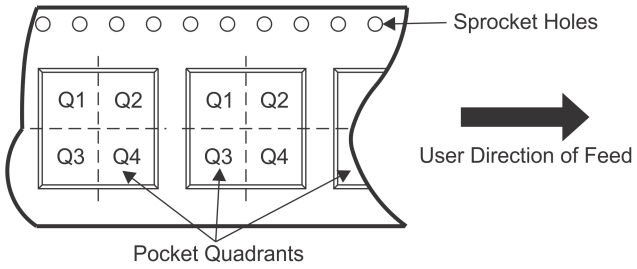


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

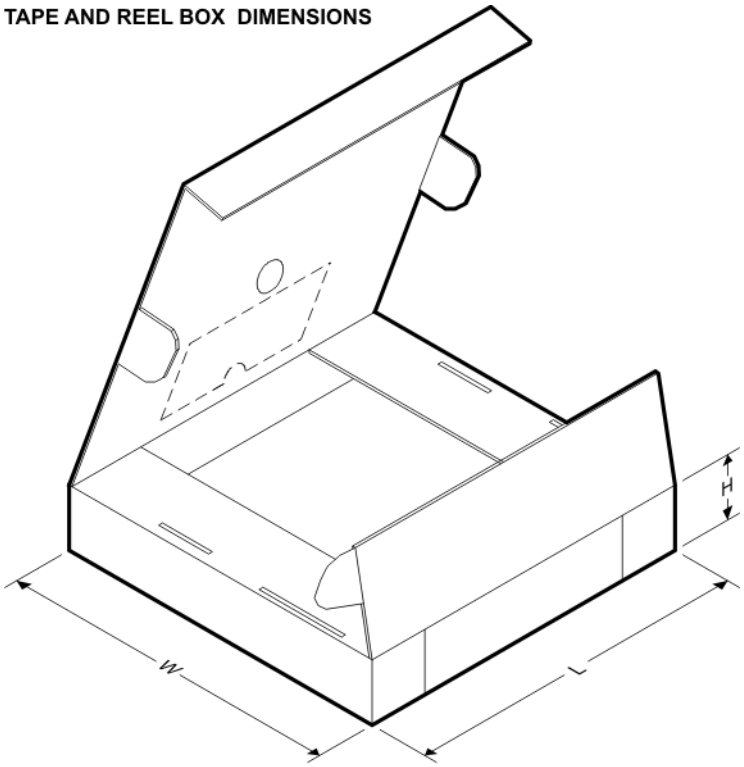
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR33630ADDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMR33630ARNXR	VQFN-HR	RNX	12	3000	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
LMR33630ARNXT	VQFN-HR	RNX	12	250	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
LMR33630BDDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMR33630BRNXR	VQFN-HR	RNX	12	3000	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
LMR33630BRNXT	VQFN-HR	RNX	12	250	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
LMR33630CDDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMR33630CRNXR	VQFN-HR	RNX	12	3000	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
LMR33630CRNXT	VQFN-HR	RNX	12	250	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



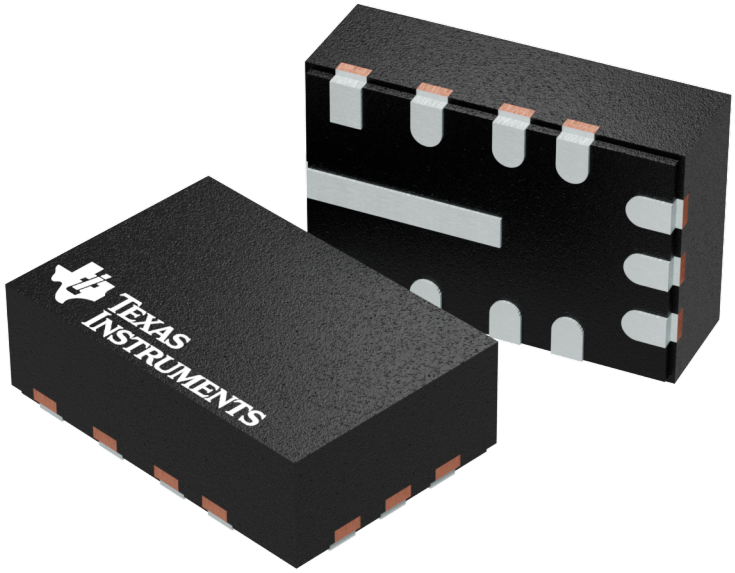
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR33630ADDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
LMR33630ARNXR	VQFN-HR	RNX	12	3000	195.0	200.0	45.0
LMR33630ARNXT	VQFN-HR	RNX	12	250	195.0	200.0	45.0
LMR33630BDDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
LMR33630BRNXR	VQFN-HR	RNX	12	3000	195.0	200.0	45.0
LMR33630BRNXT	VQFN-HR	RNX	12	250	195.0	200.0	45.0
LMR33630CDDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
LMR33630CRNXR	VQFN-HR	RNX	12	3000	195.0	200.0	45.0
LMR33630CRNXT	VQFN-HR	RNX	12	250	195.0	200.0	45.0

RNX 12 VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

2 x 3 mm, 0.5 mm pitch



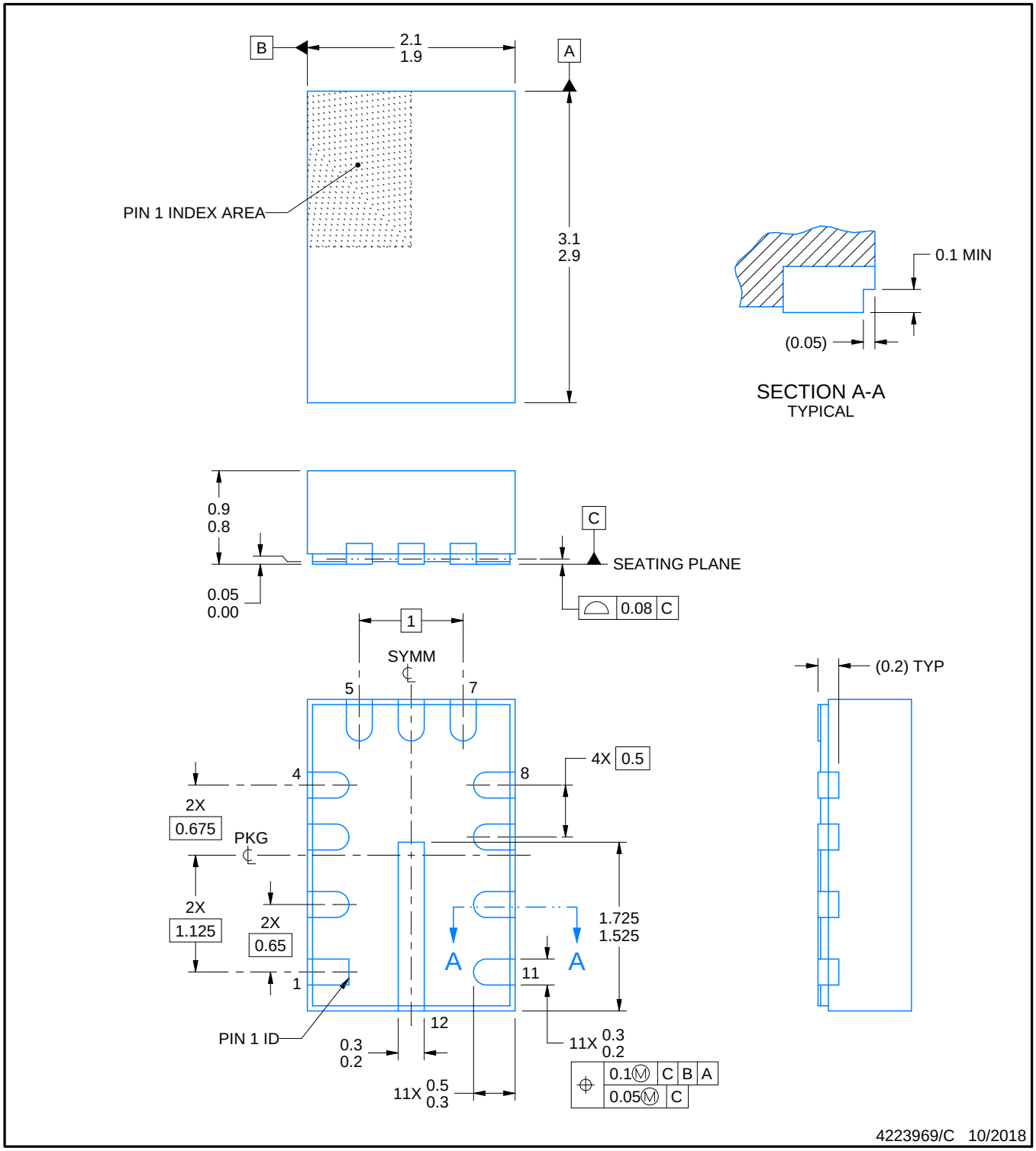
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RNX0012B

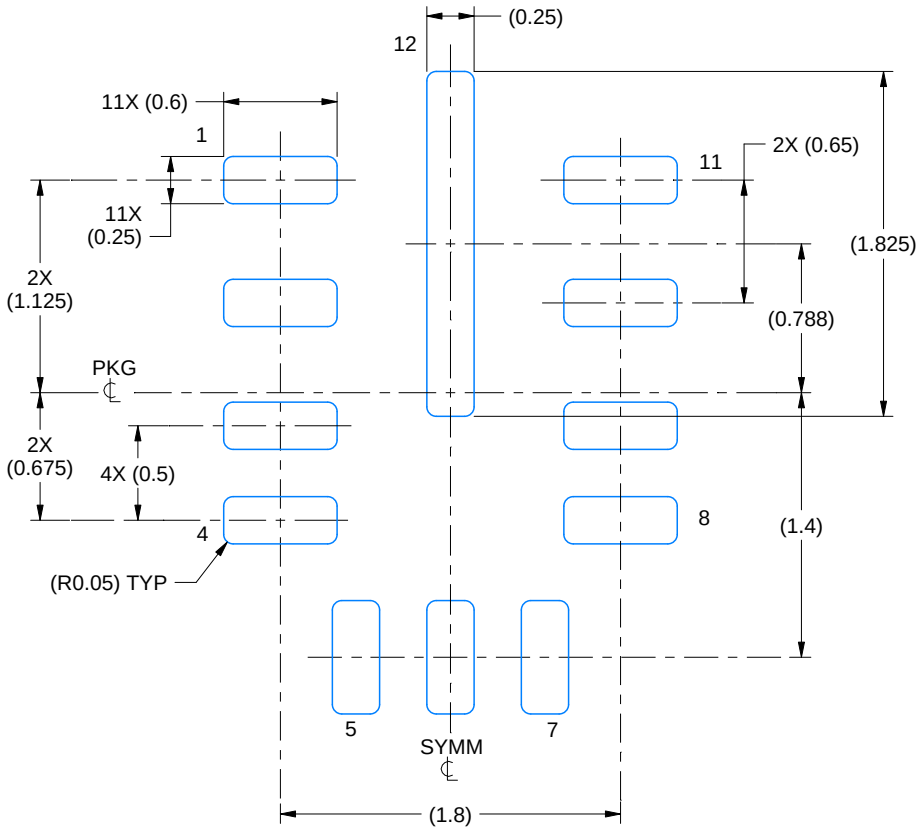
VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

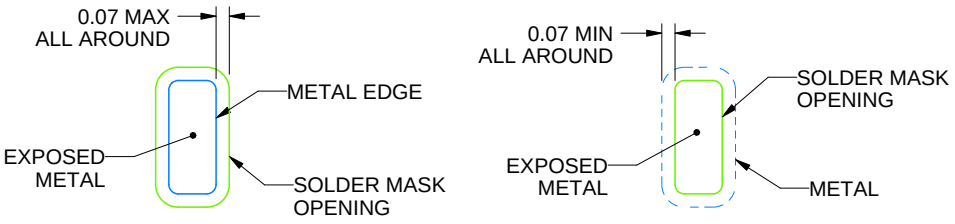


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

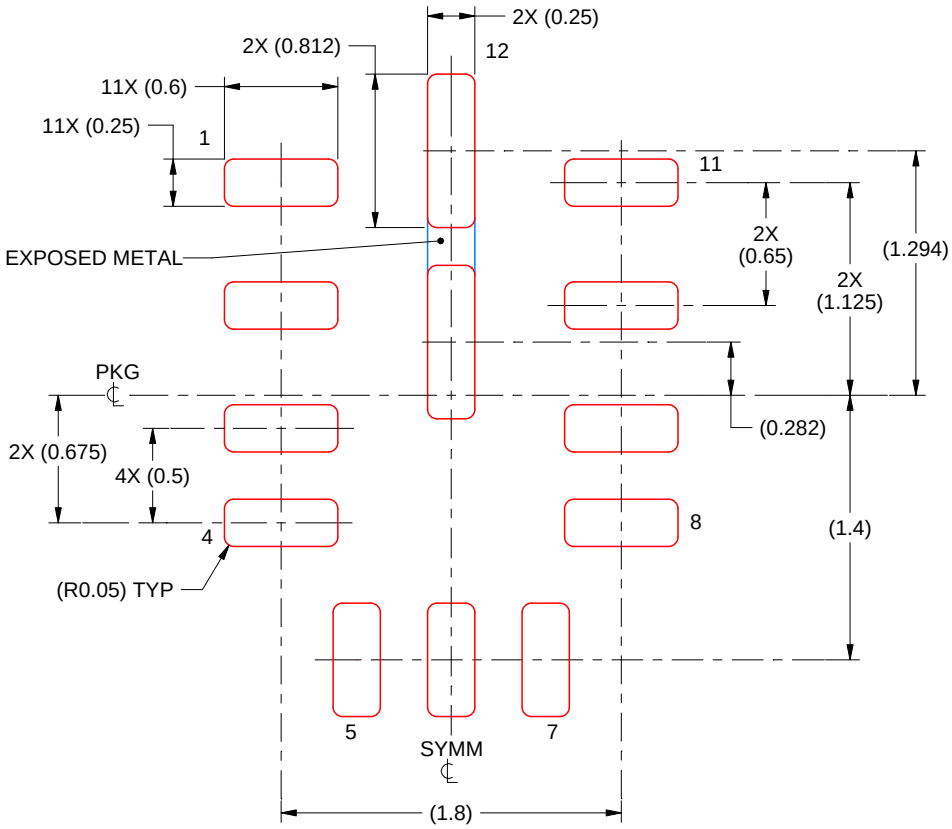


SOLDER MASK DETAILS

4223969/C 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



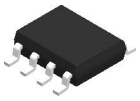
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR PAD 12
87.7% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4223969/C 10/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

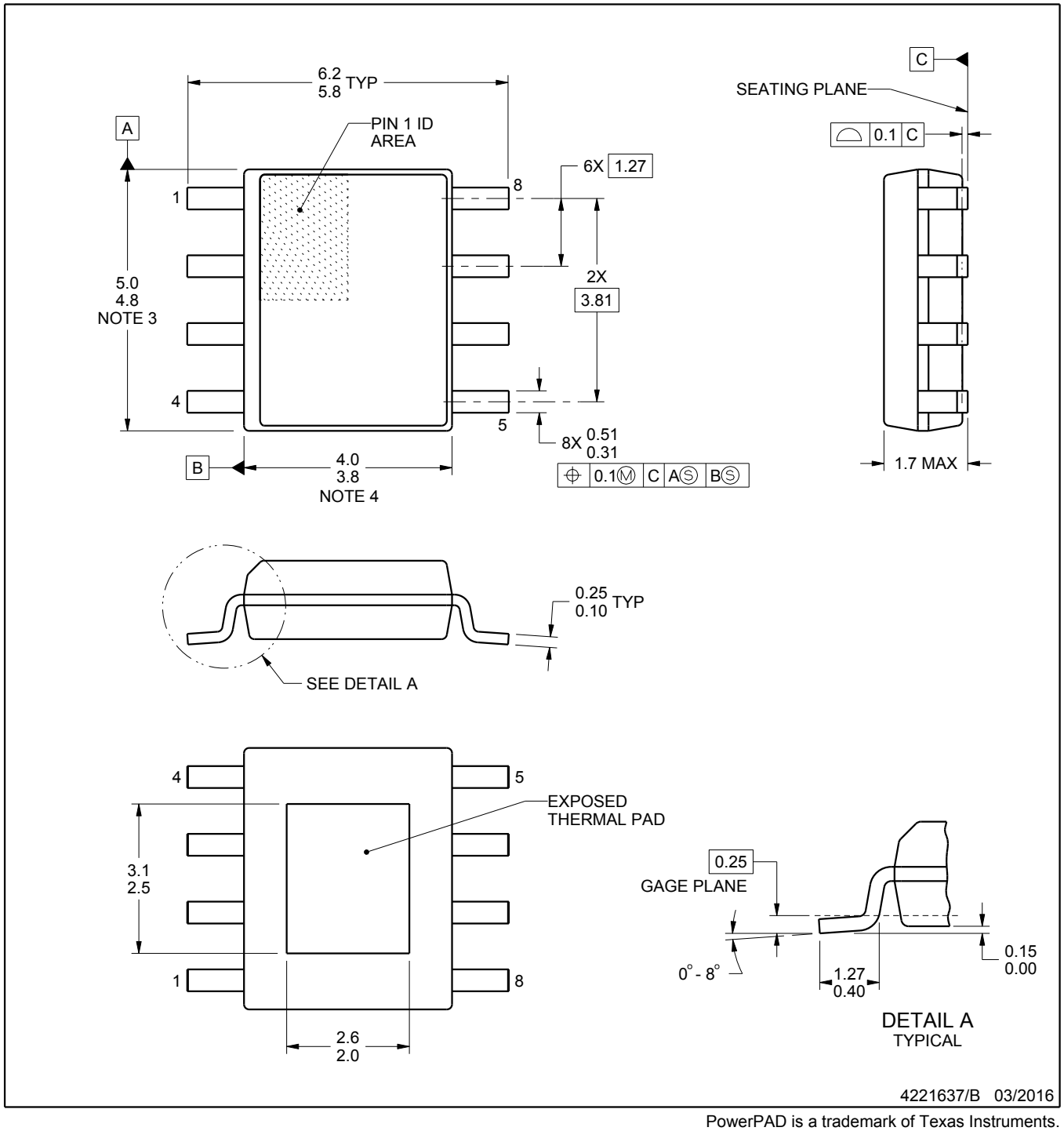


PACKAGE OUTLINE

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

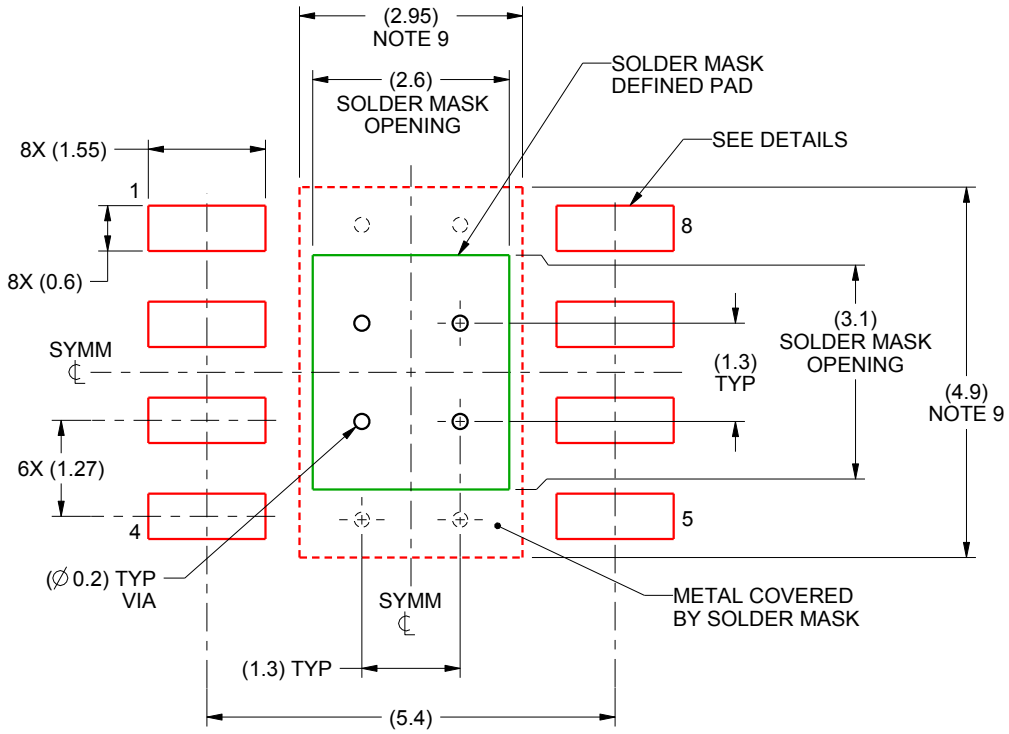
PLASTIC SMALL OUTLINE



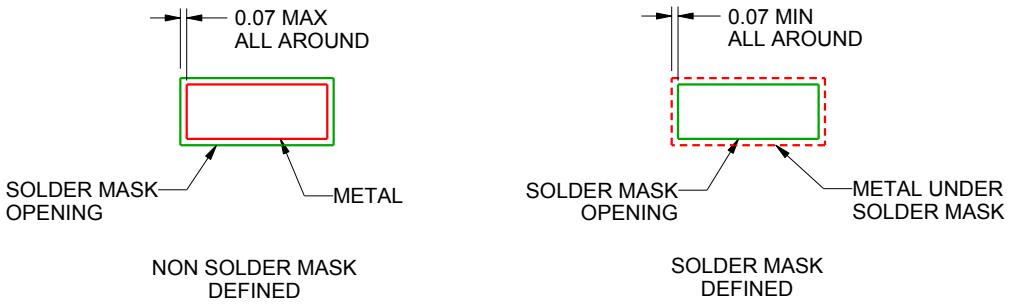
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

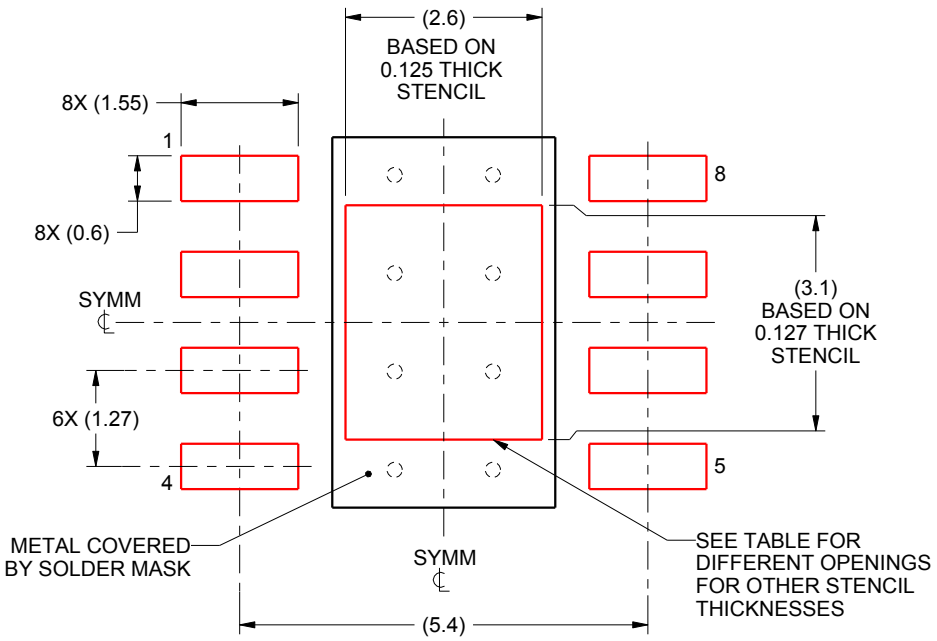


SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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