

## TPS709 具有使能功能的 150mA、30V、1 $\mu$ A I<sub>Q</sub> 稳压器

### 1 特性

- 超低 I<sub>Q</sub>: 1 $\mu$ A
- 反向电流保护
- 低 I<sub>SHUTDOWN</sub>: 150nA
- 输入电压范围: 2.7V 至 30V
- 支持 200mA 峰值输出
- 在温度范围内精度为 2%
- 可提供固定输出电压: 1.2V 至 6.5V
- 热关断及过流保护功能
- 封装: SOT-23-5、WSO-6

### 2 应用范围

- Zigbee™网络
- 家庭自动化
- 计量
- 电子秤
- 便携式功率工具
- 遥控器件
- 无线听筒, 智能电话, 掌上电脑 (PDA), 无线局域网 (WLAN), 和其它个人电脑 (PC) 扩展卡
- 大型家电

### 3 说明

TPS709 系列线性稳压器是针对功耗敏感型应用而设计的超低静态电流器件。一个精密带隙和误差放大器在温度范围内的精度为 2%。这些器件的静态电流仅为 1 $\mu$ A, 因此对于由电池供电、要求闲置状态功耗非常小的常开系统而言, 这是非常理想的解决方案。为了增加安全性, 这些器件还具有热关断、电流限制和反向电流保护功能。

关断模式通过将 EN 引脚拉为低电平进行使能。该模式的关断电流低至 150nA (典型值)。

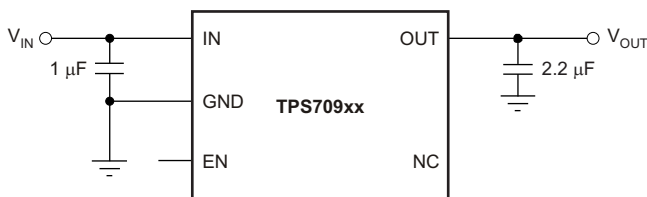
TPS709 系列采用 WSON-6 和 SOT-23-5 封装。

器件信息(1)

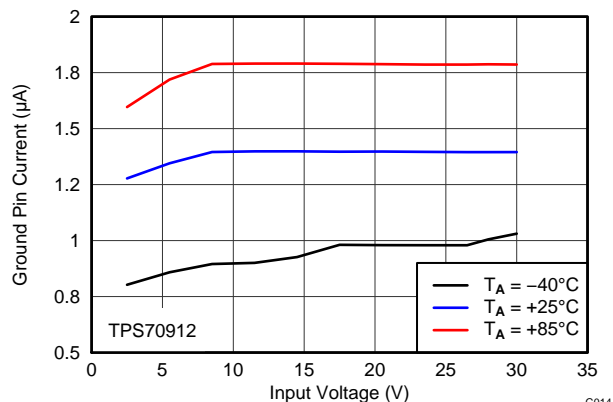
器件型号	封装	封装尺寸 (标称值)
TPS709	SOT-23 (5)	2.90mm x 1.60mm
	WSON (6)	2.00mm x 2.00mm

(1) 要了解所有可用封装, 请参见数据表末尾的封装选项附录。

典型应用电路



接地电流与 V<sub>IN</sub> 和温度间的关系



G014



## 目录

<b>1</b>	<b>特性</b> .....	<b>1</b>	<b>8</b>	<b>Application and Implementation</b> .....	<b>15</b>
<b>2</b>	<b>应用范围</b> .....	<b>1</b>	8.1	Application Information .....	15
<b>3</b>	<b>说明</b> .....	<b>1</b>	8.2	Typical Application .....	15
<b>4</b>	<b>修订历史记录</b> .....	<b>2</b>	<b>9</b>	<b>Power Supply Recommendations</b> .....	<b>16</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>4</b>	9.1	Power Dissipation .....	16
<b>6</b>	<b>Specifications</b> .....	<b>5</b>	<b>10</b>	<b>Layout</b> .....	<b>17</b>
6.1	Absolute Maximum Ratings .....	5	10.1	Layout Guidelines .....	17
6.2	ESD Ratings .....	5	10.2	Layout Example .....	17
6.3	Recommended Operating Conditions .....	5	<b>11</b>	<b>器件和文档支持</b> .....	<b>18</b>
6.4	Thermal Information .....	5	11.1	器件支持 .....	18
6.5	Electrical Characteristics .....	6	11.2	文档支持 .....	18
6.6	Typical Characteristics .....	7	11.3	社区资源 .....	18
<b>7</b>	<b>Detailed Description</b> .....	<b>13</b>	11.4	商标 .....	19
7.1	Overview .....	13	11.5	静电放电警告 .....	19
7.2	Functional Block Diagram .....	13	11.6	Glossary .....	19
7.3	Feature Description .....	13	<b>12</b>	<b>机械、封装和可订购信息</b> .....	<b>19</b>
7.4	Device Functional Modes .....	14			

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

<b>Changes from Revision F (December 2014) to Revision G</b>	<b>Page</b>
• Added DBV package for TPS709A to <i>Pin Configurations and Functions</i> section .....	4
• Added DBV package for TPS709B to <i>Pin Configurations and Functions</i> section .....	4
• Added TPS709A and TPS709B to Pin Functions table .....	4
• Moved operating junction temperature from <i>Electrical Characteristics</i> to <i>Recommended Operating Conditions</i> .....	5

<b>Changes from Revision E (November 2013) to Revision F</b>	<b>Page</b>
• 已更改标题格式以符合最新数据表标准 .....	1
• 已添加 <i>ESD</i> 额定值表，特性描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分 .....	1
• 已从文档中删除 SOT-223-4 封装 .....	1
• 已删除低压降特性要点) .....	1
• 已更改封装特性要点：已删除 SOT-223-4 和脚注 .....	1
• 已删除说明部分最后一段中的 SOT-223-4 .....	1
• 删除了第 1 页的引脚分配图 .....	1
• Deleted DCY package and footnote from Pin Configurations section .....	4
• Changed Pin Functions table: changed title and deleted DCY package .....	4
• Changed EN pin description in Pin Functions table .....	4
• Deleted the word 'range' from the last 2 rows of the Absolute Maximum Ratings table .....	5
• Deleted DCY column from Thermal Information table .....	5
• Added description text to the enabled mode discussion in the <i>Device Functional Modes</i> section .....	14

---

**Changes from Revision D (October 2013) to Revision E** **Page**


---

• 已将 DRV (SON-6) 封装状态从“产品预览”改为“量产数据” .....	1
• 已删除 脚注 1 中的 SON-6 封装 (特性部分) .....	1
• 已删除 引脚分配图注释中的 DRV 封装 .....	1
• Deleted DRV from pinout note in the <i>Pin Configurations</i> section .....	4

---

**Changes from Revision C (June 2013) to Revision D** **Page**


---

• 已将器件状态从“量产数据”改为“混合状态” .....	1
• 已更改 最后一个 特性 要点: 已添加脚注并已更改器件顺序 .....	1
• 已添加 在引脚分配图中添加了注释 .....	1
• Added product preview footnote to pin configurations .....	4

---

**Changes from Revision B (November 2012) to Revision C** **Page**


---

• 已添加 DCY (SOT-223) 和 DRV (SON) 封装至数据表 .....	1
• 已将 $I_Q$ 特性要点的值从 1.35 $\mu$ A 改为 1 $\mu$ A .....	1
• 已将 说明部分 第一段中的静态电流值从 1.35 $\mu$ A 改为 1 $\mu$ A .....	1
• 已将 说明部分 第二段中的“泄漏”改为“关断”。 .....	1
• 添加了典型应用电路 .....	1
• Added DCY and DRV packages to <i>Pin Configuration</i> section .....	4
• Added DCY and DRV packages to Pin Descriptions table .....	4
• Added DRV and DCY packages to Thermal Information table .....	5
• Changed ground pin current typical values for $I_{OUT} = 0$ -mA test conditions .....	6

---

**Changes from Revision A (October 2012) to Revision B** **Page**


---

• Added <i>Pin Configuration</i> section .....	4
• Changed <i>Line regulation</i> and <i>Load regulation</i> parameters in <i>Electrical Characteristics</i> table .....	6
• Changed $I_{GND}$ parameter test conditions in <i>Electrical Characteristics</i> table .....	6
• Changed $I_{SHUTDOWN}$ parameter test conditions in <i>Electrical Characteristics</i> table .....	6
• Changed footnote 4 in <i>Electrical Characteristics</i> table .....	6
• Changed second paragraph of <i>Dropout Voltage</i> section .....	13

---

**Changes from Original (March 2012) to Revision A** **Page**

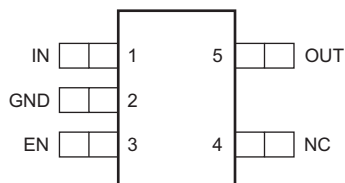

---

• 已将器件状态从“产品预览”改为“量产数据” .....	1
-------------------------------	---

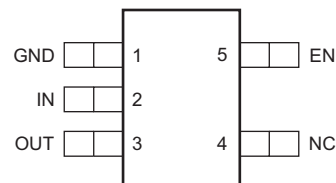
---

## 5 Pin Configuration and Functions

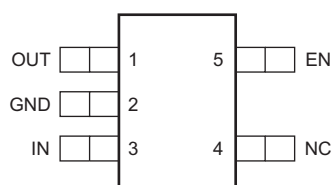
**TPS709: DBV Package  
5-Pin SOT-23  
Top View**



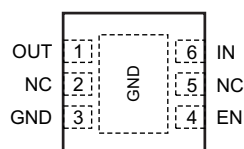
**TPS709B: DBV Package  
5-Pin SOT-23  
Top View**



**TPS709A: DBV Package  
5-Pin SOT-23  
Top View**



**DRV Package  
6-Pin WSON  
Top View**



### Pin Functions

NAME	PIN				I/O	DESCRIPTION
	DRV TPS709	DBV				
	TPS709	TPS709A	TPS709B			
EN	4	3	5	5	I	Enable pin. Drive this pin high to enable the device. Drive this pin low to put the device into low current shutdown. This pin can be left floating to enable the device. The maximum voltage must remain below 6.5 V.
GND	3	2	2	1	—	Ground
IN	6	1	3	2	I	Unregulated input to the device
NC	2, 5	4	4	4	—	No internal connection
OUT	1	5	1	3	O	Regulated output voltage. Connect a small 2.2- $\mu$ F or greater ceramic capacitor from this pin to ground to assure stability.
Thermal pad	—	—	—	—	—	The thermal pad is electrically connected to the GND node. Connect this pad to the GND plane for improved thermal performance.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

specified at  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  (unless otherwise noted); all voltages are with respect to GND<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	$V_{IN}$	-0.3	32	V
	$V_{EN}$	-0.3	7	
	$V_{OUT}$	-0.3	7	
Maximum output current	$I_{OUT}$	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	$P_{DISS}$	See <a href="#">Thermal Information</a>		
Operating junction temperature, $T_J$		-55	150	$^{\circ}\text{C}$
Storage temperature, $T_{stg}$		-55	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 2000$	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	$\pm 500$	

- (1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input voltage	2.7		30	V
$V_{OUT}$	Output voltage	1.2		6.5	V
$V_{EN}$	Enable voltage	0		6.5	V
$T_J$	Operating junction temperature	-40		125	$^{\circ}\text{C}$

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS709		UNIT
		DBV	DRV	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	212.1	73.1	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.5	97.0	$^{\circ}\text{C}/\text{W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	39.5	42.6	$^{\circ}\text{C}/\text{W}$
$\Psi_{JT}$	Junction-to-top characterization parameter	2.86	2.9	$^{\circ}\text{C}/\text{W}$
$\Psi_{JB}$	Junction-to-board characterization parameter	38.7	42.9	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	12.8	$^{\circ}\text{C}/\text{W}$

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

At ambient temperature ( $T_A$ ) =  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$  or  $2.7\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = 2\text{ V}$ , and  $C_{IN} = C_{OUT} = 2.2\text{-}\mu\text{F}$  ceramic, unless otherwise noted. Typical values are at  $T_A = 25^{\circ}\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage range		2.7		30	V
$V_{OUT}$	Output voltage range		1.2		6.5	V
$V_{OUT}$	DC output accuracy	$V_{OUT} < 3.3\text{ V}$	-2%		2%	
		$V_{OUT} \geq 3.3\text{ V}$	-1%		1%	
$\Delta V_{OUT}$	Line regulation	$(V_{OUT(\text{nom})} + 1\text{ V}, 2.7\text{ V}) \leq V_{IN} \leq 30\text{ V}$		3	10	mV
	Load regulation	$V_{IN} = V_{OUT(\text{typ})} + 1.5\text{ V}$ or $3\text{ V}$ (whichever is greater), $100\text{ }\mu\text{A} \leq I_{OUT} \leq 150\text{ mA}$		20	50	
$V_{DO}$	Dropout voltage <sup>(1)(2)</sup>	TPS70933, $I_{OUT} = 50\text{ mA}$		295	650	mV
		TPS70933, $I_{OUT} = 150\text{ mA}$		960	1400	
		TPS70950, $I_{OUT} = 50\text{ mA}$		245	500	
		TPS70950, $I_{OUT} = 150\text{ mA}$		690	1200	
		TPS70965, $I_{OUT} = 50\text{ mA}$		180	500	
		TPS70965, $I_{OUT} = 150\text{ mA}$		460	1000	
$I_{(CL)}$	Output current limit <sup>(3)</sup>	$V_{OUT} = 0.9 \times V_{OUT(\text{nom})}$	200	320	500	mA
$I_{GND}$	Ground pin current	$I_{OUT} = 0\text{ mA}$ , $V_{OUT} \leq 3.3\text{ V}$		1.3	2.05	$\mu\text{A}$
		$I_{OUT} = 0\text{ mA}$ , $V_{OUT} > 3.3\text{ V}$		1.4	2.25	
		$I_{OUT} = 150\text{ mA}$		350		
$I_{SHUTDOWN}$	Shutdown current	$V_{EN} \leq 0.4\text{ V}$ , $V_{IN} = 2.7\text{ V}$		150		nA
PSRR	Power-supply rejection ratio	$f = 10\text{ Hz}$		80		dB
		$f = 100\text{ Hz}$		62		
		$f = 1\text{ kHz}$		52		
$V_n$	Output noise voltage	BW = 10 Hz to 100 kHz, $I_{OUT} = 10\text{ mA}$ , $V_{IN} = 2.7\text{ V}$ , $V_{OUT} = 1.2\text{ V}$		190		$\mu\text{V}_{\text{RMS}}$
$t_{STR}$	Start-up time <sup>(4)</sup>	$V_{OUT(\text{nom})} \leq 3.3\text{ V}$		200	600	$\mu\text{s}$
		$V_{OUT(\text{nom})} > 3.3\text{ V}$		500	1500	
$V_{EN(\text{HI})}$	Enable pin high (enabled)		0.9			V
	Enable pin high (disabled)		0		0.4	
$I_{EN}$	EN pin current	$EN = 1.0\text{ V}$ , $V_{IN} = 5.5\text{ V}$		300		nA
$I_{(\text{REV})}$	Reverse current (flowing out of IN pin)	$V_{OUT} = 3\text{ V}$ , $V_{IN} = V_{EN} = 0\text{ V}$		10		nA
	Reverse current (flowing into OUT pin)	$V_{OUT} = 3\text{ V}$ , $V_{IN} = V_{EN} = 0\text{ V}$		100		
$t_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing		158		$^{\circ}\text{C}$
		Reset, temperature decreasing		140		

(1)  $V_{DO}$  is measured with  $V_{IN} = 0.98 \times V_{OUT(\text{nom})}$ .

(2) Dropout is only valid when  $V_{OUT} \geq 2.8\text{ V}$  because of the minimum input voltage limits.

(3) Measured with  $V_{IN} = V_{OUT} + 3\text{ V}$  for  $V_{OUT} \leq 2.5\text{ V}$ . Measured with  $V_{IN} = V_{OUT} + 2.5\text{ V}$  for  $V_{OUT} > 2.5\text{ V}$ .

(4) Startup time = time from EN assertion to  $0.95 \times V_{OUT(\text{nom})}$  and load =  $47\text{ }\Omega$ .

### 6.6 Typical Characteristics

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = 2\text{ V}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ , and  $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$  or  $2.7\text{ V}$  (whichever is greater), unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

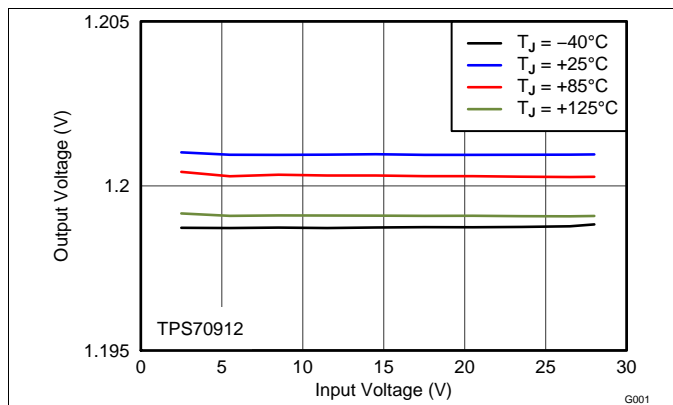


Figure 1. 1.2-V Line Regulation vs  $V_{IN}$  and Temperature

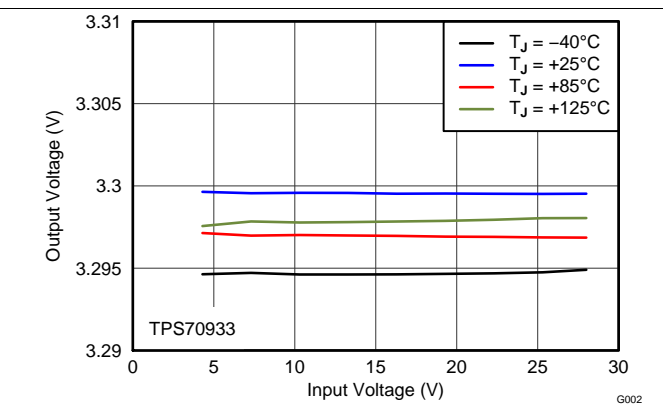


Figure 2. 3.3-V Line Regulation vs  $V_{IN}$  and Temperature

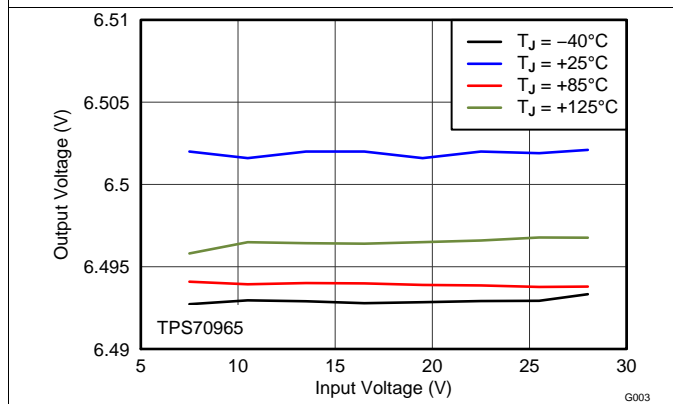


Figure 3. 6.5-V Line Regulation vs  $V_{IN}$  and Temperature

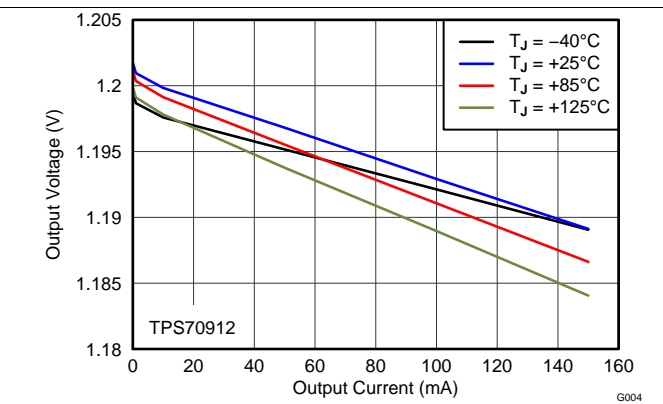


Figure 4. 1.2-V Load Regulation vs  $I_{OUT}$  and Temperature

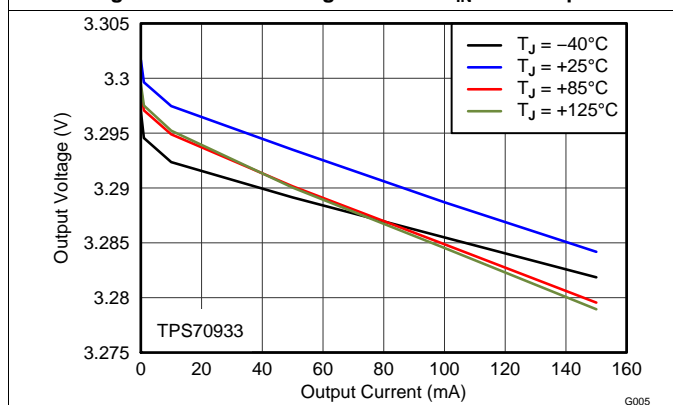


Figure 5. 3.3-V Load Regulation vs  $I_{OUT}$  and Temperature

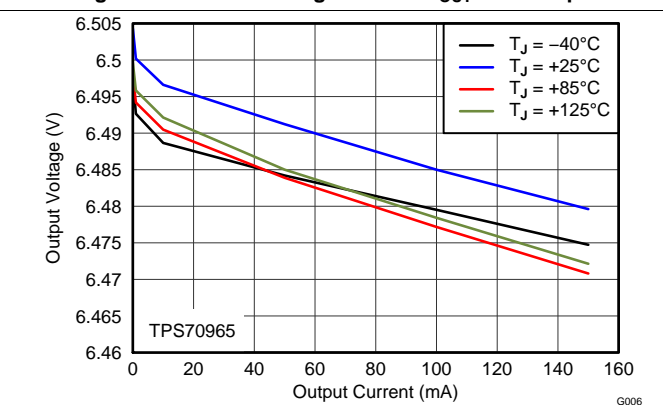


Figure 6. 6.5-V Load Regulation vs  $I_{OUT}$  and Temperature

Typical Characteristics (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = 2\text{ V}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ , and  $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$  or  $2.7\text{ V}$  (whichever is greater), unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

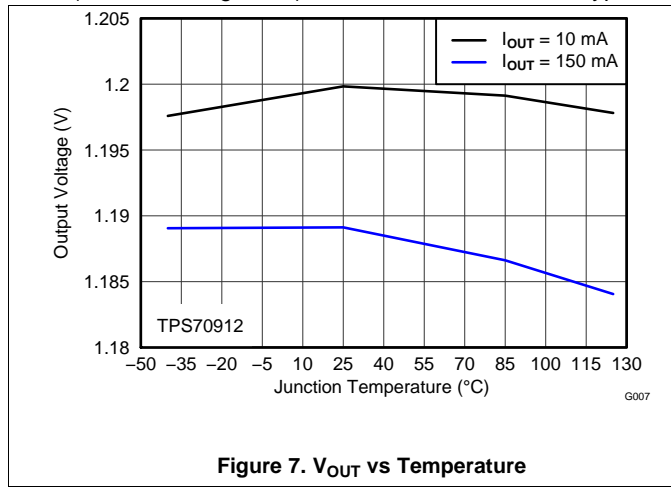


Figure 7.  $V_{OUT}$  vs Temperature

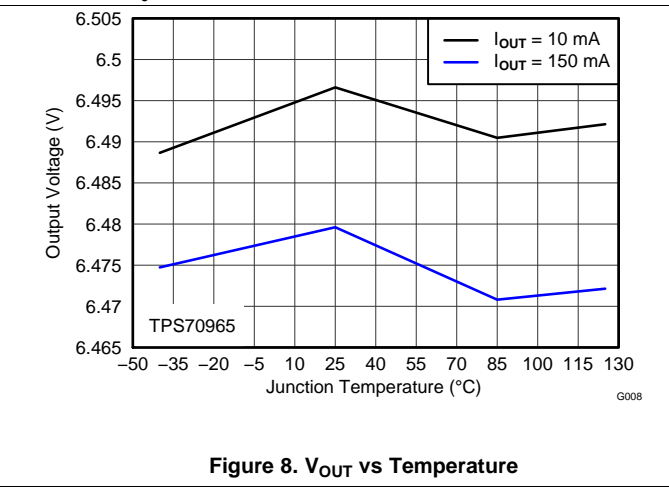


Figure 8.  $V_{OUT}$  vs Temperature

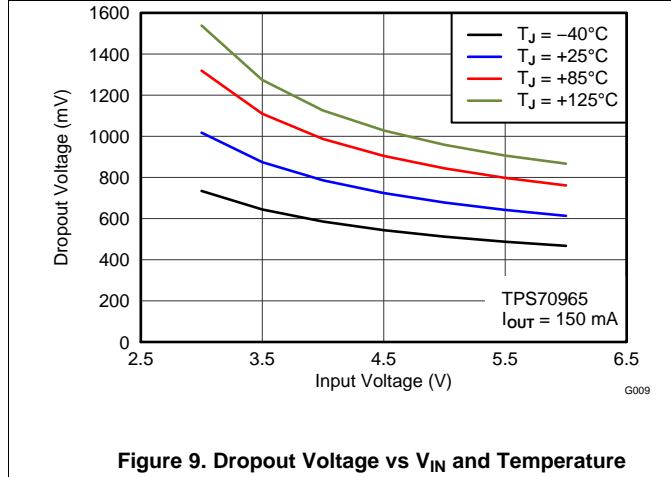


Figure 9. Dropout Voltage vs  $V_{IN}$  and Temperature

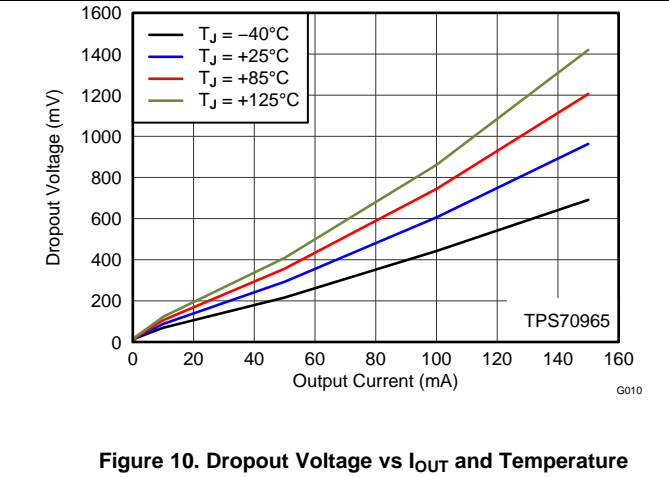


Figure 10. Dropout Voltage vs  $I_{OUT}$  and Temperature

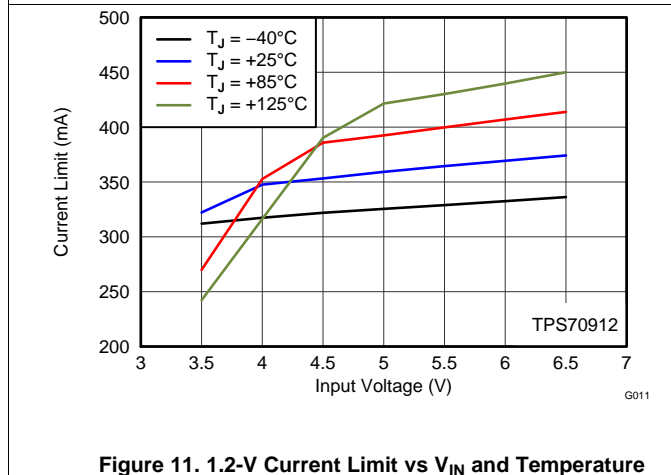


Figure 11. 1.2-V Current Limit vs  $V_{IN}$  and Temperature

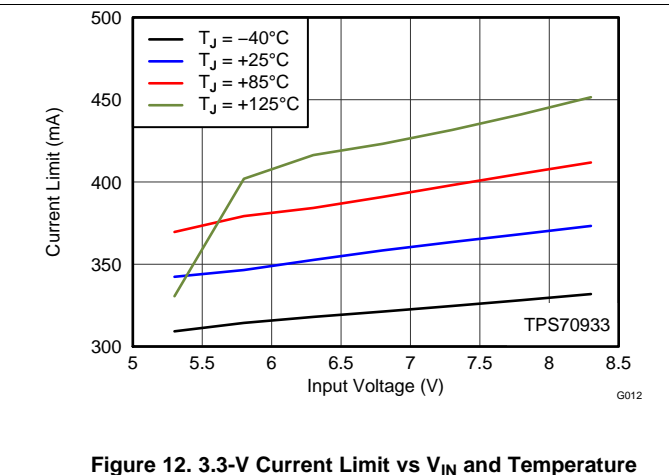


Figure 12. 3.3-V Current Limit vs  $V_{IN}$  and Temperature



Typical Characteristics (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = 2\text{ V}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ , and  $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$  or  $2.7\text{ V}$  (whichever is greater), unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

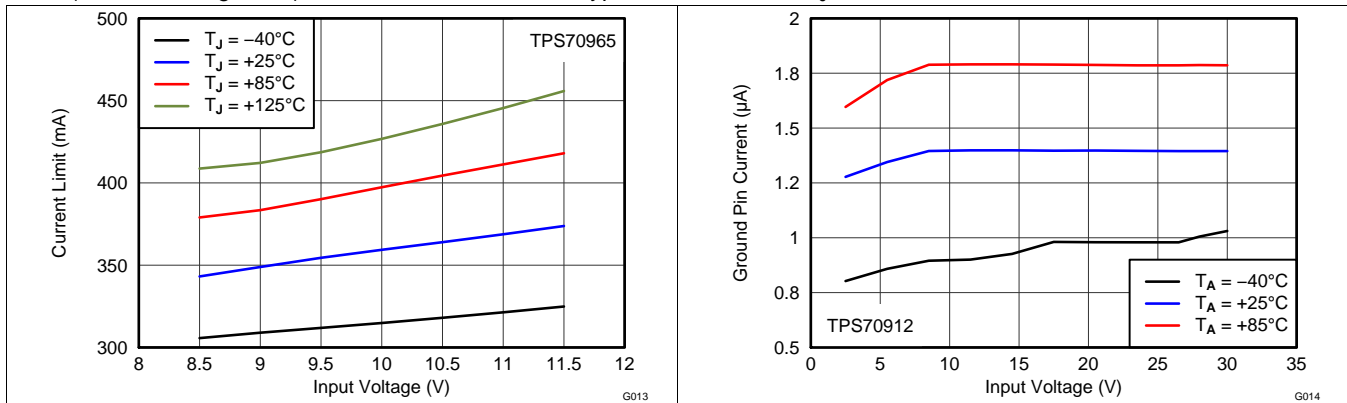


Figure 13. 6.5-V Current Limit vs  $V_{IN}$  and Temperature

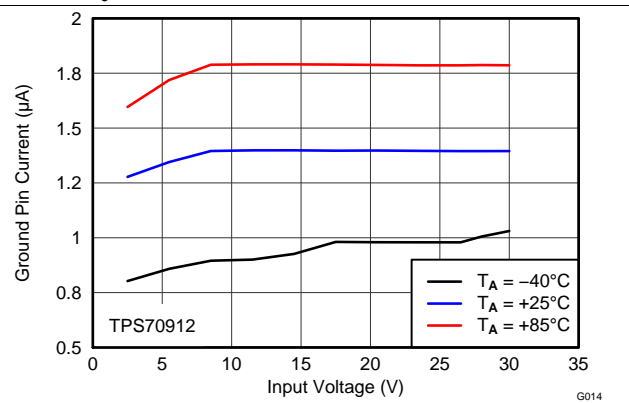


Figure 14. GND Current vs  $V_{IN}$  and Temperature

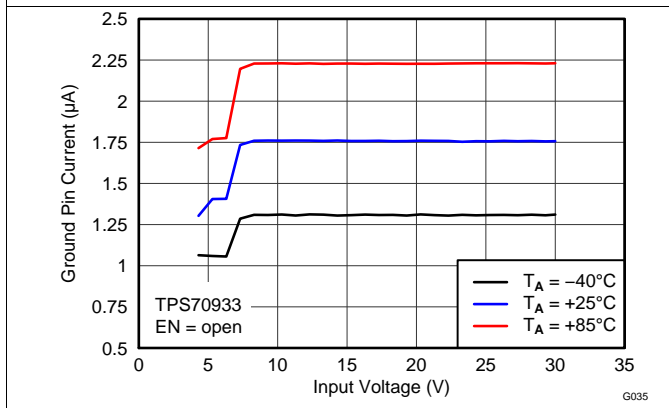


Figure 15. GND Current vs  $V_{IN}$  and Temperature

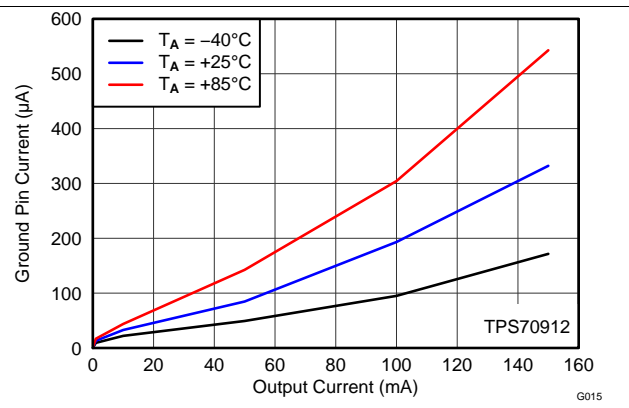


Figure 16. GND Current vs  $I_{OUT}$  and Temperature

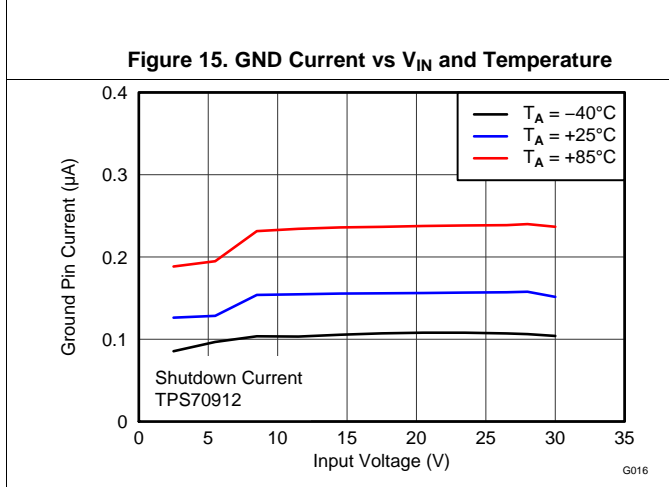


Figure 17. Shutdown Current vs  $V_{IN}$  and Temperature

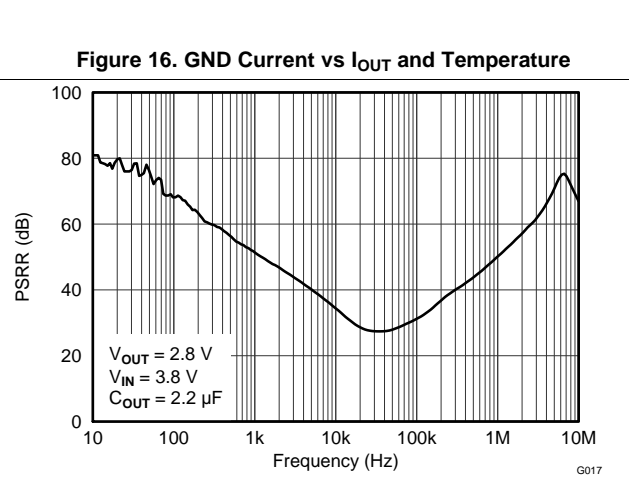


Figure 18. Power-Supply Rejection Ratio vs Frequency

Typical Characteristics (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = 2\text{ V}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ , and  $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$  or  $2.7\text{ V}$  (whichever is greater), unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

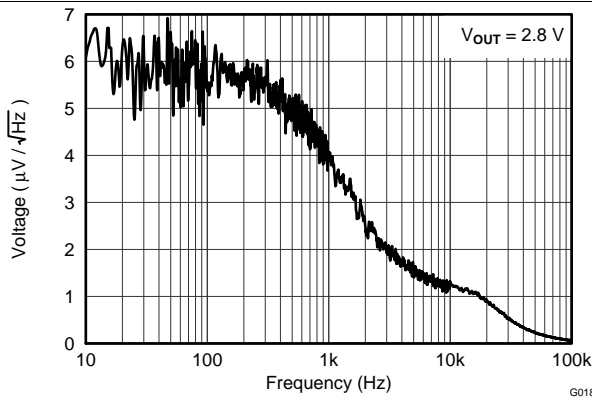


Figure 19. Noise

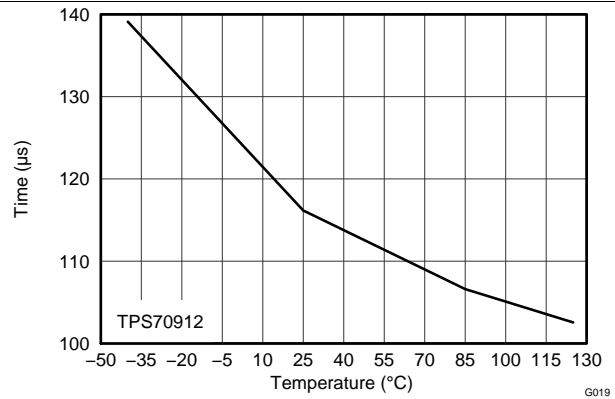


Figure 20. Start-Up Time vs Temperature

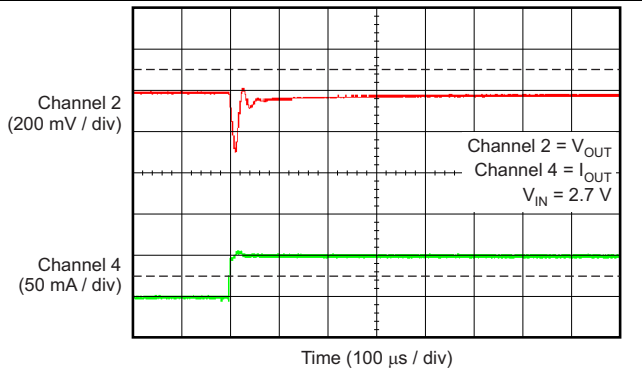


Figure 21. TPS70912 Load Transient (0 mA to 50 mA)

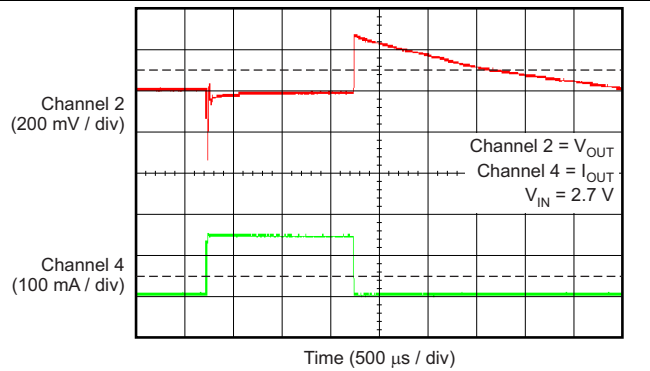


Figure 22. TPS70912 Load Transient (1 mA to 150 mA)

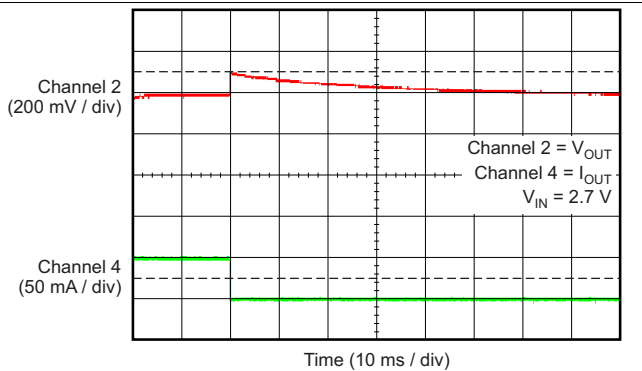


Figure 23. TPS70912 Load Transient (50 mA to 0 mA)

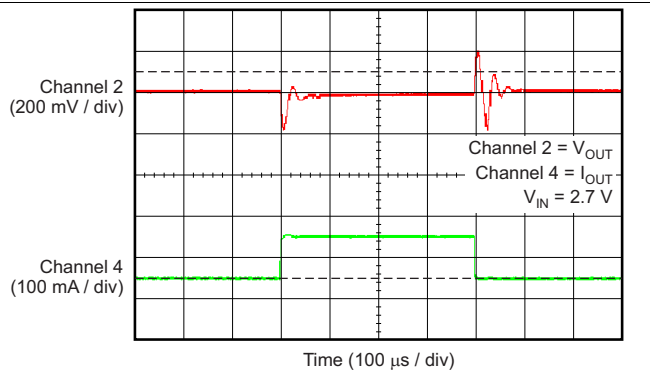


Figure 24. TPS70912 Load Transient (50 mA to 150 mA)

Typical Characteristics (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = 2\text{ V}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ , and  $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$  or  $2.7\text{ V}$  (whichever is greater), unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

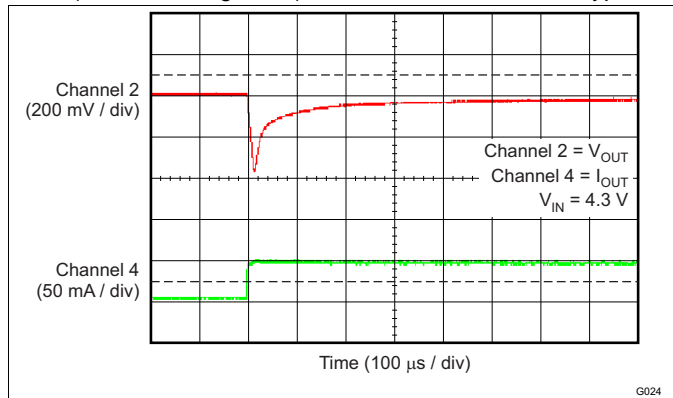


Figure 25. TPS70933 Load Transient (0 mA to 50 mA)

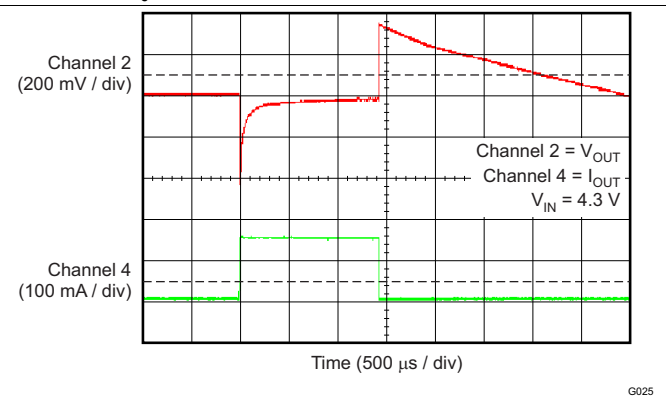


Figure 26. TPS70933 Load Transient (1 mA to 150 mA)

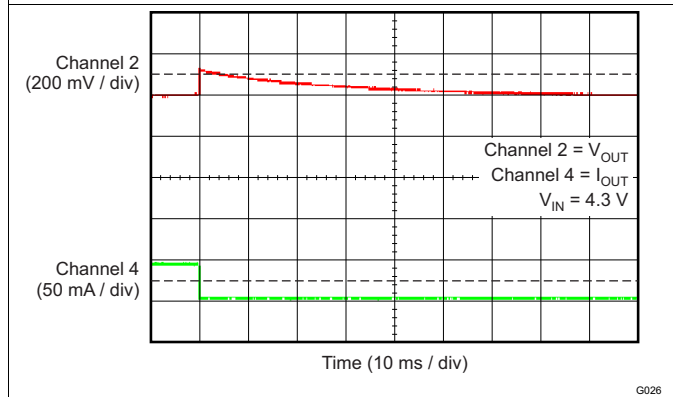


Figure 27. TPS70933 Load Transient (50 mA to 0 mA)

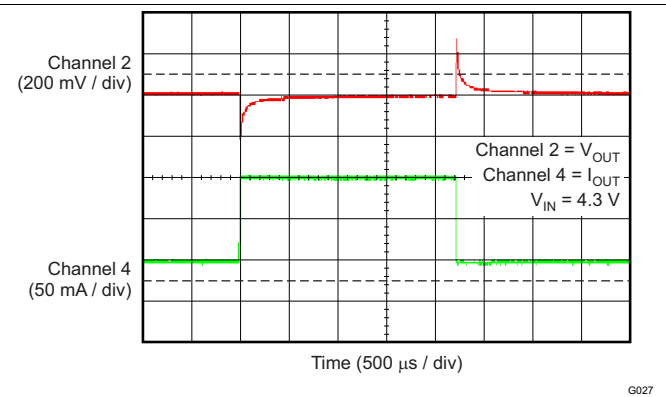


Figure 28. TPS70933 Load Transient (50 mA to 150 mA)

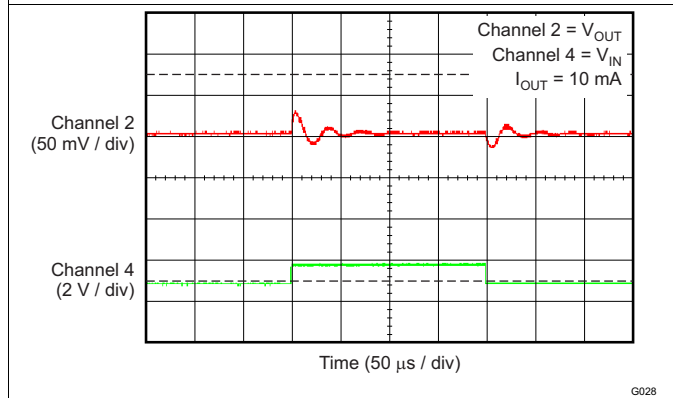


Figure 29. TPS70912 Line Transient (2.7 V to 3.7 V)

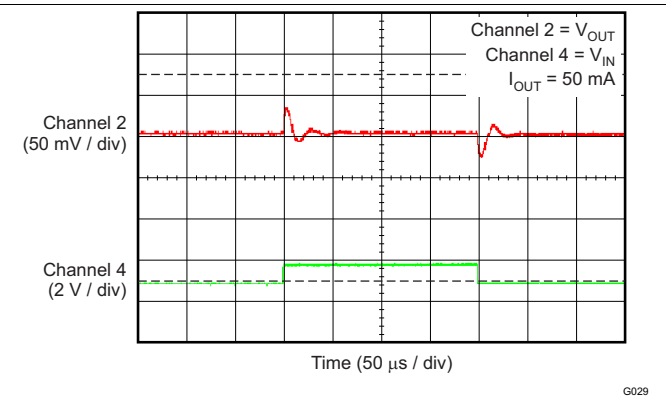


Figure 30. TPS70912 Line Transient (2.7 V to 3.7 V)

### Typical Characteristics (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = 2\text{ V}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ , and  $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$  or  $2.7\text{ V}$  (whichever is greater), unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

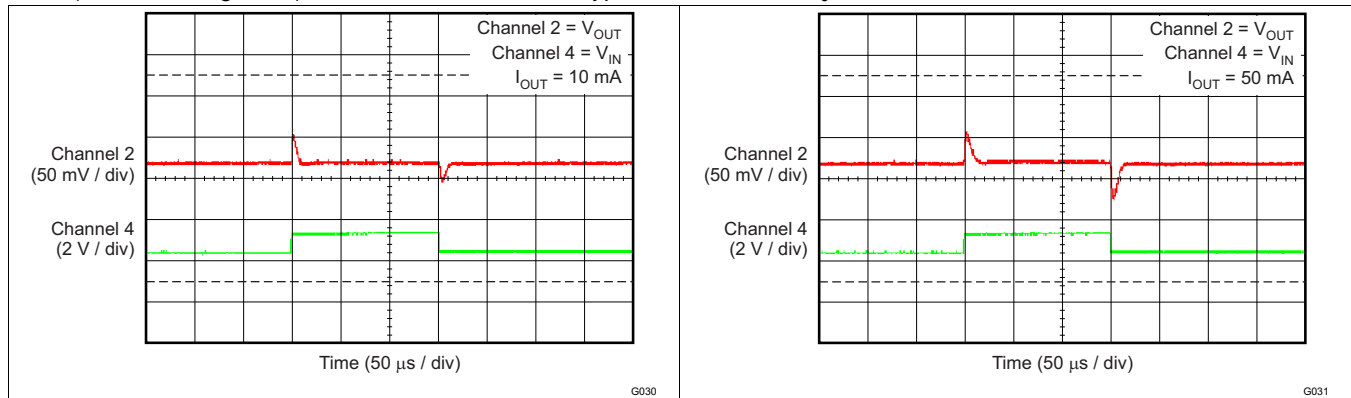


Figure 31. TPS70933 Line Transient (4.3 V to 5.3 V)

Figure 32. TPS70933 Line Transient (4.3 V to 5.3 V)

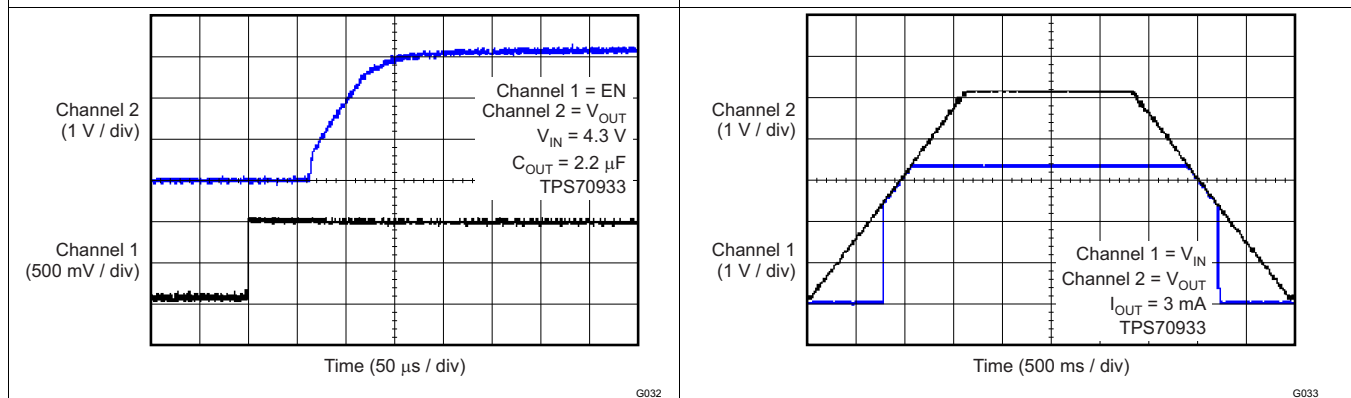


Figure 33. Power-Up with Enable

Figure 34. Power-Up and Power-Down Response

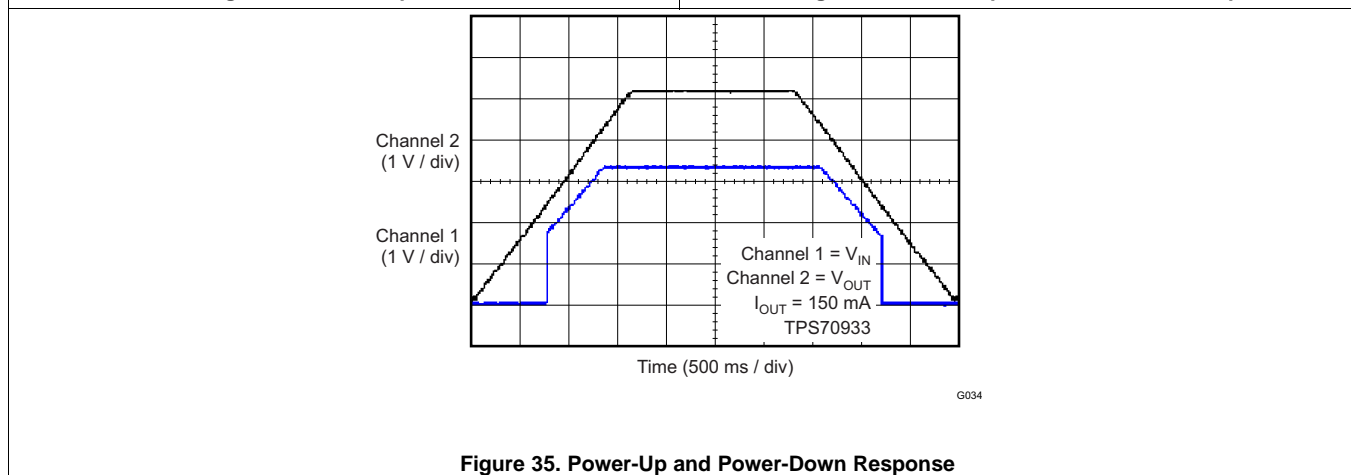


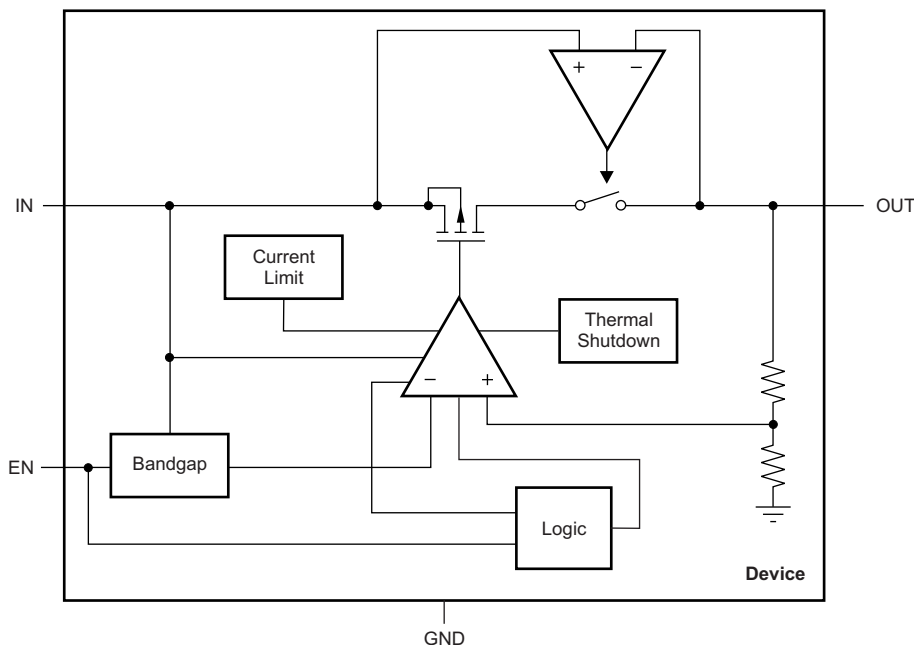
Figure 35. Power-Up and Power-Down Response

## 7 Detailed Description

### 7.1 Overview

The TPS709 series of devices are ultralow quiescent current, low-dropout (LDO) linear regulators. The TPS709 offers reverse current protection to block any discharge current from the output into the input. The TPS709 also features current limit and thermal shutdown for reliable operation.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Internal Current Limit

The TPS709 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and can be measured as  $(V_{OUT} = I_{LIMIT} \times R_{LOAD})$ . The PMOS pass transistor dissipates  $[(V_{IN} - V_{OUT}) \times I_{LIMIT}]$  until a thermal shutdown is triggered and the device turns off. When cool, the device is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the [Thermal Protection](#) section for more details.

The TPS709 is characterized over the recommended operating output current range up to 150 mA. The internal current limit begins to limit the output current at a minimum of 200 mA of output current. The TPS709 continues to operate for output currents between 150 mA and 200 mA but some data sheet parameters may not be met.

#### 7.3.2 Dropout Voltage

The TPS709 use a PMOS pass transistor to achieve low dropout voltage. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage ( $V_{DO}$ ), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the PMOS pass element.  $V_{DO}$  approximately scales with the output current because the PMOS device functions like a resistor in dropout.

The ground pin current of many linear voltage regulators increases substantially when the device is operated in dropout. This increase in ground pin current while operating in dropout can be several orders of magnitude larger than when the device is not in dropout. The TPS709 employs a special control loop that limits the increase in ground pin current while operating in dropout. This functionality allows for the most efficient operation while in dropout conditions that can greatly increase battery run times.

## Feature Description (continued)

### 7.3.3 Undervoltage Lockout (UVLO)

The TPS709 uses an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry operates properly.

### 7.3.4 Reverse-Current Protection

The TPS709 has integrated reverse-current protection. Reverse-current protection prevents the flow of current from the OUT pin to the IN pin when output voltage is higher than input voltage. The reverse-current protection circuitry places the power path in high impedance when the output voltage is higher than the input voltage. This setting reduces leakage current from the output to the input to 10 nA, typical. The reverse current protection is always active regardless of the enable pin logic state or if the OUT pin voltage is greater than 1.8 V. Reverse current can flow if the output voltage is less than 1.8 V and if input voltage is less than the output voltage.

If voltage is applied to the input pin, then the maximum voltage that can be applied to the OUT pin is the lower of three times the nominal output voltage or 6.5 V. For example, if the 1.2-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 3.6 V. If the 5.0-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 6.5 V.

## 7.4 Device Functional Modes

The TPS709 has the following functional modes:

1. **Enabled:** When the enable pin (EN) goes above 0.9 V, the device is enabled. EN is pulled high by a 300-nA current source; therefore, EN can be left floating to enable the device. Do not connect EN to VIN. The EN pin is clamped by a 6.5-V Zener diode. Do not exceed the 7-V absolute maximum rating on the enable pin or excessive current flowing into the Zener clamp will destroy the device.
2. **Disabled:** When EN goes below 0.4 V, the device is disabled. During this time, OUT is high impedance and the current into IN ( $I_{\text{SHUTDOWN}}$ ) is typically 150 nA.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS709 is a series of devices that belong to a new family of next-generation voltage regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. This performance, combined with low noise and very good PSRR with little ( $V_{IN} - V_{OUT}$ ) headroom, makes these devices ideal for RF portable applications, current limit, and thermal protection. The TPS709 is specified from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

#### 8.1.1 Input and Output Capacitor

The TPS709 devices are stable with output capacitors with an effective capacitance of  $2.0\ \mu\text{F}$  or greater for output voltages below  $1.5\ \text{V}$ . For output voltages equal or greater than  $1.5\ \text{V}$ , the minimum effective capacitance for stability is  $1.5\ \mu\text{F}$ . The maximum capacitance for stability is  $47\ \mu\text{F}$ . The equivalent series resistance (ESR) of the output capacitor must be between  $0\ \Omega$  and  $0.2\ \Omega$  for stability.

The effective capacitance is the minimum capacitance value of a capacitor after taking into account variations resulting from tolerances, temperature, and dc bias effects. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and ESR over temperature.

Although an input capacitor is not required for stability, good analog design practice is to connect a  $0.1\text{-}\mu\text{F}$  to  $2.2\text{-}\mu\text{F}$  capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is necessary if line transients greater than  $10\ \text{V}$  in magnitude are anticipated.

#### 8.1.2 Transient Response

As with any regulator, increasing the output capacitor size reduces over- and undershoot magnitude, but increases transient response duration.

### 8.2 Typical Application

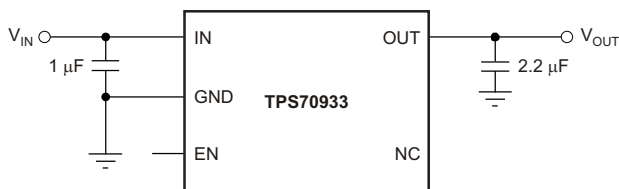


Figure 36. Wide Input, 3.3-V, Low- $I_Q$  Rail

#### 8.2.1 Design Requirements

Table 1 summarizes the design requirements for Figure 36.

Table 1. Design Requirements for a Wide Input, 3.3-V, Low- $I_Q$  Rail Application

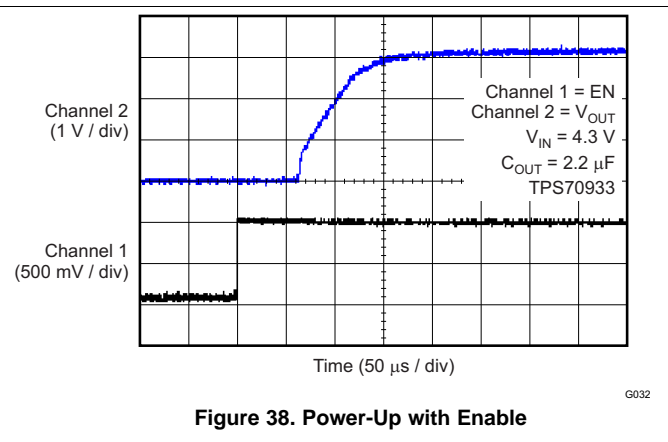
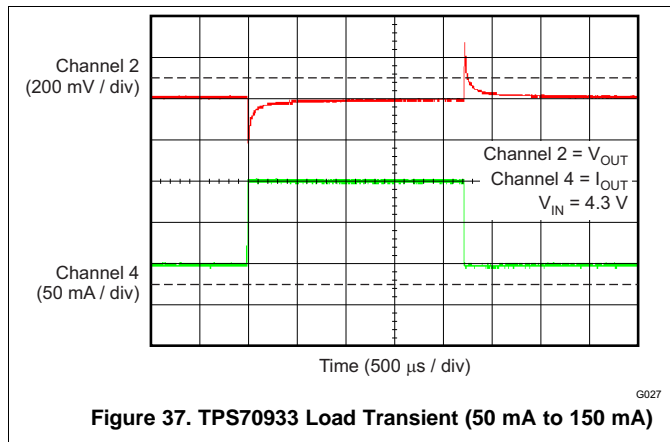
PARAMETER	DESIGN SPECIFICATION
$V_{IN}$	5 V to 20 V
$V_{OUT}$	3.3 V
$I_{(IN)}$ (no load)	$< 5\ \mu\text{A}$
$I_{OUT}$ (max)	150 mA

## 8.2.2 Detailed Design Procedure

Select a 2.2- $\mu\text{F}$ , 10-V X7R output capacitor to satisfy the minimum output capacitance requirement with a 3.3-V dc bias.

Select a 1.0- $\mu\text{F}$ , 25-V X7R input capacitor to provide input noise filtering and eliminate high-frequency voltage transients.

## 8.2.3 Application Curves



## 9 Power Supply Recommendations

This device is designed to operate with an input supply range of 2.7 V to 30 V. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise performance.

### 9.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC low and high-K boards are given in the [Thermal Information](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ( $P_{DISS}$ ) is equal to the product of the output current and the voltage drop across the output pass element, as shown in [Equation 1](#):

$$P_{DISS} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$



## 10 Layout

### 10.1 Layout Guidelines

Place input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must be connected directly to the device GND pin.

#### 10.1.1 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C, maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The TPS709 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS709 into thermal shutdown degrades device reliability.

### 10.2 Layout Example

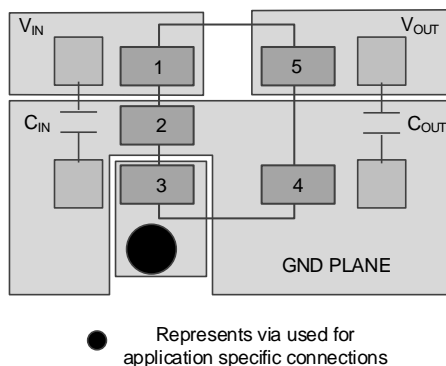


Figure 39. Layout Example for DBV Package

## 11 器件和文档支持

### 11.1 器件支持

#### 11.1.1 开发支持

##### 11.1.1.1 评估模块

评估模块 (EVM) 可与 TPS709xx 配套使用, 帮助评估初始电路性能。TPS70933EVM-110 评估模块 (和相关的用户指南) 可在德州仪器 (TI) 网站上的产品文件夹中获取, 也可直接从 TI 网上商店购买。

##### 11.1.1.2 Spice 模型

分析模拟电路和系统的性能时, 使用 SPICE 模型对电路性能进行计算机仿真非常有用。您可以从产品文件夹中的仿真模型下获取 TPS709 的 SPICE 模型。

#### 11.1.2 器件命名规则

表 2. 器件命名规则<sup>(1)</sup>

产品	V <sub>OUT</sub>
TPS709xx(x)yyyz	<b>XX(X)</b> 是标称输出电压。对于分辨率为 100mV 的输出电压, 订货编号中使用两位数字; 否则, 使用三位数字 (例如, 28 = 2.8V; 125 = 1.25V)。 <b>YYY</b> 为封装标识符。 <b>Z</b> 为卷带数量 (R = 3000, T = 250)。

(1) 要获得最新的封装和订货信息, 请参阅本文档末尾的封装选项附录, 或者登录 TI 的网站 [www.ti.com.cn](http://www.ti.com.cn) 进行查询。

### 11.2 文档支持

#### 11.2.1 相关文档

- 《TPS70933EVM-110 评估模块用户指南》, [SLVU689](#)

### 11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 商标

E2E is a trademark of Texas Instruments.

Zigbee is a trademark of ZigBee Alliance.

All other trademarks are the property of their respective owners.

## 11.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## 重要声明

德州仪器(TI)及其下属子公司有权根据 JESD46 最新标准,对所提供的产品和服务进行更正、修改、增强、改进或其它更改,并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息,并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内,且 TI 认为有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定,否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险,客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息,不能构成从 TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可,或是 TI 的专利权或其它知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分,仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时,如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分,则会失去相关 TI 组件或服务的所有明示或暗示授权,且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意,尽管任何应用相关信息或支持仍可能由 TI 提供,但他们将独立负责满足与其产品及其在应用中使用的 TI 产品相关的所有法律、法规和安全相关要求。客户声明并同意,他们具备制定与实施安全措施所需的全部专业技术和知识,可预见故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中,为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此,此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备)的授权许可,除非各方授权官员已经达成了专门管控此类使用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同意,对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用,其风险由客户单独承担,并且由客户独立负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品,这些产品主要用于汽车。在任何情况下,因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	<a href="http://www.ti.com.cn/audio">www.ti.com.cn/audio</a>	通信与电信	<a href="http://www.ti.com.cn/telecom">www.ti.com.cn/telecom</a>
放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
电源管理	<a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>	视频和影像	<a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>
微控制器 (MCU)	<a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>		
RFID 系统	<a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>		
OMAP应用处理器	<a href="http://www.ti.com/omap">www.ti.com/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122  
Copyright © 2016, 德州仪器半导体技术(上海)有限公司

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS70912DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCX	<a href="#">Samples</a>
TPS70912DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCX	<a href="#">Samples</a>
TPS70912DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCX	<a href="#">Samples</a>
TPS70912DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCX	<a href="#">Samples</a>
TPS709135DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCY	<a href="#">Samples</a>
TPS709135DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCY	<a href="#">Samples</a>
TPS70915DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIM	<a href="#">Samples</a>
TPS70915DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIM	<a href="#">Samples</a>
TPS70915DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIM	<a href="#">Samples</a>
TPS70915DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIM	<a href="#">Samples</a>
TPS70916DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCZ	<a href="#">Samples</a>
TPS70916DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCZ	<a href="#">Samples</a>
TPS70918DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDA	<a href="#">Samples</a>
TPS70918DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDA	<a href="#">Samples</a>
TPS70918DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDA	<a href="#">Samples</a>
TPS70918DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDA	<a href="#">Samples</a>
TPS70919DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDB	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS70919DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDB	<a href="#">Samples</a>
TPS70925DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDC	<a href="#">Samples</a>
TPS70925DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDC	<a href="#">Samples</a>
TPS70925DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDC	<a href="#">Samples</a>
TPS70925DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDC	<a href="#">Samples</a>
TPS70927DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDD	<a href="#">Samples</a>
TPS70927DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDD	<a href="#">Samples</a>
TPS70928DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDE	<a href="#">Samples</a>
TPS70928DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDE	<a href="#">Samples</a>
TPS70930DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDF	<a href="#">Samples</a>
TPS70930DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDF	<a href="#">Samples</a>
TPS70930DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDF	<a href="#">Samples</a>
TPS70930DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDF	<a href="#">Samples</a>
TPS70933DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDG	<a href="#">Samples</a>
TPS70933DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDG	<a href="#">Samples</a>
TPS70933DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDG	<a href="#">Samples</a>
TPS70933DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDG	<a href="#">Samples</a>
TPS70936DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SEJ	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS70936DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SEJ	<a href="#">Samples</a>
TPS70936DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1FV	<a href="#">Samples</a>
TPS70938DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIC	<a href="#">Samples</a>
TPS70938DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIC	<a href="#">Samples</a>
TPS70939DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SID	<a href="#">Samples</a>
TPS70939DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SID	<a href="#">Samples</a>
TPS70950DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDH	<a href="#">Samples</a>
TPS70950DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDH	<a href="#">Samples</a>
TPS70950DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDH	<a href="#">Samples</a>
TPS70950DRVVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDH	<a href="#">Samples</a>
TPS70960DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIT	<a href="#">Samples</a>
TPS70960DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIT	<a href="#">Samples</a>
TPS709A30DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11RF	<a href="#">Samples</a>
TPS709A30DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11RF	<a href="#">Samples</a>
TPS709A33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11SF	<a href="#">Samples</a>
TPS709A33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11SF	<a href="#">Samples</a>
TPS709B33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13C7	<a href="#">Samples</a>
TPS709B33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13C7	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS709B345DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1XSW	<a href="#">Samples</a>
TPS709B50DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13D7	<a href="#">Samples</a>
TPS709B50DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13D7	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70912DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS70912DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70912DRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70912DRVT	WSO	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS709135DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709135DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70915DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70915DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70915DRVR	WSO	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70915DRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70915DRVT	WSO	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70915DRVT	WSO	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70916DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70916DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70918DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70918DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70918DRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70918DRVT	WSO	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70919DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70919DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70925DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70925DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS70925DRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70925DRVT	WSO	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70927DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70927DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70928DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70928DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70930DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70930DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70930DRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70930DRVT	WSO	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70933DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS70933DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70933DRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70933DRVT	WSO	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70936DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS70936DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70936DRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70938DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70938DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70939DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70939DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950DRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70950DRVT	WSO	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70960DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70960DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709A30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709A30DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709A33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709A33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709B33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709B33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709B345DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709B50DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709B50DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70912DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70912DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70912DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70912DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS709135DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS709135DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70915DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70915DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70915DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS70915DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70915DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS70915DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS70916DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70916DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70918DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70918DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70918DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70918DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS70919DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70919DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70925DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70925DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70925DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70925DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS70927DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70927DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70928DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70928DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70930DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70930DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70930DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70930DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS70933DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70933DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70933DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70933DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS70936DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70936DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70936DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS70938DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70938DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70939DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70939DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70950DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70950DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70950DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
TPS70950DRVT	WSON	DRV	6	250	182.0	182.0	20.0
TPS70960DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70960DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS709A30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS709A30DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS709A33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS709A33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS709B33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS709B33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS709B345DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS709B50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS709B50DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

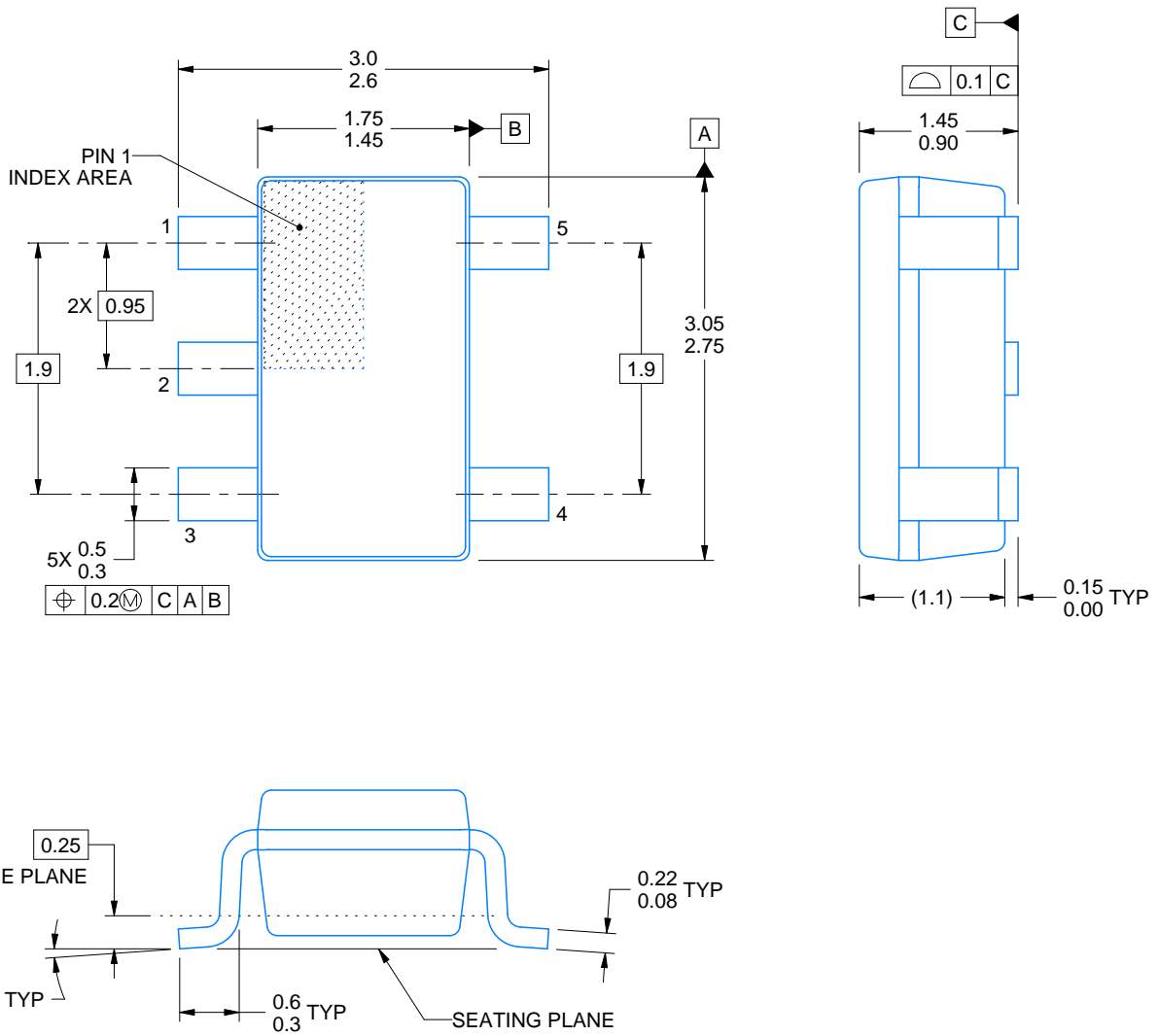
DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/E 09/2019

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

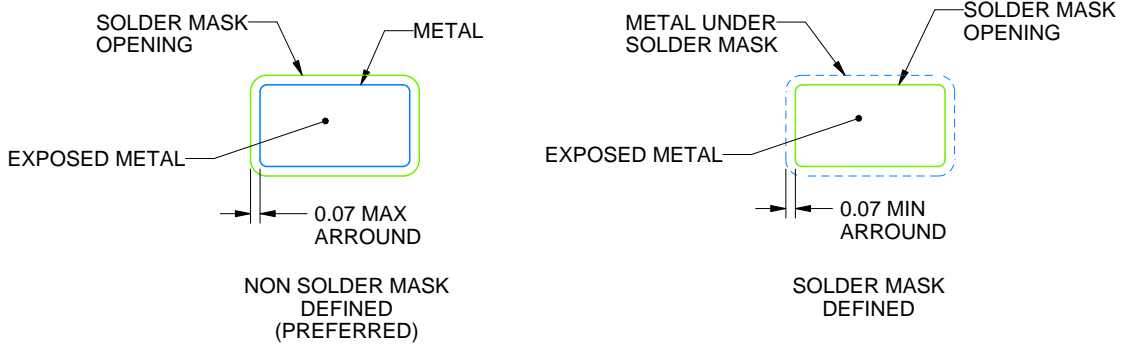
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



## GENERIC PACKAGE VIEW

DRV 6

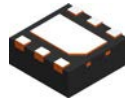
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4206925/F



4222173/B 04/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



# EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



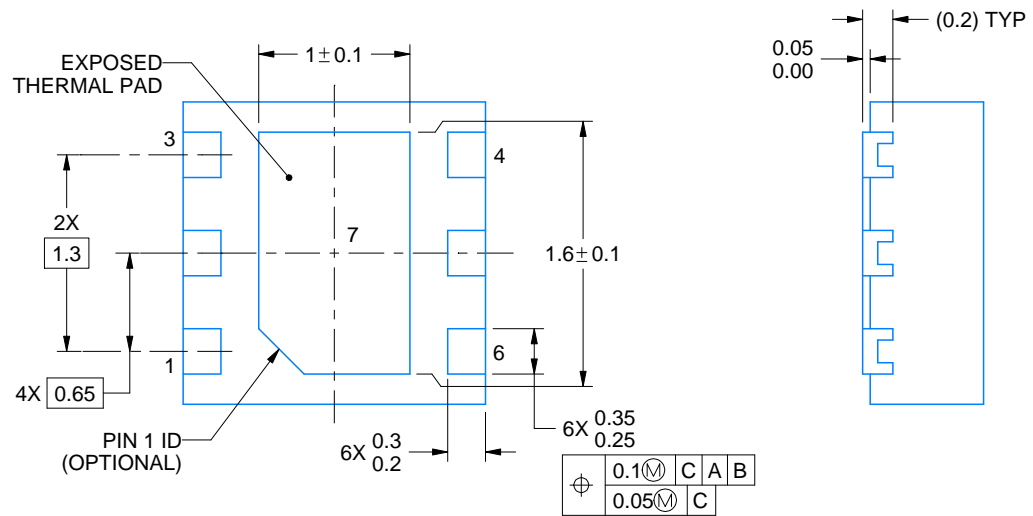
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7  
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



# EXAMPLE STENCIL DESIGN

DRV0006D

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7  
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要声明和免责声明

TI 均以“原样”提供技术性及其可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

Copyright © 2020 德州仪器半导体技术（上海）有限公司